# EXP-6 Synchornous-counters - up counter and down counter

## Aim:

To implement 4 bit up and down counters and validate functionality.

## Equipments required:

Hardware required: PC, Cyclone II , USB flasher

Software required: Quartus prime

## Theory:

### Up Counter:

The counter is a digital sequential circuit and here it is a 4 bit counter, which simply means it can count from 0 to 15 and vice versa based upon the direction of counting (up/down).

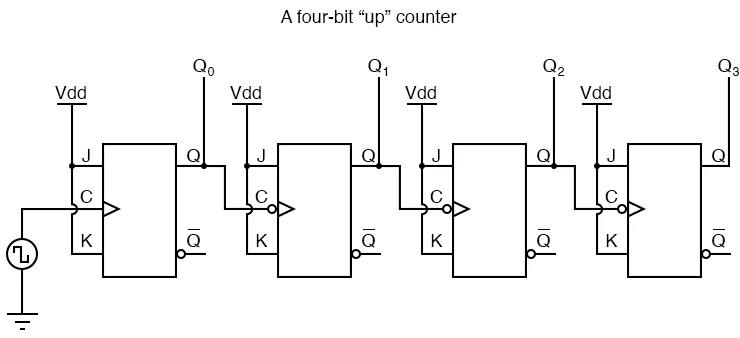
The counter (“count“) value will be evaluated at every positive (rising) edge of the clock (“clk“) cycle. The Counter will be set to Zero when “reset” input is at logic high. The counter will be loaded with “data” input when the “load” signal is at logic high. Otherwise, it will count up or down. The counter will count up when the “up\_down” signal is logic high, otherwise count down

Since we know that binary count sequences follow a pattern of octave (factor of 2) frequency division, and that J-K flip-flop multivibrators set up for the “toggle” mode are capable of performing this type of frequency division, we can envision a circuit made up of several J-K flip-flops, cascaded to produce four bits of output. The main problem facing us is to determine how to connect these flip-flops together so that they toggle at the right times to produce the proper binary sequence. Examine the following binary count sequence, paying attention to patterns preceding the “toggling” of a bit between 0 and 1: Binary count sequence, paying attention to patterns preceding the “toggling” of a bit between 0 and 1.

Note that each bit in this four-bit sequence toggles when the bit before it (the bit having a lesser significance, or place-weight), toggles in a particular direction: from 1 to 0.

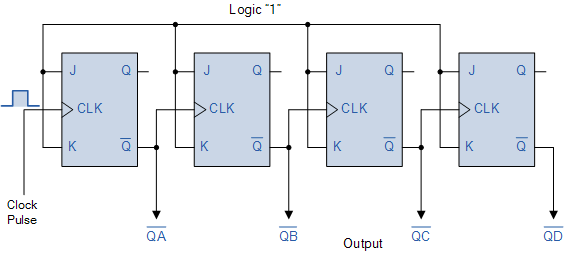
Starting with four J-K flip-flops connected in such a way to always be in the “toggle” mode, we need to determine how to connect the clock inputs in such a way so that each succeeding bit toggles when the bit before it transitions from 1 to 0.

The Q outputs of each flip-flop will serve as the respective binary bits of the final, four-bit count:

Four-bit “Up” Counter [](https://user-images.githubusercontent.com/36288975/169644758-b2f4339d-9532-40c5-af40-8f4f8c942e2c.png)

### Down Counter:

As well as counting “up” from zero and increasing or incrementing to some preset value, it is sometimes necessary to count “down” from a predetermined value to zero allowing us to produce an output that activates when the zero count or some other pre-set value is reached.

This type of counter is normally referred to as a Down Counter, (CTD). In a binary or BCD down counter, the count decreases by one for each external clock pulse from some preset value. Special dual purpose IC’s such as the TTL 74LS193 or CMOS CD4510 are 4-bit binary Up or Down counters which have an additional input pin to select either the up or down count mode. [](https://user-images.githubusercontent.com/36288975/169644844-1a14e123-7228-4ed8-81a9-eb937dff4ac8.png)

4-bit Count Down Counter

## Procedure:

1.Create a new project in Quartus2 software .

2.Name the project as uc for upcounter and dc for down counter.

3.Create a new verilog hdl file in the project file.

4.Name the module declare as dc and uc for down counter and upcounter.

5.Within the module declare input and output variables.

6.Create a loop using if-else with condition parameter as reset.

7.End the loop.

8.End the module

## Program:

### Up Counter:

module upcounter(clk,q1,q2,q3);

input clk;

output reg q1,q2,q3;

always@(posedge clk)

begin

q3 = (q1&q2)^q3;

q2 = q1^q2;

q1 = 1^q1;

end

endmodule

### Down Counter:

module downcounter(clk,q1,q2,q3);

input clk;

output reg q1,q2,q3;

always@(posedge clk)

begin

q3 = ((~q1)&(~q2))^q3;

q2 = (~q1)^q2;

q1 = 1^q1;

end

endmodule

## Output:

### State Table:

#### Up Counter:

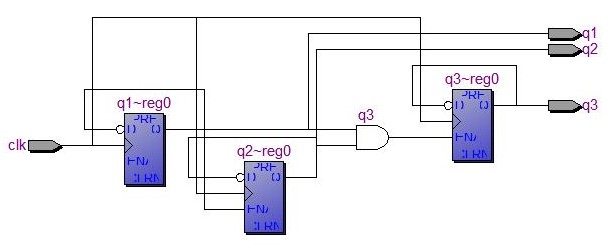
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | | Next State | | | Flip Flop | | |
| Q3 | Q2 | Q2 | Q’3 | Q’2 | Q’1 | T3 | T2 | T1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

#### Down Counter:

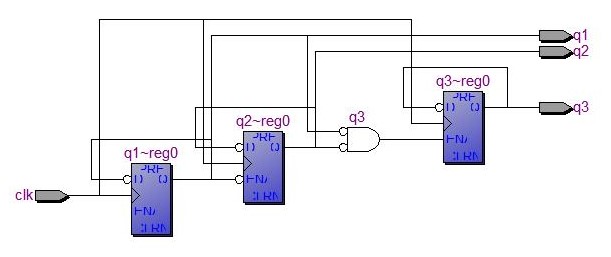
|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Present State | | | Next State | | | Flip Flop | | |
| Q3 | Q2 | Q1 | Q’3 | Q’2 | Q’1 | T3 | T2 | T1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |

### RTL logic for up and down counter:

#### Up Counter:

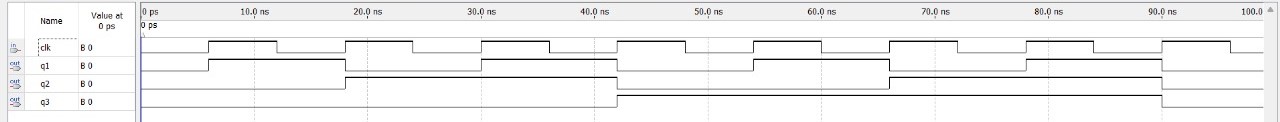
[](https://private-user-images.githubusercontent.com/139228922/292997255-b9ae1e13-4049-4a47-a3d6-87c4d4987ac3.jpg?jwt=eyJhbGciOiJIUzI1NiIsInR5cCI6IkpXVCJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTEiLCJleHAiOjE3MDM2Njc4ODYsIm5iZiI6MTcwMzY2NzU4NiwicGF0aCI6Ii8xMzkyMjg5MjIvMjkyOTk3MjU1LWI5YWUxZTEzLTQwNDktNGE0Ny1hM2Q2LTg3YzRkNDk4N2FjMy5qcGc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBSVdOSllBWDRDU1ZFSDUzQSUyRjIwMjMxMjI3JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDIzMTIyN1QwODU5NDZaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT0xNzk0MjY2ODczY2FjZDkwYTdmOWZlOGEwZDA5ZTU1ZWQwNThhNDNjOWRmNDIzY2Q5ZWM3ZTBhOGYyNDI2ZTcyJlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCZhY3Rvcl9pZD0wJmtleV9pZD0wJnJlcG9faWQ9MCJ9.MDibLmZNk5lK3XSLzrdlLISp_XTnr5_EVzNNT7BezXE)

#### Down Counter:

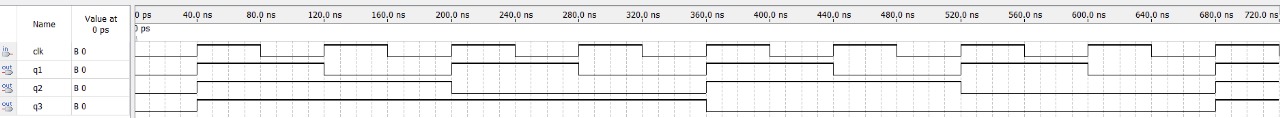
[](https://private-user-images.githubusercontent.com/139228922/292997492-4997a05f-96af-460c-809c-674ff3b09a93.jpg?jwt=eyJhbGciOiJIUzI1NiIsInR5cCI6IkpXVCJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTEiLCJleHAiOjE3MDM2Njc4ODYsIm5iZiI6MTcwMzY2NzU4NiwicGF0aCI6Ii8xMzkyMjg5MjIvMjkyOTk3NDkyLTQ5OTdhMDVmLTk2YWYtNDYwYy04MDljLTY3NGZmM2IwOWE5My5qcGc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBSVdOSllBWDRDU1ZFSDUzQSUyRjIwMjMxMjI3JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDIzMTIyN1QwODU5NDZaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT1iNGJiZTlhMWNjMWVmN2ZmNzM3OWMzMTI3YzAxNWY1NTIwNzVhODdlOThhMzNiMTdjYTBmZmMzYzNkZTczYTQyJlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCZhY3Rvcl9pZD0wJmtleV9pZD0wJnJlcG9faWQ9MCJ9.bge6akx-Q1O6sEqQZp6YUEj-Qws6vDmipbOZruRAAE8)

### Timing diagrams for up and down counter:

#### Up Counter:

[](https://private-user-images.githubusercontent.com/139228922/292997681-e82482c1-b02c-486d-9364-12010173ea06.jpg?jwt=eyJhbGciOiJIUzI1NiIsInR5cCI6IkpXVCJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTEiLCJleHAiOjE3MDM2Njc4ODYsIm5iZiI6MTcwMzY2NzU4NiwicGF0aCI6Ii8xMzkyMjg5MjIvMjkyOTk3NjgxLWU4MjQ4MmMxLWIwMmMtNDg2ZC05MzY0LTEyMDEwMTczZWEwNi5qcGc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBSVdOSllBWDRDU1ZFSDUzQSUyRjIwMjMxMjI3JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDIzMTIyN1QwODU5NDZaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT1hNGQ2MTNjM2ViOTg2MWYxYWY1ODNjMjI5ZTNjYWNlNTM4M2EzNWM3YTBkMzNkMzhkYjkxMTRkMTVmOTMzZDUwJlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCZhY3Rvcl9pZD0wJmtleV9pZD0wJnJlcG9faWQ9MCJ9.Sdm_xiuoLuoqgtEumL3-B_oQYQxATpUbtkRziuYJzvQ)

#### Down Counter:

[](https://private-user-images.githubusercontent.com/139228922/292997865-9c716603-67f0-48f7-88ab-27d5a7c9707e.jpg?jwt=eyJhbGciOiJIUzI1NiIsInR5cCI6IkpXVCJ9.eyJpc3MiOiJnaXRodWIuY29tIiwiYXVkIjoicmF3LmdpdGh1YnVzZXJjb250ZW50LmNvbSIsImtleSI6ImtleTEiLCJleHAiOjE3MDM2Njc4ODYsIm5iZiI6MTcwMzY2NzU4NiwicGF0aCI6Ii8xMzkyMjg5MjIvMjkyOTk3ODY1LTljNzE2NjAzLTY3ZjAtNDhmNy04OGFiLTI3ZDVhN2M5NzA3ZS5qcGc_WC1BbXotQWxnb3JpdGhtPUFXUzQtSE1BQy1TSEEyNTYmWC1BbXotQ3JlZGVudGlhbD1BS0lBSVdOSllBWDRDU1ZFSDUzQSUyRjIwMjMxMjI3JTJGdXMtZWFzdC0xJTJGczMlMkZhd3M0X3JlcXVlc3QmWC1BbXotRGF0ZT0yMDIzMTIyN1QwODU5NDZaJlgtQW16LUV4cGlyZXM9MzAwJlgtQW16LVNpZ25hdHVyZT03ZDEyMWQxYzRiN2VlYmE0MmY1NGYxYjg2YWYxMGNiODljZDU5N2RhYmMzZWExYzA3MTBjMzY1NWU1MjM0YjE5JlgtQW16LVNpZ25lZEhlYWRlcnM9aG9zdCZhY3Rvcl9pZD0wJmtleV9pZD0wJnJlcG9faWQ9MCJ9.e2ISSSnAS4aEfR1vv38rDWZNPdQhvPl9Xv3r6-Ixb1E)

## Result:

Thus synchornous counters up counter and down counter circuit are studied and the truth table for different logic gates are verified.