**Synthesis of Digital Systems**
**Assignment 2: Lockable Cache Ways and Scratch Pad Memory**
**Due Date: 20 September 2018**

In this you will model and simulate in VHDL a 4-way set-associative cache with *dynamically lockable ways*. When a way is locked, data in the way is never replaced. Such a feature is useful when we have some critical data in the cache that we don't want to be displaced. When a way is locked, it behaves like a *scratch pad memory* (SPM). An SPM is associated with an address space in main memory that is not subject to cache replacement [1]. When data is written to that address range, it stays there until overwritten.

- Your final submission will be a VHDL simulation of the working system, with testbenches generating input and verifying the output of the cache. Input/Output will consist of address, data, any instruction for locking/unlocking a way, hit/miss, and anything else you choose.
- Remember to carefully test the model for proper functionality. Testing is part of the assignment, and the assignment will be evaluated based on the extent of testing.
- Write a short document outlining the features of the model and the testing strategy.
- Make your own reasonable assumption about any design parameter (timing, cache size, etc.)
- Give higher priority to first building a working system. Add new features as and when time permits.

[1] Panda, Dutt, Nicolau: Efficient utilization of scratch-pad memory in embedded processor applications. ED&TC 1997: 7-11