



राष्ट्रीय प्रौद्योगिकी संस्थान रायपुर

(राष्ट्रीय महत्व का एक संस्थान)

जी.ई.रोड, रायपुर-४९२०१० (छ.ग.)

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B.Tech(5th Semester) End Semester Examination, Autumn 2022

Subject: Date Science (Code: CS105302CS) (Open Elective)

Branch: CSE/ELE/ECE/ITY/MEC/MME/CHE/CIV/BMD/BOT/MIN

Time: 3 Hours

CBCS SCHEME

Max Marks: 50

Note:

1) Solve any 2 questions from Unit I and Unit 2

2) Solve any 4 questions from Unit 3 and Unit 4.

3) Assume suitable data if necessary.

Unit – 1

A. Suppose the number of traffic signals on a road follows a Poisson process. Let 4 signals occur in distance of 2 km.

What is the conditional probability that 0 signals occur in distance of 1 km?

[2.5]

B. Calculate the variance and standard deviation for the following data:

[2.5]

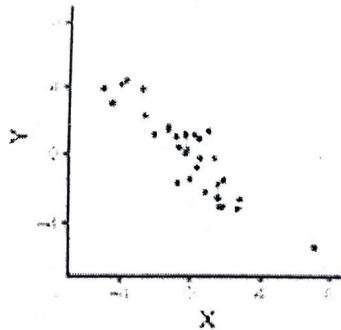
X	2	4	6	8	10
F	3	5	9	5	3

C. Explain the term “Big Data”. What are the different V’s of Big Data?

[2.5]

Unit – 2

A. Given a plot between two random variables X and Y, what can be said about the covariance of X and Y? [2.5]



B. What do you mean by data imputation? What are the different techniques that are used for data imputation? [2.5]

C. If the scatter plot between two variables contains data points such that all points lie on regression line, then the correlation coefficient must be? [2.5]

Unit - 3

A. Evaluating the Regression Model Accuracy (MAE, MSE, RMSE, R-squared and adjusted R-squared) for the original and predicted values. [5]

original = (-2.5, -1.2, -3.1, 2.3, 3.3, 5.4, 4.5, 6.2, 5.4, 6.8, 7.2)

predicted = (-1.2, -1.0, -2.7, 2.5, 3.2, 4.5, 4.1, 5.8, 5.7, 7.2, 7.0)



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B. How Lasso Regularization can be used for dimensionality reduction. Explain the mathematical intuition behind the feature selection achieved by Lasso Regularization. [5]

C. What are the different potential problems that arise when a linear regression model is fitted to a particular dataset? [5]

D. Discuss Bias-Variance Tradeoff in detail. Also provide a valid solution. [5]

E. Obtain the regression equation of Y on X and estimate Y when X=55 from the following: [5]

X	30	40	50	28	65	50	40
Y	28	50	55	70	60	48	30

F. Derive the gradient descent training rule assuming that the target function representation is:

$$o_d = w_0 + w_1 x_1 + \dots + w_n x_n.$$

Define explicitly the cost/error function E, assuming that a set of training examples D is provided, where each training example $d \in D$ is associated with the target output. [5]

A. What is the difference between logistic regression and multinomial regression? [5]

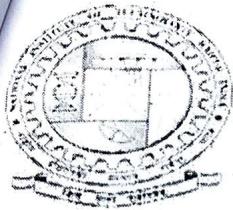
B. In multi class classification problem, where we want to correctly classify dog, cat and rabbit a confusion matrix is given below. Using it calculate Precision, Recall, and F1-Score. Also discuss the result. [5]

Sr. No	Expected	Predicted
1	Dog	Cat
2	Dog	Dog
3	Dog	Dog
4	Cat	Rabbit
5	Rabbit	Rabbit
6	Cat	Cat
7	Rabbit	Dog
8	Rabbit	Rabbit
9	Cat	Cat
10	Rabbit	Cat

Sr. No	Expected	Predicted
11	Dog	Dog
12	Cat	Dog
13	Rabbit	Dog
14	Cat	Rabbit
15	Dog	Cat
16	Dog	Dog
17	Dog	Rabbit
18	Cat	Cat
19	Cat	Dog
20	Cat	Dog

Sr. No	Expected	Predicted
21	Dog	Cat
22	Cat	Dog
23	Rabbit	Dog
24	Cat	Rabbit
25	Rabbit	Rabbit
26	Rabbit	Dog
27	Cat	Rabbit
28	Dog	Cat
29	Dog	Dog
30	Dog	Rabbit

C. The dataset of pass/fail in an exam for 5 students is given in the table below. If we use logistic regression as the classifier and assume the model suggested by the optimizer will become the following for odds of passing a course:



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$$\log(\text{Odds}) = -64 + 2 \times \text{hours}$$

Hours Studies	29	15	33	28	39
Result (1=pass, 0=fail)	0	0	1	1	1

How to calculate the probability of pass for the student who studied 33 and 10 hours? [5]

- D. Solve the following example using KNN algorithm (Euclidean) and predict the class (Species) of observation no. 11 for K=1, K=2, K=7.

Observation No.	Sepal Length	Sepal Width	Species
1	5.3	3.7	Setosa
2	5.1	3.8	Setosa
3	5.4	3.4	Setosa
4	7.2	3.0	Virginica
5	6.1	2.8	Versicolor
6	7.3	2.9	Virginica
7	6.0	2.7	Versicolor
8	5.8	2.8	Virginica
9	5.5	2.4	Versicolor
10	5.4	3.9	Setosa
11	5.2	3.1	?

- E. What is linear discriminant analysis? Explain in detail. [5]

- F. How do we estimate the coefficients in a logistic regression model? Explain with mathematical intuition behind the coefficient's estimation? [5]



Date: 17-11-2022 (Time: 10:00 AM to 01:00 PM)

Max Marks: 50

INSTRUCTIONS:

Attempt all the questions. There are the choices between (Q2 or Q3), (Q4 or Q5) and (Q6 or Q7), so you have to attempt any one question between the choices. All parts of a question should be answered together. Marks assigned for each question are mentioned in the right-hand side. Notations have their usual meanings. Assume default value if required. You are allowed to use calculators.

Q1. Part (a) Consider the sequence of machine instruction given below [5]

MUL R5, R0, R1

DIV R6, R2, R3

ADD R7, R5, R6

SUB R8, R7, R4



In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operations (PO) and (4) Write back the result (WB). The IF, OF and WB stages take 1 clock cycle each instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions is _____.

Part (b) Briefly answer the following questions. [1+2+1+1]

(i) Consider the following instructions:

I1 : Add R10, R7, R12 ; R10 = R7 + R12

I2 : Sub R12, R7, R10 ; R12 = R7 - R10

I3 : Div R12, R9, R12 ; R12 = R9 / R12

Show the types of data hazards that exist between these instructions.

(ii) There are 2 designs for a pipeline processor. Design-1 has a 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the Design-2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions?

250 2

(iii) There are five instructions, which are given below.

I1: Mul R10, R11, R12

I2: Add R15, R10, R12

I3: Add R13, R10, R14

I4: Mul R12, R11, R13

I5: Sub R15, R16, R17



Assume that 20 percent
instructions. There are
(a) Determine the
(b) Determine the
to 1.

Consider the following three statements:

- 1: Instructions I2 and I5 have an anti-dependence
 - 2: Instructions I2 and I4 have an anti-dependence
 - 3: An anti-dependence always creates one or more stalls within instruction pipeline
- Which one of the above statements is/are correct?

(iv) How many mispredictions are there for the given for loop with 1-bit branch predictor?

```
for (i=0; i<5; i++)  
{  
    a+=5;  
}
```

Initially assume to start prediction with a branch taken and you will run this iteration twice.

Q2. Part (a)

Answer the following questions for the k-ary n-cube network: [5]

(i) How many nodes does the network contain?

(ii) What is the network diameter?

(iii) What is the bisection bandwidth?

(iv) What is the node degree?

(v) Explain the graph-theoretic relationship among k-ary n-cube networks and rings, meshes, tori, binary cubes, and Omega networks.

(vi) Explain the difference between a conventional torus and a folded torus.

(vii) Under the assumption of constant wire bisection, why do low-dimensional networks (tori) have lower latency and higher hot-spot throughput than high-dimensional networks (hypercubes)?

Part (b) Compare buses, crossbar switches, and multistage networks for building a multiprocessor system with n processors and m shared-memory modules. Assume a word length of w bits and that 2×2 switches are used in building the multistage networks. The comparison study is carried out separately in each of the following four categories: [5]

(i) Hardware complexities such as switching, arbitration, wires, connector, or cable requirements.

(ii) Minimum latency in unit data transfer between the processor and memory module.

(iii) Bandwidth range available to each processor.

(iv) Communication capabilities such as permutations, data broadcast, blocking handling, etc.

OR

Q3. Part (a) Draw a 16-input Omega network using 2×2 switches as building blocks. [1+2+2]

(i) Show the switch settings for routing messages from node 1011 to node 0101 and from node 0111 to node 1001 simultaneously. Does blocking exist in this case?

(ii) Determine how many permutations can be implemented in one pass through this Omega network. What is the percentage of one-pass permutations among all permutations?

(iii) What is the maximum number of passes needed to implement any permutation through the network?

Part (b) Network embedding is a technique to implement a network A on a network B. Explain how to perform the following network embeddings: [1+2+2]

(i) Embed a two-dimensional torus on an n-dimensional hypercube with $N = 2^n$ nodes where $r^2 = 2^n$.

(ii) Embed the largest ring on a CCC with $N = K \times 2^K$ nodes and K is greater than equal to 3.

(iii) Embed a complete balanced binary tree with maximum height on a mesh of $r \times r$ nodes.

~~X~~
Assume that 20 percent of the dynamic count of the instructions executed for a program are branch instructions. There are no pipeline stalls due to data dependencies. Static branch prediction is used with a not taken assumption. [5+5]

- (a) Determine the execution times for two cases: when 30 percent of the branches are taken, and when 70 percent of the branches are taken.
- (b) Determine the speedup for one case relative to the other. Express the speedup as a percentage relative to 1.

OR

Q5. The two figures as given below represent two cache coherence models: [2+4+4]

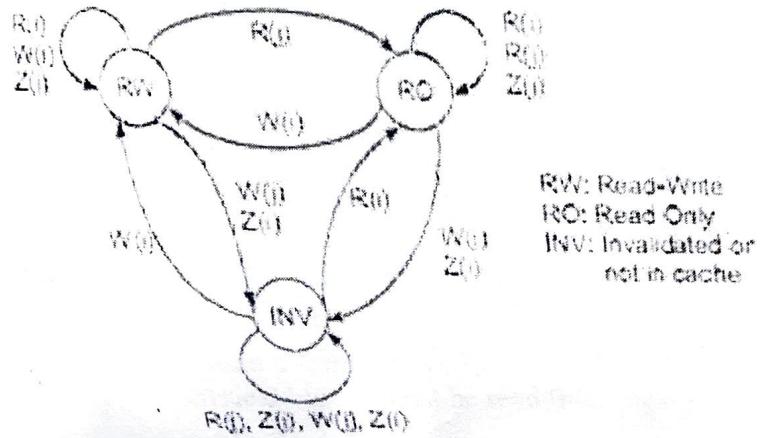


Fig: (a)

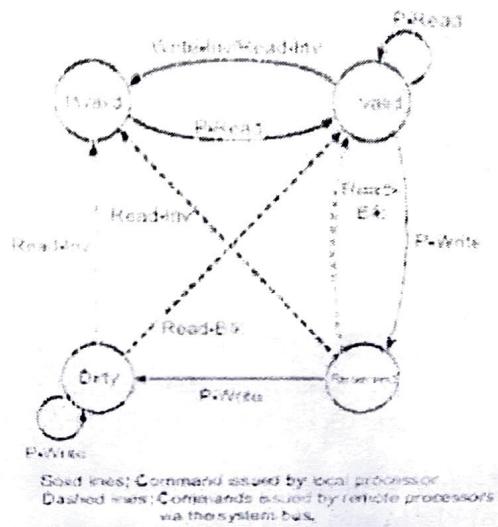


Fig: (b)

- (i) What are the names of the given (Fig. a and Fig. b) two cache coherence models?
- (ii) How are the states of each model vary when read and write by local and remote processors?
- (iii) Compare the full map directory structure with chained directories

Q6. Part (a) Explain the following terms associated with cache design: [5]

- (i) Write-through versus write back caches
- (ii) Cacheable versus non cacheable data
- (iii) Private caches versus shared caches
- (iv) Cache flushing policies
- (v) Factors affecting cache hit ratios

Part (b) Consider the simultaneous execution of the three programs on the three processors. Answer the following questions with reasoning or supported by computer simulation results: [5]

- (i) List the 90 execution interleaving orders of the six instructions {a, b, c, d, e, f} which will preserve the individual program orders. The corresponding output patterns (6-tuples) should be listed accordingly.
- (ii) Can all 6-tuple combinations be generated out of the 720 non-program-order interleavings? Justify the answer with reasoning and examples.
- (iii) Here atomic memory access is assumed in this example. Explain why the output 011001 is not possible in an atomic memory multiprocessor system if individual program orders are preserved.
- (iv) Suppose nonatomic memory access is allowed in the above multiprocessor. For example, an invalidation does not reach all private caches at the same time. Prove that 011001 is possible even if all instructions were executed in program order but other processors did not observe them in program order.

OR

B.Tech. (Fifth Semester) End Semester Examination Nov.-Dec. 2022

Code: CS105103CS

Subject: Operating System

Branch: Computer science & Engineering

Time: 3 hours

Max Marks: 50

Note: Attempt all parts from each Question.

Q.1 Consider the following set of processes with their arrival time and length of CPU burst (in millisecond), what is the average turnaround time and waiting time (rounding to the nearest hundredth) using (i) FCFS (ii) Shortest Job first (iii) Round Robin (quantum=2) Scheduling algorithms?

Process	Arrival time	Burst Time
P0	0.000	3
P1	1.001	6
P2	4.001	4
P3	6.002	2

Q.2 What is file system? Consider a file system on disk that has both logical and physical block size of 512 bytes. Assume that the information about each file is already in memory. For each of allocation strategy (contiguous, linked and indexed) answers these questions:

- (i) How is the logical -to -physical address mapping accomplished in this system?
- (ii) If we are currently at logical block 10 and want to access logical block 4, how many physical blocks must be read from the disk?

Q.3 (a) Consider a system with five number of processes and four number of resources where total instances of each type of resources are given by a vector $(3, 14, 12, 12)$ and current allocation of each process is given by a matrix A_{ij} and Maximum need of each process given in matrix M_{ij} , do the followings :

$$A_{ij} = \begin{bmatrix} 0 & 0 & 1 & 2 \\ 1 & 0 & 0 & 0 \\ 1 & 3 & 5 & 4 \\ 0 & 6 & 3 & 2 \\ 0 & 0 & 1 & 4 \end{bmatrix} \quad M_{ij} = \begin{bmatrix} 0 & 0 & 1 & 2 \\ 1 & 7 & 5 & 0 \\ 2 & 3 & 5 & 6 \\ 0 & 6 & 5 & 2 \\ 0 & 6 & 5 & 6 \end{bmatrix}$$

- (i) Find the current state of the system.
- (ii) Find the state of the system after P2 make a request for $(0, 4, 2, 0)$ resources.

(b) What is Bakery algorithm? Explain and why operating systems use this algorithm? Justify

Q.4 (a) How resource allocation graph can be useful in deadlock detection? Consider a system with four number of processes and four number of resources where

T: Total resource vector $T = (3, 3, 1, 2)$

R_i : Request vector for process P_i , $R_1 = (1, 0, 0, 0)$, $R_2 = (0, 0, 1, 0)$, $R_3 = (0, 1, 0, 0)$, $R_4 = (0, 0, 0, 1)$

A_i : Current allocation vector for process P_i , $A_1 = (1, 0, 0, 1)$, $A_2 = (1, 1, 0, 0)$, $A_3 = (1, 0, 0, 0)$,

$A_4 = (0, 1, 1, 1)$.

Do the followings: (i) draw the resource allocation graph for the above system.

(ii) Indicate if the system is deadlocked or not and justify your answer.

(b) What are semaphores? Define binary semaphores and counting semaphores. How Monitors can overcome the limitations imposed by semaphores?

Q.5 (a) What is Belady's anomaly? Using the given reference string: 1,2,3,4,1,2,5,1,2,3,4,5. Prove which of the following page replacement algorithms suffers from this anomaly.

- (i) LRU replacement (ii) FIFO (iii) Optimal replacement

(b) What is paging? How to reduce the time overhead generated by a paged system? Consider a paging system with page table stored in memory. If a memory reference takes 150 ns what is the effective access time for a memory reference using a translation look aside buffers (TLB) with 75% hit rate and 50 ns access time? What is % improvement in access time using a TLB?

Q.6 (a) Explain the paged-segmentation system with its MMU diagram and consider a system in which virtual address space consists of up to 16 segments where each segments can be up to 2^{16} bytes long. The hardware pages each segment into 512-byte pages. How many bits in the virtual address specify the following? (i) Segment number (ii) Page number (iii) Offset within page (iv) Entire virtual address

(b) What is Multilevel Paging? A system that uses a two level page table has 32-bit virtual addresses. The first 8-bit of address serve as index into the first level page table, and the next 10-bits specify the level -two page table entry.

- (i) How many bytes in a page?
- (ii) How many entries in a level-one page table?
- (iii) How many entries in a level-two page table?
- (iv) How many pages in the virtual address space?

NATIONAL INSTITUTE OF TECHNOLOGY RAIPUR

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

End Semester Exam

Time-3:00 Hours

B.Tech (V SEM. Session 2022-23)

M.M-50

Subject: Data Base Management System (DBMS)

Code: CS105102CS

Instructions:

1. Attempt any five questions.
2. Each questions carry equal marks.
3. Attempt same part of question in same place.
4. Assume missing data and explanation of answer, diagram, and example should be must in all questions.

Q.1 A Construct an E-R diagram for a hospital with a set of patients and a set of medical doctors. Associate 5 with each patient, a log of the various tests and examinations conducted.

B Given the relational schema R (A, B, C, D, E) and given the following set of FDs defined on

$$F = \{A \rightarrow BC, CD \rightarrow E, AC \rightarrow E, B \rightarrow D, E \rightarrow AB\}$$

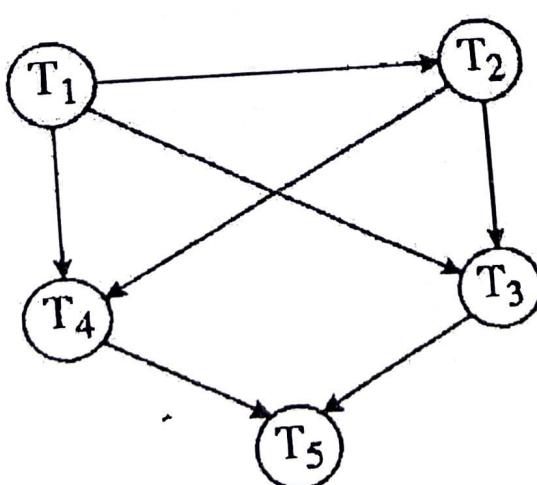
- (a) Determine a lossless-join decomposition of R.
- (b) Determine a decomposition of R which is not lossless-join.
- (c) Determine if R is in 3NF w.r.t. to F if it is not violating the 3NR.
- (d) Write candidate key
- (e) Write super key

Q.2 A i. Explain the salient features of deferred database modification and immediate database

modification schemes of recovery.

ii. Explain 'Blind-Writes' operation with help of example.

B Consider the precedence graph in given fig. Is the corresponding schedule conflict serializable ? 5
Explain your answer.



- Q.3** A i. Explain timestamp and discuss the timestamp ordering techniques for concurrency control.
 ii. Write Thomas write law.
- B State whether the following schedule is conflict serializable or not. Justify your answer.

T ₁	T ₂
read (A)	
write (A)	
	read (B)
read (B)	write (B)
write (B)	
	read (A)
	write (A)

- Q.4** A What is multiple-granularity locking? What is the difference between implicit and explicit locking in multiple-granularity locking? 5
 B What do you mean by transaction and concurrency? 5

- Q.5** A Explain Failure classification and checkpoint with the help of proper example. 5
 B Consider the following Transactions 5

T1 : read (A);
 read (B);
 if A = 0 then B := B + 1;
 write (B);
 T2 : read (A);
 read (B);
 if B = 0 then A := A + 1;
 write (A);

Add lock & unlock instruction to transactions T1 & T2 so that they observe the two-phase locking protocol.

- Q.6** A Which of the following schedules is conflict serializable? For each serializable schedule determine the equivalent serial schedules. 5
 (1) r1 (x); r3 (x); W1(X), r2(x); w3(x);
 (2) r1 (x); r3 (x); w3(X), w1(x); r2(x);
 B What is the goal of query optimization? Is it practically possible to achieve the absolute best(optimal)strategy for executing the query? 5

2011SOS2

5th Semester
 Date: 10:00 AM to 1:00 PM

End-Semester Examination Autumn 2022
 Subject: Compiler Design
 Subject Code: CS105101CS

(CBCS Scheme)

Max Marks: 50

Answer any FOUR including Question Number 1

- | Q.1 | Marks |
|---|-------|
| a) Answer the following questions. | [2] |
| The given SDT $A \rightarrow BC \{A.i = f(B.i); \}$ is | [2] |
| i. S-attributed ii. L-attributed iii. both iv. None | [2] |
| b) Convert the following language constructs to three address code | [2] |
| while ($x > 10$) do $x = x + y$ | [2] |
| c) What is the maximum number of reduce moves that can be taken by a bottom up parser for a grammar with no epsilon and unit production (i.e., not of type $A \rightarrow \lambda, A \rightarrow B$ and $A \rightarrow a$) to parse a string with n tokens? | [2] |
| d) Find the number of tokens in the following code segment | [2] |
| $x=(a>b) ? printf("Great India \n"); printf("Proud to be indian \n");$ | [2] |
| e) Check whether the grammar is LL(1) or not? | [2] |
| f) $S \rightarrow aSA \lambda, A \rightarrow abS \lambda$ | [2] |
| g) Construct the DAG for the following expression | [2] |
| $((x + y) - ((x + y) \times (x - y))) + ((x + y) \times ((x - y)))$ | [2] |
| h) Find the differences between machine dependent code optimization and machine independent code optimization. | [2] |
| i) Suppose we have a production $A \rightarrow BCD$. Each of the four non-terminals have two attributes: s is the synthesized attribute and i is the inherited attribute. Check whether the following set of rules are consistent with L-attributed or S-attributed definition
$A.s = D.i, B.i = A.s + C.s, C.i = f(B.s), \text{ and } D.i = h(B.i) + g(C.i)$ | [2] |
| j) A shift reduce parser carries out the actions specified within braces immediately after reducing with the corresponding rule of grammar
$S \rightarrow xxW \ printf("India");$
$S \rightarrow y \ printf("Great");$
$W \rightarrow Sz \ printf("Wow!");$
What is the translation of xxxxxyz using the syntax directed translation scheme described by the above rules? | [2] |
| Consider the grammar $S \rightarrow (S) a$. If the number of states in SLR(1), CLR(1) and LALR(1) are n1, n2 and n3 respectively. Then which of the following relation is true: | [2] |
| i. $n1 < n2 < n3$ | [2] |
| ii. $n1 = n3 < n2$ | [2] |
| iii. $n1 = n2 = n3$ | [2] |
| iv. $n1 > n3 > n2$ | [2] |

- Q.2. a) Construct an SLR parsing table of the given grammar: $S \rightarrow cAd, A \rightarrow ab|a$
 i. Parse the string $cabd$ using the table.
 ii. Why Canonical LR is more powerful than SLR? [5]

- Consider the grammar,
 $S \rightarrow Aa$
 b) $A \rightarrow BC|Bcf$
 $B \rightarrow b$
 $C \rightarrow c$
 i. Construct the canonical collection of sets of LR(0) items for this grammar.
 ii. Derive ACTION and GOTO tables for SLR parser. [5]

- Q.3.a) Show that the following grammar is CLR(1) but not LALR(1).
 $S \rightarrow Aa|bAc|BC|bBa$
 $A \rightarrow d$ Bc
 $B \rightarrow d$ [5]

- b) For the given grammar
 $S \rightarrow AaAb|BbBa$
 $A \rightarrow \lambda$
 $B \rightarrow \lambda$ [5]
 Check whether it is LL (1) or not? Find the position of multiple entries.
 Also verify for LR (0), SLR (1), CLR(1) and LALR(1).

- Q.4. a) Explain the following optimization techniques with appropriate examples.
 i. Constant Propagation
 ii. Dead Code Elimination
 iii. Loop Invariant Code Motion
 iv. Peephole Optimization [4]

- b) What is operator Grammar? Convert this Grammar into an operator Grammar.
 $E \rightarrow EA'E|id$
 $A \rightarrow +|\times$ [6]
 Construct the precedence relation table for the above grammar and subsequently convert this into a precedence function table using the precedence graph.

- Q.5.a) Translate the statement $x = (a + b) \times -c/d$ into
 i) Quadruples
 ii) Triples [3]

- Generate the three-address code for the following code segment:
 b)

```
int i, x[20];
i = 0;
while( i < 20 )
{
    x[i] = i ;
    i++;
}
```

 [3]

- c) Write a SDT for the evaluation of expression using the following grammar:
 $E \rightarrow E \times T|T$
 $T \rightarrow F - T|F$
 $F \rightarrow 1|3$ [4]
 If the SDT is carried by a BUP for the i/p string $w = 3 - 1 - 3 \times 1$, what will be the output.
 Modify the SDT to include number of reductions performed to parse the given i/p string.