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ECE-209 , FINAL PROJECT

*32*4 BIT RAM MEMORY*

1. All required about circuit:

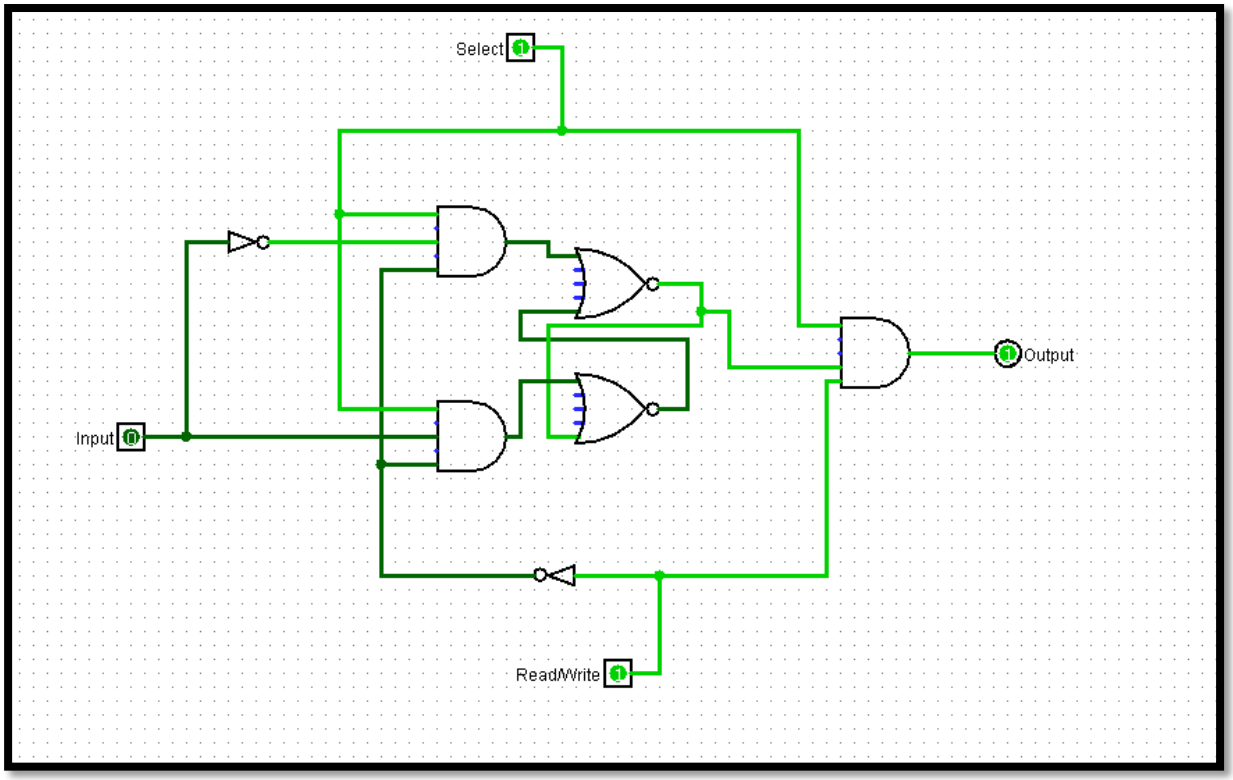
-For creating a ram we require is a basic binary cell unit

-This unit consists of a s-r latch and a combination of ‘not’ and ‘and’ gate.

-Furthur we need a 5 bit decoder. It gives 32 output.

-We need to keep enable line of decoder as 1. And the select one as a 5 bit input.

-Also we will need a clock/read-write input.



Binary Cell of SR Flip Flop

2. **Steps:**

-First of all, I have used binary cell to store one bit of memory. Binary cell as shown in above figure can be designed with the help of R-S Latch.

-Further, matrix of binary cell with dimension 32x4 has been created.

-Read/write input has been shorted with single common input.

-Selection Lines of all rows are shorted and its value is taken from 5x32 Decoder.

-When clock and E is set to 1, some input is given to selection line and memory input has been given, the input has been stored. Hence, 32x4 RAM has been designed.

3. **Working :**

-The binary cell stores one bit in its internal flip-flop.

-It has three inputs and one output.

-The select input enables the cell for reading or writing and the read/write input determines the cell operation when it is selected.

- A 1 in the read/write input providers the read operation by forming a path from the flip-flop to the output terminal.

-A 0 in the read/write input providers the write operation by forming a path from the input terminal to the flip-flop.

-Note that the flip-flop operates without a clock and is similar to an SR latch. The logical construction of RAM consists of n words of n bits each and has a total of n*n binary cells.

-The m address inputs go through a m*n decoder to select one of the n words. The decoder is enabled with the memory-enable input.

-When the memory enable is 0, all outputs of the decoder are 0 and none of the
memory words are selected.

-With the memory enable at 1, one of the n words is selected, dictated by the value in the m address lines. Once a word has been selected, the read/write input determines the operation.

-During the read operation, the n bits of the selected word go through OR gates to the
output terminals.

-During the write operation, the data available in the lines
are transferred into the n binary cells of the selected word.

-The binary cells that are not selected are disabled and their previous binary values remain unchanged. When the memory-enable input that goes into the decoder to 0, none of the words are selected and the contents of all cells remain unchanged regardless of the value of the read/write input.

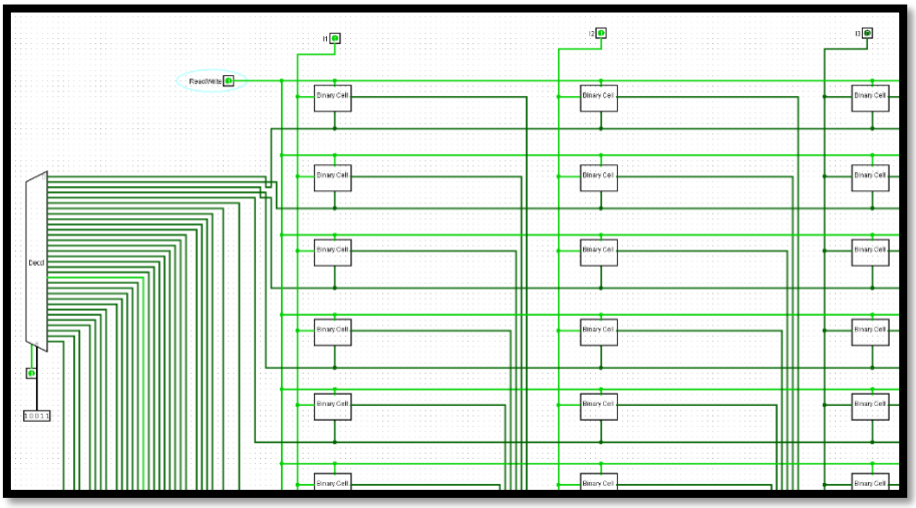
4. **Input:**

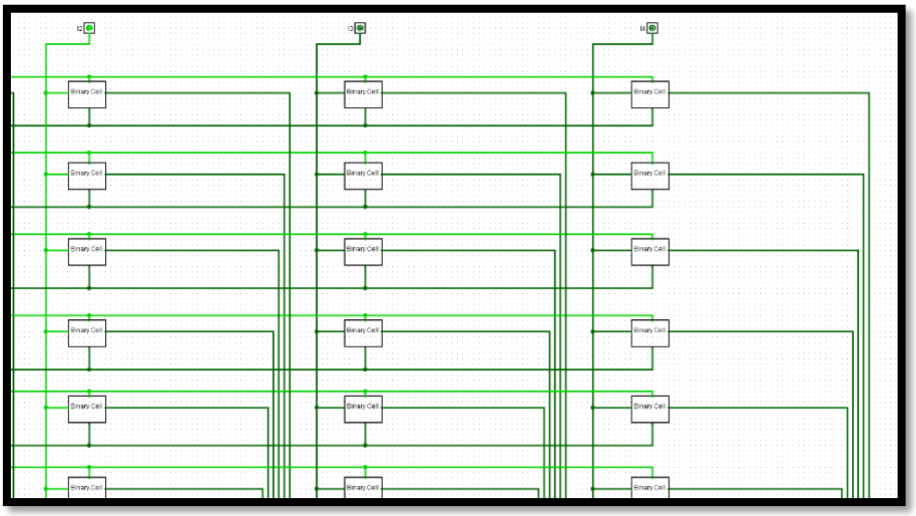
-Here I have taken the value of enable line of encoder as 1

-The value in encoder of select as 10011.

-Values of input as I1=1, I2 =1, I3=0, I4=0.

-The value of clock/read-write as 1.





5. **Output:**
   - For such inputs we will get output as 0011.
   - As shown in below diagram.