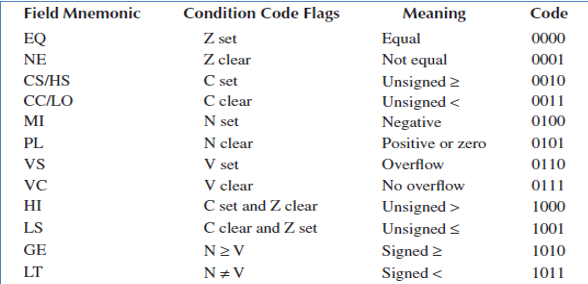
The part of ARM Cortex M4 code is as below, where in the error “Specified condition is not consistent with previous IT” raised by the instruction lines 3 to 6 are solved by the below shown replacements.

1: CMP R8, R3 ; do R8 - R3 & updated N & V flags  
2: ITTTE LT ; or N != V  
3: MOV R3, #0x100 -> ADDLT r3, r3,r8  
4: MOV R8, #0x200 -> MOVLT r4, #0  
5: MOV R7, #0x200 -> MOVLT R0, #1  
6: MOV R6, #0x200 -> SUBGE r3, r3, r3 ; Z != 1 pr N == V

Line 1 has a CMP instruction that compares the two register values R8 and R3 and updates the N and V flags. The state of these two flags are used in the control instruction (line 2) ITTTE (If then then then else) which means the next four instructions are conditional instructions.

Conditional instructions are the instructions that also contain conditional codes like show in the figure below which are governed by the state of the flags that were set by the CMP instruction of line 1.



The conditional instructions that follow control instructions like ITTTE are basically the usual ARM cortex M4 instructions appended with any one of the above conditional code. This suggests the compiler the condition under which the respective instruction needs to be executed.

Example:

1. MOVLT and ADDLT moves and adds the data in respective registers when N flag is not equal to V flag.
2. SUBGE subtracts the data in respective registers when N flag is greater than or equal to V flag.

In CODE 1, the control instruction ITTTE was not followed by four conditional instructions. That is the ITTTE construct in CODE 1 had simple ARM cortex instructions without any conditional code that need to be specified in the ITTTE construct instructions. Hence, all the four instruction lines 3-6 threw the error that the statements are inconsistent with the IT construct.