Test Write Allocation

Config.txt

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 8

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000110000101010101001
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

```
    LI R4, 256
    LI R5, 288
    LI R8, 352
    LI R1, 3
    LI R2, 1
    LI R3, 1
GG: L.D F1, 0(R4)
    L.D F2, 0(R5)
    ADD.D F6, F1, F2
    SUB.D F5, F7, F6
    MUL.D F4, F5, F5
    ADD.D F4, F1, F7
    ADD.D F6, F1, F4
    S.D F6, 0(R8)
    DADDI R4, R4, 4
    DADDI R5, R5, 4
    DADDI R8, R8, 4
    DSUB R1, R1, R2
    BNE R1, R3, GG
    HLT
    HLT
```

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	25 I-Cache miss 1fetch+3cycle x 8word Mem I-Cache block 0 filled with 0x00~0x1F	26	27	28	29	N	N	N
LI R5, 256	26	30 structural hazard	31	32	33	N	N	Y
LI R8, 352	30	34 structural hazard	35	36	37	N	N	Y
LI R1, 3	34	38 structural hazard	39	40	41	N	N	Y
LI R2, 1	38	42 structural hazard	43	44	45	N	N	Y
LI R3, 1	42	46 structural hazard	47	48	49	N	N	Y
GG: L.D F1, 0(R4)	46	47	48	85 Memory bus conflict D-Cache miss for 0x100~0x107 (256~263) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1 Memory bus released at the end of 83	86	N	N	N
L.D F2, 0(R5)	47	87 structural hazard	88	102 D-Cache miss for 0x120~0x127 (288~295) 2+3cycle x 4word Mem D-Cache set 0 block 1 filled with 0x120~0x12F (288~303) LRU of set 0 set to block 0 Memory bus released at the end of 70	103	N	N	Y
ADD.D F6, F1, F2	87 I-Cache miss 1fetch+3cycle x 8word Mem I-Cache block 1 filled with 0x20~0x3F Memory bus released at the end of 71	88	104 RAW hazard on F2 to L.D F2, 8(R5)	106	107	Y	N	N
SUB.D F5, F7, F6	88	89	108 RAW hazard on F6 to ADD.D F5, F7, F6	110	111	Y	N	N
MUL.D F4, F5, F5	89	90	112 RAW hazard on F5 to SUB.D F5, F7, F1	142	143	Y	N	N
ADD.D F4, F1, F7	90	144 WAW hazard on F4 to MUL.D F4, F1, F5	145	147	148	N	Y	N

ADD.D F6, F1, F4	144	145	149 RAW hazard on F4 to ADD.D F4, F1, F7	151	152	Y	N	N
S.D F6, 0(R8)	145	146	153 RAW hazard on F6 to ADD.D F6, F1, F4	185 Memory bus conflict D-Cache miss for 0x160~0x167 (352~359) 2+3cycle x 4word Mem D-Cache set 0 block 0 replaced with 0x160~0x16F (352~367) LRU of set 0 set to block 1 Memory bus released at the end of 183	186	Y	N	N
DADDI R4, R4, 4	146	147	148	149	150	N	N	N
DADDI R5, R5, 4	147	151 structural hazard, not enough integer ALU	152	153	154	N	N	Y
DADDI R8, R8, 4	172 I-Cache miss 1fetch+3cycle x 8word Mem I-Cache block 2 filled with 0x40~0x5F Memory bus released at the end of 171	173	174	175	176	N	N	N
DSUB R1, R1, R2	173	177 structural hazard, not enough integer ALU	178	179	180	N	N	Y
BNE R1, R3, GG	177	178	181 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	178					N	N	N
GG: L.D F1, 0(R4)	182 I-Cache hit on block 0	187 structural hazard	188	202 D-Cache miss for 0x104~0x10B (260~267) 2+3cycle x 4word Mem D-Cache set 0 block 1 replaced with 0x100~0x10F (256~271) LRU of set 0 set to block 0	203	N	N	Y
L.D F2, 0(R5)	187	204 structural hazard	205	231 D-Cache miss for 0x124~0x12B(272~299) 3cycle x 4word Write +2+3cycle x 4word Mem set 0 block 0 replaced with 0x120~0x12F (288~303) LRU of set 0 set to block 1	232	N	N	Y
ADD.D F6, F1, F2	204 I-Cache hit on block 1	205	233 RAW hazard on F2 to L.D F2, 8(R5)	235	236	Y	N	N
SUB.D F5, F7, F6	205	206	237 RAW hazard on F6 to ADD.D F5, F7, F6	239	240	Y	N	N
MUL.D F4, F5, F5	206	207	241	271	272	Y	N	N

			RAW hazard on F5 to SUB.D F5, F7, F1					
ADD.D F4, F1, F7	207	273 WAW hazard on F4 to MUL.D F4, F1, F5	274	276	277	N	Y	N
ADD.D F6, F1, F4	273	274	278 RAW hazard on F4 to ADD.D F4, F2, F6	280	281	Y	N	N
S.D F6, 0(R8)	274	275	282 RAW hazard on F6 to ADD.D F6, F1, F4	296 D-Cache miss for 0x164~0x16B(356~363) 2+3cycle x 4word Mem set 0 block 1 replaced with 0x160~0x16F (352~367) LRU of set 0 set to block 0	297	Y	N	N
DADDI R4, R4, 4	275	276	277	278	279	N	N	N
DADDI R5, R5, 4	276	280 structural hazard, not enough integer ALU	281	282	283	N	N	Y
DADDI R8, R8, 4	280 I-Cache hit on block 2	284 structural hazard, not enough integer ALU	285	286	287	N	N	Y
DSUB R1, R1, R2	284	288 structural hazard, not enough integer ALU	289	290	291	N	N	Y
BNE R1, R3, GG	288	289	292 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	289	290				N	N	N
HLT	293					N	N	N

Total number of access requests for instruction cache: 35

Number of instruction cache hits: 32

Total number of access requests for data cache: 12

Number of data cache hits: 6