Write Allocation

Config.txt

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000110000101010101001
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000010000101011100101010
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

```
    LI R4, 256
    LI R5, 288
    LI R1, 3
    LI R2, 1
    LI R3, 1
    LI R8, 264
GG: L.D F1, 4(R4)
    L.D F2, 8(R5)
    ADD.D   F4,     F6,   F2
    SUB.D   F5,     F7,   F1
    MUL.D   F6,     F1, F5
    ADD.D   F7,   F2,   F6
    ADD.D   F6,   F1,   F7
    S.D       F6, 0(R8)
    DADDI   R4,   R4,   32
    DADDI   R5,   R5,   32
    DADDI   R8,   R8,   24
    DSUB   R1,    R1,   R2
    BNE   R1,    R3,   GG
    HLT
    HLT
```

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	13 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 filled with 0x00~0x0F	14	15	16	17	N	N	N
LI R5, 288	14	18 structural hazard	19	20	21	N	N	Y
LI R1, 3	18	22 structural hazard	23	24	25	N	N	Y
LI R2, 1	22	26 structural hazard	27	28	29	N	N	Y
LI R3, 1	35 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 filled with 0x10~0x1F	36	37	38	39	N	N	N
LI R8, 264	36	40 structural hazard	41	42	43	N	N	Y
GG: L.D F1, 4(R4)	40	41	42	68 Memory bus conflict D-Cache miss for 0x104~0x10B (260~267) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1	69	N	N	Y
L.D F2, 8(R5)	41	70 structural hazard	71	85 D-Cache miss for 0x128~0x12F (296~303) 2+3cycle x 4word Mem D-Cache set 0 block 1 filled with 0x120~0x12F (288~303) LRU of set 0 set to block 0	86	N	N	Y
ADD.D F4, F6, F2	70 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 2 filled with 0x20~0x2F	71	87 RAW hazard on F2 to L.D F2, 8(R5)	89	90	Y	N	N
SUB.D F5, F7, F1	71	72	73	75	76	N	N	N
MUL.D F6, F1, F5	72	73	77 RAW hazard on F5 to SUB.D F5, F7, F1	107	108	Y	N	N
ADD.D F6, F1, F7	73	77 structural hazard, not enough FP adder	108 WAW hazard on F6 to MUL.D F6, F1, F5	110	111	Y	Y	Y
ADD.D F7, F2, F6	86 I-Cache miss 1fetch+3cycle x 4word Mem	91 structural hazard, not enough FP adder	112 RAW hazard on F6 to ADD.D F6, F1, F7	114	115	Y	N	Y

	I-Cache block 3 filled with 0x30~0x3F							
S.D F6, 0(R8)	91	92	93	95 D-Cache hit for 0x108~0x10F(264~271)on set 0 block 0 LRU of set 0 set to block 1	96	N	N	N
DADDI R4, R4, 32	92	93	94	95	96	N	N	N
DADDI R5, R5, 32	93	97 structural hazard, not enough integer ALU	98	99	100	N	N	Y
DADDI R8, R8, 24	106 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 replaced with 0x40~0x4F	107	108	109	110	N	N	N
DSUB R1, R1, R2	107	111 structural hazard, not enough integer ALU	112	113	114	N	N	Y
BNE R1, R3, GG	111	112	115 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	112					N	N	N
GG: L.D F1, 4(R4)	113 I-Cache hit on block 1	114	115	117 D-Cache hit for 0x124~0x133 (292~307) on set 0 block 1 LRU of set 0 set to block 0	118	N	N	N
L.D F2, 8(R5)	114	119 structural hazard	120	146 D-Cache miss for 0x140~0x14F (320~335) Set 0 block 0 should be replaced but dirty 2+3cycle x 4word Write +3cycle x 4word Read D-Cache set 0 block 0 replaced with 0x140~0x14F (320~335) LRU of set 0 set to block 1	147	N	N	Y
ADD.D F4, F6, F2	119 I-Cache hit on block 2	120	148 RAW hazard on F2 to L.D F2, 8(R5)	150	151	Y	N	N
SUB.D F5, F7, F1	120	121	122	124	125	N	N	N
MUL.D F6, F1, F5	121	122	126 RAW hazard on F5 to SUB.D F5, F7, F1	156	157	Y	N	N
ADD.D F6, F1, F7	122	126 structural hazard, not enough FP adder	158 WAW hazard on F6 to MUL.D F6, F1, F5	160	161	Y	Y	Y
ADD.D F7, F2, F6	126 I-Cache hit on block 3	152 structural hazard, not enough FP adder	162 RAW hazard on F6 to ADD.D F6, F1, F7	164	165	Y	N	Y

S.D F6, 0(R8)	152	153	154	156 D-Cache hit for 0x120~0x128(288~296)on set 0 block 1 LRU of set 0 set to block 0	157	N	N	N
DADDI R4, R4, 32	153	154	155	156	157	N	N	N
DADDI R5, R5, 32	154	158 structural hazard, not enough integer ALU	159	160	161	N	N	Y
DADDI R8, R8, 24	158 I-Cache hit on block 0	162 structural hazard, not enough integer ALU	163	164	165	N	N	Y
DSUB R1, R1, R2	162	166 structural hazard, not enough integer ALU	167	168	169	N	N	Y
BNE R1, R3, GG	166	167	170 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	167	168				N	N	N
HLT	180 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 replaced with 0x50~0x5F					N	N	N

Total number of access requests for instruction cache: 35
Number of instruction cache hits: 29
Total number of access requests for data cache: 12
Number of data cache hits: 6