Test memory bus conflict

Config.txt

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000110000101010101001
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

LI R4, 256
LI R5, 256
LI R1, 3
LI R2, 1
LI R3, 1
GG: DADDI R4, R4, 4
DADDI R5, R5, 4
L.D F1, 4(R4)
DSUB R1, R1, R2
ADD.D F4, F6, F2
SUB.D F5, F7, F2
MUL.D F6, F2, F5
L.D F2, 4(R5)
ADD.D F7, F2, F6
ADD.D F6, F1, F7
BNE R1, R3, GG
HLT
HLT

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	13 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 filled with 0x00~0x0F	14	15	16	17	N	N	N
LI R5, 256	14	18 structural hazard	19	20	21	N	N	Y
LI R1, 3	18	22 structural hazard	23	24	25	N	N	Y
LI R2, 1	22	26 structural hazard	27	28	29	N	N	Y
LI R3, 1	35 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 filled with 0x10~0x1F	36	37	38	39	N	N	N
GG: DADDI R4, R4, 4	36	40 structural hazard	41	42	43	N	N	Y
DADDI R5, R5, 4	40	44 structural hazard	45	46	47	N	N	Y
L.D F1, 4(R4)	44	45	46	70 Memory bus conflict D-Cache miss for 0x108~0x10F (264~271) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1 Memory bus released at the end of 68	71	N	N	N
DSUB R1, R1, R2	57 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 2 filled with 0x20~0x2F Memory bus released at the end of 56	58	59	60	61	N	N	N
ADD.D F4, F6, F2	58	59	60	62	63	N	N	N
SUB.D F5, F7, F2	59	60	61	63	64	N	N	N
MUL.D F6, F2, F5	60	61	65 RAW hazard on F5 to SUB.D F5, F7, F1	95	96	Y	N	N
L.D F2, 4(R5)	81 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 3 filled with 0x30~0x3F Memory bus released at the end of 80	82	83	85 D-Cache hit for 0x108~0x10F (264~271) on set 0 block 0 LRU of set 0 set to block 1	86	N	N	N

ADD.D F7, F2, F6	82	83	97 RAW hazard on F6 to MUl.D F6, F2, F5	99	100	Y	N	N
ADD.D F6, F1, F7	83	97 WAW hazard on F6 to MUL.D F6, F1, F5	101 RAW hazard on F7 to ADD.D F7, F2, F6	103	104	Y	Y	N
BNE R1, R3, GG	97	98	99			N	N	N
HLT	110 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 replaced with 0x40~0x4F					N	N	N
GG: DADDI R4, R4, 4	111 I-Cache hit on block 1	112	113	114	115	N	N	N
DADDI R5, R5, 4	112	116 structural hazard	117	118	119	N	N	Y
L.D F1, 4(R4)	116	117	118	132 D-Cache hit for 0x10C~0x10F (268~271) on set 0 block 0 LRU of set 0 set to block 1 D-Cache miss for 0x110~0x113 (272~275) 2+3cycle x 4word Mem D-Cache set 1 block 0 filled with 0x110~0x11F (272~287) LRU of set 1 set to block 1	133	N	N	N
DSUB R1, R1, R2	117 I-Cache hit on block 2	120 structural hazard	121	122	123	N	N	Y
ADD.D F4, F6, F2	120	121	122	124	125	N	N	N
SUB.D F5, F7, F2	121	122	123	125	126	N	N	N
MUL.D F6, F2, F5	122	123	127 RAW hazard on F5 to SUB.D F5, F7, F1	157	158	Y	N	N
L.D F2, 4(R5)	123 I-Cache hit on block 3	134	135	137 D-Cache hit for 0x10C~0x11F(268~275)on set 0 block 0 and set 1 block 0 LRU of set 0 set to block 1 LRU of set 1 set to block 1	138	N	N	Y
ADD.D F7, F2, F6	134	135 structural hazard	159 RAW hazard on F6 to MUl.D F6, F2, F5	161	162	Y	N	Y
ADD.D F6, F1, F7	135	159 WAW hazard on F6 to MUL.D F6, F1, F5	163 RAW hazard on F7 to ADD.D F7, F2, F6	165	166	Y	Y	N
BNE R1, R3, GG	159	160	161			N	N	N
HLT	160 I-Cache hit on block 0	161				N	N	N

HLT	162					N	N	N

Total number of access requests for instruction cache: 30
Number of instruction cache hits: 25
Total number of access requests for data cache: 8
Number of data cache hits: 6