Test WAW

Config.txt

FP adder: 3, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000110000101010101001
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

LI R4, 256
LI R5, 256
LI R1, 3
LI R2, 1
LI R3, 1
GG: L.D F1, 4(R4)
L.D F2, 8(R5)
ADD.D F1, F4, F4
ADD.D F6, F3, F7
SUB.D F2, F7, F4
MUL.D F6, F4, F5
ADD.D F7, F2, F6
DADDI R4, R4, 4
DADDI R5, R5, 4
DSUB R1, R1, R2
BNE R1, R3, GG
HLT
HLT

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	13 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 filled with 0x00~0x0F	14	15	16	17	N	N	N
LI R5, 256	14	18 structural hazard	19	20	21	N	N	Y
LI R1, 3	18	22 structural hazard	23	24	25	N	N	Y
LI R2, 1	22	26 structural hazard	27	28	29	N	N	Y
LI R3, 1	35 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 filled with 0x10~0x1F	36	37	38	39	N	N	N
GG: L.D F1, 4(R4)	36	37	38	52 D-Cache miss for 0x104~0x10B (260~267) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1	53	N	N	N
L.D F2, 8(R5)	37	54 structural hazard	55	57 D-Cache hit for 0x108~0x10F (264~271) on set 0 block 0 LRU of set 0 set to block 1	58	N	N	Y
ADD.D F1, F4, F4	54	55	56	58	59	N	N	N
ADD.D F6, F3, F7	67 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 2 filled with 0x20~0x2F	68	69	71	72	N	N	N
SUB.D F2, F7, F4	68	69	70	72	73	N	N	N
MUL.D F6, F4, F5	69	73 WAW hazard on F6 to ADD.D F6, F3, F7	74	104	105	N	Y	N
ADD.D F7, F2, F6	73	74	106 RAW hazard on F6 to MUL.D F6, F4, F5	108	109	Y	N	N
DADDI R4, R4, 4	86 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 3 filled with 0x30~0x3F	87	88	89	90	N	N	N
DADDI R5, R5, 4	87	91	92	93	94	N	N	Y

		structural hazard, not enough integer ALU						
DSUB R1, R1, R2	91	95 structural hazard, not enough integer ALU	96	97	98	N	N	Y
BNE R1, R3, GG	95	96	99 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	108 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 replaced with 0x40~0x4F					N	N	N
GG: L.D F1, 4(R4)	109 I-Cache hit on block 1	110	111	113 D-Cache hit for 0x108~0x10F (264~271) on set 0 block 0 LRU of set 0 set to block 1	114	N	N	N
L.D F2, 8(R5)	110	115 structural hazard	116	130 D-Cache hit for 1st word 0x108~0x10F(268~271)on set 0 block 0 LRU of set 0 set to block 1 D-Cache miss for 2nd word 0x110~0x103 (272~275) Set 1 block 0 filled with 0x110~0x11F (272~287) LRU of set 1 set to block 1	131	N	N	Y
ADD.D F1, F4, F4	115	116	117	119	120	N	N	N
ADD.D F6, F3, F7	116 I-Cache hit on block 2	117	118	120	121	N	N	N
SUB.D F2, F7, F4	117	132 WAW hazard on F2 to LD.D F2, 8(R5)	133	135	136	N	Y	N
MUL.D F6, F4, F5	132	133	134	164	165	N	N	N
ADD.D F7, F2, F6	133	134	166 RAW hazard on F6 to MUL.D F6, F4, F5	168	169	Y	N	N
DADDI R4, R4, 4	134 I-Cache hit on block 3	135	136	137	138	N	N	N
DADDI R5, R5, 4	135	139 structural hazard, not enough integer ALU	140	141	142	N	N	Y
DSUB R1, R1, R2	139	143 structural hazard, not enough integer ALU	144	145	146	N	N	Y
BNE R1, R3, GG	143	144	147 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	144 I-Cache hit on block 0					N	N	N
HLT	148					N	N	N

Total number of access requests for instruction cache: 30
Number of instruction cache hits: 25
Total number of access requests for data cache: 8
Number of data cache hits: 6