Test WAW

Config.txt

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000011000010101010101
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

```
    LI R4, 256
    LI R5, 256
    LI R1, 3
    LI R2, 1
    LI R3, 1
GG: L.D F1, 4(R4)
    L.D F2, 8(R5)
    ADD.D  F4,   F6,  F2
    SUB.D  F5,   F7,  F1
    MUL.D  F6,   F1, F5
    ADD.D  F6,  F1,  F7
    ADD.D  F7,  F2,  F6
    DADDI  R4,   R4,  4
    DADDI  R5,   R5,  4
    DSUB  R1,   R1,  R2
    BNE  R1,   R3,  GG
    HLT
    HLT
```

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	13 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 filled with 0x00~0x0F	14	15	16	17	N	N	N
LI R5, 256	14	18 structural hazard	19	20	21	N	N	Y
LI R1, 3	18	22 structural hazard	23	24	25	N	N	Y
LI R2, 1	22	26 structural hazard	27	28	29	N	N	Y
LI R3, 1	35 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 filled with 0x10~0x1F	36	37	38	39	N	N	N
GG: L.D F1, 4(R4)	36	37	38	52 D-Cache miss for 0x104~0x10B (260~267) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1	53	N	N	N
L.D F2, 8(R5)	37	54 structural hazard	55	57 D-Cache hit for 0x108~0x10F (264~271) on set 0 block 0 LRU of set 0 set to block 1	58	N	N	Y
ADD.D F4, F6, F2	54	55	59 RAW hazard on F2 to L.D F2, 8(R5)	61	62	Y	N	N
SUB.D F5, F7, F1	67 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 2 filled with 0x20~0x2F	68	69	71	72	N	N	N
MUL.D F6, F1, F5	68	69	73 RAW hazard on F5 to SUB.D F5, F7, F1	103	104	Y	N	N
ADD.D F6, F1, F7	69	105 WAW hazard on F6 to MUL.D F6, F1, F5	106	108	109	N	Y	N
ADD.D F7, F2, F6	105	106 r	110 RAW hazard on F6 to ADD.D F6, F1, F7	112	113	Y	N	N
DADDI R4, R4, 20	118 I-Cache miss 1fetch+3cycle x 4word Mem	119	120	121	122	N	N	N

	I-Cache block 3 filled with 0x30~0x3F							
DADDI R5, R5, 8	119	123 structural hazard, not enough integer ALU	124	125	126	N	N	Y
DSUB R1, R1, R2	123	127 structural hazard, not enough integer ALU	128	129	130	N	N	Y
BNE R1, R3, GG	127	128	131 RAW hazard on R1 to DSUB R1, R1, R2			Y	N	N
HLT	140 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 replaced with 0x40~0x4F					N	N	N
GG: L.D F1, 4(R4)	141 I-Cache hit on block 1	142	143	157 D-Cache miss for 0x120~0x123 (280~287) 2+3cycle x 4word Mem D-Cache set 1 block 0 filled with 0x110~0x11F (272~287) LRU of set 1 set to block 1	158	N	N	N
L.D F2, 8(R5)	142	159 structural hazard	160	162 D-Cache hit for 0x110~0x117(272~279)on set 1 block 0 LRU of set 1 set to block 1	163	N	N	Y
ADD.D F4, F6, F2	159	160	164 RAW hazard on F2 to L.D F2, 8(R5)	166	167	Y	N	N
SUB.D F5, F7, F1	160 I-Cache hit on block 2	161	162	164	165	N	N	N
MUL.D F6, F1, F5	161	162	166 RAW hazard on F5 to SUB.D F5, F7, F1	196	197	Y	N	N
ADD.D F6, F1, F7	162	198 WAW hazard on F6 to MUL.D F6, F1, F5	199	201	202	N	Y	N
ADD.D F7, F2, F6	198	199	203 RAW hazard on F6 to ADD.D F7, F2, F6	205	206	Y	N	N
DADDI R4, R4, 20	199 I-Cache hit on block 3	200	201	202	203	N	N	N
DADDI R5, R5, 8	200	204 structural hazard, not enough integer ALU	205	206	207	N	N	Y
DSUB R1, R1, R2	204	208 structural hazard, not enough integer ALU	209	210	211	N	N	Y
BNE R1, R3, GG	208	209	212			Y	N	N

			RAW hazard on R1 to DSUB R1, R1, R2					
HLT	209 I-Cache hit on block 0					N	N	N
HLT	213					N	N	N

Total number of access requests for instruction cache: 30
Number of instruction cache hits: 25
Total number of access requests for data cache: 8
Number of data cache hits: 6