Memory bus conflict

Config.txt

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

data.txt

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000011000010101010101
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

inst.txt

```
    LI R4, 256
    LI R5, 256
    LI R1, 3
    LI R2, 1
    LI R3, 1
GG: DADDI  R4,   R4,  4
    DADDI  R5,   R5,  4
    DSUB   R1,   R1,  R2
    L.D  F1,  4(R4)
    L.D  F2,  8(R5)
    ADD.D  F4,    F6,  F2
    SUB.D  F5,    F7,  F1
    MUL.D  F6,    F1, F5
    ADD.D  F7,  F2,  F6
    ADD.D  F6,  F1,  F7
    BNE  R1,   R3,  GG
    HLT
    HLT
```

result.txt

Instruction	Fetch	Issue	Read	Exec	Write	RAW	WAW	Struct
LI R4, 256	13 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 filled with 0x00~0x0F	14	15	16	17	N	N	N
LI R5, 256	14	18 structural hazard	19	20	21	N	N	Y
LI R1, 3	18	22 structural hazard	23	24	25	N	N	Y
LI R2, 1	22	26 structural hazard	27	28	29	N	N	Y
LI R3, 1	35 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 filled with 0x10~0x1F	36	37	38	39	N	N	N
GG:DADDI R4, R4, 4	36	37	38	39	40	N	N	N
DADDI R5, R5, 4	37	41 structural hazard on ALU	42	43	44	N	N	Y
L.D F1, 4(R4)	41	42	43	68 Memory bus conflict D-Cache miss for 0x104~0x10B (260~267) 2+3cycle x 4word Mem D-Cache set 0 block 0 filled with 0x100~0x10F (256~271) LRU of set 0 set to block 1	69	N	N	Y
DSUB R1, R1, R2	54 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 2 filled with 0x20~0x2F	55	56	57	58	N	N	N
L.D F2, 8(R5)	55	70 structural hazard	71	73 D-Cache hit for 0x108~0x10F (264~271) on set 0 block 0 LRU of set 0 set to block 1	74	N	N	Y
ADD.D F4, F6, F2	70	71	75 RAW hazard on F2 to L.D F2, 8(R5)	77	78	Y	N	N
SUB.D F5, F7, F1	71	72	73	75	76	N	N	N
MUL.D F6, F1, F5	84 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 3 filled with 0x30~0x3F	85	86	116	117	N	N	N

ADD.D F7, F2, F6	85	86	118 RAW hazard on F6 to MUL.D F6, F1, F5	120	121	Y	N	N
ADD.D F6, F1, F7	86	118 WAW Hazard on F6 to MUL.D F6, F1, F5	122 RAW hazard on F6 to ADD.D F7, F2, F6	124	125	Y	Y	N
BNE R1, R3, GG	118	119	120			N	N	N
HLT	131 I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 0 replaced with 0x40~0x4F					N	N	N
GG:DADDI R4, R4, 4	132 I-Cache hit on block 1	133	134	135	136	N	N	N
DADDI R5, R5, 4	133	137 structural hazard on ALU	138	139	140	N	N	Y
L.D F1, 4(R4)	137	138	139	153 D-Cache hit on set 0 block 0 for the 1st word 0x10C~0x10F (268~271) D-Cache miss for the 2nd word 0x110~0x113 (272~275) 2+3cycle x 4word Mem D-Cache set 0 block 1 filled with 0x120~0x12F (288~287) LRU of set 0 set to block 0	154	N	N	N
DSUB R1, R1, R2	138 I-Cache hit on block 2	141 structural hazard	142	143	144	N	N	Y
L.D F2, 8(R5)	141	155 structural hazard	156	158 D-Cache hit for 0x110~0x117 (272~279) on set 0 block 0 LRU of set 0 set to block 1	159	N	N	Y
ADD.D F4, F6, F2	155	156	160 RAW hazard on F2 to L.D F2, 8(R5)	162	163	Y	N	N
SUB.D F5, F7, F1	156	157	158	160	161	N	N	N
MUL.D F6, F1, F5	157 I-Cache hit on block 3	158	162 RAW hazard on F5 to SUB.D F5, F7, F1	192	193	Y	N	N
ADD.D F7, F2, F6	158	162 structural hazard on FP adder	194 RAW hazard on F6 to MUL.D F6, F1, F5	196	197	Y	N	Y
ADD.D F6, F1, F7	162	194 WAW Hazard on F6 to MUL.D F6, F1, F5	198 RAW hazard on F6 to ADD.D F7, F2, F6	200	201	Y	Y	N
BNE R1, R3, GG	194	195	196			N	N	N
HLT	195 I-Cache hit on block 0	196				N	N	N

HLT	196					N	N	N

Total number of access requests for instruction cache: 30
Number of instruction cache hits: 25
Total number of access requests for data cache: 8
Number of data cache hits: 5