Write Allocation

### *Config.txt*

FP adder: 2, 2
FP Multiplier: 2, 30
FP divider: 1, 50
I-Cache: 4, 4

### *data.txt*

00000000000000000000000000000010
00000000000000000010000101010101
00000000001001110101010100010100
00000101010111110001010101010101
00000000101010101010101010101111
00000100010010010101110000001010
00000000000000001111111111111111
00000000000000001111111111111111
00000000000000001111100010100110
00000000000000001010101101110110
00000000000101011010011110101011
00000000000100000000000000000111
00000000000000101110000000010101
00000000000000000010101110101101
00000000000000000000000000000000
00000000000001101101010011110101
00000000000000000000000001100001
00000000000000110000101010101001
00000000000000000000010101010101
00000000000000001111111111111000
00000000000000000000000000000011
00000000000000000000000000000001
00000000000000001111100110100110
00000000000000000001010101010101
00000000000001101101010011110101
00000000000001000010101110010101
00000000000001101101111001010101
00000000000000000101010101110100
00000000000001001010101011110101
00000000000000000000000000010101
00000000000111101110000000000000
00000000000001101101010011110100

### *inst.txt*

```
    LI R4, 256
    LI R5, 288
    LI R1, 3
    LI R2, 1
    LI R3, 1
    LI R8, 264
GG: L.D F1, 4(R4)
    L.D F2, 8(R5)
    ADD.D   F4,     F6,   F2
    SUB.D   F5,     F7,   F1
    MUL.D   F6,     F1, F5
    ADD.D   F6,   F1,   F7
    ADD.D   F7,   F2,   F6
    S.D       F6, 0(R8)
    DADDI   R4,     R4,   32
    DADDI   R5,     R5,   32
    DADDI   R8,     R8,   24
    DSUB    R1,     R1,   R2
    BNE   R1,     R3,   GG
    HLT
    HLT
```

***result.txt***

| Instruction | Fetch | Issue | Read | Exec | Write | RAW | WAW | Struct |
|---|---|---|---|---|---|---|---|---|
| LI R4, 256 | 13<br>I-Cache miss<br>1fetch+3cycle x 4word Mem<br>I-Cache block 0 filled with 0x00~0x0F | 14 | 15 | 16 | 17 | N | N | N |
| LI R5, 288 | 14 | 18<br>structural hazard | 19 | 20 | 21 | N | N | Y |
| LI R1, 3 | 18 | 22<br>structural hazard | 23 | 24 | 25 | N | N | Y |
| LI R2, 1 | 22 | 26<br>structural hazard | 27 | 28 | 29 | N | N | Y |
| LI R3, 1 | 35<br>I-Cache miss<br>1fetch+3cycle x 4word Mem<br>I-Cache block 1 filled with 0x10~0x1F | 36 | 37 | 38 | 39 | N | N | N |
| LI R8, 264 | 36 | 40<br>structural hazard | 41 | 42 | 43 | N | N | Y |
| GG: L.D F1, 4(R4) | 40 | 41 | 42 | 67<br>Memory bus conflict<br>D-Cache miss for 0x104~0x10B (260~267)<br>2+3cycle x 4word Mem<br>D-Cache set 0 block 0 filled with 0x100~0x10F (256~271)<br>LRU of set 0 set to block 1 | 68 | N | N | N |
| L.D F2, 8(R5) | 41 | 69<br>structural hazard | 70 | 84<br>D-Cache miss for 0x128~0x12F (296~303)<br>2+3cycle x 4word Mem<br>D-Cache set 0 block 1 filled with 0x120~0x12F (288~303)<br>LRU of set 0 set to block 0 | 85 | N | N | Y |
| ADD.D F4, F6, F2 | 69<br>I-Cache miss<br>1fetch+3cycle x 4word Mem<br>I-Cache block 2 filled with 0x20~0x2F | 70 | 86<br>RAW hazard on F2 to L.D F2, 8(R5) | 88 | 89 | Y | N | N |
| SUB.D F5, F7, F1 | 70 | 71 | 72 | 74 | 75 | N | N | N |
| MUL.D F6, F1, F5 | 71 | 72 | 76<br>RAW hazard on F5 to SUB.D F5, F7, F1 | 106 | 107 | Y | N | N |
| ADD.D F6, F1, F7 | 72 | 108<br>WAW hazard on F6 to MUL.D F6, F1, F5 | 109 | 111 | 112 | N | Y | Y |
| ADD.D F7, F2, F6 | 108<br>I-Cache miss<br>1fetch+3cycle x 4word Mem | 109 | 113<br>RAW hazard on F6 to ADD.D F6, F1, F7 | 115 | 116 | Y | N | N |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | I-Cache block 3 filled with 0x30~0x3F | | | | | | | |
| S.D F6, 0(R8) | 109 | 110 | 113<br>RAW hazard on F6 to ADD.D F6, F1, F7 | 115<br>D-Cache hit for 0x108~0x10F(264~271)on set 0 block 0<br>LRU of set 0 set to block 1 | 116 | Y | N | N |
| DADDI R4, R4, 32 | 110 | 111 | 112 | 113 | 114 | N | N | N |
| DADDI R5, R5, 32 | 111 | 115<br>structural hazard, not enough integer ALU | 116 | 117 | 118 | N | N | Y |
| DADDI R8, R8, 24 | 124<br>I-Cache miss 1fetch+3cycle x 4word Mem<br>I-Cache block 0 replaced with 0x40~0x4F | 125 | 126 | 127 | 128 | N | N | N |
| DSUB R1, R1, R2 | 125 | 129<br>structural hazard, not enough integer ALU | 130 | 131 | 132 | N | N | Y |
| BNE R1, R3, GG | 129 | 130 | 133<br>RAW hazard on R1 to DSUB R1, R1, R2 | | | Y | N | N |
| HLT | 130 | | | | | N | N | N |
| GG: L.D F1, 4(R4) | 134<br>I-Cache hit on block 1 | 135 | 136 | 138<br>D-Cache hit for 0x124~0x12C (292~300) on set 0 block 1<br>LRU of set 0 set to block 0 | 139 | N | N | N |
| L.D F2, 8(R5) | 135 | 140<br>structural hazard | 141 | 167<br>D-Cache miss for 0x148~0x14F (328~335)<br>Set 0 block 0 should be replaced but dirty<br>2+3cycle x 4word Write +3cycle x 4word Read<br>D-Cache set 0 block 0 replaced with 0x140~0x14F (320~335)<br>LRU of set 0 set to block 1 | 168 | N | N | Y |
| ADD.D F4, F6, F2 | 140<br>I-Cache hit on block 2 | 141 | 169<br>RAW hazard on F2 to L.D F2, 8(R5) | 171 | 172 | Y | N | N |
| SUB.D F5, F7, F1 | 141 | 142 | 143 | 145 | 146 | N | N | N |
| MUL.D F6, F1, F5 | 142 | 143 | 147<br>RAW hazard on F5 to SUB.D F5, F7, F1 | 177 | 178 | Y | N | N |
| ADD.D F6, F1, F7 | 143 | 179<br>WAW hazard on F6 to MUL.D F6, F1, F5 | 180 | 182 | 183 | N | Y | Y |
| ADD.D F7, F2, F6 | 179<br>I-Cache hit on block 3 | 180 | 184<br>RAW hazard on F6 to ADD.D F6, F1, F7 | 186 | 187 | Y | N | N |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S.D F6, 0(R8) | 180 | 181 | 184<br>RAW hazard on F6 to ADD.D F6, F1, F7 | 186<br>D-Cache hit for 0x120~0x128(288~296)on set 0 block 1<br>LRU of set 0 set to block 0 | 187 | Y | N | N |
| DADDI R4, R4, 32 | 181 | 182 | 183 | 184 | 185 | N | N | N |
| DADDI R5, R5, 32 | 182 | 186<br>structural hazard, not enough integer ALU | 187 | 188 | 189 | N | N | Y |
| DADDI R8, R8, 24 | 186<br>I-Cache hit on block 0 | 190<br>structural hazard, not enough integer ALU | 191 | 192 | 193 | N | N | Y |
| DSUB R1, R1, R2 | 190 | 194<br>structural hazard, not enough integer ALU | 195 | 196 | 197 | N | N | Y |
| BNE R1, R3, GG | 194 | 195 | 198<br>RAW hazard on R1 to DSUB R1, R1, R2 | | | Y | N | N |
| HLT | 195 | | | | | N | N | N |
| HLT | 211<br>I-Cache miss 1fetch+3cycle x 4word Mem I-Cache block 1 replaced with 0x50~0x5F | | | | | N | N | N |

Total number of access requests for instruction cache: 35
Number of instruction cache hits: 29
Total number of access requests for data cache: 12
Number of data cache hits: 9