There are 7 files namely alu.vhd, control_fsm.vhd, data_memory.vhd, flags.vhd, register_file.vhd, stage4.vhd and testbench.vhd.

alu.vhd:	handles all the arithmetic operations and also incrementes pc.
data_memory.vhd:	reads and write in the program memory and the data memory. The size of data_memory is 128x32 out of which first half stores program memory and second half stores data memory.
flags.vhd:	it sets the C, N, V and Z flags.
register_file.vhd:	it reads and write in the 16 registers of the program.
control_fsm.vhd:	it sets all the control signals depending on the current state and update the state also.
stage4.vhd:	this is glue code for this stage.

(At some places all the functionality are not implemented because only few instructions have to be implemented in this stage (especially in flags.vhd) like functionality related to shift and rotate operations).

The code is almost similar to the code in stage 3. The changes made are:

- in flag.vhd code for updating flags corresponding to all the DP instruction has been added.
- in control_fsm.vhd write enable of register will be zero for DP instructions like cmn, tst, teq in addition to cmp.
- in control_fsm.vhd check for all the conditions have been added (i.e. now in addition to beq and bne instructions like bgt, bhi, bmi, bcc, etc. will also work correctly).