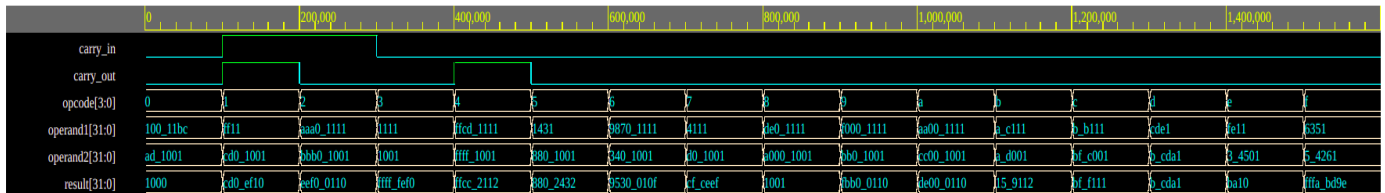


There are 8 files namely alu.vhd, register_file.vhd, data_memory.vhd, program_memory.vhd, testbench_alu.vhd, testbench_rf.vhd, testbench_dm.vhd and testbench_pm.vhd.

1. alu.vhd:

(a) EPWave

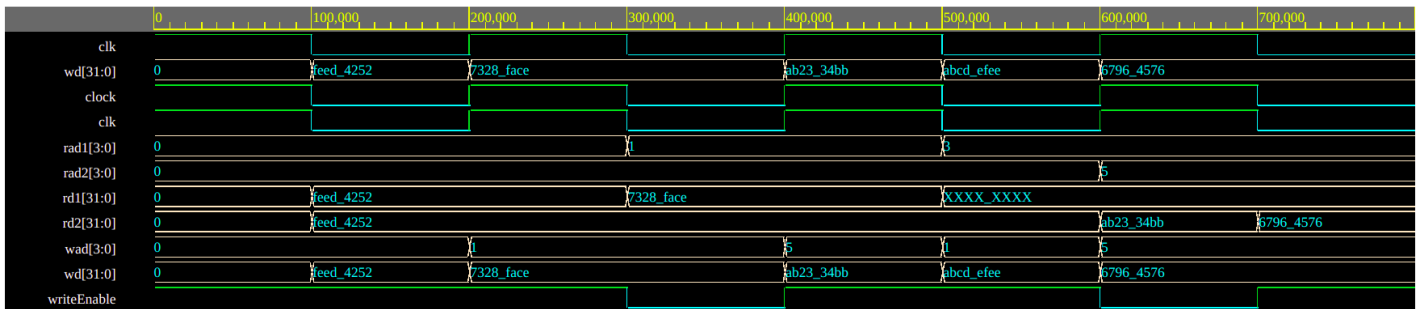


(b) Synthesis Results

```
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: IOs                    102     210     48.57%
# Info: Global Buffers          0       32      0.00%
# Info: LUTs                     420    63400    0.66%
# Info: CLB Slices              105    15850    0.66%
# Info: Dffs or Latches          0    126800    0.00%
# Info: Block RAMs               0      135    0.00%
# Info: DSP48E1s                0      240    0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: ALU    View: rtl
# Info: *****
# Info: Number of ports :                102
# Info: Number of nets :                832
# Info: Number of instances :           763
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of LUTs :                420
# Info: Number of Primitive LUTs :      421
# Info: Number of LUTs with LUTNM/HLUTNM :      2
# Info: Number of MUX CARRYs :          142
# Info: Number of accumulated instances :      763
# Info: *****
# Info: IO Register Mapping Report
# Info: *****
# Info: Design: work.ALU.rtl
```

2. register_file.vhd:

(a) EPWave

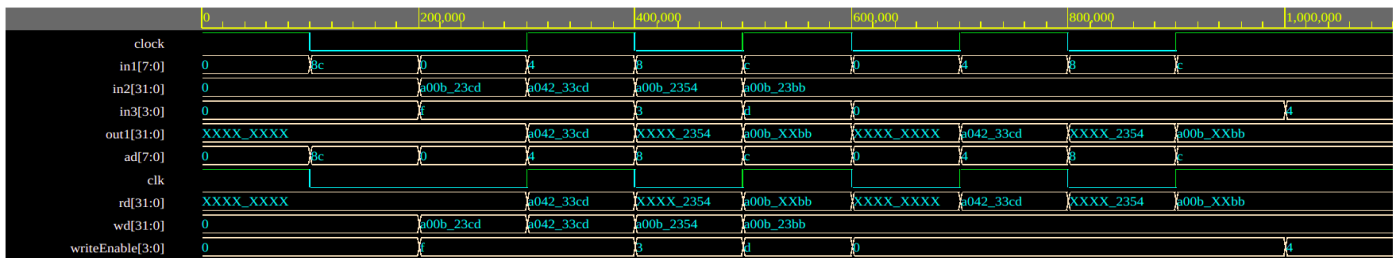


(b) Synthesis Results

```
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    110     210     52.38%
# Info: Global Buffers          1       32      3.12%
# Info: LUTs                    272    63400   0.43%
# Info: CLB Slices              68     15850   0.43%
# Info: Dffs or Latches         512    126800  0.40%
# Info: Block RAMs              0       135     0.00%
# Info: DSP48E1s                0       240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: Register_File_16x32    View: behavioral
# Info: *****
# Info: Number of ports :                110
# Info: Number of nets :                 218
# Info: Number of instances :            110
# Info: Number of references to this view :      0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :        512
# Info: Number of LUTs :                 272
# Info: Number of Primitive LUTs :        272
# Info: Number of MUXF7 :                128
# Info: Number of MUXF8 :                 64
# Info: Number of accumulated instances :    1086
# Info: *****
# Info: IO Register Mapping Report
# Info: *****
# Info: Design: work.Register_File_16x32.behavioral
```

3. data_memory.vhd:

(a) EPWave



(b) Synthesis Results

```
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used    Avail    Utilization
# Info: -----
# Info: I/Os                    77      210     36.67%
# Info: Global Buffers          0       32      0.00%
# Info: LUTs                    898    63400    1.42%
# Info: CLB Slices              256    15850    1.62%
# Info: Dffs or Latches         2048   126800    1.62%
# Info: Block RAMs              0      135     0.00%
# Info: DSP48E1s                0      240     0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: Data_Memory_64x32    View: behavioral
# Info: *****
# Info: Number of ports :                77
# Info: Number of nets :                148
# Info: Number of instances :            75
# Info: Number of references to this view :    0
# Info: Total accumulated area :
# Info: Number of Dffs or Latches :        2048
# Info: Number of LUTs :                898
# Info: Number of Primitive LUTs :        900
# Info: Number of LUTs with LUTNM/HLUTNM :    4
# Info: Number of MUXF7 :                64
# Info: Number of MUXF8 :                32
# Info: Number of accumulated instances :    3120
# Info: *****
# Info: IO Register Mapping Report
# Info: *****
# Info: Design: work.Data_Memory_64x32.behavioral
```

4. program_memory.vhd:

(a) EPWave

	0	200,000	400,000	600,000	800,000
in1[7:0]	0	4	8	c	10
out1[31:0]	1239_843f	0	1239_843f	0	1239_843f
ad[7:0]	0	4	8	c	10
rd[31:0]	1239_843f	0	1239_843f	0	1239_843f

(b) Synthesis Results

```
# Info: Device Utilization for 7A100TCSG324
# Info: *****
# Info: Resource                Used      Avail    Utilization
# Info: -----
# Info: I/Os                    40       210     19.05%
# Info: Global Buffers          0        32      0.00%
# Info: LUTs                     1      63400   0.00%
# Info: CLB Slices               1     15850   0.01%
# Info: Dffs or Latches          0    126800   0.00%
# Info: Block RAMs               0       135   0.00%
# Info: DSP48E1s                 0       240   0.00%
# Info: -----
# Info: *****
# Info: Library: work    Cell: Program_Memory_64x32    View: behavioral
# Info: *****
# Info: Number of ports :                40
# Info: Number of nets :                 36
# Info: Number of instances :            35
# Info: Number of references to this view :    0
# Info: Total accumulated area :
# Info: Number of LUTs :                 1
# Info: Number of Primitive LUTs :       1
# Info: Number of accumulated instances :   35
# Info: *****
# Info: IO Register Mapping Report
# Info: *****
# Info: Design: work.Program_Memory_64x32.behavioral
```