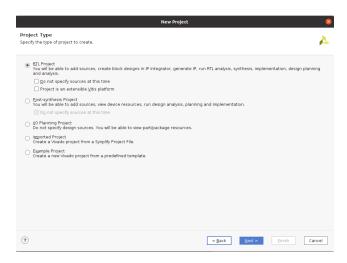
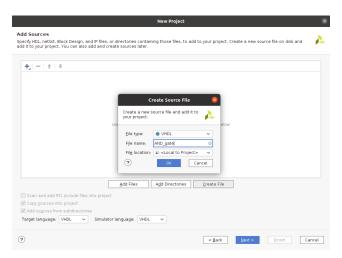
Vivado tutorial

- 1. To launch Vivado, type **vivado** in the terminal.
- 2. When the tool opens, click on Create New project and click Next.
- 3. Select the project directory and name.
- 4. In the next dialog box, select **RTL project.**



5. Create a new file names **AND_gate.** Select the file type as VHDL. Ensure that Target and simulator language is VHDL.



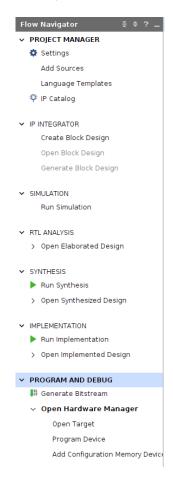
6. In the next dialog window, add the provided basys3.xdc file using "Add Files".

- 7. Select part number xc7a35tcpg236-1 and click next. After this the project creation is done.
- 8. Under design source, double click **AND_gate** file to open it in the editor and add the following code for the basic AND gate.

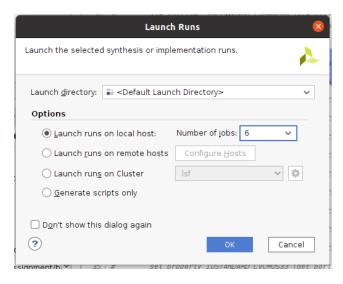
```
entity AND_gate is
    Port ( sw : in STD_LOGIC_VECTOR (1 downto 0);
        C : out STD_LOGIC);
end AND_gate;
architecture Behavioral of AND_gate is
begin
    C <= sw(0) and sw(1);
end Behavioral;</pre>
```

9. Next under the **Constraints section**, edit the **basys3.xdc** file to connect the switches and LED to the declared port. In this module, switches V17 and V16 act as inputs to the gate and LED U16 as the output of the gate.

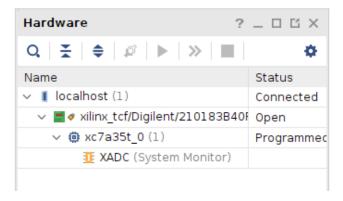
10. Under the Flow Navigator, Click on Run synthesis then Run implementation.



(a) Additional info: Number of jobs can be increased depending upon the available cores. This may improve the running time. For now, use the default value given in the dialog box.



- 11. After this click on Generate Bitstream.
- 12. Once this is done, click on Open Hardware Manager => Open Target => Auto Connect. Ensure that basys3 board is connected to the system via micro-USB cable.



- 13. Click on **Program Device**. Make sure the correct bit file is selected.
- 14. Once the process is complete, toggle the bottom right corner switches (V16 snd V17, the AND gate inputs). This should change the LED (LD0/U16) according to the AND gate logic.

