COL215 Digital Logic and System Design

Department of Computer Science & Engineering

Lab instructions

- **Lab Timings**: 2-5PM
- **Lab Venue**: Room-502, Digital Hardware Design Lab, Bharti School Building
- **Schedule**: Class is divided into five groups with the following schedule:

Group	**Lab session**
Group1	Monday
Group2	Tuesday
Group3	Wednesday
Group4	Thursday
Group5	Friday

General Instructions:

1. Students will work in teams of two. Team partner cannot be changed during the semester. You need to find a partner within your group. Kindly fill the following form: `https://forms.gle/9g69R5Vhzq3zEiUN7`.
2. If you do not have GCL account, kindly fill the form available on the moodle and submit it on the lab day.
3. Lab assignment will require you to work with VHDL language. Before the lab session you should be ready with your design, and during the session, perform validation of the design by downloading it into the FPGA board.
4. Group division is as follows:

COL215P	`https://bit.ly/3d97RdS`
COL215	`https://bit.ly/3JDOK9H`

5. VHDL resources
   - IEEE document: `https://ieeexplore.ieee.org/document/8938196`
   - Basys 3 board reference manual: `https://digilent.com/reference/_media/basys3:basys3_rm.pdf`
   - Online VHDL simulator: `https://www.edaplayground.com/x/A4`