

# Communications

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# **Scope of Commun ication**

Telephones  
and Cell  
Phones



# Scope of Communication

## Internet



# **Scope of Commun ication**

Wireless  
networks



# **Scope of Commun ication**

Satellite  
Networks

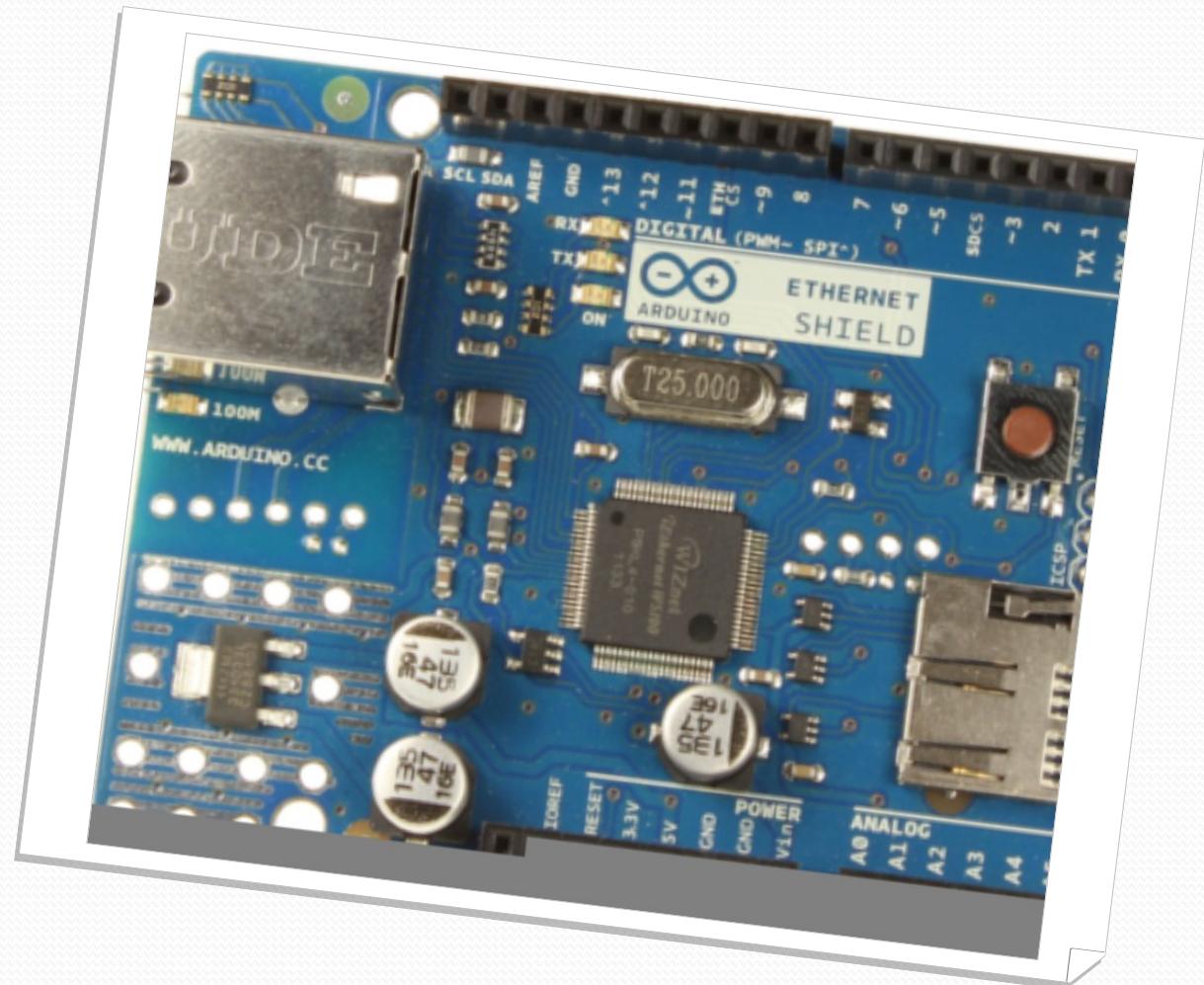




# **Our Interests !!**

# Arduino Ethernet Shield

Uses SPI to  
communicate with  
Master board



# Accelero meters

## Communication through SPI

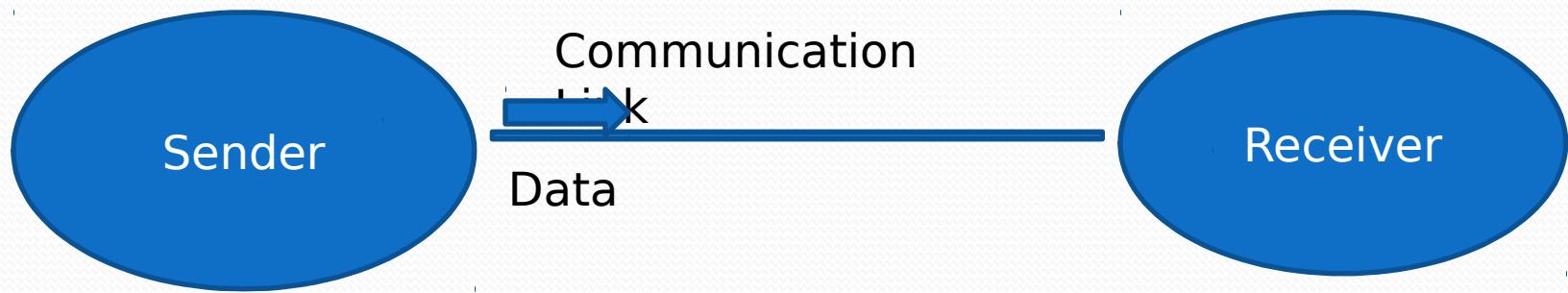


# JPG Color Camera

Uses UART to  
communicate  
with Master  
board



# Essentials of Communication



But this simple model requires many guarantees.

# Guarantees in Communications

- The communication link exists.
- The communication link is sound.
- The sender and receiver are the correct nodes.
- The sender is sending the correct data.
- The receiver is able to correctly interpret the incoming data.

# Protocols in Communication

- In order to have robust communication, the guarantees needs to be realized.
- To do so, we need an elaborate and standardized mechanism.
- These standard rules that defines the parameters of communications and ensures these guarantees are called protocol.

# Advantages of Protocols

- Standardized, so interoperability is ensured.
- Usually include error-detection and error-correction mechanisms.
- Are available as implemented chips that can be directly used.

# Types of Protocols

- There are different ways of categorizing protocols
- First Categorization :

Serial Mode Transfer

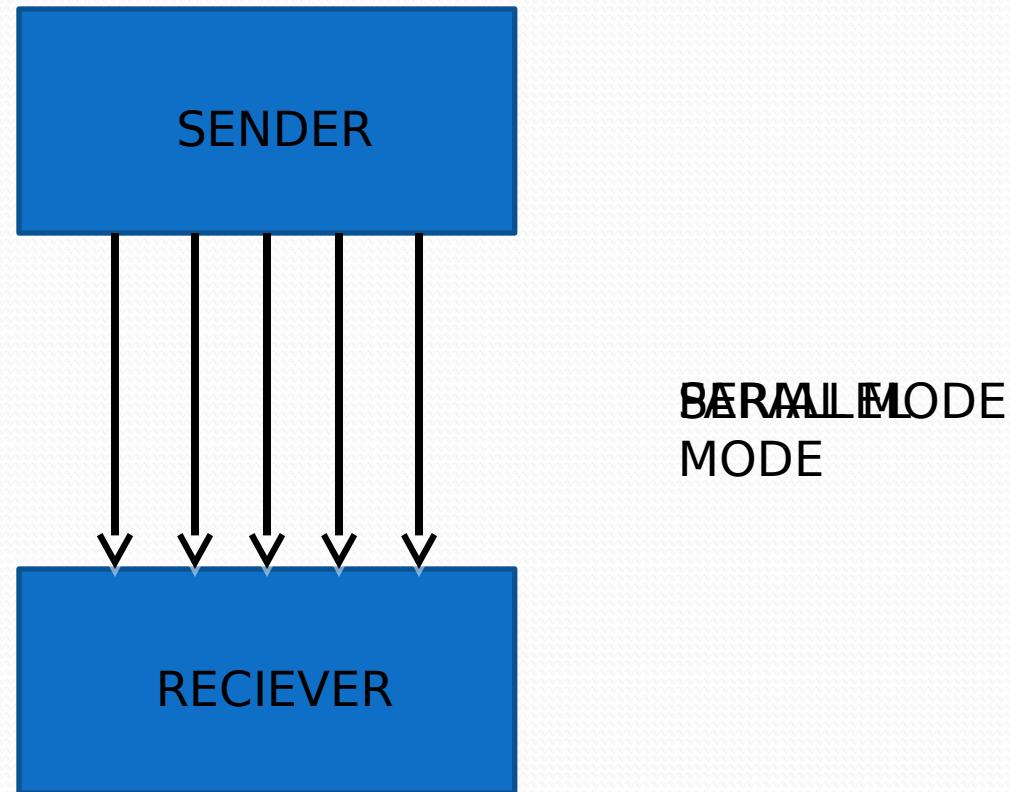
Parallel Mode Transfer

- Second Categorization :

Synchronous  
Mode  
Transfer

Asynchronous  
Mode  
Transfer

# Serial and Parallel Mode



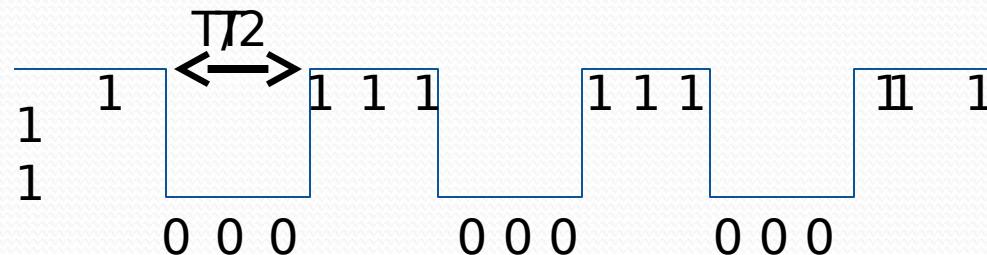
# Serial Vs Parallel Mode

| Parameter   | Serial Mode | Parallel Mode |
|-------------|-------------|---------------|
| Reliability | ✓ Reliable  | Unreliable    |
| Speed       | ✗ Slow      | Fast ✓        |
| Power       | ✓ Low       | High ✗        |
| Cost        | ✓ Low       | High ✗        |
| Complexity  | ✗ High      | Low ✓         |
| Range       | ✓ Long      | Short ✗       |

# Synchronous and Asynchronous Mode

- Pertains to sender-receiver synchronization.
- Sender sends data at a certain speed. For flexibility, protocols allow for multiple speeds.

# Need of Synchronization

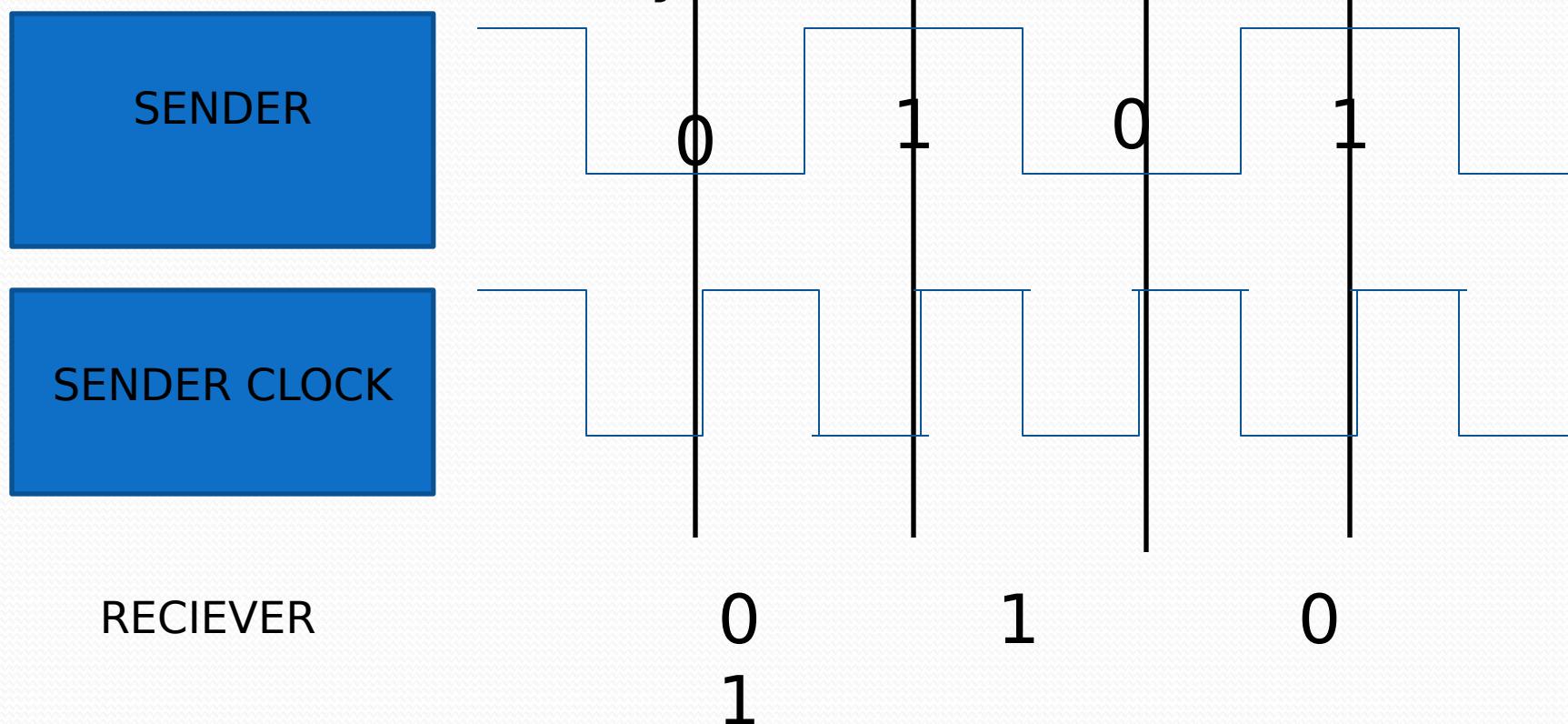


Suppose Sender sends data with a Time Period  
of  $T$

What if Receiver doesn't know the speed and assume it to be  
say  $T/2$   
The Data received will be

# Synchronous Mode

- Sender sends a clock signal along with data at every rising / falling edge of the clock, the data value is read by the receiver.



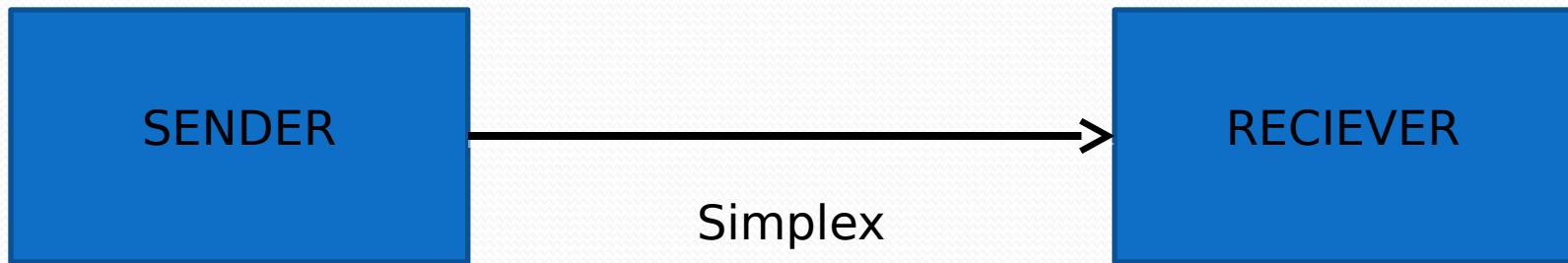
# Asynchronous Mode

- There is no clock signal.
- The receiver and the sender communicate at a predetermined speed (bauds or bits per second).
- Baud Rate : Baud Rate is a measurement of transmission speed in asynchronous communication. The devices that allows communication must all agree on a single speed of information - 'bits per second'.

# Synchronous Vs Asynchronous Mode

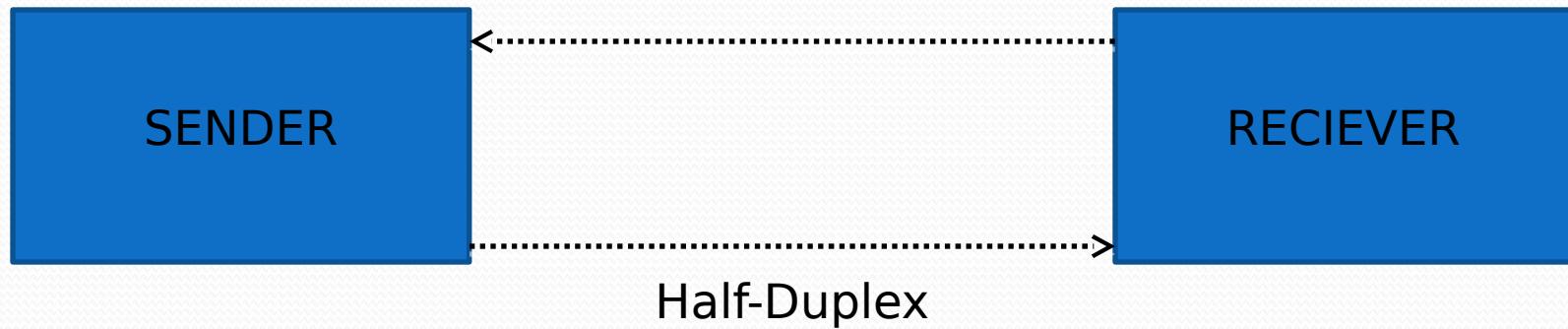
| Parameter   | Synchronous   | Asynchronous  |
|-------------|---------------|---------------|
| Reliability | ✓ reliable    | Error ✗ prone |
| Cost        | ✗ expensive   | Ir✓ensive     |
| Complexity  | ✗ complicated | ✓ imple       |

# Transmission Modes



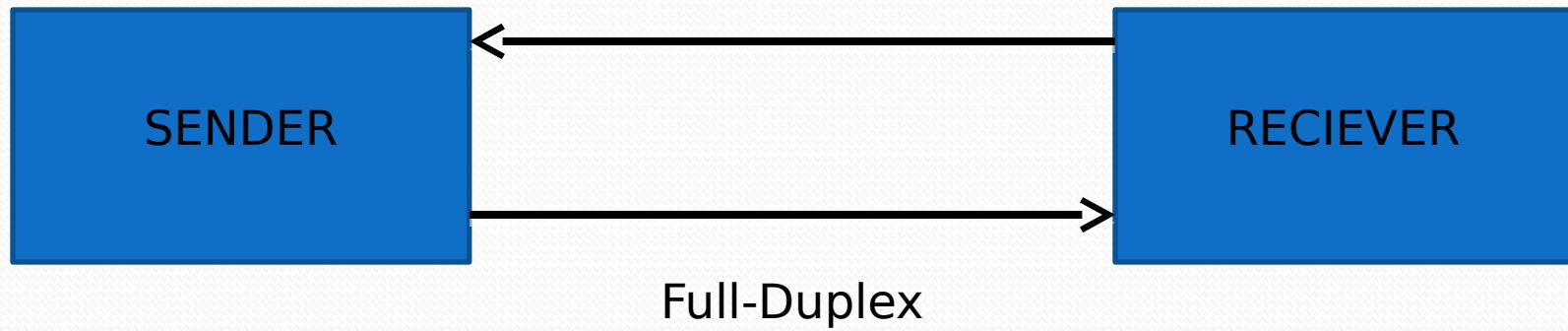
Only one way transmission takes place

# Transmission Modes



Two way transmission takes place but only one end can communicate at a time

# Transmission Modes



Two way transmission takes place and both end can communicate simultaneously

# SPI - Serial Peripheral Interface

# SPI

- Serial ??
- Because it works on serial mode of transfer. It is also synchronous and full duplex.
- Peripheral Interface.
- Because it has the capability of communicate with many nodes.
- How?? Let us see.

# SPI

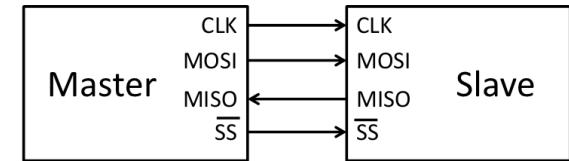
- In SPI, the sender and receiver follows a master-slave relationship.
- There may be multiple nodes in the network.
- One node is master, the rest are slaves.
- The communication is always initiated by the master.
- The slaves can communicate only with the master.
- How do master selects the slave??

# SPI Schematics: Single Slave



# SPI Pins

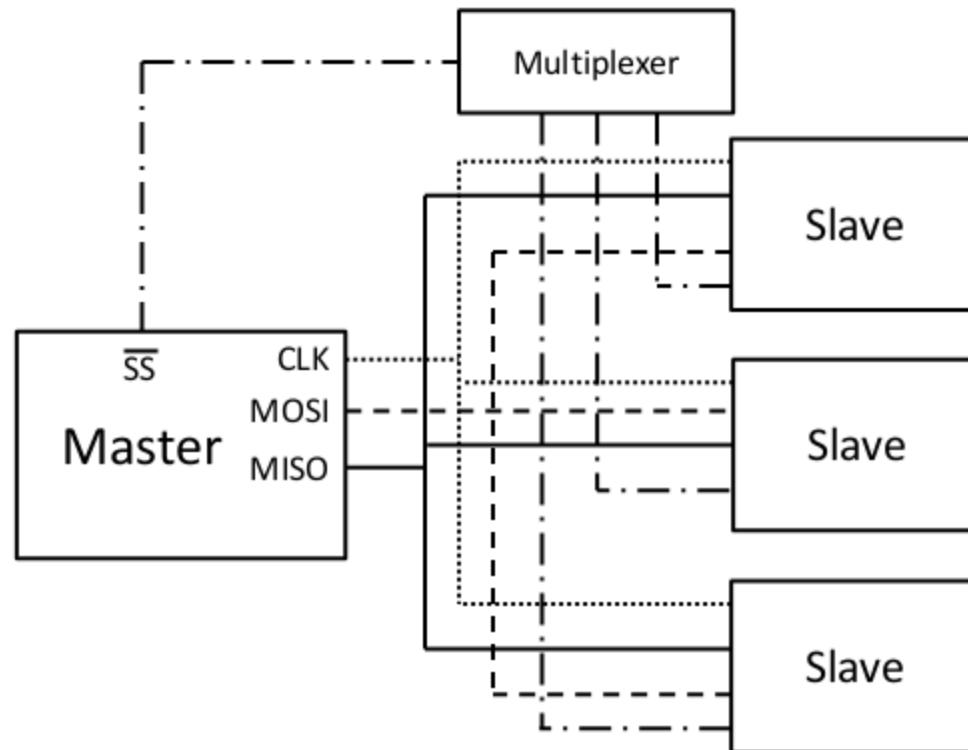
- CLK is generated by Master and is used as the mode is synchronous.
- MOSI is Master Out Slave In: Data sent by Master to Slave.
- MISO is Master In Slave Out: Data sent by Slave to Master.
- $\overline{SS}$  is slave select: Slave communicates with Master only if this pin's value is set as LOW.



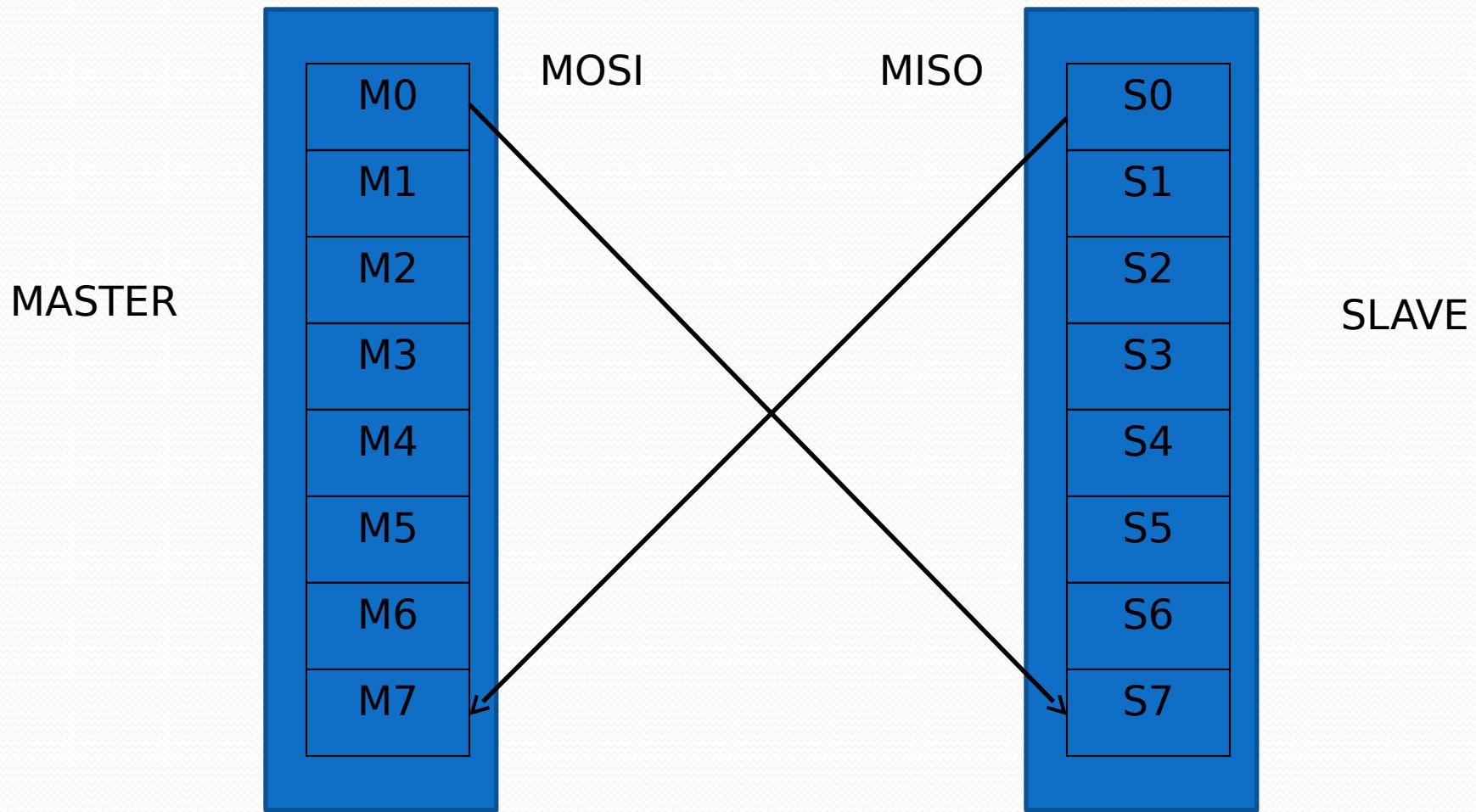
# SPI Schematics: Single Slave



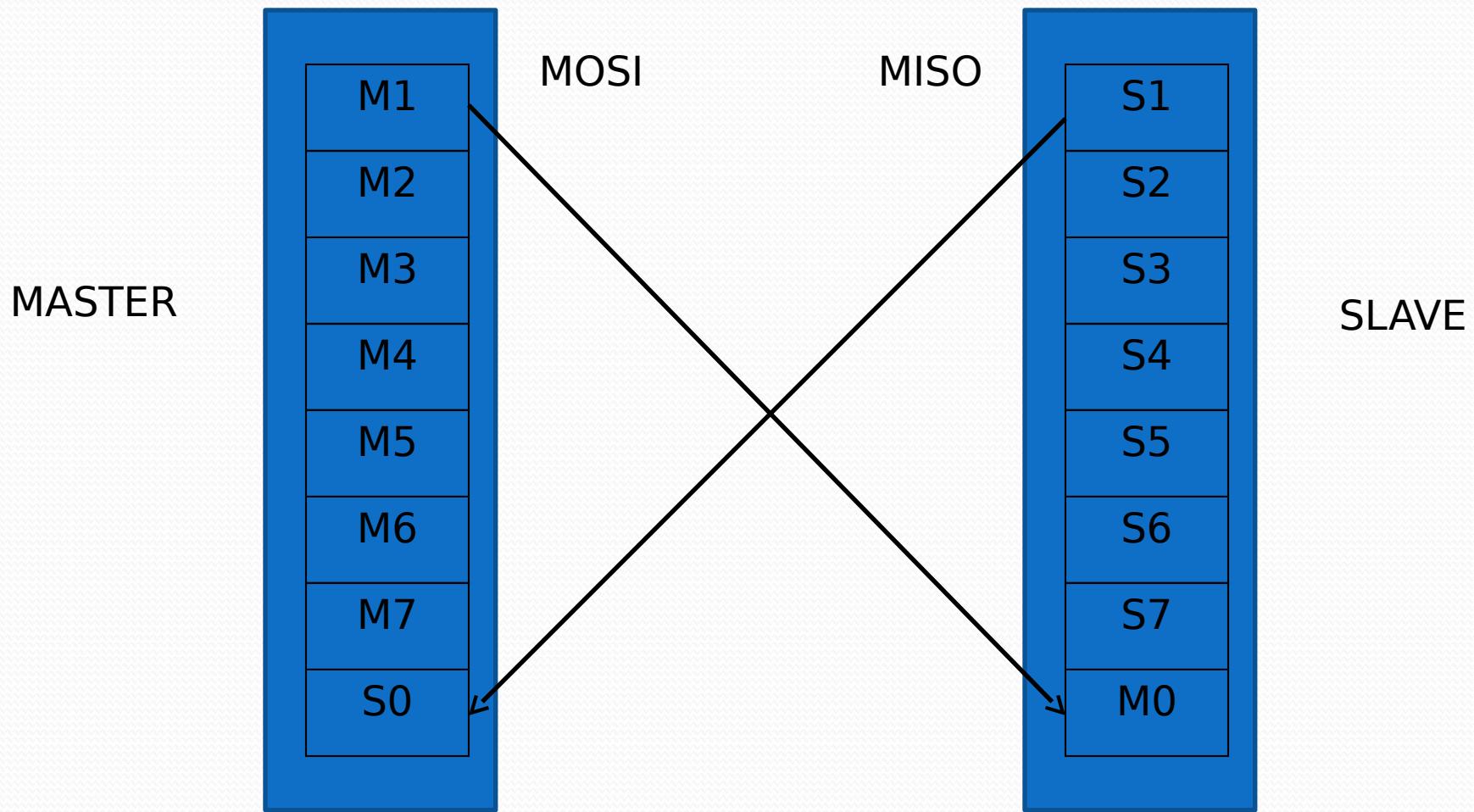
# SPI Schematics: Multiple Slaves



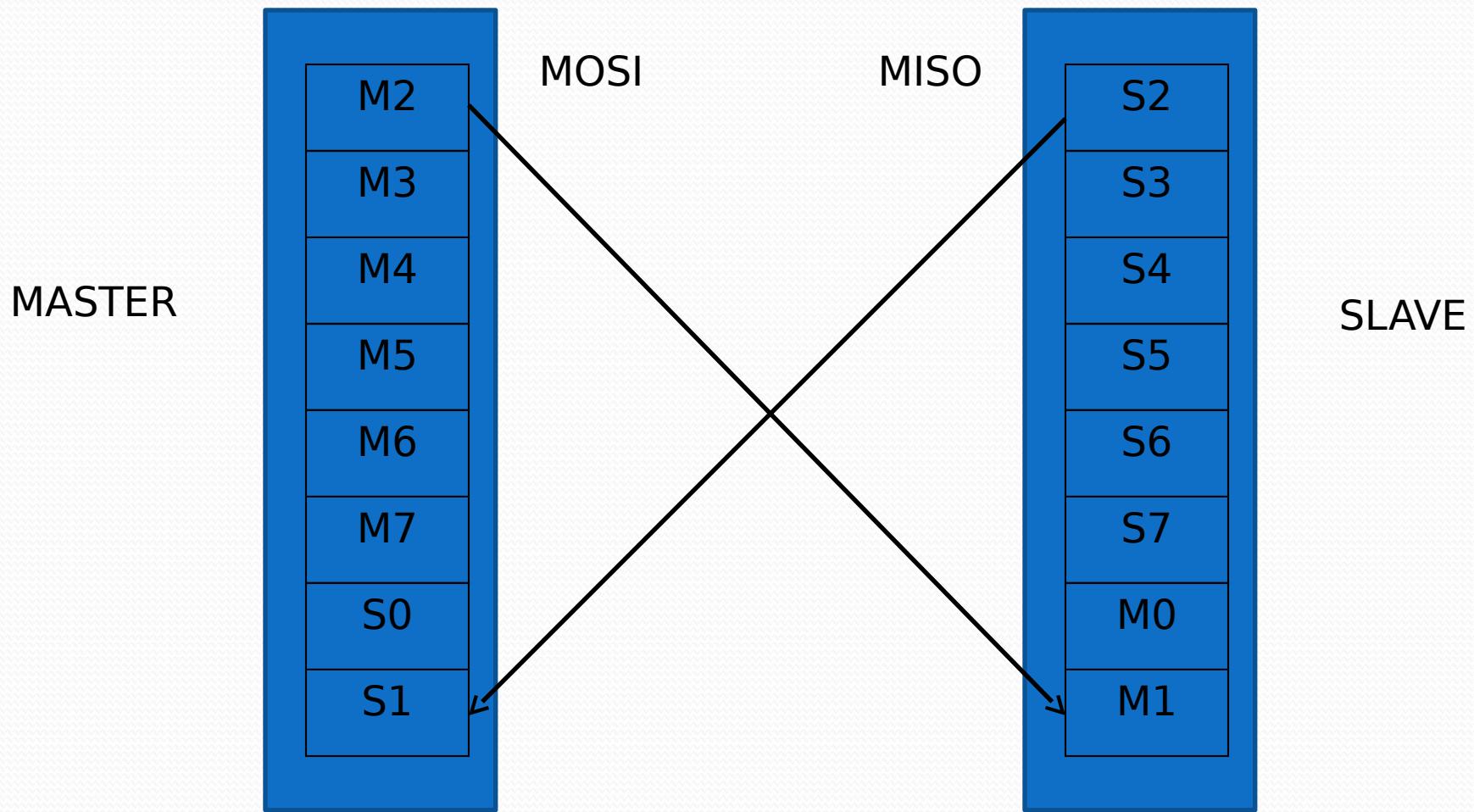
# Data Transfer in SPI



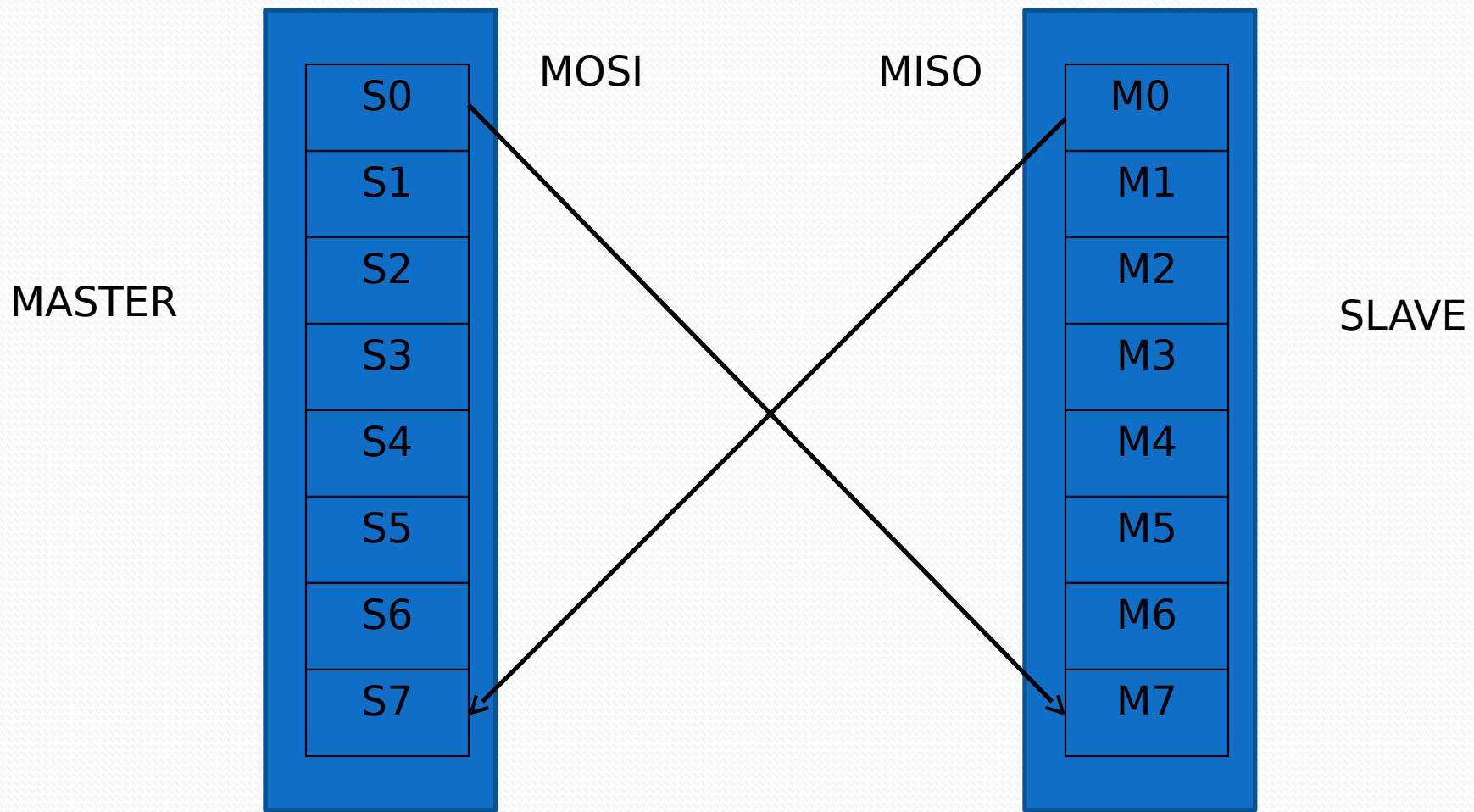
# Data Transfer in SPI



# Data Transfer in SPI



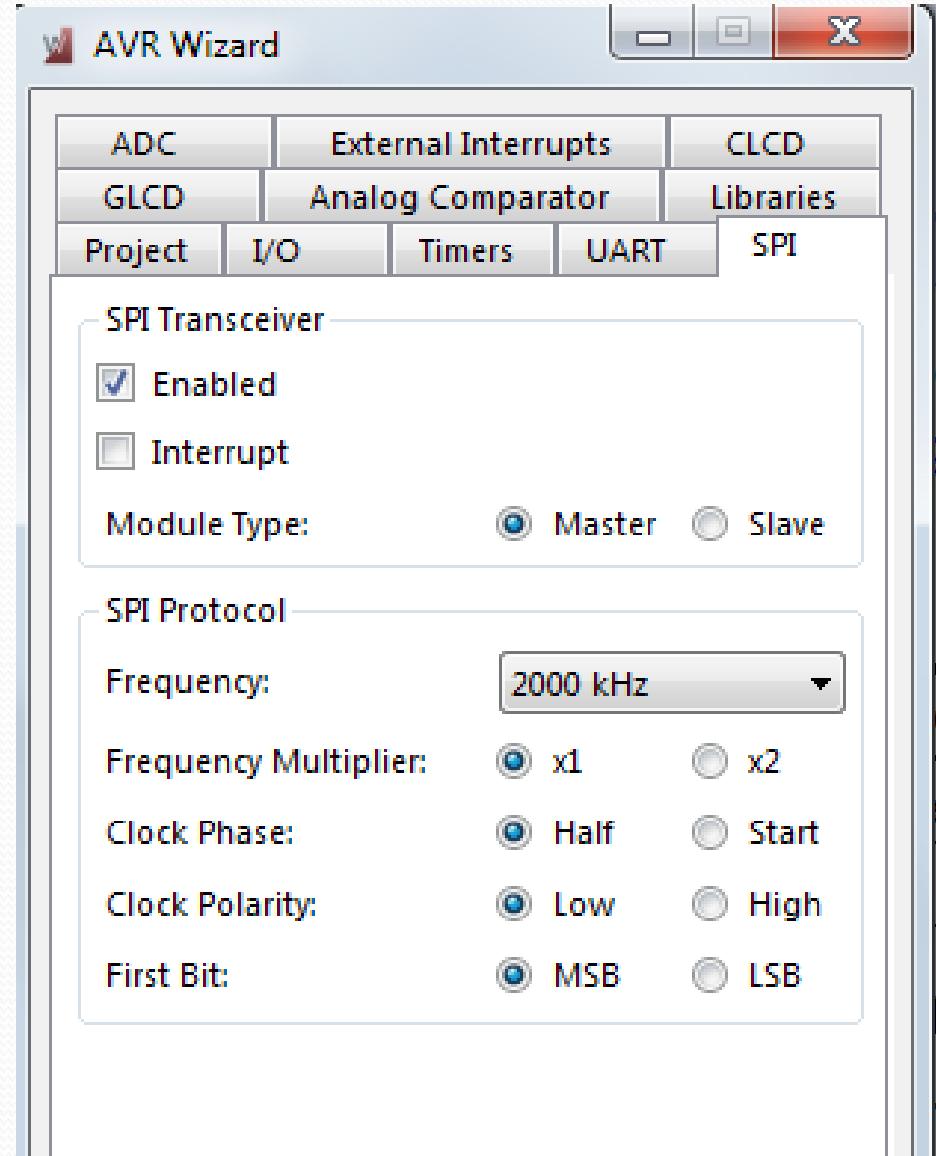
# Data Transfer in SPI



# SPI in Atmega 16

|             |     |    |    |             |
|-------------|-----|----|----|-------------|
| (XCK/T0)    | PB0 | 1  | 40 | PA0 (ADC0)  |
| (T1)        | PB1 | 2  | 39 | PA1 (ADC1)  |
| (INT2/AIN0) | PB2 | 3  | 38 | PA2 (ADC2)  |
| (OC0/AIN1)  | PB3 | 4  | 37 | PA3 (ADC3)  |
| (SS)        | PB4 | 5  | 36 | PA4 (ADC4)  |
| (MOSI)      | PB5 | 6  | 35 | PA5 (ADC5)  |
| (MISO)      | PB6 | 7  | 34 | PA6 (ADC6)  |
| (SCK)       | PB7 | 8  | 33 | PA7 (ADC7)  |
| RESET       |     | 9  | 32 | AREF        |
| VCC         |     | 10 | 31 | GND         |
| GND         |     | 11 | 30 | AVCC        |
| XTAL2       |     | 12 | 29 | PC7 (TOSC2) |
| XTAL1       |     | 13 | 28 | PC6 (TOSC1) |
| (RXD)       | PD0 | 14 | 27 | PC5 (TDI)   |
| (TXD)       | PD1 | 15 | 26 | PC4 (TDO)   |
| (INT0)      | PD2 | 16 | 25 | PC3 (TMS)   |
| (INT1)      | PD3 | 17 | 24 | PC2 (TCK)   |
| (OC1B)      | PD4 | 18 | 23 | PC1 (SDA)   |
| (OC1A)      | PD5 | 19 | 22 | PC0 (SCL)   |
| (ICP1)      | PD6 | 20 | 21 | PD7 (OC2)   |

# SPI Coding



# Clock Polarity (CPOL)

- The value of CPOL bit decides the value of Clock (SCK) in its idle state.
- When CPOL = 1 , SCK is 5V in idle state.
- When CPOL = 0 , SCK is 0V in idle state.

| CPOL     | Leading (First) Edge | Trailing (Last) Edge |
|----------|----------------------|----------------------|
| 0 (low)  | Rising               | Falling              |
| 1 (high) | Falling              | Rising               |

# Clock Phase ( CPHA)

- The settings of the Clock Phase bit (CPHA) determine if data is sampled on the leading (first) or trailing (last) edge of SCK

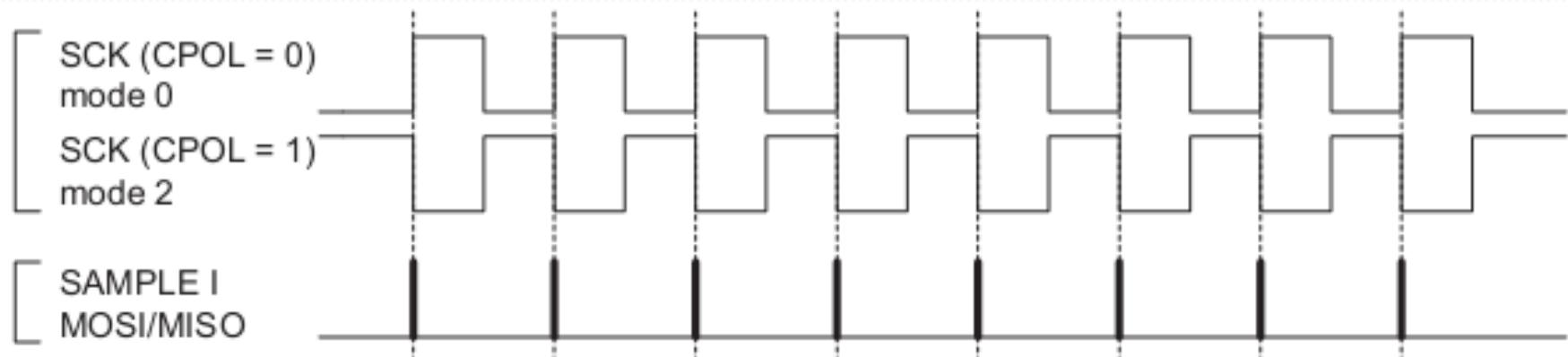
| CPHA      | Sample        |
|-----------|---------------|
| 0 (half)  | Leading Edge  |
| 1 (start) | Trailing Edge |

# Modes of SPI

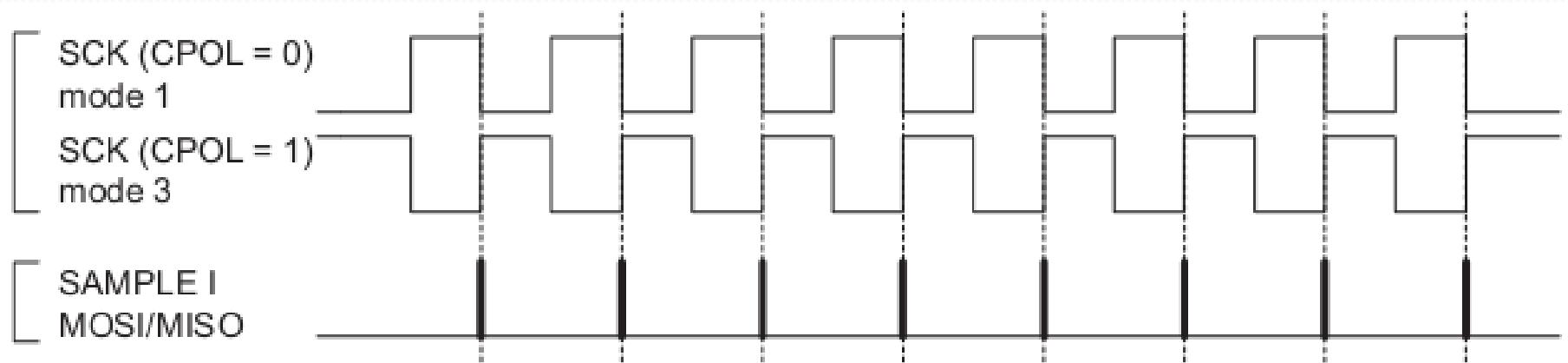
- Two - Two possible values of CPOL and CPHA bits gives rise to 4 modes of SPI

| Mode | Clock Polarity (CPOL) | Clock Phase (CPHA) |
|------|-----------------------|--------------------|
| 0    | 0                     | 0                  |
| 1    | 0                     | 1                  |
| 2    | 1                     | 0                  |
| 3    | 1                     | 1                  |

# SPI Transfer Format with CPHA = 0



# SPI Transfer Format with CPHA = 1



# Simple SPI Code

```
char data = SPITransmit('a');
```

In case of master, the data is written on the register and send to the slave.

In case of slave the data is written on the register and it waits for the master to transmit the data, when it also transmits its own data.

# Master Code

```
DDRB = 0b10110000; // configure SPI Master Pins
```

```
ISR(INT0_vect)
```

```
{
```

```
    // External Interrupt 0
```

```
    data = SPITransmit(0x01); // when switch is  
    pushed
```

```
    // send data
```

```
}
```

# Slave Code

```
DDRB = 0b10000000; // configure SPI Slave Pins
```

```
ISR(SPI_STC_vect)
```

```
{
```

```
    // SPI Transceiver Interrupt
```

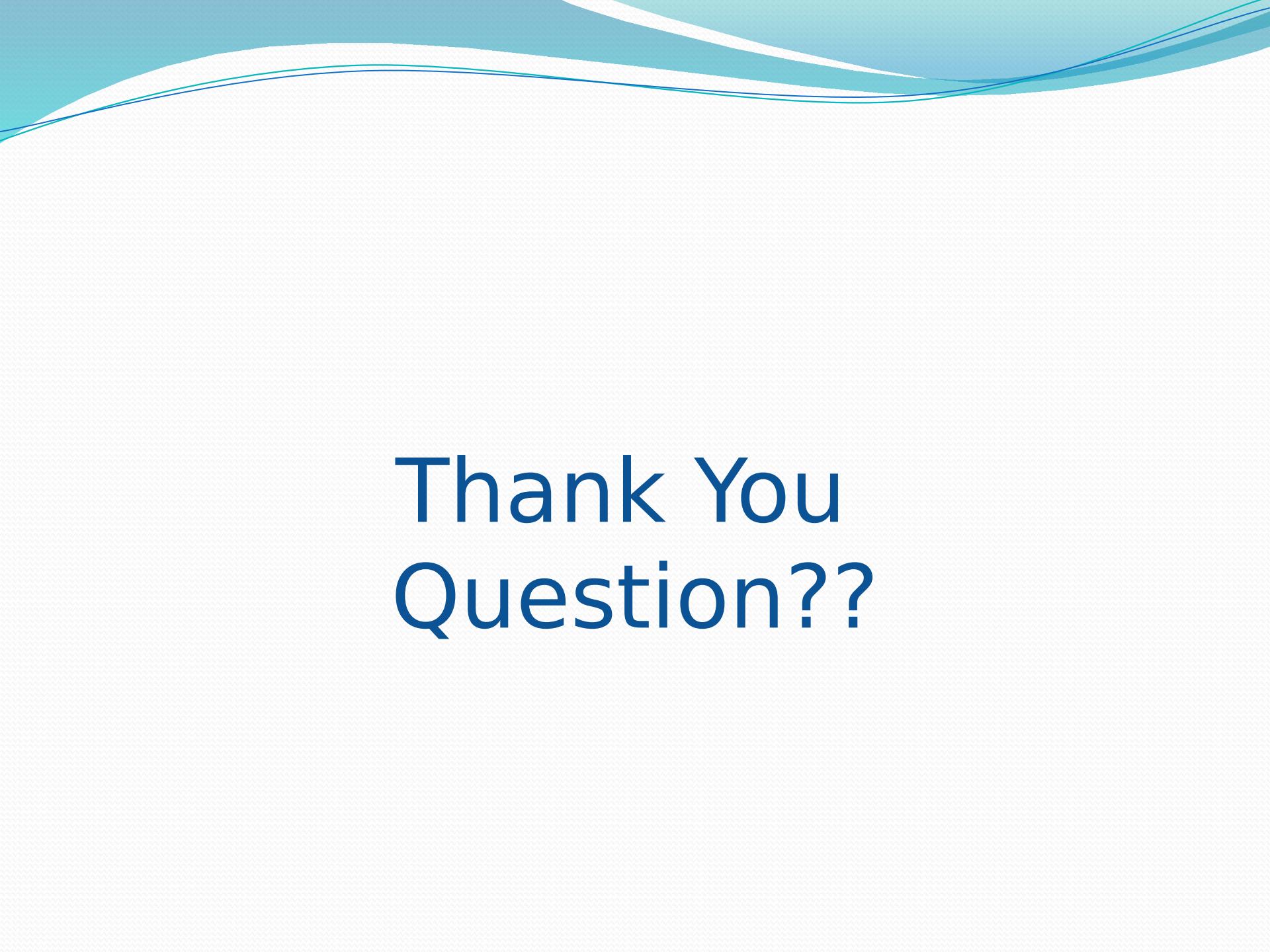
```
    data = SPDR ; // read the data
```

```
    if(data == 0x01){
```

```
        PORTA = ~PORTA; // if data is correct toggle Led
```

```
}
```

```
}
```



Thank You  
Question??