BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
II SEMESTER 2013-2014
IS F242 COMPUTER ORGANIZATION
CS C342 ADVANCED COMPUTER ORGANIZATION
COMPREHENSIVE EXAM PART B (OPEN BOOK)

TIME: 60 Min. **5/5/2014** **MM: 25**

Q1. Consider the following piece of code executed on a MIPS 5- stage pipelined processor:

```
        BEV R1, L1        # Branch to L1 if number in R1 is even (branch b1)
        ADDI R1,R1,1
L1:     BO R1,L2          # Branch to L2 if number in R1 is odd (branch b2)
        ADDI R1,R1,1
L2:     BTHREE R1, L3     # Branch to L3 if number in R1 is divisible by 3 (branch b3)
….
L3:
```

Assume that BEV,BO and BTHREE are instructions available in MIPS instruction set with functions as explained above.

The piece of code given above is executed four times with the starting value of R1 as 3,2,5 and 6. If a (2,1) correlating branch predictor is used fill the table given below (draw a similar table in your answer sheet) with T or NT. Assume all entries of the predictor are initialized to NT for the first iteration and there is no branch aliasing. [6]

R1➔	1	2	4	7
b1 prediction				
b1 actual				
b2 prediction				
b2 actual				
b3 prediction				
b3 actual				

Q2. (a) Using Tomasulo's algorithm, for each instruction in the following sequence determine when (in which cycle, counting from the start=1) it issues, begins execution, ends execution and writes its result to the CDB. ***Assume that the result of an instruction can be written in one cycle after end of its execution***. The execution time of all instructions is two cycles, except for multiplication (which takes 5 cycles) and division (which takes 10 cycles). The processor has multiply/divide units and add/subtract units. The multiply/divide unit has two reservation stations and the add/subtract unit has three reservation stations. There are one load and one store reservation stations as well. Assume that at start all instructions are already in the instruction queue, but none has yet been issued to any reservation stations. The processor can issue only one instruction per cycle, and there is only one CDB for writing results.

```
LD.D F6, 0(R1)
DIV F4,F5,F6
ADD F8,F2,F4
ADD F2,F5,F3
SUB F4, F4, F2
ADD F3, F8,F2
SD.D F4, 4(R1)
```

Q3. (a) How many total bits (tag+data+valid) are required for a direct-mapped cache with 512 KB of data and 8-byte block size, assuming a 32-bit address?
(b) How many total bits (tag+data+valid) are required for a 4-way set associative cache with 1024 KB of data and 8-byte block size, assuming a 32-bit address?
(c) Assume a memory system with cache in part(a) as L1 and cache in part (b) as L2. The hit time of L1 is given as 2 cycles, GMR of L1 is 3%, hit time of L2 is 8 cycles, GMR of L2 is 2% and miss penalty of L2 is 80 cycles. Calculate the AMAT of the memory system. [5]

Q4. A RISC Processor having a five stage pipeline as discussed in class is used. The Pipeline hardware detects all possible data hazards and stalls the pipeline (no forwarding) when necessary for correct program behavior. For such a Processor draw cycle by cycle execution schedule in the pipeline for the following program for one iteration of the loop through this pipeline.

```
                    Destination   Source
LOOP:   LW          R1,           4($R2)
        SW          R1,           8($R2)
        ADD         R2,           R2, R1
        LW          R3,           6($ R2)
        ADD         R4,           R3, R2
        ADDI        R1,           R3, 4
        ADDI        R8,           R4, 4
        BNEZ        R8    LOOP
```
[6]