



## Research Interests:

Compute-in-Memory, Neuromorphic Circuits, Energy-Efficient Neural Systems

## RESEARCH EXPERIENCE

### COMPUTE-IN-MEMORY GROUP @IITM | MAY'25 - PRESENT

Guide: [Prof. Janakiraman Viraraghavan](#), Dept. of EE IITM

#### Hybrid IMC Chip Tapeout (TSMC 28nm)

- Designing the layout of SRAM array along with its Read/ Write peripherals and performing RC extracted simulations to characterize the cells.
- Synthesizing and performing constrained PnR for several digital blocks.

#### Time-Domain Chip Testing

- Designed a 4 layer PCB to configure a taped-out Time-Domain based macro and enable communication with an FPGA to facilitate the **post-silicon testing**.
- Characterized and calibrated the analog peripherals for MAC computation.
- Ran various neural network inferences on the macro to analyze layer-wise statistics based on output resolution limitations to maintain negligible loss in accuracy.

### MODELLING THE MEMORY SUBSYSTEM | DEC'24 - APR'25

Research Project ([report](#)) under Prof. Gopalakrishnan Srinivasan, Department of CSE IITM

- Modified [SCALE-Sim](#), a systolic-array simulator, to analyze memory traffic in a custom hybrid SNN-ANN accelerator exploiting dual sparsity in spikes and weights.
- Introduced **Memory Banks** to the simulator, potentially **reducing the stall cycles by >90%** in the convolution layers of RESNET-20 model.

## ENGINEERING EXPERIENCE

### EMBEDDED SYSTEMS ENGINEER | SEPT'23 - JUL'24

Team [Avishkar Hyperloop](#), Centre For Innovation, IIT Madras

- Recognized among the **Top 5 Teams** at **European Hyperloop Week 2024**, hosted by ETH Zürich, Switzerland.

#### On-Track Electronics Control Card

- Designed a **4-layer Signal Conditioning PCB** to drive the inverter and relay data from 25+ sensors for the Linear Synchronous booster Motor.
- Integrated TI's C2000 Delfino DSP and MSP432 MCU boards, reducing communication latency by 2x through **DSP offloading**
- Enabled seamless wireless communication between 3 nodes in a **near-Faraday cage environment** for synchronized pod operation.

#### Master Control Unit

- Developed **CAN communication stack** based on Ti-RTOS for the TI development board MSP432E401Y on Code Composer Studio.
- Designed, simulated and thoroughly **tested CAN architecture** spanning 3 buses, 20 nodes and 500+ signals using **Vector CANoe**.
- **Simulated a Finite State Machine** with 20+ states capturing ~100 fault cases.

#### Full Pod Integration

- Developed an **autonomous Hyperloop Pod** and implemented methods to lower the communication latency at both hardware and software levels.
- Performed **end to end HIL & SIL testing** to ensure reliable performance in diverse environments and conditions.

## EDUCATION

### INDIAN INSTITUTE OF TECHNOLOGY MADRAS

B.TECH IN ENGINEERING PHYSICS  
M.TECH IN ELECTRICAL ENGINEERING  
(Dual Degree) | Chennai, India  
Nov 2022 - Jul 2027 (Expected)  
CGPA: 9.71 / 10

## COURSEWORK

### IC & SYSTEMS

- Systems Engineering for DL
- Digital IC Design
- Embedded Memory Design \*\*
- Computer Organization
- VLSI Modelling/Optimization
- Mapping Algos. to DSP Arch.
- Analog Circuits
- Analog Systems & Lab
- Digital Systems & Lab

### OTHER RELEVANT CORE

- Intro to Deep Learning
  - Devices for Neuromorphic Computing
  - Solid State Devices
  - Probability, Stats and Stochastic Processes
  - Quantum Mechanics
- \*\* *audited*

## SKILLS

### EDA TOOLS

Cadence Virtuoso • Genus • Innovus • Synopsys IC Compiler II • ADS • Altium Designer • KiCAD • Vivado • Vitis HLS • Electric • LTSpice

### PROGRAMMING LANGUAGES / FRAMEWORKS

Python • PyTorch • C • C++ • Verilog • x86 Assembly • Mathematica • Simulink • Stateflow • Vector CANoe

### GENERAL

Git/Github • L<sup>A</sup>T<sub>E</sub>X • LINUX

## COURSE PROJECTS

### EMBEDDED MEMORY DESIGN | FEB'25 - APR'25

Instructor: Prof. Janakiraman Viraraghavan, Dept. of EE IITM

- Designed an SRAM-based CIM array to run inferences on the MNIST dataset with <1% accuracy drop from the software baseline.
- Performed Monte Carlo simulations to verify the functionality over thermal noise and ensure appropriate transistor scaling to preserve accuracy.

### SYSTEMS ENGINEERING FOR DEEP LEARNING | JUL'25 - NOV'25

Instructors: Prof. Gopalakrishnan Srinivasan & Dr. Karthik Sankaranarayanan, Department of CSE IITM

#### Mixed Precision Quantization for IMC Hardware

- Proposed & implemented a **quantization strategy** for vision CNN models tailored for analog IMC hardware through **bit-slicing**.
- Validated the model compression of VGG-15 and performance tradeoffs by modifying **MICSIM**, an IMC simulator wrapped over **NeuroSIM**.

#### Selected Course Assignments

- Plotted roofline of Intel i5 CPU for processing inference of GPT-2 model using llama
- Performed **deep compression** through structured pruning and k-means clustering quantization, of mobilenetv2 to achieve **15x** model size reduction.

### MODELLING & OPTIMIZATION IN VLSI | JAN' 25 - MAY' 25

Instructors: Prof. Janakiraman & Prof. Ramprasath, Dept. of EE IITM

#### Objective-Constrained Gate Sizing Optimization

- Developed a Geometric Programming based continuous **gate sizing framework** using STA for timing-aware area minimization on ISCAS-85 benchmark circuits.
- Discretized the continuous solution through Multi-Moves Heuristics to map to standard cell sizes.
- Achieved **<4% area overhead** while retaining delays within **<1.5% positive slack**.

### DIGITAL IC DESIGN | JULY' 24 - DEC' 24

Instructor: Prof. Ramprasath, Department of EE IITM

#### 8-bit Carry Save Multiplier

- Designed a transistor-level schematic and layout of an **8-bit Carry Save Multiplier**.
- Implemented **Dadda-Tree Adder** for partial products reduction and **Kogge-Stone Carry Lookahead Adder** for efficient Vector merging.
- Achieved **~1.3x delay reduction** over an Array Multiplier

### DEVICES & TECH FOR AI AND NEUROMORPHIC COMPUTING | JUL'25 - DEC'25

Instructor: Prof. Bhaswar Chakrabarty, Dept. of EE IITM

#### NVM-based Compute In-Memory Engine

- Designed a 2-layer MLP feedforward neural network using **1T1R - RRAM synaptic arrays** and CMOS "Quadratic ReLU" activation function to bridge the layers.
- Calibrated programming of RRAMs ensuring uniform conductance across the array.
- **Simulated** the validation **inference in ADS** and benchmarked the performance.

### ANALOG SYSTEMS AND LAB | JAN' 24 - MAY' 24

Instructor: Prof. Saurabh Saxena, Dept. of EE IITM

- Built and analyzed closed-loop analog systems including a DC-DC regulator, peak detector, and sPWM generator using through-hole OpAmp ICs, MOSFETs and BJTs.
- Simulated circuits in LTSpice and performed loop-stability verification to validate accuracy and control performance.

## TEACHING ASSISTANT

### COMPUTER ORGANISATION

- Summer, 2025 (Online BS - ES, IITM)
- Fall, 2025 (B.Tech - IITM)
- Reviewed the lecture material and created animations
- Set questions for assignments
- Led the TA activity for a group of 15 TAs

### DIGITAL SYSTEMS LAB

- Spring, 2025 (B.Tech - IITM)
- Helped students with implementing a Traffic-Signal Controller project

### C PROGRAMMING AND ASSEMBLY LANGUAGE

- Fall, 2025 (NPTEL)
- Set the weekly assignments and recorded solution videos
- Helped with student's doubts over the NPTEL forum.

## VOLUNTEERING

### AVANTI FELLOWS

Mentored and guided class 11, 12 students for competitive exams like JEE, KVPY and olympiads

### SAATHI

Guided college freshmen with academic and non-academic issues through their first year