Lab 3

ECE 3300 LAB

SECTION 02

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Group I

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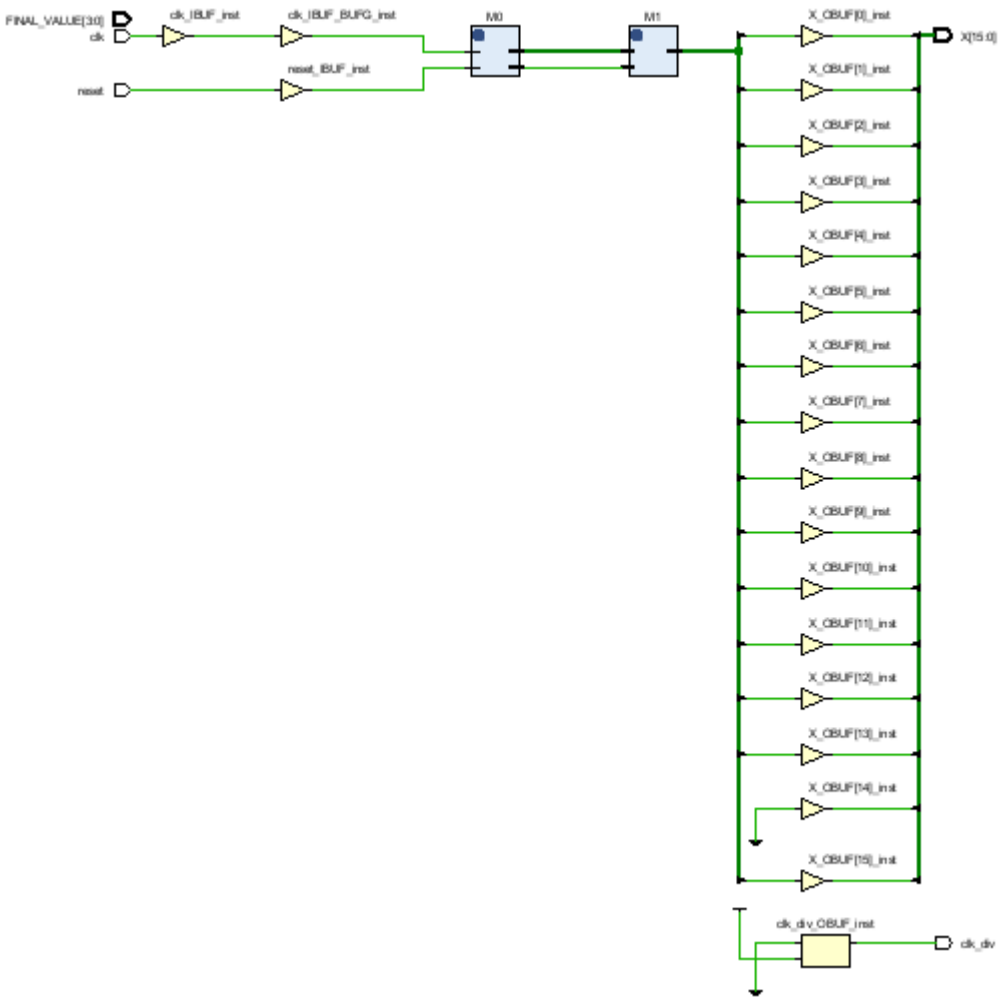
Abstract

Purpose of the experiment was to create a variable clock divider on the Arty 7 FPGA board. Task was to create 4x16 decoder by instantiation. One button would be used to reset the clock speed. Decoder was created using structural modeling. From there, the high frequencies would make the LED flash at a fast paced while low frequencies would be slower.

Theory: Sketch of Design

Area/Resources Information

Elaborated Design

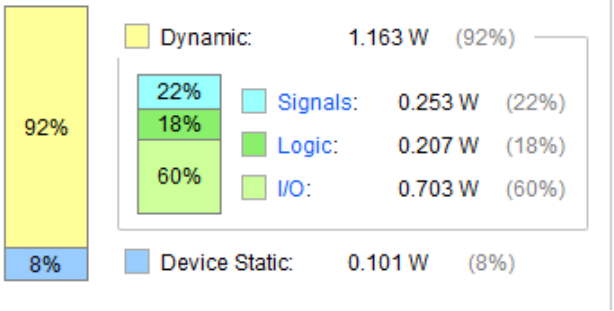


Power Usage

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.264 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**30.8°C**
Thermal Margin:	54.2°C (11.8 W)



Post-Implementation Resource Utilization

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM
✓ synth_1	constrs_1	synth_design Complete!								11	4	0.0
✓ impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	1.161	0	11	4	0.0