Lab 4

ECE 3300 LAB

SECTION 02

Instructor: Mohamed Aly

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Group I

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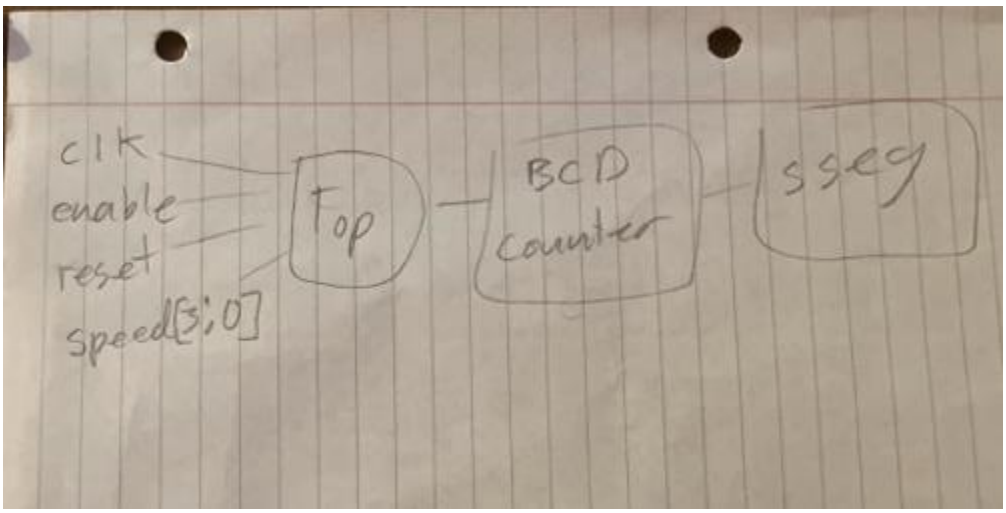
Abstract

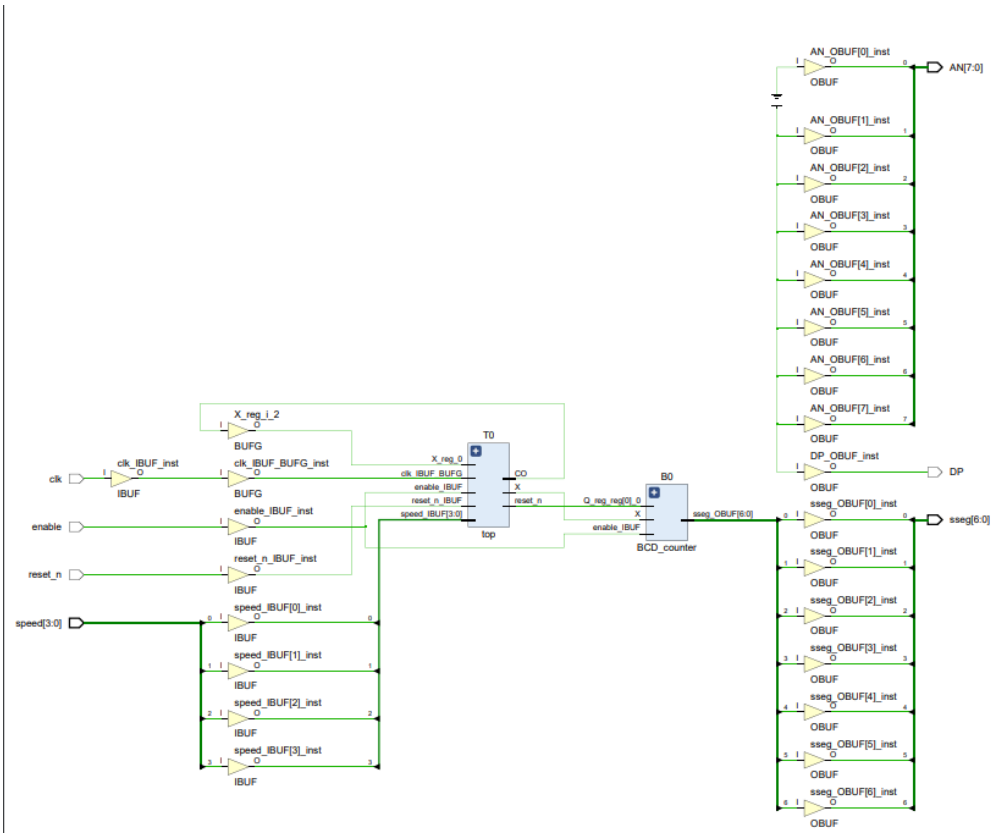
Purpose of the experiment was to loop from 0-9 on the Arty 7 FPGA board. Task was to create 4x16 decoder, BCD counter and segment display. One button would be used to reset the clock speed. Decoder was created using structural modeling. From there, the switches would be used to change how quickly the numbers would be displayed.

Theory: Sketch of Design

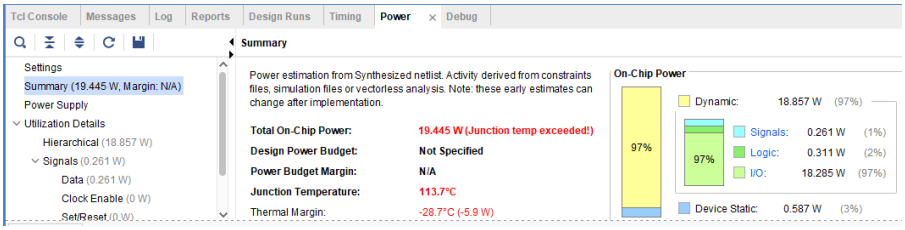


Area/Resources Information

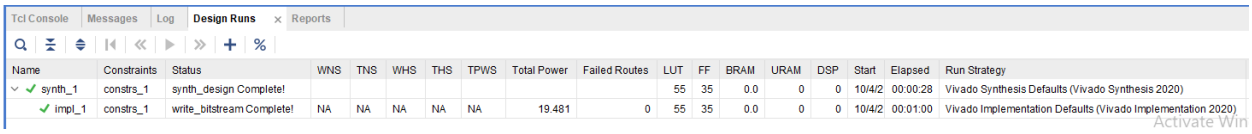
Elaborated Design



Power Usage



Post-Implementation Resource Utilization



Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								55	35	0.0	0	0	10/4/2	00:00:28	Vivado Synthesis Defaults (Vivado Synthesis 2020)
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	19.481	0	55	35	0.0	0	0	10/4/2	00:01:00	Vivado Implementation Defaults (Vivado Implementation 2020)