Lab 8

ECE 3300 LAB

SECTION 02

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November 22, 2021

Group I

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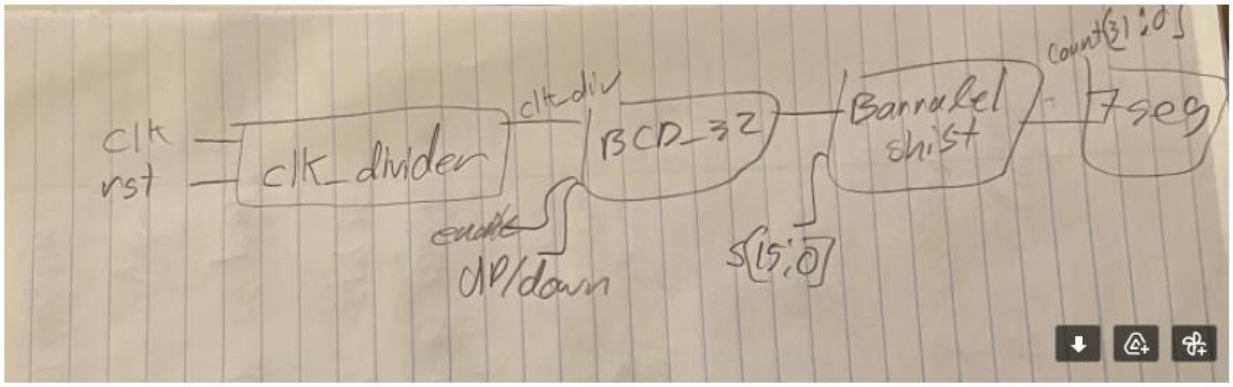
Abstract

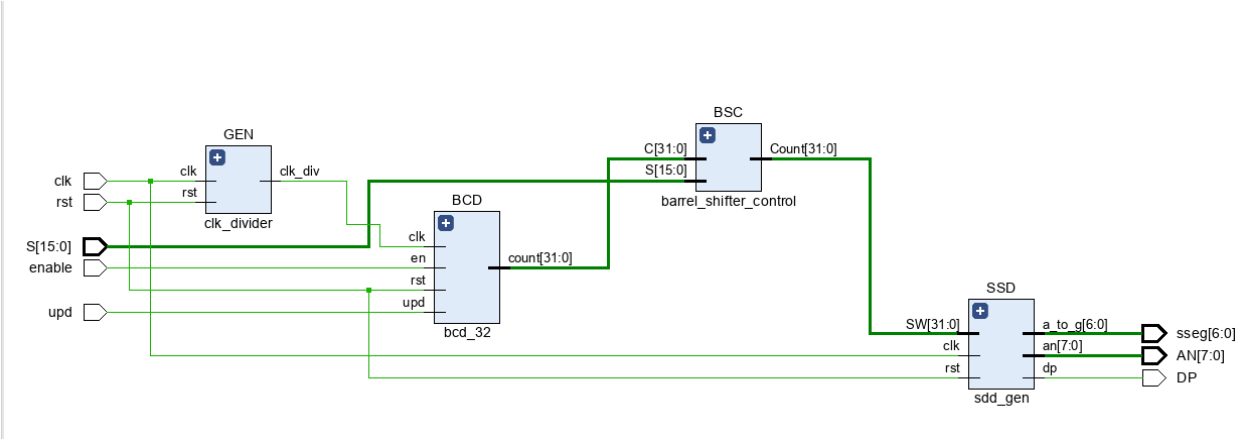
Purpose of the experiment was to create a system using up/down counter and barrel shifter . A barrel shifter was used to shift a data by a specified number of bits in one clock cycle in a left rotation or right rotation. In this experiment the number of bits that was used were 32 since 8 displays were used. To create 4-bit barrel shifter, 2 multiplexors were used. The total number of multiplexors used was 8 multiplexors. Similar to lab 5, a button was used as the up/down counter instead of using a switch.

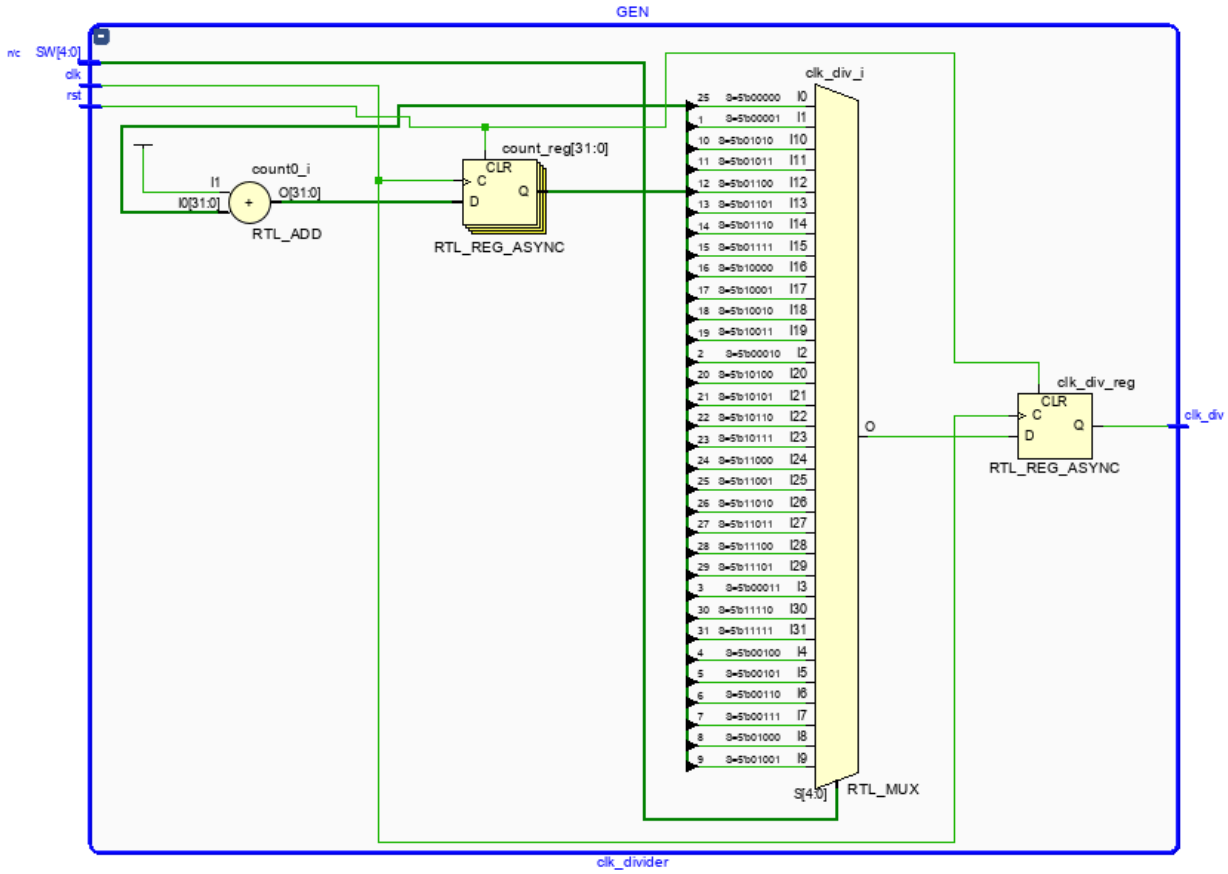
Theory: Sketch of Design

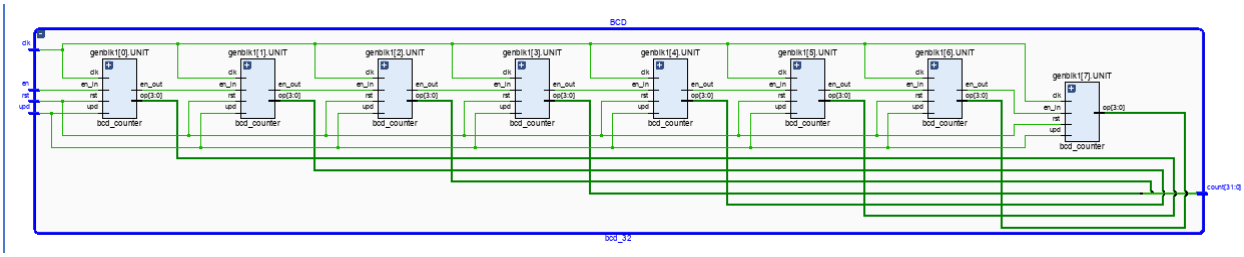


Area/Resources Information

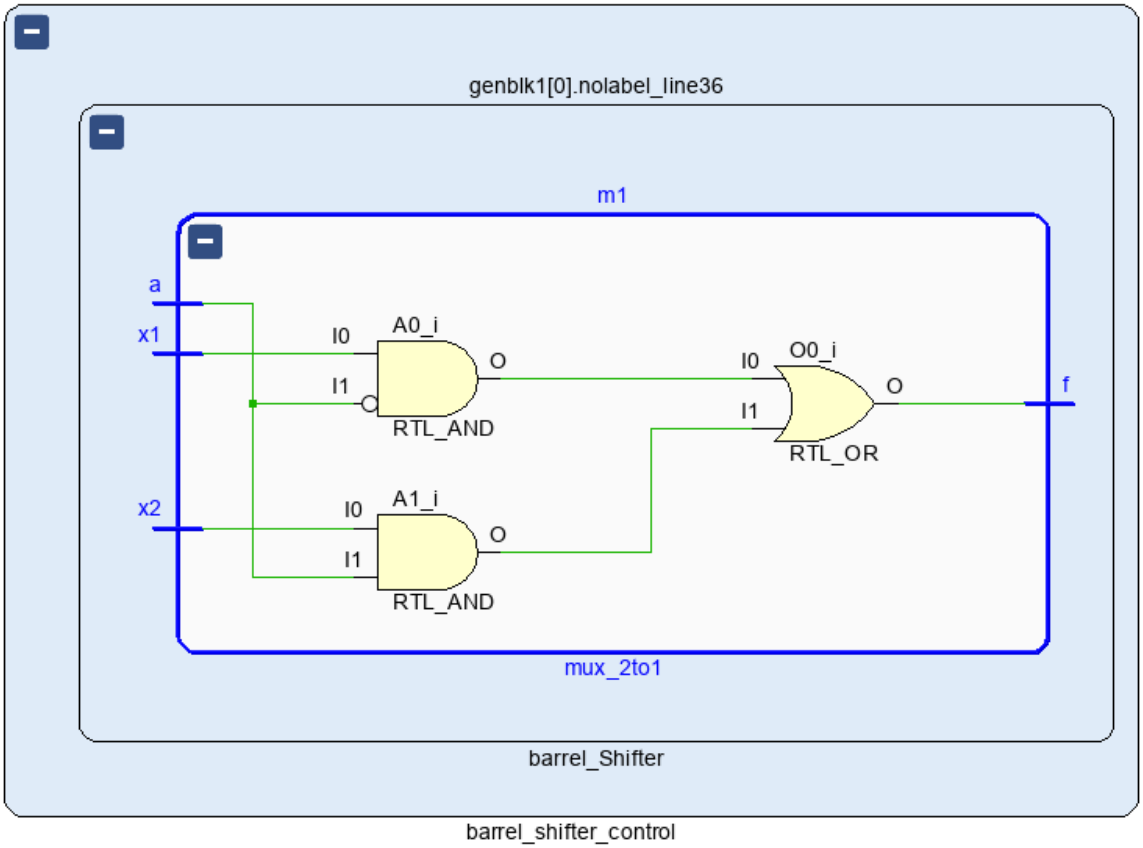
Elaborated Design

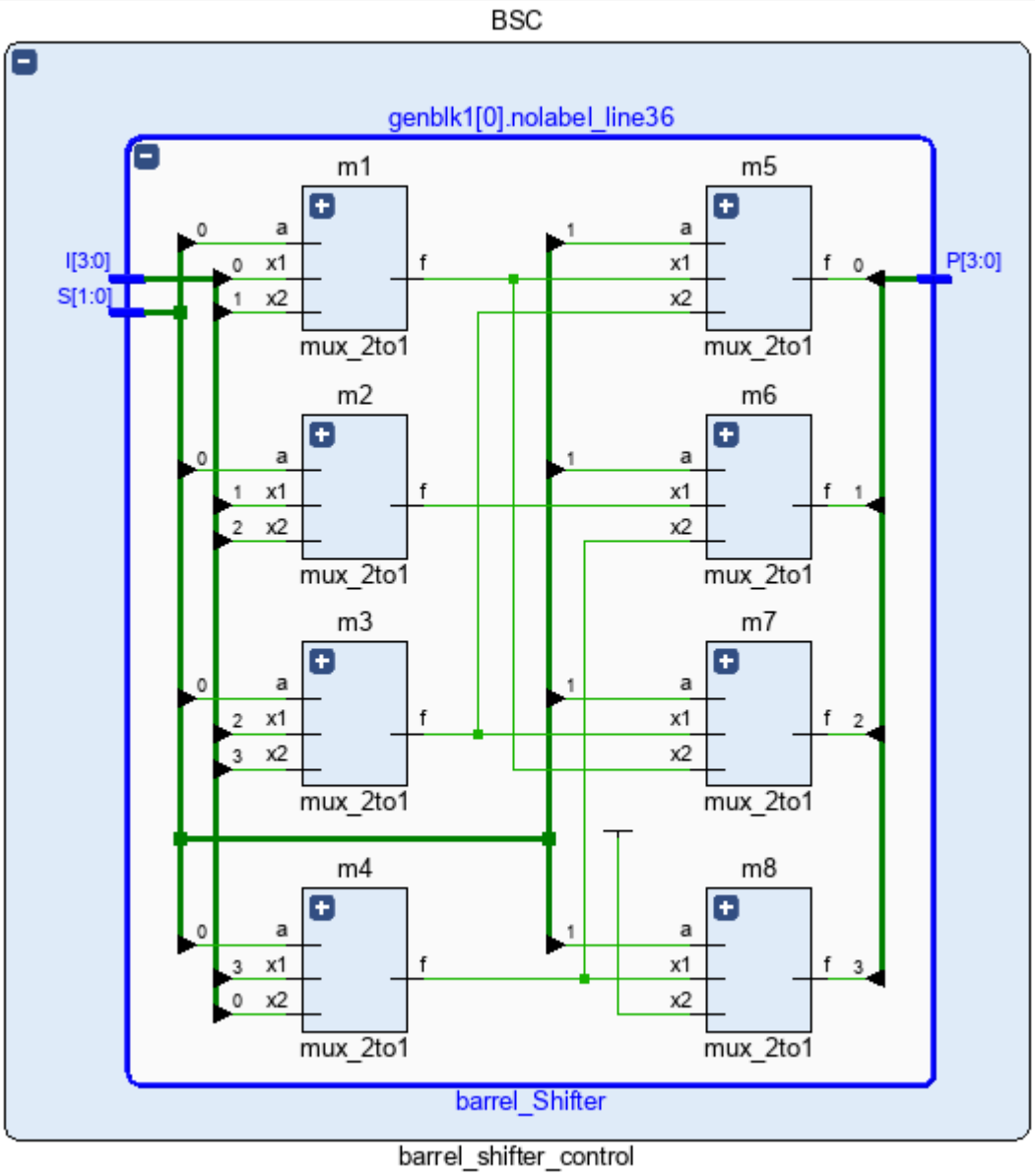



GEN
SW[4:0]
clk
rst
count0_i
I1
I0[31:0]
O[31:0]
RTL_ADD
count_reg[31:0]
CLR
C
D
Q
RTL_REG_ASYNC
clk_div_i
25 8'b00000 I0
1 8'b00001 I1
10 8'b01010 I10
11 8'b01011 I11
12 8'b01100 I12
13 8'b01101 I13
14 8'b01110 I14
15 8'b01111 I15
16 8'b10000 I16
17 8'b10001 I17
18 8'b10010 I18
19 8'b10011 I19
2 8'b00010 I2
20 8'b10100 I20
21 8'b10101 I21
22 8'b10110 I22
23 8'b10111 I23
24 8'b11000 I24
25 8'b11001 I25
26 8'b11010 I26
27 8'b11011 I27
28 8'b11100 I28
29 8'b11101 I29
3 8'b00011 I3
30 8'b11110 I30
31 8'b11111 I31
4 8'b00100 I4
5 8'b00101 I5
6 8'b00110 I6
7 8'b00111 I7
8 8'b01000 I8
9 8'b01001 I9
S[4:0]
RTL_MUX
O
clk_div_reg
CLR
C
D
Q
RTL_REG_ASYNC
clk_div
clk_divider

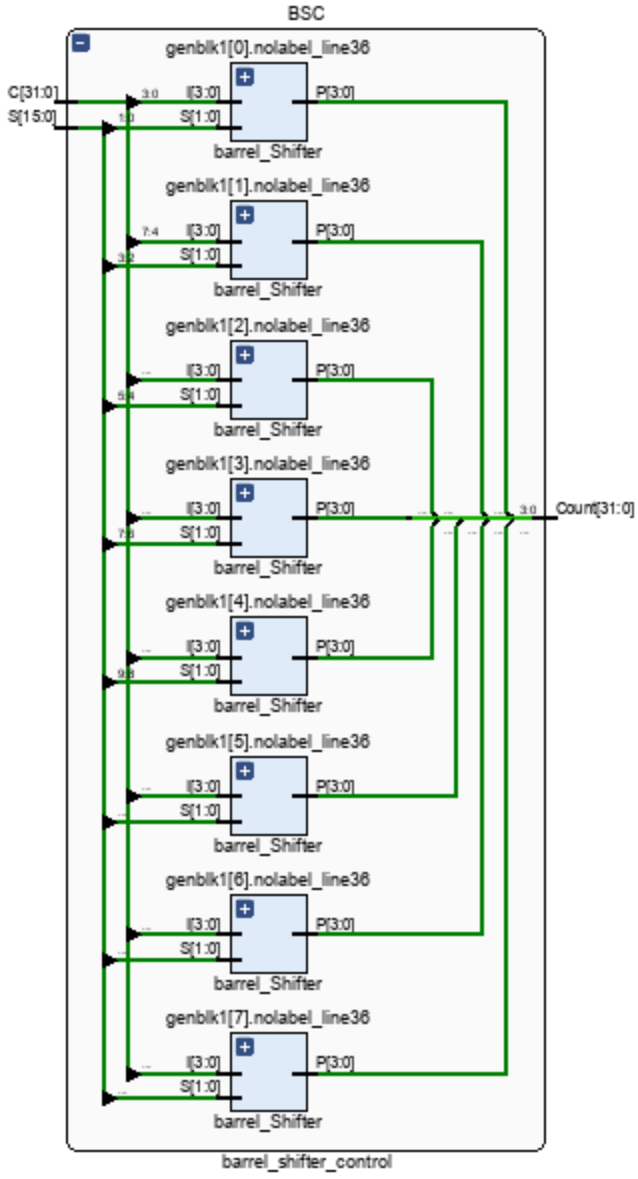

BCD
genblk1[0].UNIT
genblk1[1].UNIT
genblk1[2].UNIT
genblk1[3].UNIT
genblk1[4].UNIT
genblk1[5].UNIT
genblk1[6].UNIT
genblk1[7].UNIT
bcd_counter
bcd_32

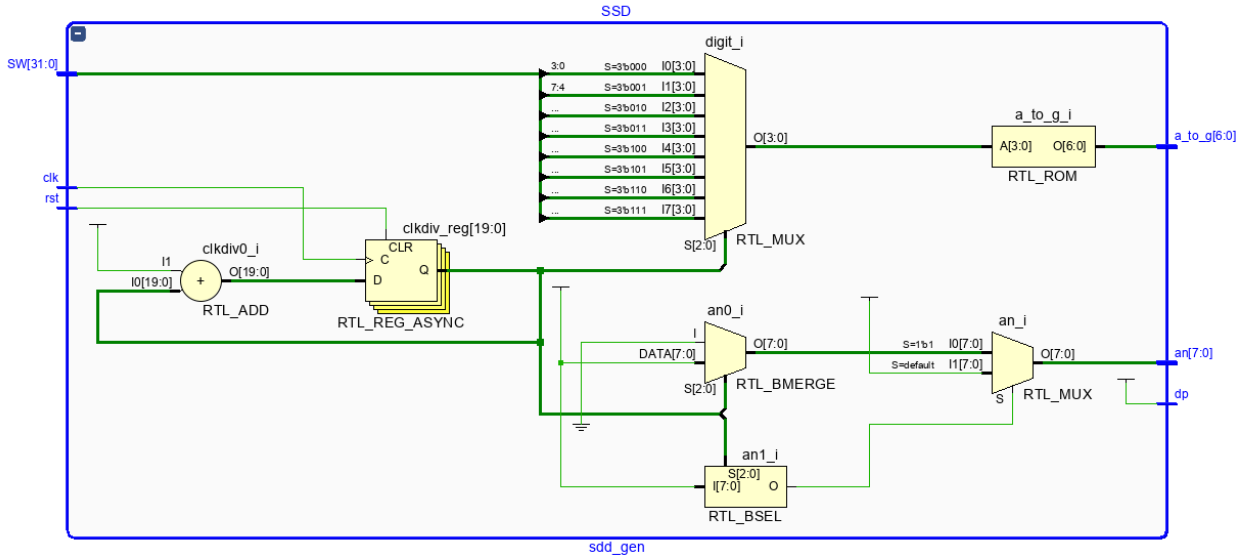
BSC


genblk1[0].nolabel_line36
m1
a
x1
x2
I0
I1
A0_i
A1_i
RTL_AND
RTL_AND
O
O0_i
RTL_OR
f
mux_2to1
barrel_Shifter
barrel_shifter_control

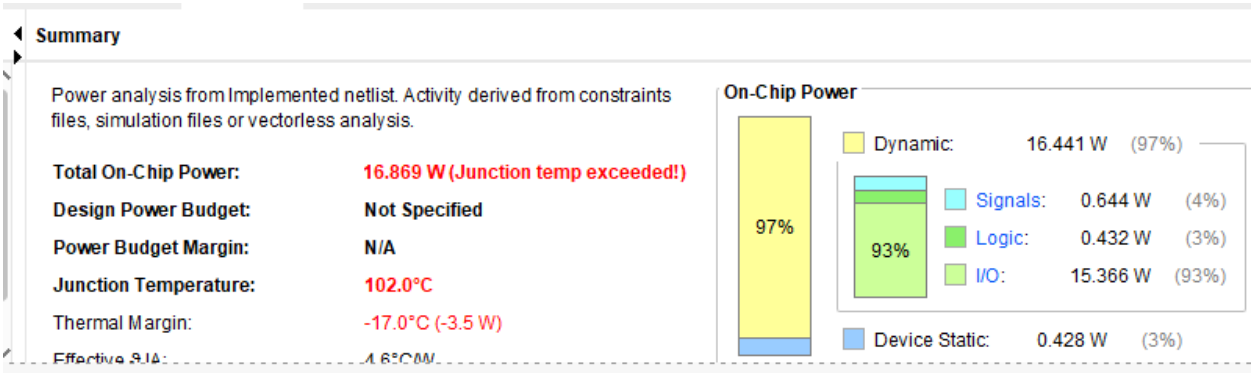


4-bit barrel shifter uses 2 multiplexors however for our implementation, total muxes used was 8 multiplexors due to using the number of displays

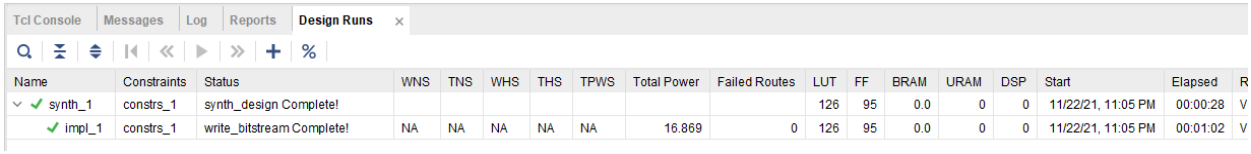

BSC
genblk1[0].nolabel_line36
C[31:0]
S[1:0]
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[1].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[2].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[3].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[4].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[5].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[6].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
genblk1[7].nolabel_line36
I[3:0]
S[1:0]
P[3:0]
barrel_Shifter
Count[31:0]
barrel_shifter_control



Power Usage



Post-Implementation Resource Utilization



Tcl Console | Messages | Log | Reports | Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	R
synth_1	constrs_1	synth_design Complete!								126	95	0.0	0	0	11/22/21, 11:05 PM	00:00:28	V
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	16.869	0	126	95	0.0	0	0	11/22/21, 11:05 PM	00:01:02	V