Lab 5

ECE 3300 LAB

SECTION 02

Instructor: Mohamed Aly

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Group I

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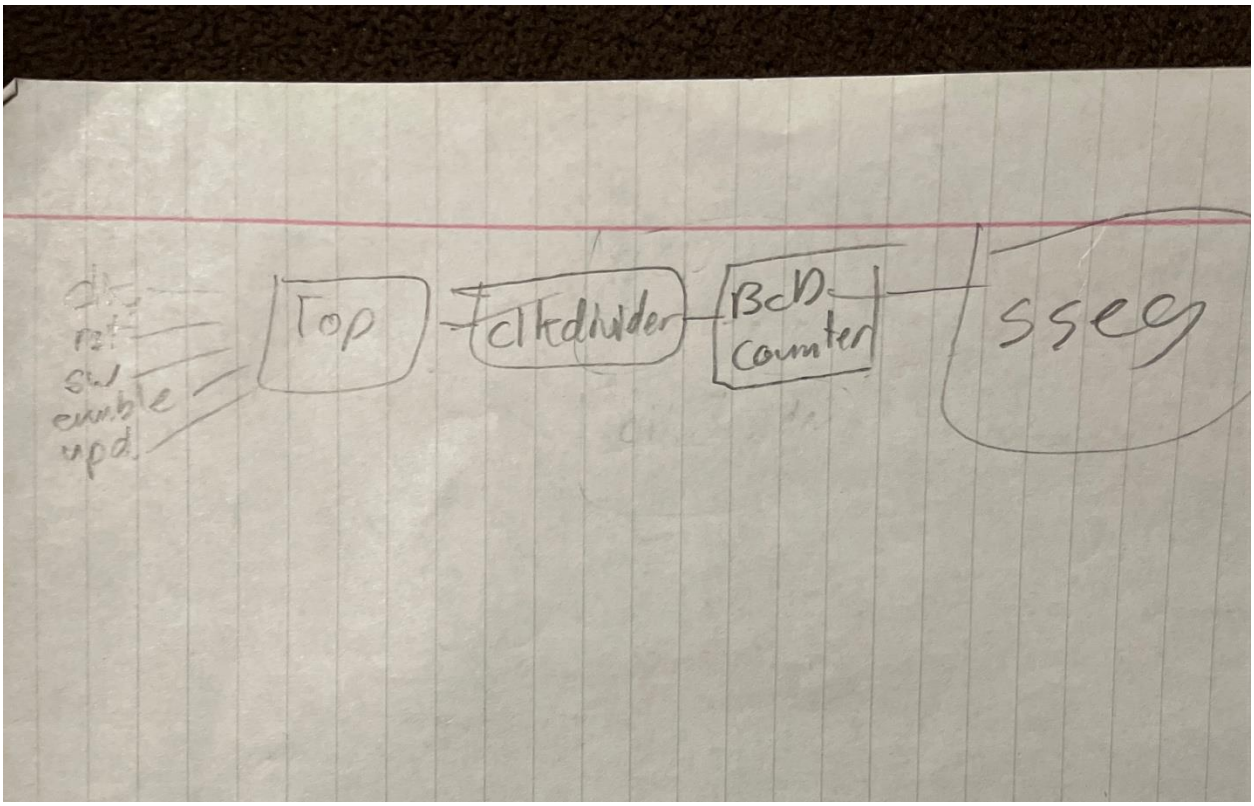
Abstract

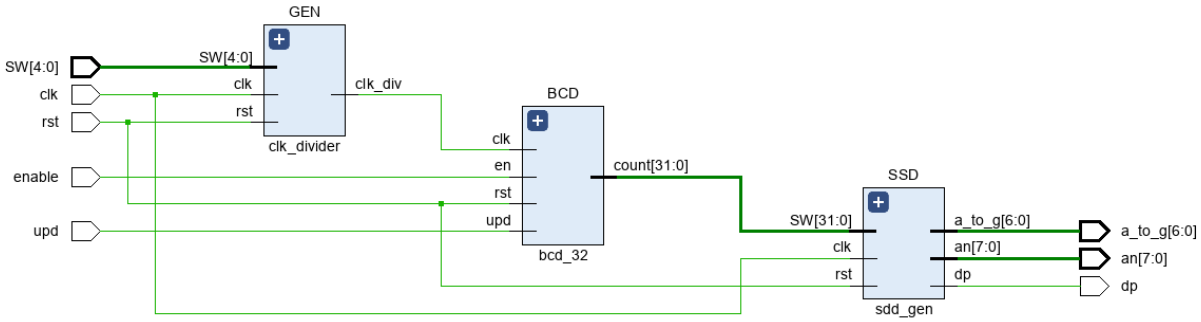
Purpose of the experiment was to reuse seven segment display code from previous lab, implementing a up/down BCD counter, and fixing errors in the codes that were provided. Task was to identify corner cases and creating testbenches to debug errors. The first four switches were for the clock speeds while the last two switches were for enable and up/down counter. One button would be used to reset the clock speed. One error that was needed to be fix was the down counter displaying random numbers and not decreasing sequentially. Another error that was shown in the instructions was up/down counter working even though the enable switch is off .From there, the switches would be used to change how quickly the numbers would be displayed.

Theory: Sketch of Design



Area/Resources Information

Elaborated Design



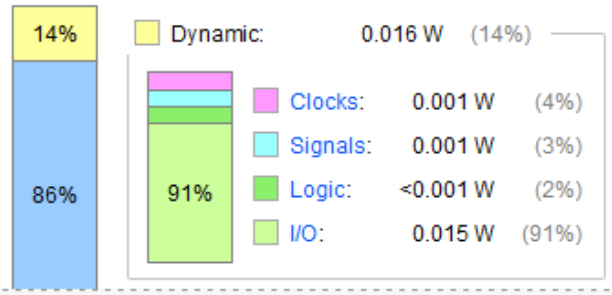
Power Usage

Summary

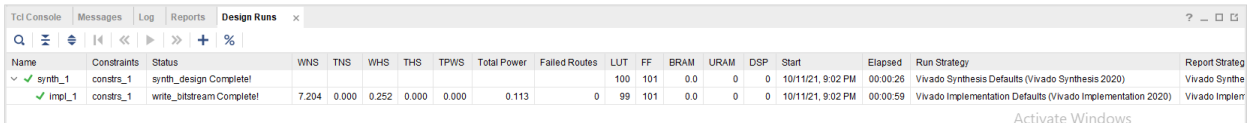
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.113 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	59.5°C (12.9 W)

On-Chip Power



Post-Implementation Resource Utilization



Tcl Console | Messages | Log | Reports | Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy	Report Strateg
synth_1	constrs_1	synth_design Complete!								100	101	0.0	0	0	10/11/21, 9:02 PM	00:00:26	Vivado Synthesis Defaults (Vivado Synthesis 2020)	Vivado Synthe
impl_1	constrs_1	write_bitstream Complete!	7.204	0.000	0.252	0.000	0.000	0.113	0	99	101	0.0	0	0	10/11/21, 9:02 PM	00:00:59	Vivado Implementation Defaults (Vivado Implementation 2020)	Vivado Implen