PROJECT PROPOSAL

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Project Title: Cache Memory Access Patterns in the GPU Architecture

Tools used: Multi2Sim

Project Description: Study the MRU(most recently used) and LRU(least recently used) cache accesses in L1 and L2 caches. To record and compare GPU cache access patterns for different workloads on AMD Radeon. These simulations will be studied on the Multi2Sim.

Benchmarks to be studied:
AMD SI(Southern Island) – Histogram, Radix Sort, Matrix Multiplication, Simple Convulation, Binary Search

Work breakdown:
Week 1(23rd – 29th March): Study the Multi2Sim Simulator and the GPU architecture of AMD.
Week 2(30th March - 5th April): Study and configure the MRU and LRU for targeted architectures.
Week 3 (6th April – 10th April): Run different benchmarks and document the results.

Expected Grade:
A: All benchmarks studied and documented for both the architectures.
A- : All benchmarks studied and documented for one of the architectures.
B : Configure Multi2Sim and configure the Cache accesses.

References:

1. Nimkar, Yash, "Cache Memory Access Patterns in the GPU Architecture" (2018). Thesis. Rochester Institute of Technology
2. X. Gong, R. Ubal and D. Kaeli, “Multi2Sim Kepler: A detailed architectural GPU simulator,” 2017 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), Santa Rosa, CA, 2017