Doulos does not endorse training material from other suppliers on EDA Playground.

Languages & Libraries

► Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Examples

212

testbench.sv

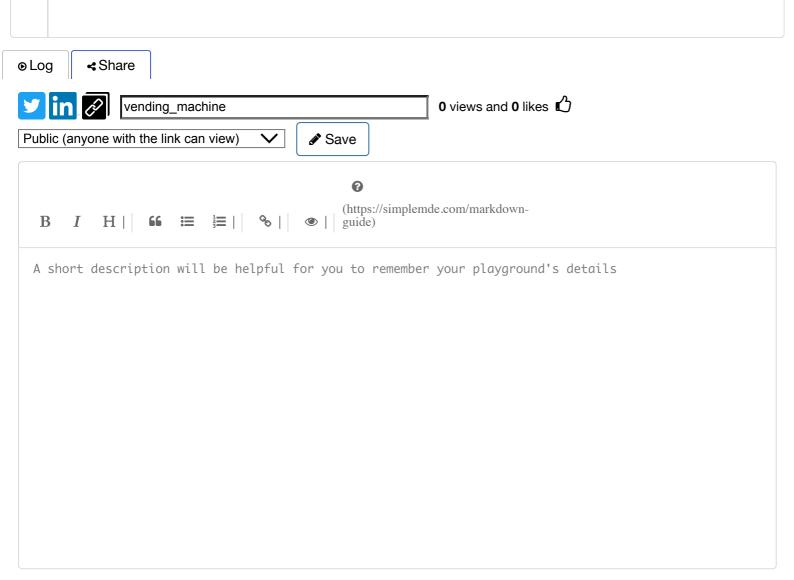
```
\oplus
```

```
module vm_tb;
2
     // inputs
3
     logic clk;
4
5
     logic rst;
6
     logic [1:0] in;
7
8
     // outputs
9
     logic out;
10
     logic [3:0] change;
11
     // DUT
12
     vending_machine dut (
13
14
        .clk(clk),
15
        .rst(rst),
16
        .in(in),
17
        .out(out)
18
        .change(change)
     );
19
20
21
     // Clock generation
22
     always #5 clk = \simclk;
23
     // Stimulus
24
     initial begin
25
          $dumpfile("vending_machine.vcd");
$dumpvars(0,vm_tb);
26
27
28
        clk = 0;
29
30
        rst = 1;
31
        in = 0;
32
33
       #10 \text{ rst} = 0;
                              // release reset
34
       // Insert 5, then 10 (should dispense)
#10 in = 2'b01; // 5
35
36
        #10 in = 0;
37
        #10 in = 2'b10;
                             // 10
38
       #10 in = 0;
39
40
        // Insert 10, then 10 (should dispense + return 5)
41
        #10 in = 2'b10;
                             // 10
42
        #10 in = 0;
43
        #10 in = 2'b10;
                             // 10
44
45
        #10 in = 0;
46
        // Insert 5, then 5, then 5 (should dispense)
47
        #10 in = 2'b01;
48
        #10 in = 0;
49
        #10 in = 2'b01;
50
       #10 in = 0;
#10 in = 2'b01;
51
52
        #10 in = 0;
53
54
       #50 $finish;
55
```

```
56 end
57
58 endmodule
59
60
```

```
design.sv
```

```
1 module vending_machine(
       input logic
                           clk,
2
3
       input logic
                           rst,
       input logic [1:0] in,
                                       // coin input: 01 = 5Rs, 10 = 10Rs
 4
       output logic
5
                                       // product dispense
                           out,
       output logic [3:0] change
                                       // change return (max 15, so 4 bits)
6
7
  );
8
9
     // State encoding with parameters
     parameter s0 = 2'b00;
                               // 0 Rs
10
     parameter s5 = 2'b01;
                               // 5 Rs
11
                               // 10 Rs
12
     parameter s10 = 2'b10;
13
     logic [1:0] c_state, n_state;
14
15
     // Sequential state update
16
     always_ff @(posedge clk or posedge rst) begin
17
       if (rst)
18
         c_state <= s0;
19
       else
20
21
         c_state <= n_state;</pre>
     end
22
23
24
     // Next-state & output logic
25
     always_comb begin
       // default values
26
27
       n_state = c_state;
28
       out
             = 0;
29
       change = 0;
30
       case (c_state)
  s0: begin
31
32
           if (in == 2'b01) n_state = s5;  // insert 5
33
           else if (in == 2'b10) n_state = s10; // insert 10
34
         end
35
36
         s5: begin
37
           if (in == 2'b01) n_state = s10;
                                                     // 5 + 5 = 10
38
39
           else if (in == 2'b10) begin
                                                      // 5 + 10 = 15 \rightarrow dispense
40
                     = 1;
41
             n_state = s0;
42
           end
43
         end
44
45
         s10: begin
           if (in == 2'b01) begin
                                                      // 10 + 5 = 15
46
             out = 1;
47
48
             n_state = s0;
49
           end
           else if (in == 2'b10) begin
                                                      // 10 + 10 = 20
50
             out = 1;
51
             change = 5;
                                                      // return 5
52
53
             n_state = s0;
54
           end
55
         end
56
         default: n_state = s0;
57
58
       endcase
59
     end
60
61 endmodule
```



lines: 1 words: 0 0:0