

EDA

playground

New

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DOULOS

DOULOS does not endorse training material from other suppliers on EDA Playground.

Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM

None

Other Libraries

None

OVL

SVUnit

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Icarus Verilog 12.0

Compile Options

-Wall -g2012

Run Options

Run Options

Use run.bash shell script

Open EPWave after run

Show output file after run

Download files after run

testbench.sv

```

1 // Code your testbench here
2 // or browse Examples
3 module counter_tb;
4     logic clk,rst;
5     logic [3:0]q;
6
7     counter uut(
8         .clk(clk),
9         .rst(rst),
10        .q(q)
11    );
12    initial clk=0;
13    always #5 clk=~clk;
14
15    initial begin
16        $monitor("time=%t,b=%b,rst=%d",$time,rst,q);
17
18        rst=1;
19        #10 rst=0;
20        #150 $finish;
21    end
22    initial begin
23        $dumpfile("counter.vcd");
24        $dumpvars(0,counter_tb);
25    end
26 endmodule
27
28
29

```

design.sv

```

1 // Code your design here
2 module counter(
3     input logic clk,
4     input logic rst,
5     output reg[3:0]q
6 );
7     always_ff @(posedge clk)
8     begin
9         if(rst)
10            q<=4'b0000;
11        else
12            q<=q+1'b1;
13        end
14 endmodule
15

```

Log

Share

16-bit synchronous counter

0 views and 0 likes

Public (anyone with the link can view)

Save

16-bit synchronous counter

https://www.edaplayground.com/x/cfND

From: 0s To: 160s

Radix

100%

0s

^

v

x

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Waveform output