B.TECH APPLIED ELECTRONICS AND INSTRUMENTATION ENGINEERING

LAB MANUAL

for the course

AEL331 ANALOG INTEGRATED CIRCUITS AND INSTRUMENTATION LAB

FIFTH SEMESTER B.TECH APPLIED ELECTRONICS & INSTRUMENTATION ENGINEERING

affliated to

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

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Part I

ANALOG INTEGRATED CIRCUITS LAB EXPERIMENTS

EXPERIMENT NO: 1

FAMILIARIZATION OF OPERATIONAL AMPLIFIER

AIM

1. To familiarize with OPAMP 741 IC
2. To design and set up Inverting amplifier using 741 OPAMP IC and plot the frequency response characteristics.
3. To design and set up Non Inverting amplifier using 741 OPAMP IC and plot the frequency response characteristics.
4. To design and set up an Integrator and Differentiator using 741 OPAMP IC .

THEORY

OPERATIONAL AMPLIFIERS

An operational amplifier is a direct coupled, high gain amplifier consisting of one or more differential amplifiers followed by a level translator and an output stage (Figure 1.1). It is available as a single Integrated Circuit package. It has two differential i/p terminals and one o/p terminal. The inputs, identified by the "$-$" and "$+$" symbols, are designated inverting and noninverting inputs respectively. Their voltages with respect to ground are denoted v_N and v_P, and the output voltage as v_O

The ideal and practical equivalent circuits for an op-amp are shown in figure 1.2. In the absence of output loading, $v_O = av_D = a(v_P - v_N)$, where a is the open loop gain of the op-amp.

Ideal characteristics of an Op-amp are

- Open loop voltage gain, $A_{OL} = \infty$
- Input impedance, $R_i = \infty$
- Output impedance, $R_O = 0$
- Bandwidth $= \infty$
- Zero offset. i.e., $v_O = 0$, when $v_P = v_N = 0$
- Ideal OPAMP draws no current at its input terminals, $i_P = i_N = 0$
- Output voltage is independent of the current drawn from the circuit
- Common Mode Rejection Ratio, $CMRR = \infty$
- Slew Rate $\mu = \infty$

μA741 OPAMP IC

The μA741 device is a general-purpose operational amplifier featuring offset-voltage null capability(Figure 1.3). The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low-value potentiometer may be connected between the offset null inputs to null out the offset voltage. The μA741 device is specified for operation from ± 5 to ± 15 V; many specifications apply from 0^O C to 70^OC. It has a $0.5V/\mu s$ slew rate. The circuit symbol of OPAMP is shown in figure 1.4.

Linear Op-amp circuits

Linearity is achieved by using negative feedback to force the op amp to operate within its linear region AND Implementing the feedback network with linear elements. E.g.: Inverting and Non-inverting amplifiers, Buffer amplifiers, Instrumentation amplifiers etc.

Nonlinear Op-amp circuits

Nonlinearity is either achieved by

1. Using positive feedback (or even no feedback at all), causing the op amp to operate primarily in saturation. E.g.: voltage-comparator and Schmitt-trigger or

2. Implementing negative feedback network with nonlinear elements, such as diodes and analog switches. E.g.: precision rectifiers, peak detectors, logarithmic amplifiers etc.

Virtual Ground

When operated with negative feedback, an ideal op amp will output whatever voltage and current it takes to drive v_D to zero or, equivalently, to force v_N to track v_P, but without drawing any current at either input terminal. Thus for voltage purposes the input port appears a short circuit and for current purposes the input port appears as an open circuit. Hence, it is referred to as a virtual short or virtual ground. This considerably simplifies the analysis of a ideal op-amp circuit with negative feedback.

INVERTING AMPLIFIER

It is a most widely used of all the operational amplifier circuits. The output voltage is fed back to the inverting input terminal through the $R_f - R_1$ network where R_f is feedback resistor. Input signal V_i is applied to the inverting input terminal through R_1 and non inverting input terminal of operational amplifier is grounded (Figure 1.5).

Since the inverting terminal is at ground terminal, the current i_1 through R_i is $\frac{V_i}{R_i}$. Also, since operational amplifier draws no current, all the current flowing through R_1 must flow through R_f. The output voltage, $V_O = -i_1 R_f = -\frac{V_i}{R_1} R_f$. Hence gain of the inverting amplifier (also refers to as closed loop gain) is

$$A_v = \frac{V_O}{V_i} = -\frac{R_f}{R_1}$$

The closed loop gain A_v is independent of a, and its value is set exclusively by the external resistance ratio.

The negative sign indicates a phase shift of 180^O between V_i and V_O. Also since inverting input terminal is at virtual ground, the effective input impedance is $R_i = R_1$. The value of R_i should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit.Output Resistances of Inverting Amplifier is $R_O = 0$ (ideally).

NON INVERTING AMPLIFIER

If a signal is applied to the non inverting input terminal and feedback is given as shown in figure 1.6. The circuit amplifies without inverting the input signal. Such a circuit is called Non Inverting Amplifier. It may be noted that it is also a negative feedback system as output is being feedback to the inverting input terminal.

As the differential voltage at the input terminal of operational amplifier is zero, the voltage at inverting terminal node is V_i, same as the input voltage applied to non inverting input terminal.

Now R_f and R_1 forms a potential divider. Hence, $V_i = \frac{V_O R_1}{R_1 + R_f}$ as no current flows into the operational amplifier. Thus, for non inverting amplifier the voltage gain,

$$A_v = 1 + \frac{R_f}{R_1}$$

The gain can be adjusted to unity or more, by proper selection of R_f and R_1. Compared to the inverting amplifier, the input resistance of non inverting amplifier extremely large (= ∞) as operational amplifier draws negligible current from the signal source.

INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or integration amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The output voltage is given by

$$V_O = -\frac{1}{R_1 C_f} \int V_{in} dt + v_O(0)$$

where $v_O(0)$ is the value of output voltage at time t=0 seconds. The equation for output voltage indicates that the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant $R_1 C_f$. If the input is a sine wave, the output will be cosine wave or if the input is a square wave,the output will be triangular wave.

When $V_{in} = 0$, the integrator works as open loop amplifier. This is because the capacitor C_f acts as an open circuit($X_{C_f} = \infty$) to the input offset voltage V_{in}. In other words, the input offset voltage $V_{in}$and the part of the input current charging capacitor C_f produce the error voltage at the output of the integrator. Therefore, in the practical integrator , to reduce the error voltage at the output a resistor R_f is connected across the feedback capacitor C_f. Thus R_f limits the low frequency gain and hence minimizes the variations in the output voltage. Both the stability and low frequency roll off problems can be corrected by the addition of a resistor R_f. The term stability refers to a constant gain as frequency of an input signal is varied over a certain range. Also, low frequency roll off refers to the rate of decrease in gain at lower frequencies. In the frequency response characteristics, for some relative frequency f to f_a, gain $\frac{R_f}{R_1}$ is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b, the circuit acts an integrator. f_b is the frequency at which the gain becomes zero dB and it is given by

$$f_b = \frac{1}{2\pi R_1 C_f}$$

The gain limiting frequency f_a is given by

$$f_a = \frac{1}{2\pi R_f C_f}$$

Generally, the value of f_a and in turn R_1C_f values should be selected such that $f_a < f_b$. For example, if $f_a = \frac{f_b}{10}$, then $R_f = 10R_1$. In fact, the input signal will be integrated properly if the time period T of the signal is larger than or equal to R_fC_f. That is, $T \geq R_fC_f$, where $R_fC_f = \frac{1}{2\pi f_a}$.

The integrator is most commonly used in analog computers and analog to digital(ADC) and signal wave shaping circuits.

DIFFERENTIATOR

The differentiator or differentiation amplifier circuit performs the mathematical operation of differentiation i.e., the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The output voltage is given by

$$V_0 = -R_fC_1\frac{dV_{in}}{dt}$$

Thus the output V_0 is equal to R_fC_1 times the negative instantaneous rate of change of the input voltage V_{in} with time. Since the differentiator performs the reverse of integrator's function, a cosine wave input will produce a sine wave output, or a triangular input will produce a square wave output.

The gain of the circuit $(\frac{R_f}{X_{C_1}})$ increases with increase in frequency at a rate of 20dB/decade. This makes the circuit unstable. Also, the input impedance X_{C_1} decreases with increase in frequency, which makes the circuit very susceptible to high frequency noise. When amplified, this noise can completely override the differentiated output signal.

Both the stability and the high frequency noise problems can be corrected by the addition of two components: R_1 and C_f. In the frequency response characteristics, from from frequency f to f_b, the gain increases at 20 dB/decade. However after f_b, the gain decreases at 20 dB/decade. This 40 dB/decade change in gain is caused by the R_1C_1 and R_fC_f combinations. The gain limiting frequency f_b is given by

$$f_b = \frac{1}{2\pi R_1C_1}$$

where $R_1C_1 = R_fC_f$. f_a is the frequency at which the gain is 0dB and is given by

$$f_a = \frac{1}{2\pi R_fC_1}$$

Also, $f_c$is the unity gain bandwidth of the op-amp, and f is some relative operating frequency. The R_1C_1 and R_fC_f help to reduce significantly the effect of high frequency input, amplifier noise, and offsets. Above all, R_1C_1 and R_fC_f make the circuit more stable by preventing the increase in gain with frequency. Generally, the value of f_b and in turn R_1C_1 and R_fC_f values should be selected such

way that $f_a < f_b < f_c$. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_f C_1$ i.e., $T \geq R_f C_1$.

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in an input signal and also as a rate of change detector in FM modulators.

PROCEDURE

Common Steps

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

Inverting Amplifier

• Give a 1 V_{PP} sine wave with 1KHz frequency as the input

• Observe input and output waveforms on the two channels of the CRO simultaneously

• Note down the amplitude of the output wave and verify the CL gain

• Verify that the output and input have a 180^O phase shift

• Repeat the experiment with sine waves of different frequency keeping the input amplitude the same. Observe the output amplitudes and plot the frequency response

• Find maximum gain and Higher cutoff frequency.

Non Inverting Amplifier

• Give a 1 V_{PP} sine wave with 1KHz frequency as the input

• Observe input and output waveforms on the two channels of the CRO simultaneously

• Note down the amplitude of the output wave and verify the CL gain

• Verify that the output and input are inphase.

• Repeat the experiment with sine waves of different frequency keeping the input amplitude the same.

Observe the output amplitudes and plot the frequency response

• Find maximum gain and Higher cutoff frequency.

Integrator and Differentiator

• Give integrator a square wave input of $1V_{PP}$ and frequency equal to cutoff frequency.

• Observe input and output waveforms on the two channels of the CRO simultaneously

• Repeat the same for frequency 10 time less and greater than cutoff frequency.

• Plot the waveforms

• For plotting frequency response, Give a 1 V_{PP} sine wave with 1KHz frequency as the input

• Observe input and output waveforms on the two channels of the CRO simultaneously

• Note down the amplitude of the output wave

• Repeat the experiment with sine waves of different frequency keeping the input amplitude the same.

Observe the output amplitudes and plot the frequency response

• Find the cutoff frequency from frequency response plot.

• Repeat the same for differentiator.

OPERATIONAL AMPLIFIER

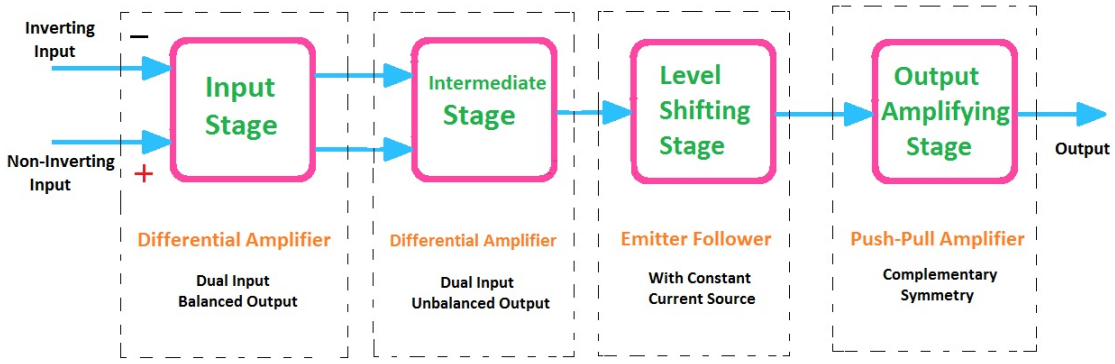


Figure 1.1: Block Diagram of OPAMP

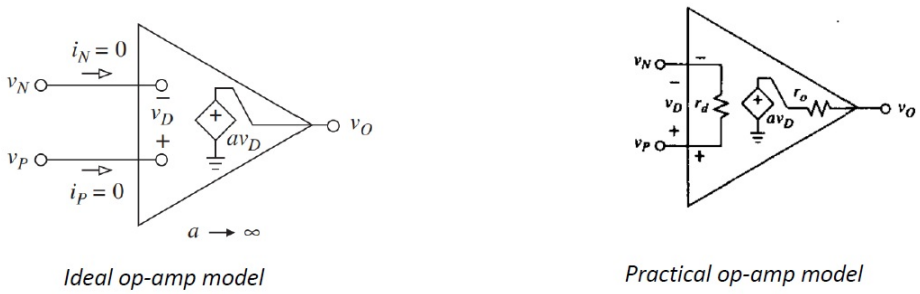


Figure 1.2: Small Signal Model of OPAMP

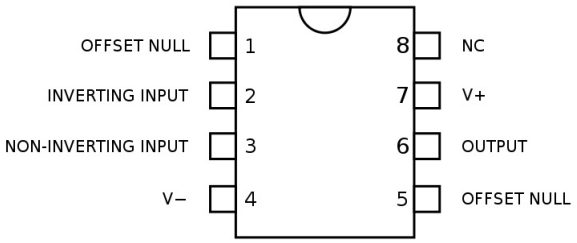


Figure 1.3: Pin Diagram of 741 OPAMP IC

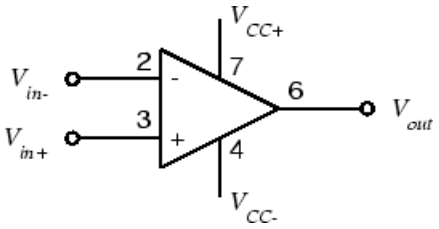


Figure 1.4: Circuit Symbol Of OPAMP

INVERTING AND NON INVERTING AMPLIFIER

Circuit Diagram

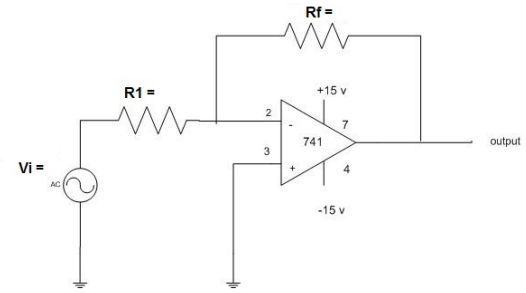


Figure 1.5: Inverting Amplifier

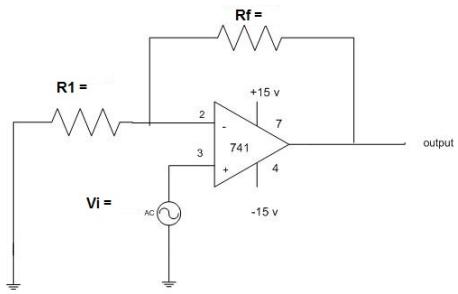


Figure 1.6: Non Inverting Amplifier

Design of Inverting Amplifier

$A_v = -\frac{R_f}{R_1}$

Choose A_v=10

Select $R_1 = 1K\Omega$std

$R_f = 10K\Omega$ std.

Design of Non Inverting Amplifier

$A_v = 1 + \frac{R_f}{R_1}$

Choose A_v=11

Select $R_1 = 1K\Omega$std

$R_f = 10K\Omega$ std.

Observation

Table 1-1: Frequency Response of Inverting Amplifier
$V_{in} = 2V_{pp}$

Frequency(Hz)	$V_o(V_{pp})$	log f	Gain = $\frac{V_o}{V_{in}}$	Gain in dB = 20 log($\frac{V_o}{V_{in}}$)

Table 1-2: Frequency Response of Non Inverting Amplifier
$V_{in} = 2V_{pp}$

Frequency(Hz)	$V_o(V_{pp})$	log f	Gain = $\frac{V_o}{V_{in}}$	Gain in dB = 20 log($\frac{V_o}{V_{in}}$)

Sample Graph

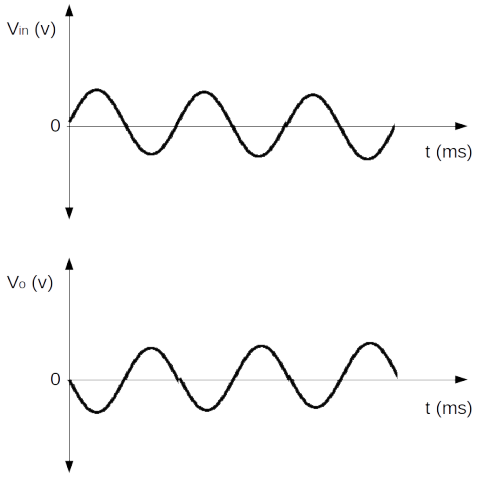


Figure 1.7: Inverting Amplifier

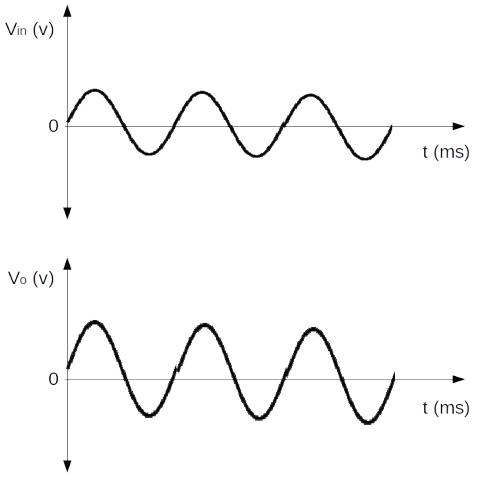


Figure 1.8: Non-inverting Amplifier

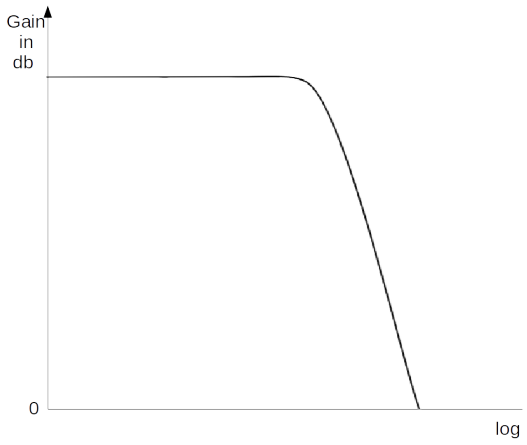


Figure 1.9: Frequency Response Characteristics of Inverting Amplifier

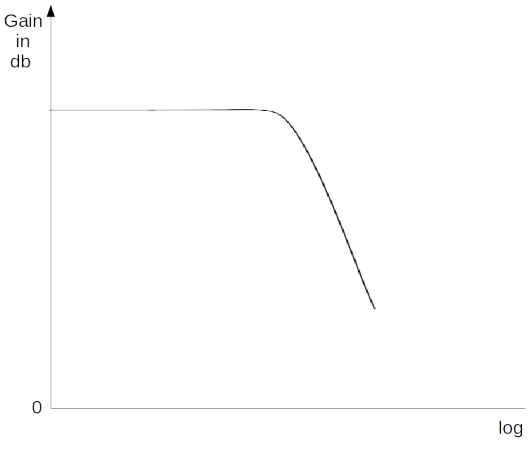


Figure 1.10: Frequency Response Characteristics of Non-inverting Amplifier

Output

INTEGRATOR AND DIFFERENTIATOR

Circuit Diagram of Integrator

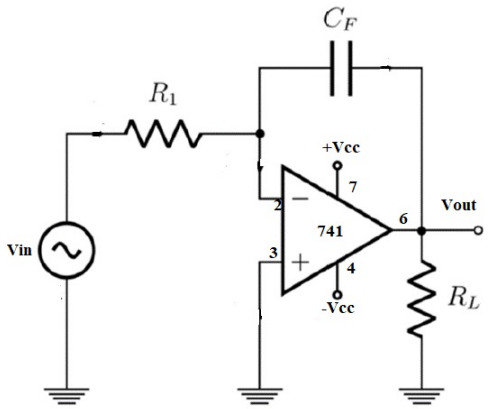


Figure 1.11: Basic Integrator

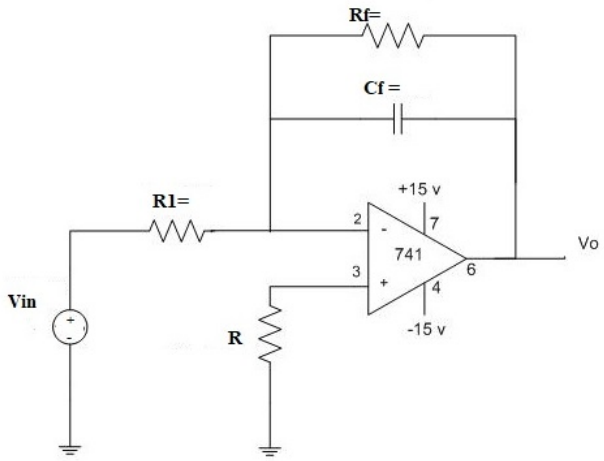


Figure 1.12: Practical Integrator

Circuit Diagram of Differentiator

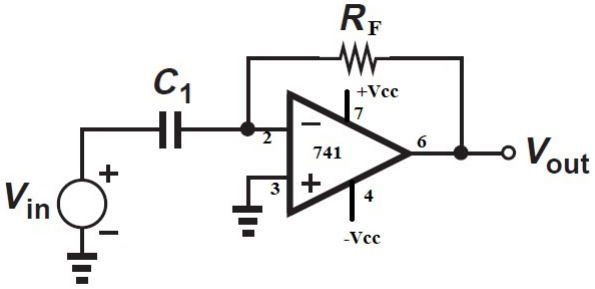


Figure 1.13: Basic Differentiator

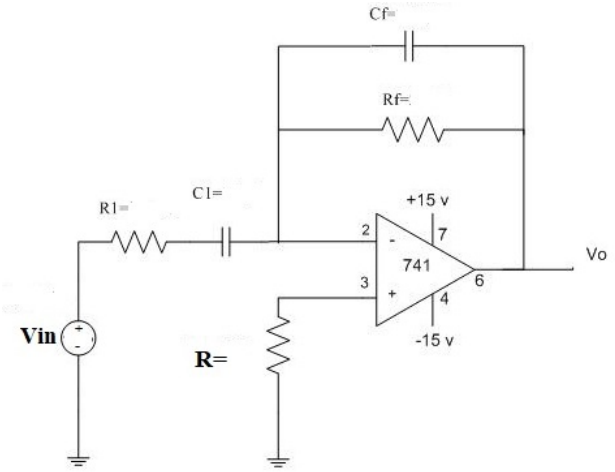


Figure 1.14: Practical Differentiator

Design of Integrator

We have $f_a = \frac{1}{2\pi R_f C_f}$ and $f_b = \frac{1}{2\pi R_1 C_f}$

Assume f_a : f_b=1:10

Choose f_a=1 KHz, f_b =10KHz

Select C_f=0.01μF std.

R_f=$\frac{1}{2\pi f_a C_f}$=15KΩ std

R_1=$\frac{1}{2\pi f_b C_f}$=1.5KΩ std

Take $R = R_1 = 1.5K\Omega std$

Design of Differentiator

Select $f_a = 500\text{Hz}$, $f_a = \frac{1}{2\pi R_f C_1}$

Choose $C_1 = 0.1\mu\text{F}$ std.

R_f =2.7K std.

$f_b = 10 f_a = 10 \times 500 = 5kHz = \frac{1}{2\pi R_1 C_1}$

$R_1 = 330\Omega\text{std}$

$R_1 C_1 = R_f C_f$

$C_f = 0.01\mu\text{F}$ std.

Observation

Table 1-3: Frequency Response of Integrator
$V_{in} = 1V_{pp}$

Frequency(Hz)	$V_o(Volt)$	log f	Gain in dB = 20 log($\frac{V_o}{V_{in}}$)

Table 1-4: Frequency Response of Differentiator
$V_{in} = 1V_{pp}$

Frequency(Hz)	$V_o(Volt)$	log f	Gain in dB = 20 log($\frac{V_o}{V_{in}}$)

Sample Graph

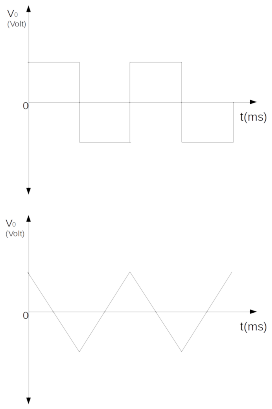


Figure 1.15: Integrator - Input Square wave

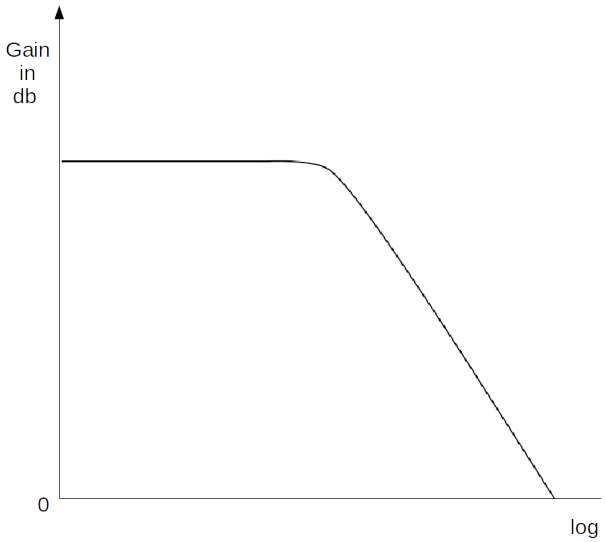


Figure 1.16: Integrator - Frequency Response Characteristics

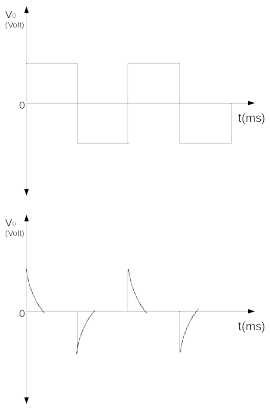


Figure 1.17: Differentiator - Input Square wave

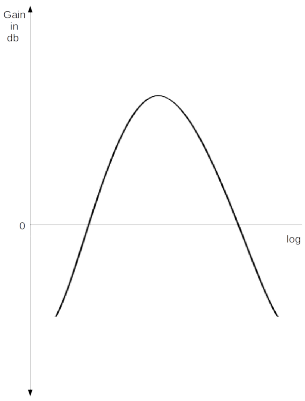


Figure 1.18: Differentiator - Frequency Response Characteristics

Output

RESULT

1. Familiarized with 741 Opamp IC

2. Designed and set up inverting amplifier for a voltage gain of 10 using IC 741 and plotted the frequency response.
   Higher cut-off frequency, f_H=

3. Designed and set up Non inverting amplifier for a voltage gain of 11 using IC 741 and plotted the frequency response.
   Higher cut-off frequency, f_L=

4. Designed and set up an integrator for cutoff frequency 10KHz using IC 741 and observed the output for squarewave input. Also plotted the frequency response.
   CutOff frequency, f_b=
   Gain Limiting Frequency, f_a=
   Roll off rate=

5. Designed and set up an differentiator for cutoff frequency 1KHz using IC 741 and observed the output for squarewave input. Also plotted the frequency response.
   CutOff frequency, f_a=
   Gain Limiting Frequency,f_b=
   Roll off rate=

EXPERIMENT NO: 2

DESIGN OF ADDERS USING 741 IC

AIM

1. To design and set up Inverting adder using 741 OPAMP IC.

2. To design and set up Non Inverting adder using 741 OPAMP IC.

THEORY

SUMMING AMPLIFIER

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a **Summing Amplifier or Adder**. The output is a weighted sum of the inputs, with the weights being established by resistance ratios.

Inverting Adder: It is an adder that gives an inverted sum. A typical two input summing amplifier consists of two input resistors R_1 and R_2 to which the input voltages V_1 and V_2 are applied and a feedback resistor R_f. The op-amp is assumed to be ideal i.e., $A_{OL} = \infty$ and $R_i = \infty$. Since the input current is assumed to be zero, there is no voltage drop at non inverting terminal and hence it is at ground potential. So the voltage at inverting terminal is also zero as virtual short exist between the inverting and non inverting terminals. So output voltage

$$V_O = -(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2)$$

If $R_1 = R_2 = R_f$, the output will be the inverted sum of the input signals.

Non Inverting Adder: A summer that gives a non inverted sum is the non inverting adder. A typical two input non inverting adder consists of two input resistors R_1 and R_2 at non inverting

terminal through which input voltage V_1 and V_2 are applied, a resistors R_i connected to inverting terminal and a feedback resistors R_f. The output voltage is

$$V_O = (1 + \frac{R_f}{R_i}) \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

which is the non inverted weighted sum of inputs.

PROCEDURE

Common Steps

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

Summing Amplifier

• Give the inputs 1V, 2V and 0.5V DC.

• Observe input and output waveforms on the two channels of the CRO simultaneously

• Check whether the output is weighted sum of Inputs.

• Plot the waveforms

SUMMING AMPLIFIERS OR ADDERS

Circuit Diagram

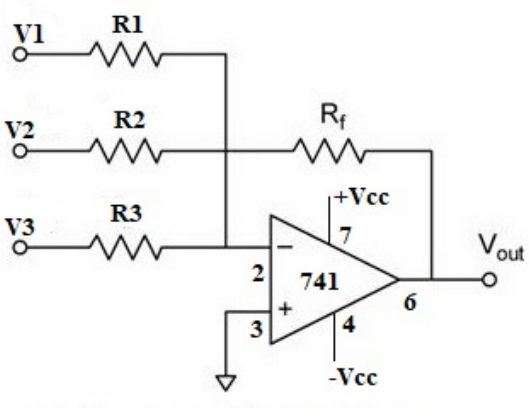


Figure 2.1: 3 Input Inverting Adder

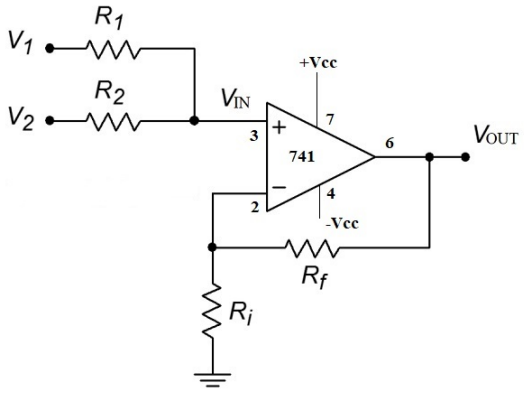


Figure 2.2: 2 Input Non Inverting Adder

Design of Inverting Adder

To design a inverting adder with $V_O = -(2V_1 + 3V_2 + V_3)$

$$V_O = -(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3)$$

So $\frac{R_f}{R_1}$=2, $\frac{R_f}{R_2}$=3, and $\frac{R_f}{R_3}$=1
Select $R_f = 10K\Omega$ std

$R_1 = 2K\Omega = 1.8K\Omega$ std, $R_2 = 3.3K\Omega$ std, $R_3 = 10K\Omega$ std

Design of Non Inverting Adder

To design a non-inverting adder with $V_O = V_1 + V_2$

$$V_O = (1 + \frac{R_f}{R_i})\frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}}$$

Take $R_1 = R_2 = R = 10K\Omega$ std, then $V_O = (1 + \frac{R_f}{R_i})\frac{V_1 + V_2}{2}$

Take $A_v = 2 = 1 + \frac{R_f}{R_i}$

Select $R_f = 10K\Omega$ std, then $R_i = 10K\Omega$ std

Sample Graph

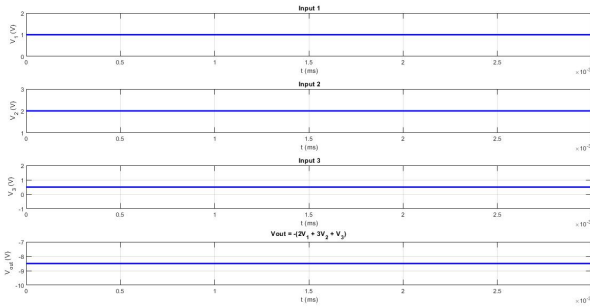


Figure 2.3: 3 Input Inverting Adder

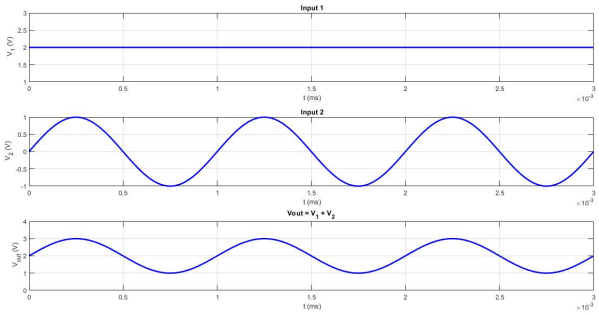


Figure 2.4: 2 Input Non Inverting Adder

Output

RESULT

1. Designed and set up inverting adder for $V_{out} = -(2V_1 + 3V_2 + V_3)$ using IC 741 and verified the output.

2. Designed and set up Non inverting adder for $V_{out} = V_1 + V_2$ using IC 741 and verified the output.

EXPERIMENT NO: 3

MEASUREMENT OF OPERATIONAL AMPLIFIER PARAMETERS

AIM

To measure the following OPAMP parameters of LM741 IC

1. Input Offset Voltage
2. Input Bias Current
3. Input Offset Current
4. Slew Rate
5. CMRR

THEORY

An ideal OPAMP has the following parameter values.

- Open loop voltage gain, $A_{OL} = \infty$
- Input impedance, $R_i = \infty$
- Output impedance, $R_O = 0$
- Bandwidth $= \infty$
- Zero offset. i.e., $v_O = 0$, when $v_P = v_N = 0$
- Ideal OPAMP draws no current at its input terminals, $i_P = i_N = 0$
- Output voltage is independent of the current drawn from the circuit

• Common Mode Rejection Ratio, $CMRR = \infty$

• Slew Rate $\mu = \infty$

A practical op-amp has neither infinite gain and bandwidth nor zero output resistance. It may have a non-zero input offset voltage and a finite slew rate. These non-ideal parameters may have a significant impact on the circuit performance.

INPUT OFFSET VOLTAGE

The ideal op-amp produces zero volts output for zero volts input. In a practical op-amp, however, a small dc voltage, appears at the output even when no differential input voltage is applied. Its primary cause is a slight mismatch of the base-emitter voltages of the differential input stage of an op-amp. Input Offset Voltage is defined as the voltage that must be applied between the two input terminals of an opamp to nullify the output.
Maximum value of $V_{io} = 6mV$ for 741

INPUT BIAS CURRENT

The input terminals of a bipolar differential amplifier are the transistor bases and, therefore, the input currents are the base currents. i.e., The input bias current I_B is the average of the current entering the input terminals. It is used for biasing the input transistors.

$$I_B = \frac{I_{B1}+I_{B2}}{2}$$

$I_B = 500nA$ for 741.

INPUT OFFSET CURRENT

Ideally, the two input bias currents are equal, and thus their difference is zero. In a practical op-amp, however, the bias currents are not exactly equal. The input offset current I_{io} is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier.

$$I_{io} = |I_{B1} - I_{B2}|$$

Maximum $I_{io} = 200nA$ for 741.

SLEW RATE

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions. Slew rate indicates how rapidly the output of an opamp can change in response to

changes in the input frequency. It is expressed in $V/\mu s$.

$$SR = \frac{dV_o}{dt}|_{max}$$

The slew rate changes with change in voltage gain and is normally specified at unity gain Its low slew rate ($0.5V/\mu s$) is a drawback for 741

COMMON MODE REJECTION RATIO

CMRR is the ratio of the Differential Voltage Gain A_d to the Common Mode Voltage Gain A_{CM}. An ideal opamp has infinite CMRR.Typical value of CMRR=9OdB for 741C. The higher the value of CMRR, the better is the matching between two input terminals & the smaller is the output common mode voltage.

CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown below. Note that inverting mode operating op amps will have less CMRR error. Since both inputs are held at a ground (or virtual ground), there is no CM dynamic voltage. The sensitivity to CM can be modeled with an input-offset-voltage term of value $v_{CM}/CMRR$

PROCEDURE

Common Steps

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

Input Offset Voltage

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Measure the dc output voltage, V_{os}

• Divide this value with the gain of the amplifier (1001) to obtain the input offset voltage V_{is}

Input Bias Current and Input Offset Current

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Measure the voltages V_- and V_+ at the inverting and non inverting input terminals of the opamp respectively.

• Compute Base currents I_{B-} and I_{B+}

• Compute Input bias current I_B and Input Offset Current I_{io}

Slew Rate

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Apply a square wave of $20V_{PP}$ amplitude and 1kHz frequncy at inverting terminal of op-amp and observe the output waveform on the CRO

• Increase the frequency of the square wave until the output becomes triangular (with $20V_{PP}$ amplitude)

• Compute the rising edge slope of the triangle-wave at the output. This value is taken as the slew rate of the op-amp.

CMRR

• Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Give $V_{in} = 1V$ dc and measure V_{out}

• Give $V_{in} = 2V$ dc and measure V_{out}

• Compute $\triangle V_{out}$ and substitute in the expression below expression to obtain the CMRR value

$$CMRR = \frac{\triangle V_{in}}{\triangle V_{out}} \times \frac{R_2}{R_1+R_2}(1+\frac{R_2}{R_1})$$

INPUT OFFSET VOLTAGE

Circuit Diagram

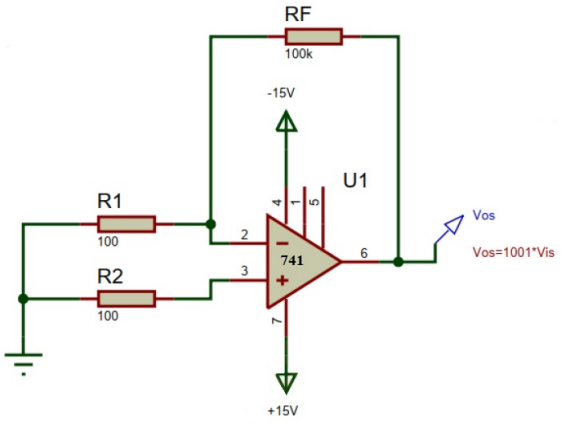


Figure 3.1: Input Offset Voltage Measurement

Design

Choose $R_F = 100K\Omega$ and $R_1 = 100\Omega$ so that the gain of the non-inverting amplifier,

$A_v = 1 + \frac{R_F}{R_1} = 1001$

Thus $V_{is} = \frac{V_{os}}{1001}$

INPUT BIAS CURRENT & INPUT OFFSET CURRENT

Circuit Diagram

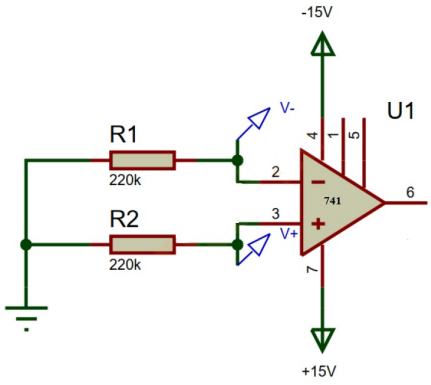


Figure 3.2: Input Bias Current and Input Offset Current Measurement

Design

Choose $R_1 = R_2 = 220K\Omega$ $I_{B-} = \frac{V_-}{220K}$ and $I_{B+} = \frac{V_+}{220K}$ Thus, Input Bias Current, $I_B = \frac{I_{B-}+I_{B+}}{2}$ and Input Offset Current, $I_{io} = |I_{B-} - I_{B+}|$

SLEW RATE

Circuit Diagram

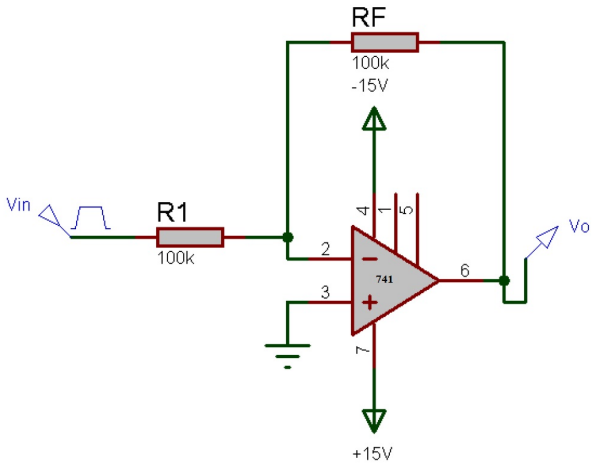


Figure 3.3: Slew Rate Measurement

Design

Choose $R_F = 100K\Omega$ and $R_1 = 100K\Omega$ Ideally, $V_o = V_{in}$

Expected Waveform

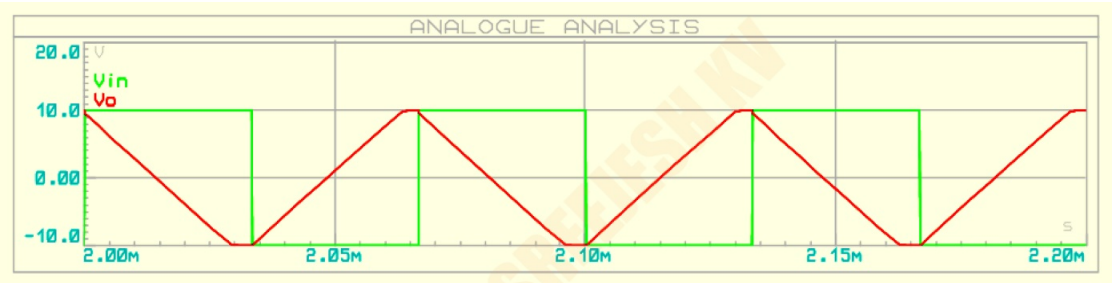


Figure 3.4: Slew Rate Measurement

COMMON MODE REJECTION RATIO (CMRR)

Circuit Diagram

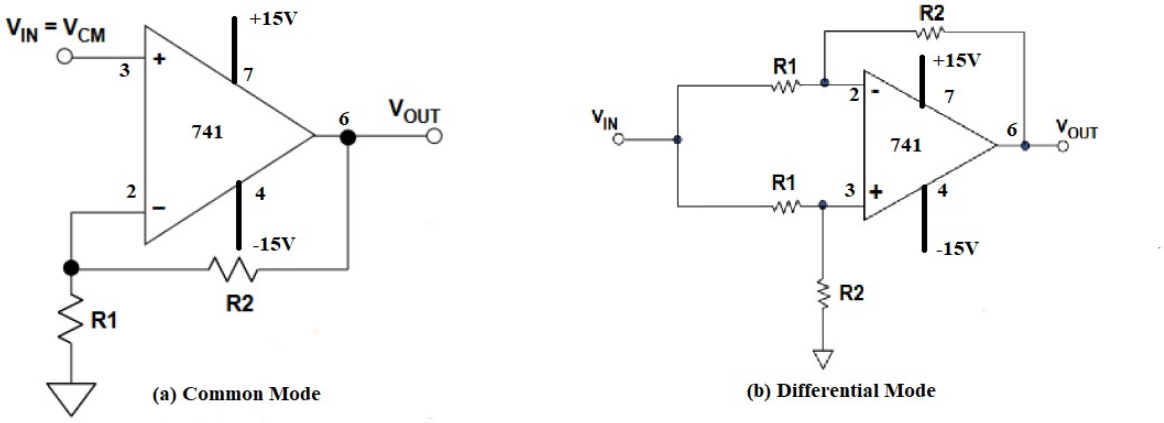


Figure 3.5: CMRR Measurement

Design

For Common Mode Input

$ERROR[RTI] = \frac{V_{CM}}{CMRR} = \frac{V_{IN}}{CMRR}$

$V_{OUT} = [1 + \frac{R_2}{R_1}][V_{IN} + \frac{V_{IN}}{CMRR}]$

$ERROR[RTO] = [1 + \frac{R_2}{R_1}][\frac{V_{IN}}{CMRR}]$

For Differential Mode Input

$\triangle V_{OUT} = \frac{\triangle V_{IN}}{CMRR}[1 + \frac{R_2}{R_1}]$

Resistors must match with $1ppm(0.0001\%)$ to measure CMRR > 100dB.

Here $v_P = v_{IN} \times \frac{R_2}{R_1+R_2} = v_{CM}$

Also $v_N = v_P$ due to virtual short.

$v_{OUT} = (v_P + \frac{v_{CM}}{CMRR})(1 + \frac{R_2}{R_1}) - v_{IN}(\frac{R_2}{R_1})$

$= v_{IN} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1}) + \frac{v_{IN}}{CMRR} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1}) - v_{IN}(\frac{R_2}{R_1})$

$= \frac{v_{IN}}{CMRR} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1})$

Thus, $\triangle V_{out} = \frac{\triangle V_{in}}{CMRR} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1})$

$\Rightarrow CMRR = \frac{\triangle V_{in}}{\triangle V_{out}} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1})$

OBSERVATIONS

Input Offset Voltage

$V_{os} =$

$V_{is} = \frac{V_{os}}{1001} =$

Input Bias Current and Input Offset Current

$I_{B-} = \frac{V_-}{220K} =$

$I_{B+} = \frac{V_+}{220K} =$

Input Bias Current, $I_B = \frac{I_{B-}+I_{B+}}{2} =$

Input Offset Current, $I_{io} = |I_{B-} - I_{B+}| =$

Input Offset Voltage

$SR = \frac{dV_o}{dt}|_{max} =$

CMRR

For $V_{in} = 1V$ DC, $V_{out} =$

For $V_{in} = 2V$ DC, $V_{out} =$

$\triangle V_{in} =$

$\triangle V_{out} =$

$CMRR = \frac{\triangle V_{in}}{\triangle V_{out}} \times \frac{R_2}{R_1+R_2}(1 + \frac{R_2}{R_1}) =$

RESULT

Thus designed and setup ciruits for measuring OPAMP parameters and measured the following parameters

1. Input Offset Voltage, $V_{is} =$
2. Input Bias Current, $I_B =$
3. Input Offset Current, $I_{io} =$
4. Slew Rate, $SR =$
5. CMRR

EXPERIMENT NO: 4

SCHMITT TRIGGER USING 741 IC

AIM

1. To design and set up Non-Inverting Schmitt trigger circuits using IC 741 for Symmetric Trigger Points, V_{UTP}=..... and V_{LTP}=.....

2. To design and set up Inverting Schmitt trigger circuits using IC 741
   a) For Symmetric Trigger Points, V_{UTP}=..... and V_{LTP}=.....
   b) For Asymmetric Trigger Points, V_{UTP}=..... and V_{LTP}=.....
   c) For Asymmetric Trigger Points, V_{UTP}=..... and V_{LTP}=.....

THEORY

A comparator with positive feedback which converts an irregular shaped waveform to a square wave or pulse is known as Schmitt trigger or squaring circuit. Schmitt triggers are special type of comparators with hysteresis, which can be implemented by providing operational amplifiers/comparators with positive feedback. Its output voltage has two stable states namely $v_O = V_{OH}$ and $v_O = V_{OL}$. For an op-amp $V_{OH} = +V_{sat}$ and $V_{OL} = -V_{sat}$ respectively.

INVERTING SCHMITT TRIGGER

The inverting Schmitt trigger circuit can be viewed as an inverting-type threshold detector whose threshold is controlled by the output. Since the output has two stable states, this threshold has two possible values, namely $V_{UTP} = \frac{R_1}{R_1+R_2}V_{OH}$ and $V_{LTP} = \frac{R_1}{R_1+R_2}V_{OL}$.

For $v_{IN} << 0$, the amplifier saturates at V_{OH}, giving $v_O = V_{OH}$ and $v_P = V_{UTP}$. Increasing v_{IN} moves the operating point along the upper segment of the Voltage Transfer Curve(VTC) until v_{IN}

reaches V_{UTP}. At this point, the regenerative action ofpositive feedback causes v_O to snap from V_{OH} to V_{OL}. This, in turn, causes v_P to snap from V_{UTP} to V_{LTP}. If we wish to change the output state again to V_{OH}, we must now lower v_{IN} all the way down to $v_P = V_{LTP}$.

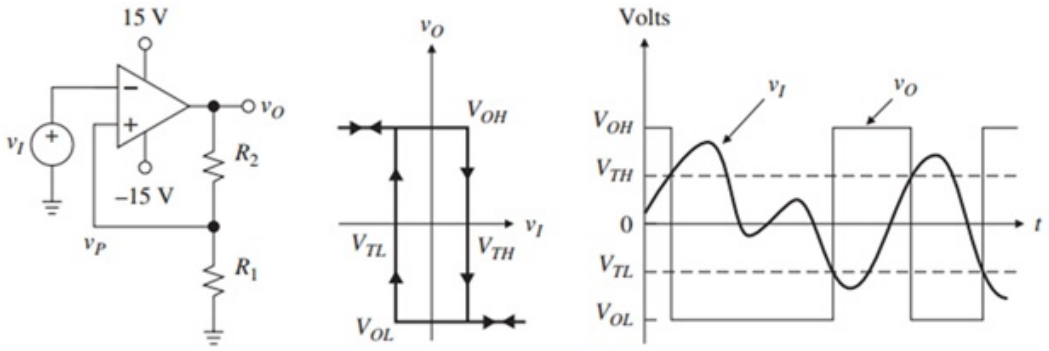


Figure 4.1: Inverting Schmitt Trigger

Thus, the Voltage Transfer Curve of an Inverting Schmitt trigger exhibits hysteresis (i.e., has two separate tripping points). When coming from the left, the threshold is V_{UTP}, and when coming from the right, it is V_{LTP}. The horizontal portions of the VTC can be traveled in either direction, but the vertical portions can be traveled only clockwise.

The hysteresis width, $\Delta V_T = V_{UTP} - V_{LTP} = \frac{R_1}{R_1+R_2}(V_{OH} - V_{OL})$ ΔV_T can be varied by changing the ratio R_1/R_2. Decreasing R_1/R_2 will bring V_{UTP} and V_{LTP} closer together.

NON-INVERTING SCHMITT TRIGGER

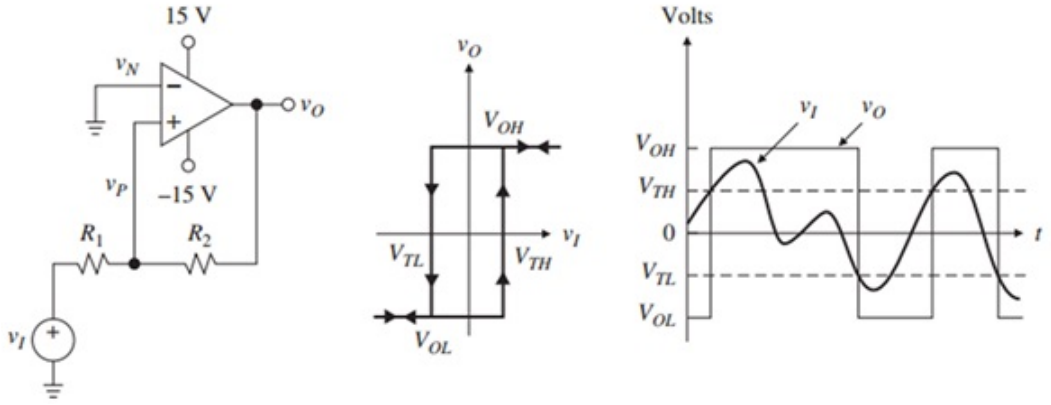


Figure 4.2: Non-Inverting Schmitt Trigger

For $v_{IN} << 0$, the op-amp saturates at V_{OL}. For v_O to switch state, v_{IN} must be raised to a high enough value(called V_{UTP}) to cause $v_P > v_N (= 0V)$.

$\implies \frac{V_{UTP}-0}{R_1} = \frac{0-V_{OL}}{R_2} \implies V_{UTP} = -\frac{R_1}{R_2}V_{OL}$

Once v_O has reached V_{OH}, in order to step it back toV_{OL}, v_{IN} must be lowered below V_{LTP}.

$\Longrightarrow \frac{V_{OH}-0}{R_2} = \frac{0-V_{LTP}}{R_1} \Longrightarrow V_{UTP} = -\frac{R_1}{R_2}V_{OH}$

The hysteresis width is $\Delta V_T = V_{UTP} - V_{LTP} = \frac{R_1}{R_2}(V_{OH} - V_{OL})$. It can be varied by changing the ratio R_1/R_2.

Thus, the Voltage Transfer Curve of a Non-inverting Schmitt trigger exhibits hysteresis (i.e., has two separate tripping points). When coming from the left, the threshold is V_{UTP}, and when coming from the right, it is V_{LTP}. The horizontal portions of the VTC can be traveled in either direction, but the vertical portions can be traveled only counter-clockwise

SCHMITT TRIGGERS WITH ASYMMETRICAL TRIGGER POINTS

The hysteresis loop can be shifted to either side of zero point by connecting a reference voltage source.

For an inverting Schmitt trigger with asymmetric trigger points,

$V_{UTP} = \frac{R_1}{R_1+R_2} \times V_{OH} + \frac{R_2}{R_1+R_2} \times V_{ref}$

and

$V_{LTP} = \frac{R_1}{R_1+R_2} \times V_{OL} + \frac{R_2}{R_1+R_2} \times V_{ref}$.

$\Delta V_T = V_{UTP} - V_{LTP} = \frac{R_1}{R_1+R_2}(V_{OH} - V_{OL})$ i.e., the hysteresis width remains the same.

If v_{REF} is positive, the hysteresis loop is shifted to right side; if v_{REF} is negative, the loop is shifted to the left side.

PROCEDURE

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower. • Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Apply a sine wave input of 100Hz and $20V_{pp}$.

• The output and transfer characteristics are observed in CRO and plotted on a graph sheet.

NON INVERTING SCHMITT TRIGGER

Circuit Diagram

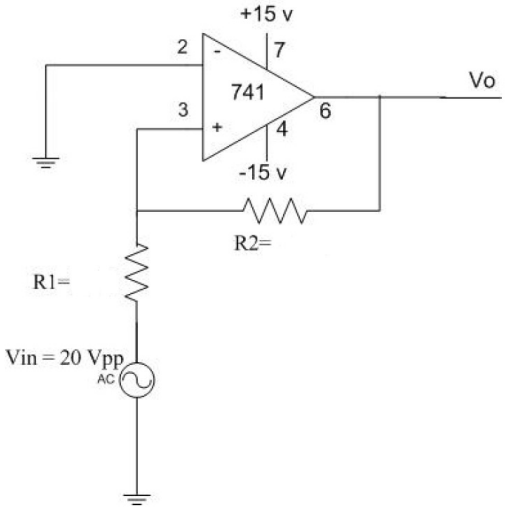


Figure 4.3: Non Inverting Schmitt Trigger

Design

We have $V_{UTP} = \frac{R_1}{R_2} V_{sat}$ and $V_{UTP} = -\frac{R_1}{R_2} V_{sat}$

Given V_{UTP}=.....V and V_{LTP}=.....V

For $\pm V_{CC} = \pm 15V$, Choose $V_{sat} = 13.5V$.

Select $R_1 = 1K\Omega$ std, then R_2 = ... = ... std

INVERTING SCHMITT TRIGGER

Circuit Diagram For Equal UTP And LTP

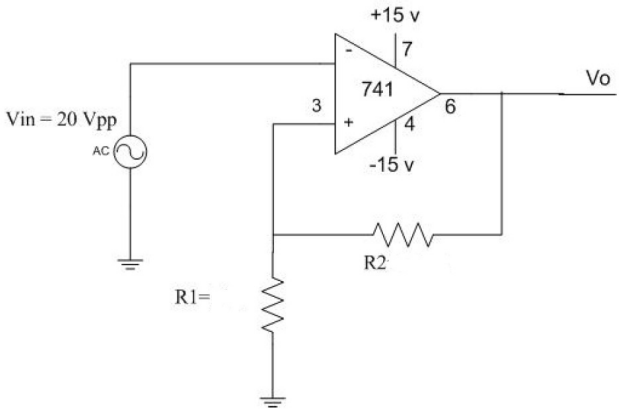


Figure 4.4: Inverting Schmitt Trigger with equal UTP and LTP

Design

We have $V_{UTP} = \beta V_{sat}$ and $V_{UTP} = -\beta V_{sat}$

where $\beta = \frac{R_1}{R_1+R_2}$

Given V_{UTP}=.....V and V_{LTP}=.....V

For $\pm V_{CC} = \pm 15V$, Choose $V_{sat} = 13.5V$.

Select $R_1 = 1K\Omega$ std, then

R_2 = ... = ... std

Circuit Diagram for Unequal UTP And LTP

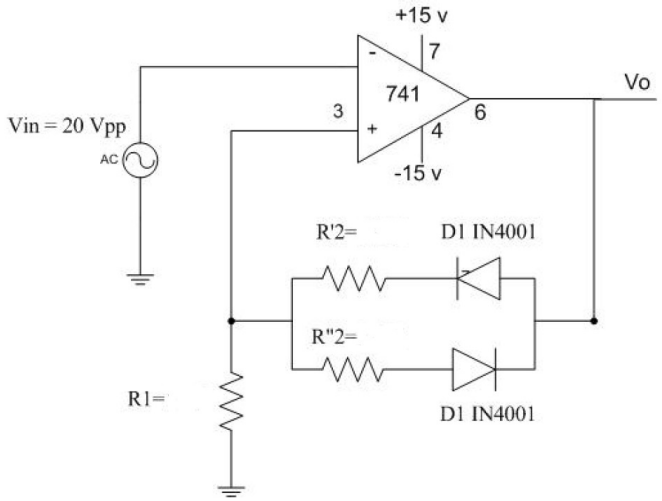


Figure 4.5: Inverting Schmitt Trigger with unequal UTP and LTP

Design

We have $V_{UTP} = \frac{R_1}{R_1+R_2'} V_{sat}$ and $V_{UTP} = -\frac{R_1}{R_1+R_2''} V_{sat}$

Given V_{UTP}=.....V and V_{LTP}=.....V

For $\pm V_{CC} = \pm 15V$, Choose $V_{sat} = 13.5V$.

Select $R_1 = 1K\Omega$ std, then

R_2' = ... = ... std, and

R_2'' = ... = ... std

Circuit Diagram for Unequal UTP and LTP Using Reference

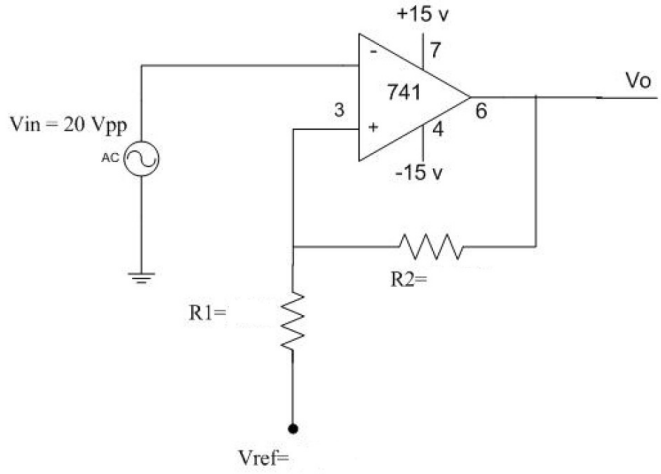


Figure 4.6: Inverting Schmitt Trigger with unequal UTP and LTP using Reference

Design

We have

$V_{UTP} = \frac{R_1}{R_1+R_2} \times V_{sat} + \frac{R_2}{R_1+R_2} \times V_{ref}$

$V_{LTP} = \frac{R_1}{R_1+R_2} \times -V_{sat} + \frac{R_2}{R_1+R_2} \times V_{ref}$

Given V_{UTP}=.....V and V_{LTP}=.....V

For $\pm V_{CC} = \pm 15V$, Choose $V_{sat} = 13.5V$.

Select $R_1 = 1K\Omega$ std, then

R_2 = ... = ... std, and

V_{ref} = ...V

SAMPLE GRAPH

Non Inverting Schmitt Trigger

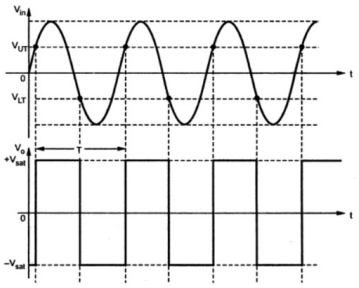


Figure 4.7: Input Output Waveforms of Non Inverting Schmitt Trigger

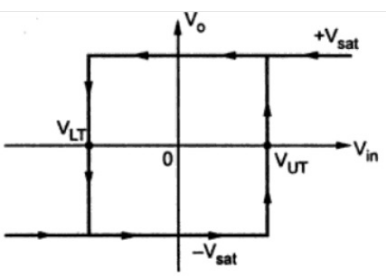


Figure 4.8: Hysteresis Loop of Non Inverting Schmitt Trigger

Non Inverting Schmitt Trigger

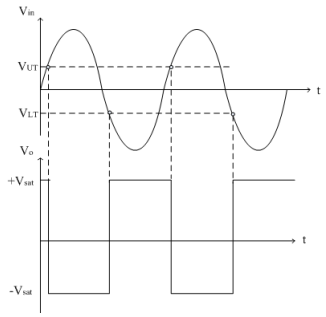


Figure 4.9: Input Output Waveforms of Inverting Schmitt Trigger

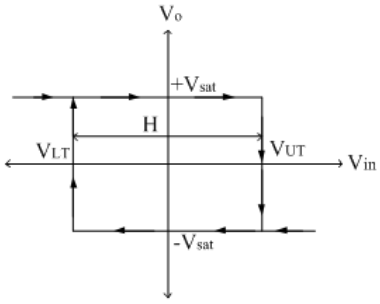


Figure 4.10: Hysteresis Loop of Inverting Schmitt Trigger

RESULT

The following Schmitt trigger are designed and set up using IC 741. Their input-output waveforms and transfer characteristics are plotted. The observed values are

Non Inverting Schmitt trigger

V_{UTP}=....., V_{LTP}=.....

Inverting Schmitt trigger

Case 1: V_{UTP}=....., V_{LTP}=.....

Case 2: V_{UTP}=....., V_{LTP}=.....

Case 3: V_{UTP}=....., V_{LTP}=.....

EXPERIMENT NO: 5

ASTABLE AND MONOSTABLE MULTIVIBRATORS USING 741 IC

AIM

To design and set up an astable multivibrator for a frequency of 1kHz with duty cycles 50% and 10% using IC 741.
To design and set up a monostable multivibrator for a pulse width of 1 ms using IC 741.

THEORY

ASTABLE MULTIVIBRATOR

Astable multivibrator is capable of producing square wave for given frequency, amplitude and duty cycle. A simple op-amp square wave generator (astable multivibrator) also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. The output of the op-amp will be $+ve$ saturation if differential input voltage is negative and vice versa. Fraction $\beta = R_2/(R_1+R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βV_0 and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (-) input terminal after integrating by means of low pass RC combination. Whenever input at the (-) input terminal just exceeds V_{ref} switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R. The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and

R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$ reference voltage. When the voltage at the (-) input terminal becomes just greater than this reference voltage,the output is driven to $-V_{sat}$. At this instant,the voltage on the capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is charges towards $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $-V_{sat}$. The cycle repeats itself.

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. Here the voltage across the capacitor is given by $V_c(t) = V_{sat} - V_{sat}(1+\beta)e^{-\frac{T}{RC}}$. The time period is given by $T = 2RCln(\frac{1+\beta}{1-\beta})$ (50 duty cycle). The output swings from $+V_{sat}$ to $-V_{sat}$, so, v_0 peak-peak is equal to $2V_{sat}$.

As with the sine wave oscillator, the highest frequency generated by the square wave generator is also set by the slew rate of the op-amp. An attempt to operate the circuit at relatively higher frequencies causes the output to become triangular. A reduced peak to peak output voltage swing can be obtained in the square wave generator by using back-to-back zeners at the output terminal.

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. the circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only an external components connected to the op-amp. The circuit diagram of monostable multi vibrator is a modified form of the astable multivibrator. A diode D_1 clamps the capacitor voltage to 0.7V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_3C_1 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output V_0 is at V_{sat}. The diode D_1 conducts and V_c, the voltage across the capacitor C gets clamped to +0.7V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V i.e., $([\beta V_{sat} + (-V_1)] < 0.7V)$, the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts changing exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until V_c is 0.7V as capacitor C gets

clamped to the voltage.

The pulse width T of the monostable multivibrator is obtained as $T = RCln(\frac{1}{1-\beta})$ where $\beta = \frac{R_2}{(R_1+R_2)}$. For monostable operation, the trigger pulse width T_p should be much less than T_1 pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of the input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

PROCEDURE

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

• If it is found good, Set up the astable multivibrator circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Verified that square wave is generated at the output.

• If it is working as an astable multivibrator,the diode and the triggering circuits are connected to make it a monostable multivibrator.

• Then a gating pulse is applied and the output is verified by checking whether the pulse width is constant while varying the trigger frequency.

ASTABLE MULTIVIBRATOR

Circuit Diagram I

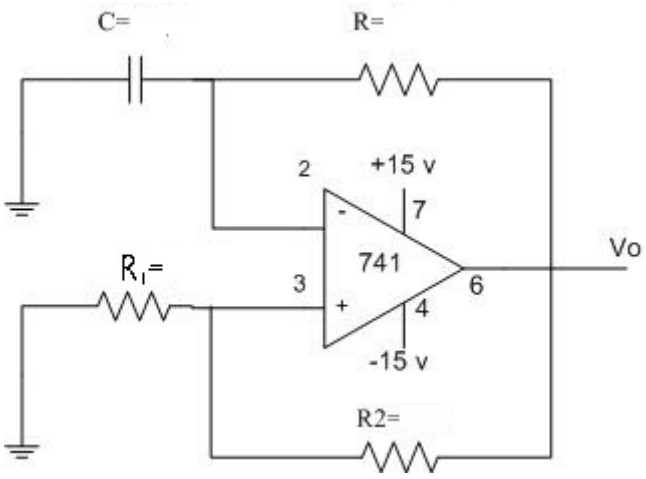


Figure 5.1: ASTABLE MULTIVIBRATOR(FOR 50% DUTY CYCLE)

DESIGN

Select β=0.5

$\beta = \frac{R_1}{R_1+R_2}$=0.5

Choose $R_1 = R_2 =$1 K std

Select frequency, f=1 kHz

T=1 ms

Time period is given by, T=$2RC\ln(\frac{1+\beta}{1-\beta}) = 2RC\ln 3$

Choose C=0.1μF

R=$\frac{T}{2C\ln 3}$=4.7 K std.

SAMPLE GRAPH

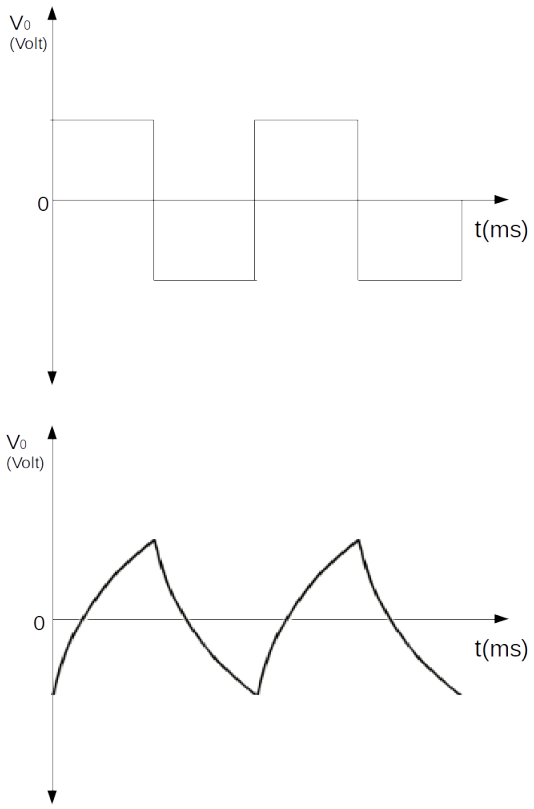


Figure 5.2: ASTABLE MULTIVIBRATOR OUTPUT FOR 50 % DUTY CYCLE

Circuit Diagram II

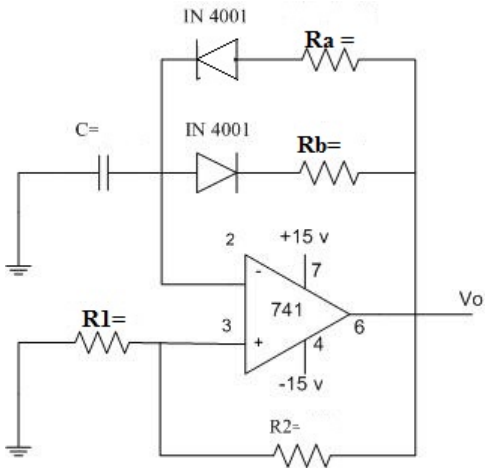


Figure 5.3: ASTABLE MULTIVIBRATOR(FOR 2/3 DUTY CYCLE)

DESIGN

Select β=0.5

$\beta = \frac{R_1}{R_1+R_2}$=0.5

Choose $R_1 = R_2$ =1 K std

Select frequency, f=1 kHz

Duty cycle=10%

So, T_a (+ve half cycle)=0.1 ms

T_b (-ve half cycle)=0.9 ms

$T_a = R_a C \ln(\frac{1+\beta}{1-\beta}) = R_a C \ln 3$

Choose C=0.1μF

R_a=$\frac{T_a}{C \ln 3}$=1 K std.

$T_b = R_b C \ln(\frac{1+\beta}{1-\beta}) = R_b C \ln 3$

R_a=$\frac{T_a}{C \ln 3}$=8.2 K std.

SAMPLE GRAPH

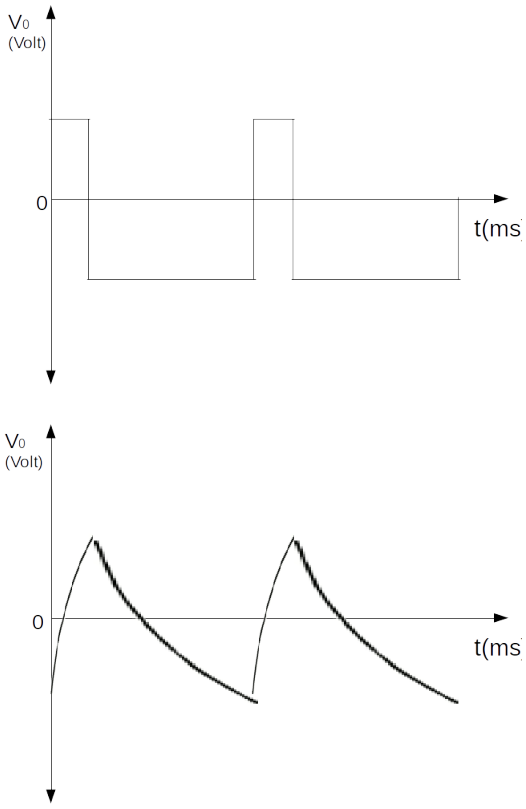


Figure 5.4: 10 % DUTY CYCLE

Circuit Diagram III

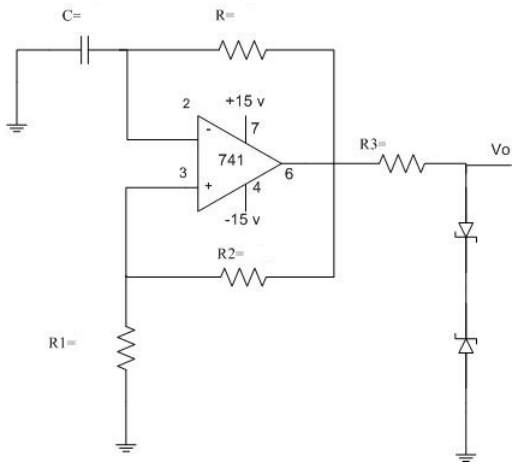


Figure 5.5: ASTABLE MULTIVIBRATOR (FOR AN AMPLITUDE 6 V)

DESIGN

Given V_{opeak}=6 v

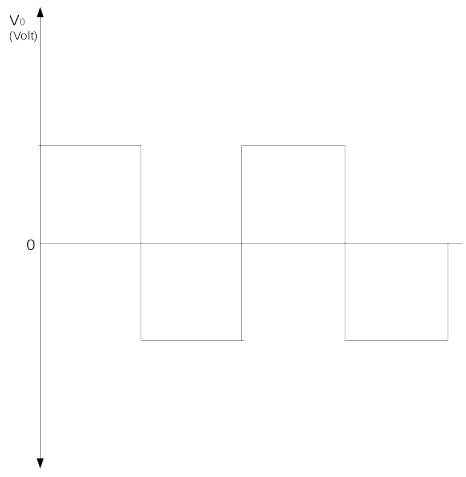
So choose V_2=5.6 V

V_{sat}=13 v

$R_3 = \frac{V_{sat} - V_o}{I_z}$

Choose I_z=1 mA, R_3=1.5 K std.

SAMPLE GRAPH



MONOSTABLE MULTIVIBRATOR

CIRCUIT DIAGRAM

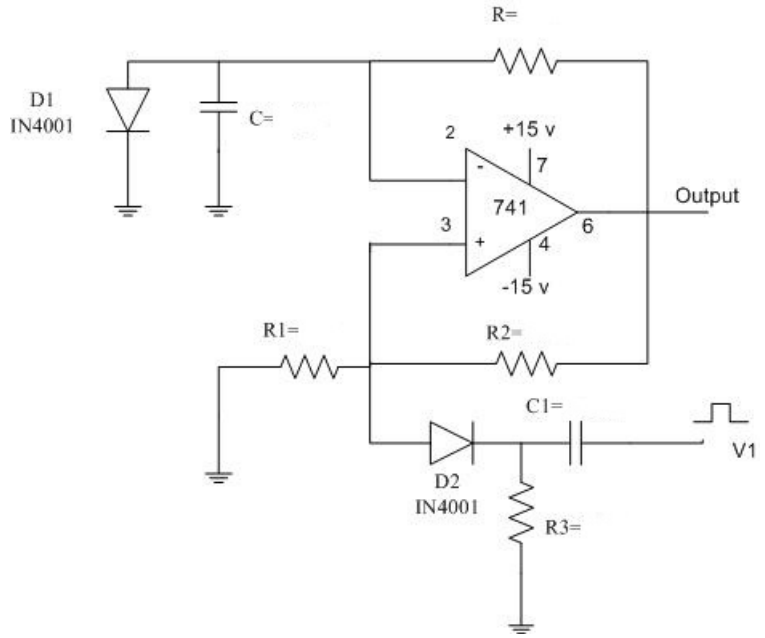


Figure 5.6: Monostable Multivibrator

DESIGN

Trigger pulse width, T=1ms

T=RCln($\frac{1}{1-\beta}$)

Choose $\beta = \frac{R_1}{R_1+R_2}$=0.5

$R_1 = R_2$=10 KΩstd

Select C=0.1μF std

Therefore R=15 K std

To design differentiator, RC $\leq$0.0016T

RC=0.0016T

Choose T=5 ms, Select C_1=0.01μF std

$R_3 \frac{0.0016T}{C_1}$=8.2K std.

SAMPLE GRAPH

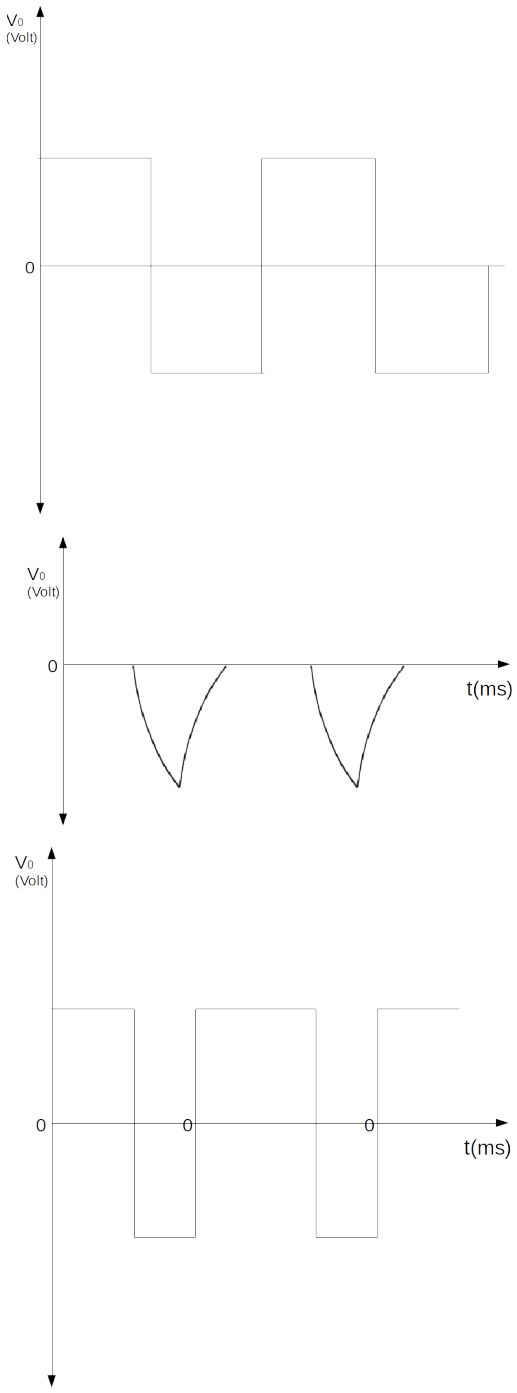


Figure 5.7: Monostable Multivibrator Output

RESULT

1. Designed and set up an astable multivibrator using IC 741 for a frequency of 1 kHz with duty cycle 50% and 10%.

2. Designed and set up monostable multivibrator using IC 741.
   Pulse width, T=

EXPERIMENT NO: 6

TRIANGULAR WAVE AND SAWTOOTH WAVE GENERATORS USING 741 IC

AIM

1. To design and set up a triangular wave generator using IC 741.

2. To design and set up a Sawtooth wave generator using IC 741.

THEORY

Triangular wave generator is the circuit which generates triangular output waveform. The output waveform of the integrator is triangular if its input is a square wave. This means that a triangular wave generator can be formed by simply connecting an integrator to the square wave generator. The circuit requires a dual op-amp, two capacitors, and at least five resistors. The frequencies of the square wave and triangular wave are the same. For fixed $R_1, R_2 and C$ values, the frequency of the square wave as well as triangular wave depends on the resistance R. As R is increased or decreased, the frequency of the triangular wave will decrease or increase respectively. Although the amplitude of the square wave is constant ($\pm V_{sat}$), the amplitude of the triangular wave decreases with an increase in its frequency and vice-versa.

A practical triangular wave generator which requires fewer components consists of a comparator A_1 compares the voltage at non inverting input that is at 0V. When voltage at P goes slightly below or above 0V, the output of A_1 is at -ve or +ve saturation level, respectively.

To illustrate the circuit's operation, let us set the output of A_1 at +ve saturation $+V_{sat}$. This $+V_{sat}$ is an input of the integrator A_2. The output of A_2, therefore, will be a negative going ramp. Thus one end of the voltage divider $R_2 - R_3$ is the positive saturation voltage $+V_{sat}$ of A_1 and the other is negative going ramp attains a certain value $-V_{ramp}$, point P is slightly below 0V; hence the output of A_1 will switch from positive saturation to negative saturation $-V_{sat}$. This means that the output of A_2 will now stop going negatively and will begin to go positively. The output of A_2 will continue to increase until it reaches $+V_{ramp}$. At this time the point P is slightly above 0V, therefore, the output of A, is switched back to the positive saturation level $+V_{sat}$. The sequence then repeats.

The desired output voltage amplitude can be obtained by using appropriate zeners at the output of A_1. The frequency of oscillation is $f_0 = \frac{R_3}{4R_1C_1R_2}$.

PROCEDURE

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

• If it is found good, Set up the circuit as per the given circuit diagram

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• Observe the output in oscilloscope.

CIRCUIT DIAGRAM

Circuit Diagram I

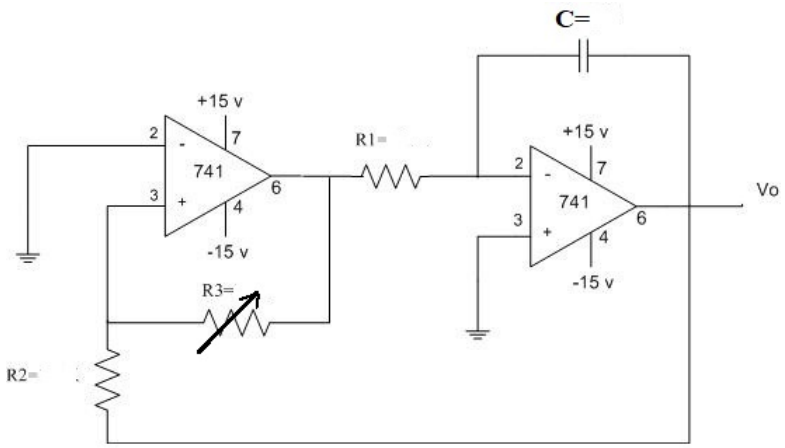


Figure 6.1: Triangular Wave Generator

DESIGN

$T = \frac{4R_1C_1R_2}{R_3}$ $V_{ramp} = \frac{R_2}{R_3}V_{out}$

Choose V_{out} =13.5 V , V_{ramp}=10V

$\frac{R_2}{R_3} = \frac{10}{13.5}$

Assume T=1ms , Select R_2=1.8K std, C_1=0.1μF

R_3=2.2 K std.

$R_1 = \frac{TR_3}{4C_1R_2}$=3.3 Kstd.

Circuit Diagram II

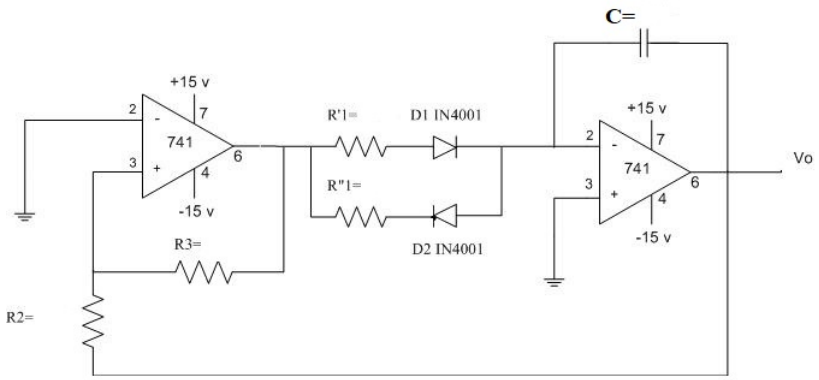


Figure 6.2: Sawtooth Wave Generator

DESIGN

Choose $T_1 = \frac{2R_1'C_1R_2}{R_3}$=0.9ms, $T_2 = \frac{2R"_1C_1R_2}{R_3}$=0.1 ms

Select R_2=1.8K std, C_1=0.1μF

R_3=2.2 K std.

R_1'=5.6 Kstd.

$R"_1$=680 Ωstd.

SAMPLE GRAPH

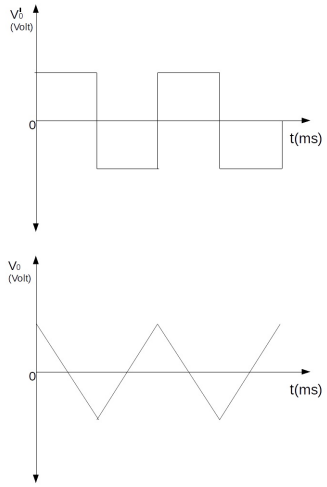


Figure 6.3: Triangular Wave Generator Output

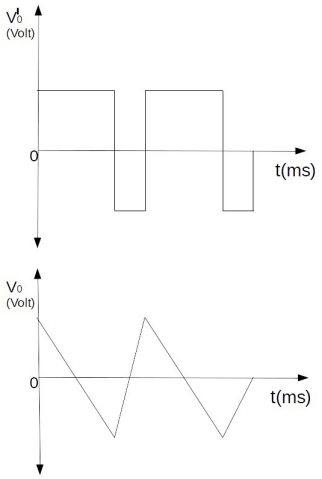


Figure 6.4: Sawtooth Wave Generator Output

RESULT

1. Designed and set up a triangular wave generator using IC 741.

   Time Period, T = ...ms

2. Designed and set up a Sawtooth wave generator using IC 741.

   T_1=.....ms

   T_2=.....ms

   T =.....ms

EXPERIMENT NO: 7

RC PHASE SHIFT OSCILLATOR USING 741 IC

AIM

To design and set up an RC phase shift oscillator with an oscillating frequency of 1 kHz using IC 741.

THEORY

RC phase shift oscillator is an RC oscillator used to produce frequencies verifying from a few Hertz to several hundred kHz. In the RC phase shift oscillator circuit the op-amp is used in inverting mode and therefore it provides a phase shift of 180^0. The additional phase shift of 180^0 is provided by the RC feedback network consists of three identical RC stages. Each of the RC stages provides a 60^0 phase shift so that the total phase shift due to the feedback network is 180^0. It is not necessary that all the three RC sections are identical so long the total phase shift is 180^0. However if we use non-identical stages, it is possible that the total phase shift is 180^0 for more than one frequency. This phenomenon can lead to undesirable inter-modal oscillations.

The feedback factor β of RC network is $\frac{1}{29}$. The frequency of oscillation, f_0 is given by $f_0 = 1/(2\pi RC\sqrt{6})$.

Since $|A\beta| = 1$, for sustained oscillations $|A| = 29$. That is the gain of inverting op-amp should be atleast 29 or $R_2 = 29R_1$. For low frequencies, op-amp IC 741 is used.

PROCEDURE

• IC is firmly fixed on the breadboard.

• The positive and negative power supplies are connected to the respective pins i.e.,+15V is applied to the pin 7 and -15V is connected to the pin 4.

• Then the pin 6 is shorted to pin 2 and a test signal of 1V peak and 1kHz is applied at the pin 3 from a function generator.

• Ensured that the IC is good by checking whether it is working as a voltage follower.

• It is found good, RC phase shift oscillator circuit is set up as shown in the circuit diagram.

• Provide +15V and -15V supply is given to the 7th and 4th pins of the Op-Amp IC respectively.

• By varying the potentiometer the gain is made to 29 in order to produce sustained oscillations.

• Observe the output in oscilloscope.

• The output is observed in a CRO. The frequency of oscillation is calculated by the formula $f = \frac{1}{T}$.

CIRCUIT DIAGRAM

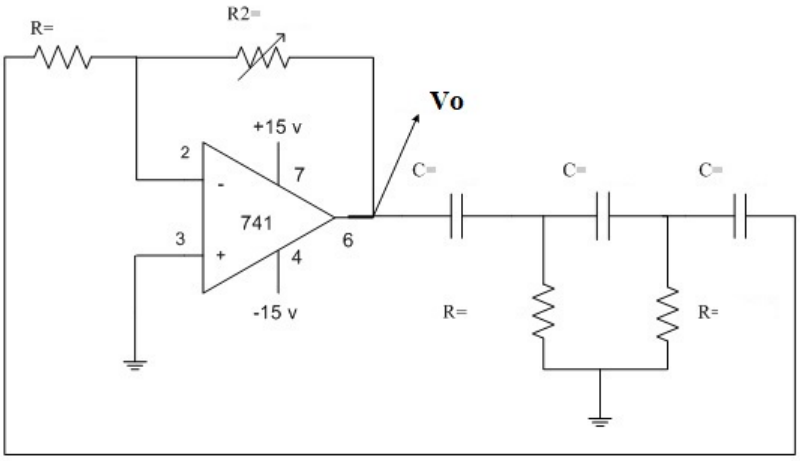


Figure 7.1: RC Phase Shift Oscillator

DESIGN

Select oscillating frequency, f=1 kHz.

f=$\frac{1}{2\pi RC\sqrt{6}}$, choose C=0.1 μ F

R=680 Ω std.

Expected frequency, f=$\frac{1}{2\pi RC\sqrt{6}}$=955.51 Hz.

We have, Voltage gain, A_v=29

$A_v = \frac{R_2}{R_1}$=29

Choose $R_1 = 680\Omega$ std.

$R_2 = 19.72K$, Use 100 K pot.

SAMPLE GRAPH

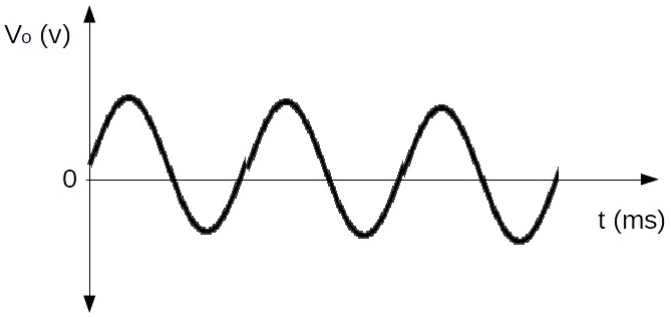


Figure 7.2: RC Phase Shift Oscillator Output

RESULT

Designed and set up a RC phase shift oscillator using IC 741.

Oscillating Frequency, f=

Output Voltage, $V_{pp} =$

INFERENCE

Expected value of oscillating frequency, f=955 Hz. Deviation in the expected value may be due to the variation in resistor or capacitor values or both.

EXPERIMENT NO: 8

ASTABLE AND MONOSTABLE MULTIVIBRATORS USING 555 TIMER IC

AIM

1. To design and set up an astable multivibrator using 555 Timer IC for a
   a) Duty cycle of 75% and a time period of 2*ms* with amplitude of 6V.
   b) Duty cycle of 50% and a time period of 2*ms* with amplitude of 9V.
   c) Duty cycle of 20% and a time period of 2*ms* with amplitude of 7.5V.
2. To design and set up a monostable multivibrator using 555 Timer IC to produce a pulse of width 4*ms* and amplitude 6V.

THEORY

555 Timer IC

IC 555 is a popular monolithic timer IC which can be used for timing applications

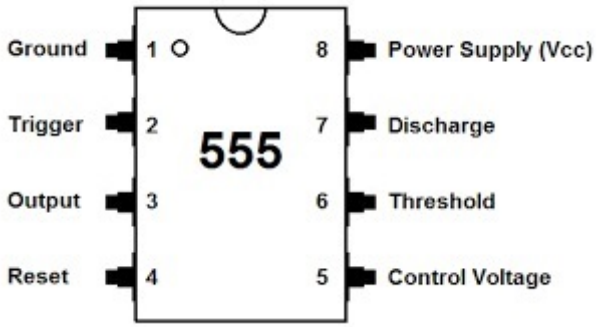


Figure 8.1: Pinout of 555 Timer IC

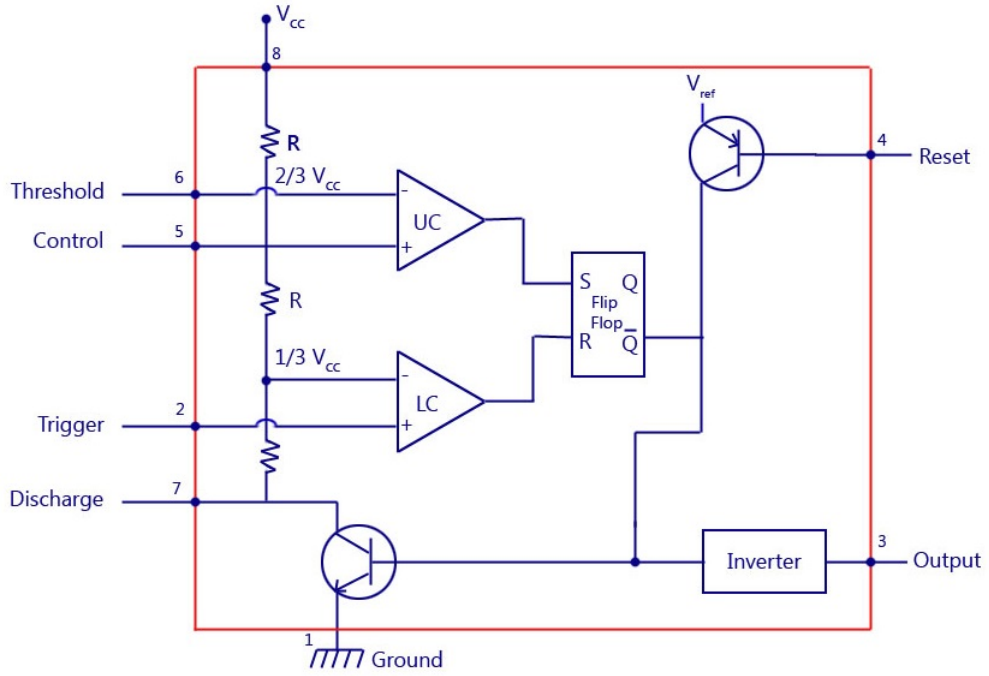


Figure 8.2: Internal Block Diagram of 555 Timer IC

The basic blocks of the 555 timer are

- A trio of identical resistors (5KΩ)
- A pair of Voltage Comparators
- An RS flip-flop and
- A BJT Switch

The resistances set the comparator thresholds at $V_{TH} = \frac{2}{3}V_{CC}$ and $V_{TL} = \frac{1}{3}V_{CC}$. The upper threshold node is also externally accessible via pin 5(control) so that the user can modulate the value of V_{TH}. The non-inverting input of Comparator 1 UC is connected to the threshold pin(pin 6) and the inverting i/p of Comparator 2 LC is connected to trigger pin(pin 2). The outputs of the comparators goes to an RS Flip-flop whose o/p is connected to the output pin(pin 3). The state of the flip-flop is controlled by the comparators:

- Whenever the voltage at the trigger input drops below V_{TL}, LC fires and sets the flip-flop, forcing Q high and $\overline{Q}$ low; With a low voltage at its base, transistor Q_O is in cutoff.

- Whenever the voltage at the threshold input rises above V_{TH}, UC fires and clears the flip-flop, forcing Q low and $\overline{Q}$ high. With a high voltage applied to its base via the 100Ω resistance, Q_O is now ON

The 555 IC is available in both bipolar and CMOS versions.

Astable Mutivibrator Using 555 Timer IC

An astable multivibrator often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running. However,the time during which the output is either high or low is determined by two resistors and a capacitor, which are externally connected to the timer. Initially, when the output is high, capacitor C starts charging towards V_{cc} through R_A and R_B. However, as soon as voltage across the capacitor equals $\frac{2}{3}V_{cc}$, comparator triggers the flipflop and output switches low. Now capacitor C start discharging through $R_(B)$ and transistor Q_0 when the voltage across C equals $\frac{1}{3}V_{cc}$, comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$ respectively. The frequency of oscillation is given by $f_O = \frac{1.45}{(R_A+2R_B)C}$ and the duty cycle is $\frac{R_A+R_B}{R_A+2R_B}(100)\%$.

Astable multivibrator is used in square wave oscillator and free running ramp generators.

Monostable Mutivibrator Using 555 Timer IC

A monostable multivibrator, often called a one-shot multivibrator, is a pulse generating circuit in which the duration of the pulse is determined by a RC network connected externally to the 555 timer. In a stable or stand by state, the output of the circuit is approximately zero or at logic low level. When the external trigger pulse is applied,the output is forced to go high (V_cc). The time the output remains high is determined by the external RC network connected to the timer. At the end of timing interval, the output automatically reverts back to its logic low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low) hence the name monostable. Normally, the output of the monostable multivibrator is low.

The time during which the output remains high is given by $T = 1.1R_AC$.

PROCEDURE

Astable Mutivibrator Using 555 Timer IC

- Set up the circuit and give Power supply
- Observe the output waveform V_O and the capacitor waveform v_C simultaneously on the CRO
- Note the on and off times and compute the duty cycle of the output waveform.

• Repeat the same for various duty cycle.

Monostable Mutivibrator Using 555 Timer IC

• Set up the circuit and give Power supply

• At the trigger input give a square wave of 2ms from a function generator.

• Observe the trigger waveform V_t, the output waveform V_O and the capacitor waveform v_C simultaneously on the CRO

• Measure the time period T of the output pulse.

CIRCUIT DIAGRAM

Astable Mutivibrator Circuit using 555 for 75% Duty Cycle

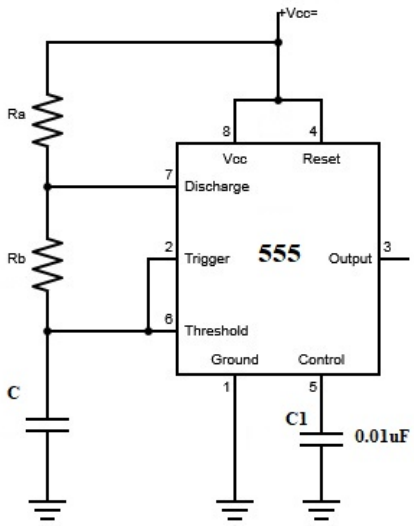


Figure 8.3: Astable multivibrator for duty cycle 75%

Design for 75% Duty Cycle

To design Astable Mutivibrator Circuit for a Duty cycle of 75% and a time period of $2ms$ with amplitude of 6V.

Given $V_{out} = 6V$. Hence $V_{CC} = 6V$

Given Time period, T = $2ms$ and Duty Cycle = 75%

Then, $T_H = 1.5ms$ and $T_L = 0.5ms$

$T_H = 0.693(R_A + R_B)C$

$T_L = 0.693R_BC$

Select $C = 0.1\mu F std$ then $R_B =$ ..... $\approx$ ..... std

$R_A =$ ..... $\approx$ ..... std

Astable Mutivibrator Circuit using 555 for 50% and 20% Duty Cycle

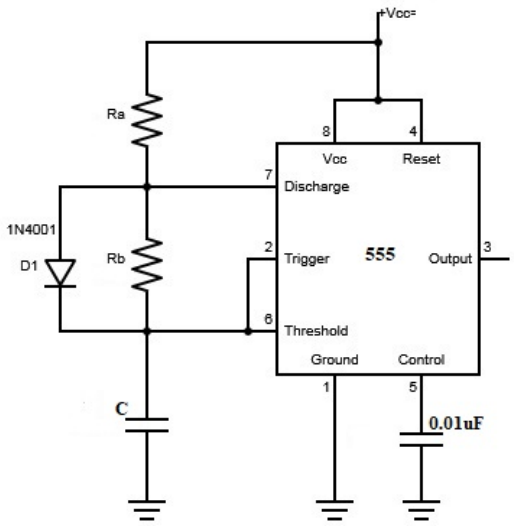


Figure 8.4: Astable multivibrator for duty cycle 50% and 20%

Design for 50% Duty Cycle

To design Astable Mutivibrator Circuit for a Duty cycle of 50% and a time period of 2ms with amplitude of 9V.

Given $V_{out} = 9V$. Hence $V_{CC} = 9V$

Given Time period, T = 2ms and Duty Cycle = 50%

Then, $T_H = 1ms$ and $T_L = 1ms$

$T_H = 0.693 R_A C$

$T_L = 0.693 R_B C$

Select $C = 0.1\mu F std$ then $R_A =$ ..... $\approx$ ..... std

$R_B =$ ..... $\approx$ ..... std

Design for 20% Duty Cycle

To design Astable Mutivibrator Circuit for a Duty cycle of 20% and a time period of 2ms with amplitude of 7.5V.

Given $V_{out} = 7.5V$. Hence $V_{CC} = 7.5V$

Given Time period, T = $2ms$ and Duty Cycle = 20%

Then, $T_H = 0.4ms$ and $T_L = 1.6ms$

$T_H = 0.693R_AC$

$T_L = 0.693R_BC$

Select $C = 0.1\mu Fstd$ then $R_A =$ ..... $\approx$ ..... std and $R_B =$ ..... $\approx$ ..... std

Monostable Mutivibrator Circuit using 555

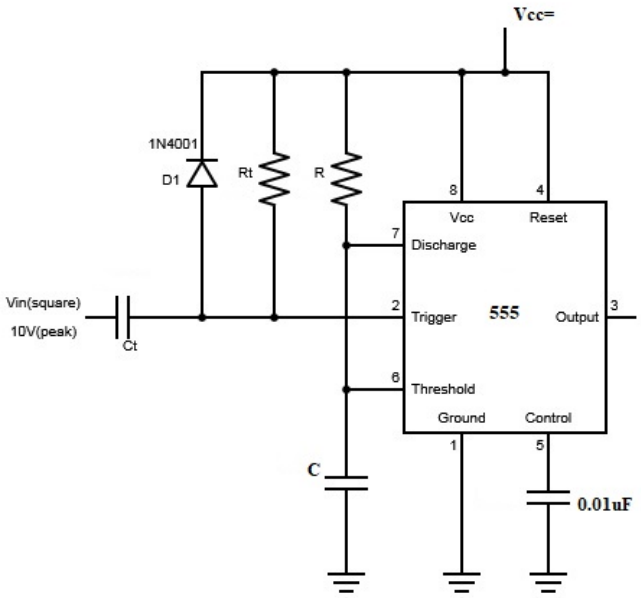


Figure 8.5: Monostable multivibrator

Design of Monostable Mutivibrator

To design a monostable multivibrator for a pulse of width $4ms$ and amplitude 6V.

Given $V_{out} = 6V$. Hence $V_{CC} = 6V$

Given Pulse Width T = $4ms$

$T = 1.1RC$

Choose $C = 0.1\mu Fstd$, then $R =$ ..... $\approx$ ..... std

Choose Trigger Timeperiod $T_T = 8ms$

$R_TC_T << 0.0016T_T$

Select $C_T = 0.01\mu Fstd$, then $R_T =$ ..... $\approx$ ..... std

SAMPLE GRAPH

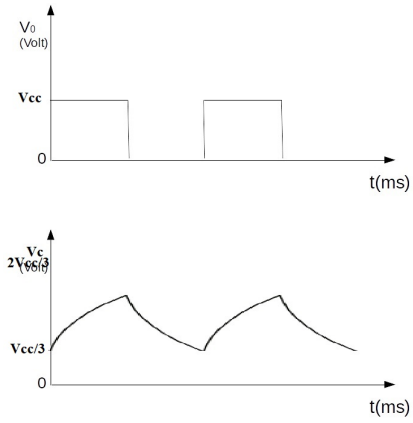


Figure 8.6: Astable Multivibrator output for 75% Duty Cycle

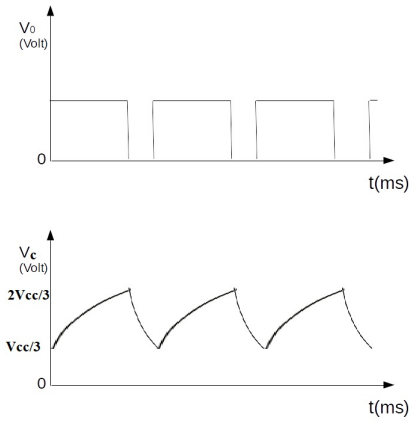


Figure 8.7: Astable Multivibrator output for 50% Duty Cycle

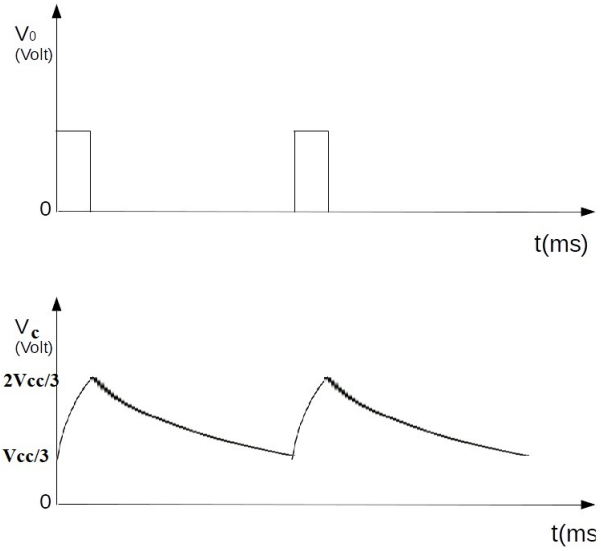


Figure 8.8: Astable Multivibrator output for 20% Duty Cycle

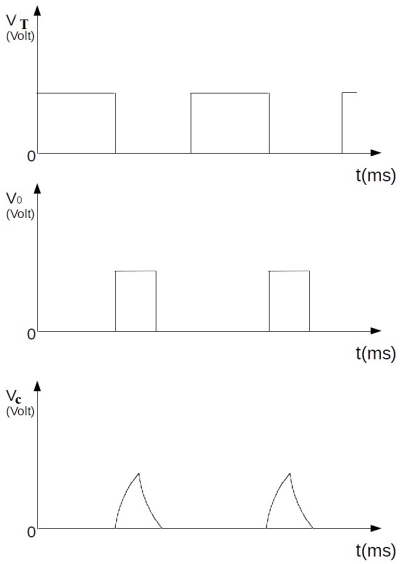


Figure 8.9: Monostable Multivibrator output

RESULT

1. Designed and set up Astable multivibrator for various duty cycle using 555 Timer IC.

   a) For 75% duty cycle, $T_H =$ ....., $T_L =$ ....., $V_O =$ .....

   b) For 50% duty cycle, $T_H =$ ....., $T_L =$ ....., $V_O =$ .....

   c) For 20% duty cycle, $T_H =$ ....., $T_L =$ ....., $V_O =$ .....

2. Designed and set up a monostable multivibrator using 555 Timer IC.

   Observed Pulse width T=.....

Part II

INSTRUMENTATION LAB EXPERIMENTS