An FPGA Implementation of Multi-channel Video Processing and 4K Real-Time Display System

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Abstract—**An Field-Programmable Gate Array (FPGA) implementation to merge and process the Multi-channel independent videos and reconstruct 4K real-time display system is presented. The video system is capable to receive multi-channel Full High Definition (FHD) (1920 x 1080 pixels) videos, to process each video channel and to reconstruct and display the merged video up to 4K (3840 x 2160 pixels) Ultra High Definition (UHD) format. To guarantee the high efficiency and less delay, we adopt the parallel processing design and 'hardware' based structure. The multi-channel independent video can be processed at the same time to ensure real-time display and each channel video could be displayed stably in 4K format. Additionally, Xilinx spartan-6 FPGA module works as the core hardware to control the input, video reconstruction and output processes. High-speed memory chips double data rate type three synchronous dynamic random-access memory (DDR3-SDRAM) and high-frequency Printed Circuit Board (PCB) with ten layers layout are used to ensure the efficient cache of video data and integrity of video signals. This FPGA based real-time UHD implementation can be used not only for modern surgical, patient monitoring, diagnostics, but also for office meeting, video surveillance and so on.**

Keywords- FPGA; multi-channel video; UHD video; real-time video

I. INTRODUCTION

Video is becoming the mainstream information carrier. Camera, tablet computer and even mobile phones can produce the video information [1]-[3]. All the different source videos require too many displays, and it's difficult to analyze all channels' video data at the same time. The implementation is aimed to settle the multi-channel video data real-time processing difficulties. Moreover, with the continuous development of hardware and video processing ability, the quantity of 4K (3840x2160) resolution screen is increasing in daily life. To maximize the efficiency of the 4K screen, multi-channel video processing is demand in some specific application scenarios, such as modern surgical, patient monitoring and diagnostics in modern medicine [4]-[7].

Most of the current multi-channel display devices are Personal Computer (PC) software-based design, but when it comes to process the ever-increasing massive data, high frame rate and high video resolution multi-source scenes those devices become powerless [8]-[10]. Therefore, FPGA-based hardware design with multi-thread and real-time processing capabilities can be a great solution to these problems and the video time delay problem [11]. Parallel video processing design is much more suitable for high speed and multi-task applications.

Nowadays, many researchers focus on the video processing with FPGA. The character of flexibility, high efficiency and low power consumption make the FPGA much more popular. Weiguo Zhou and Yunhui Liu [12] post a method to processing the camera video with image mosaic algorithm based on FPGA. Peng Sun [13] presented a video fusion with Central Processing Unit (CPU) + FPGA architecture, which can efficiently accelerate the process speed. Luis Araneda and Miguel Figueroa [14] presented a hardware architecture for digital video stabilization based on FPGA.

However, the works mentioned above are for limited video channel with low resolution. To processing FHD or UHD videos, a new architecture should be designed. FPGA based design can efficiently reach the demand of real-time processing, low power consumption and stable performance. To meet the requirement of real-time video processing, the proposed design is implemented through hardware architecture. The architecture includes FPGA core processor, SiI9616 video processor, Advanced RISC Machines (ARM) coprocessor and DDR3 memory. SiI9616 video processor can decode, encode and enhance lots of video formats based on the hardware core. FPGA can implement the parallelism video processing algorithm and drive the DDR3 storage through hardware architecture. ARM coprocessor control the whole system by analyzing the system states. Obviously, the 4K resolution can be handled by the implementation.

The video processing contains lots of parts. From the very beginning, some basic processing based on FPGA hardware architecture needed to be settle, such as video scaling, Gamma conversion, on-screen display (OSD) and so on. All these previous works based on FPGA architecture with the capacity to process real-time FHD videos sequences at more than 60 frames per-second (60fps), which is contributed to the multi-channel video merge implementation. To satisfy the demand of 4K real-time video processing, the speed of DDR3 storage also is the key of the implementation. Therefore, we have used Verilog code construct the DDR3 driver and efficiently control the video storage process. Based on the memory process, all

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the arithmetic can be implemented by the hardware description language Verilog. These previous works are focus on one channel video processing. However, the expectation is to process multi-channel videos at same time and display the merged real-time video, which implementation need reconsider the video management and DDR3 SDRAM storage strategy. Four to nine channel videos will be considered into the design, which data quantity is much bigger than the previous work. All the channels' balanced, different channel data switch, timing design and the stability of display are needed to be considered seriously. With the help of the previous research work, the brand new hardware architecture was reconstructed for the high-performance multi-channel video processing.

The rest paper is organized as follow: Section II presents an over view of implementation architecture, Section III will demonstrate the implementation result and Section IV concludes the work.

II. PROPOSED ARCHITECTURE

To process higher resolution videos, it is necessary to redesign a higher performance hardware board system. As shown in Fig. 1, the proposed implementation is suitable for nine paths real-time video data processing. To processing multi-channel videos, previous designed video processing boards also can seamless merged two High Definition (HD) video channels, and send the merged videos to new designed higher performance hardware system. The new designed system is powerful enough to process the higher resolution videos, and construct 4K real-time videos, which is the core of the implementation.

The new video processing board storage data throughput rate is up to 25.6Gbits/s, which is faster enough to the 4K video processing. The core video processor, Xilinx FPGA XC6SLX150, contains about 147K logic cells, which is enough for the video processing. Moreover, the new system supports hardware core based video processing, such as High Definition Multimedia Interface (HDMI) signal decoding and encoding, noise reduction, video smooth and picture enhancement. ARM Cortex A9 can supports a powerful operation system to analyze the video states and manage the whole implementation.

The details about the new board system can be described in two parts: hardware implementation architecture and Hardware Description Language (HDL) implementation architecture.

A. Hardware implementation architecture

The new designed processing board is composed of two channel HDMI video inputs, two channel HDMI video outputs, Xilinx FPGA XC6SLX150 core processor, SiI9616 video processors, ARM 9 Coprocessor, Ethernet ports and DDR3

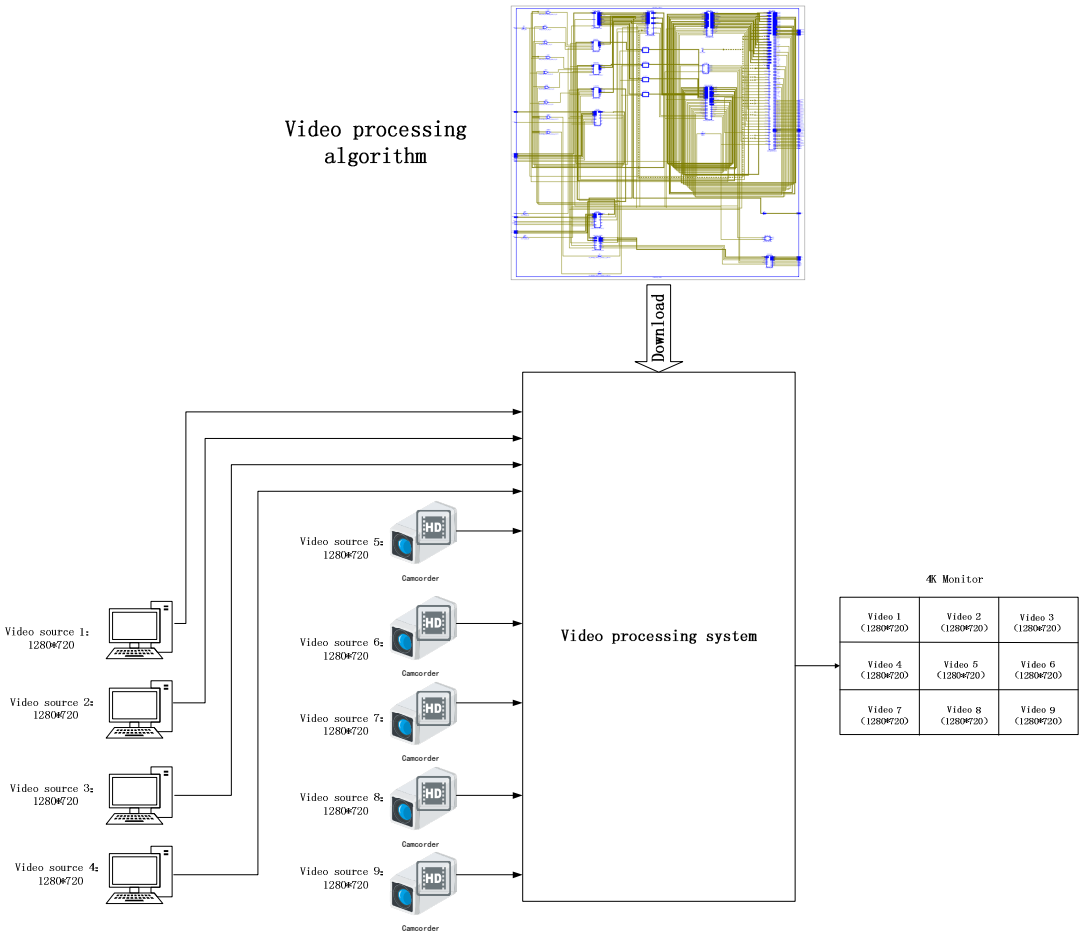


Fig. 1. The function overview of the whole system

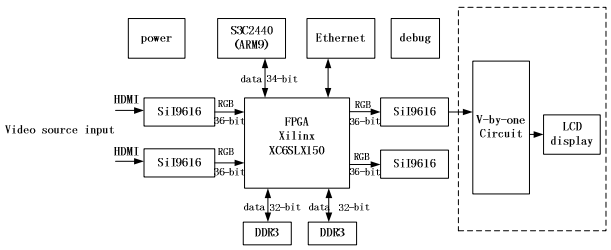


Fig. 2. The processing board architecture

memory. FPGA is the core processor in the whole system, which can drive the DDR3 memory at 25.6Gbits/s and implements the video data processing algorithm. Moreover, ARM 9 is the core controller of the whole system. So, the ARM 9 will configure the SiI9616 and communicate with the FPGA processor. The Ethernet is a useful port, which can communicate with the system and achieve online controlling. The structure of the processing board is shown in Fig. 2.

HDMI video input module can receive a group of differential signals to SiI9616 processor. The HDMI signals have a good anti-interference ability. And the HDMI interface has smaller volume than the traditional DVI digital interface. The HDMI video data is organized in standard format. Therefore, to simplify the FPGA processing works and make sure the HDMI videos can be decoded with low time delay, HDMI format data will be converted to parallel data. The parallel data can be converted to 12-bits true color by the SiI9616 processor. The hard process core can convert the format efficiently.

HDMI video output module is similar to the input module. FPGA video processor directly drive the SiI9616 processor by transmitting 36-bit parallel video output. Due to the requirement that the implementation support 4K resolution videos, the speed of parallel data is about 268MHZ. For a normal 1080p FHD video, the speed is only 148.5MHZ. Therefore, the timing of 4K video should pay more attention. At last, the encoded HDMI 4K resolution video will be transformed to the screen.

Xilinx FPGA XC6SLX150 core processor is the core part in the whole system, which will implement the video processing algorithm, and manage multi-channel video data streams.

SiI9616 video processors feature a digital processing core that performs real-time video format conversion and image improvement. The format is supported from any input format to 4K resolutions. The video processor supports multicolor space conversion, mosquito noise reduction, video smoothing, detail enhancement and so on. All of the process are based on the hard core designed. Therefore, the delay of the videos will be extremely reduced.

ARM 9 Coprocessor is the controller of the whole system. To make the implementation more convenient to control, the image analysis and top-level operating platform should be constructed. The Coprocessor will configure the SiI9616 processor, write video information to FPGA and analysis the key image and FPGA state.

Ethernet ports can be used to receive control commands. So, we can control the multi-channel videos display through Wireless Fidelity (WIFI).

DDR3 memory will be used to store the plenty of video data. In the design, there are 4Gbits space for video data storage. The outside video data is coming into the system in an independent clock. But their speed is much lower than the DDR3 operation speed. Therefore, First Input First Outputs (FIFOs) will be introduced into the system to match the DDR3 operation speed. Also, the DDR3 memory is driven by FPGA core processor.

B. HDL implementation architecture

The video processing algorithm and simulation is conducted on the ISE software. The video data timing and storage strategy need to be carefully designed and simulated. After all the prepare works, the ISE program will generate the bit-stream file. The next step is downloading the file into the board and beginning to debug the system on board. The HDL implementation architecture is shown in Fig. 3. The architecture included seven kinds of modules: input controller and optimizing module, FIFO buffer module, configure module, video processing arithmetic module, DDR3 controller module, DDR3 driver module and output controller module.

The video processing board can receive and transmit 2 channels video data at the same time. For the input channels, the videos are totally independent. Therefore, the timing of the two channel videos are different and the pixel clock are not synchronous. The input controller and optimizing module receive and preprocess the video data, which can enhance the color and image quality and reduce the noises. FIFO is an ideal way to deal with the multi-clock problem, which is part and parcel of multi-channel video processing. Configure module is in charge of convert the control words to the detailed parameters of each modules. DDR3 state control module controls both the videos data write and read processes. The DDR3 driver module is controlled by DDR3 state control module and directly drives the DDR3 IP-core. The output controller module generates 4K frames by state machines. To processing a stable frame, the timing need to carefully construct. Video processing arithmetic module is the core part of the HDL implementation. The detailed flow of which is shown in Fig. 4.

To processing two path videos, the most important task is controlling the timing, which is to decide the imaging processing sequence and storage blocks arrangement. According to the configuration parameters, the computing storage parameters module will calculate the video storage addresses, video read numbers, video write numbers, and frame packaging parameters. The video storage map will be settle down. The time significands of dispatching correspond video can be get from configuration parameters. After dispatched videos, each frame need filtering and noise reducing. Then, the video data will dispatch to the corresponded storage space. The output data controller can generated 4K resolution videos, according to the system state what the configuration parameters described.

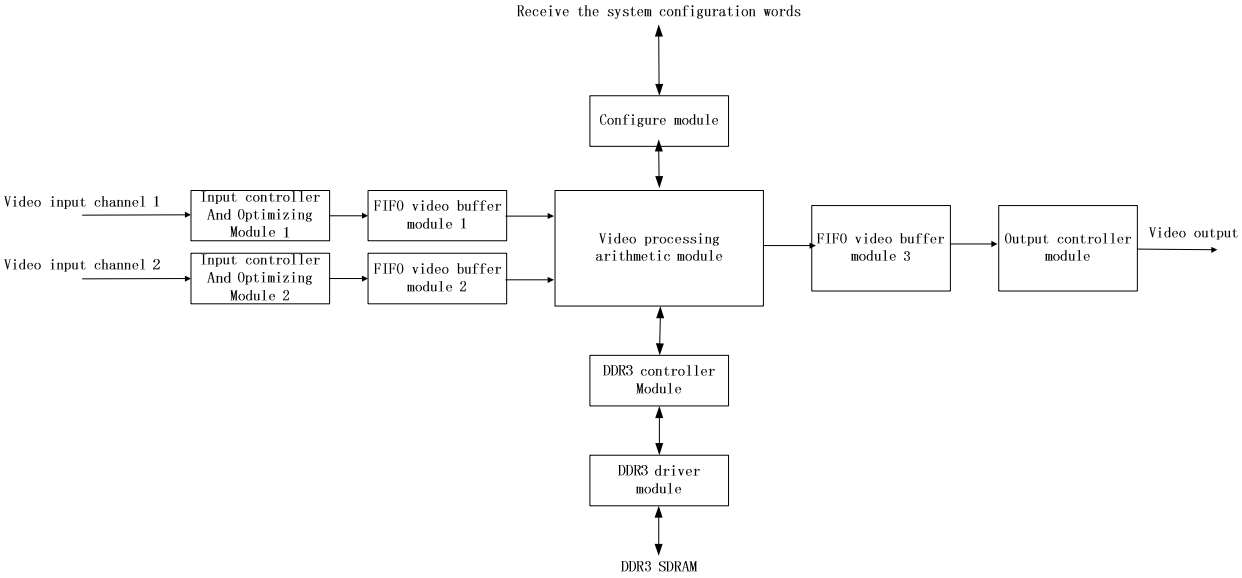


Fig. 3. HDL implementation architecture

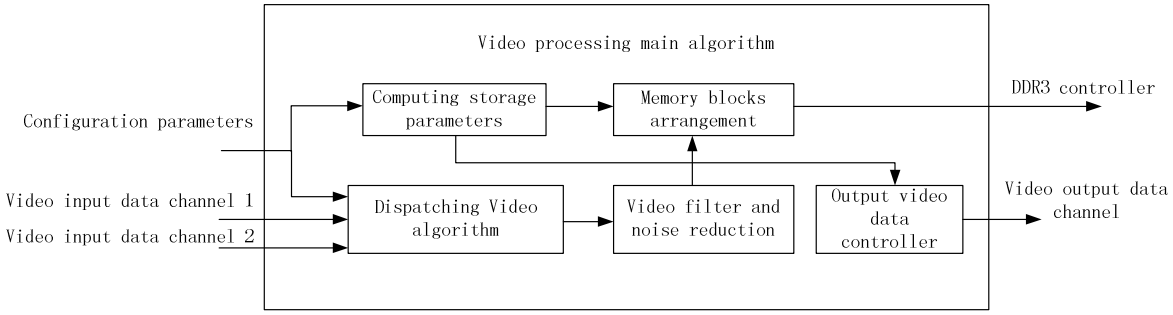


Fig. 4. A block diagram of video processing arithmetic module

III. RESULT

A. Experiment Result

The platform is designed for multi-channel video processing and displaying the 4K real-time videos on the screen. The algorithm can be implemented on the board. The structures of the video processing board is shown in Fig. 5.

The HDL implementation is downloaded into FPGA chip. The SiI9616 processor can decode and encode the video sources and enhance the video qualities. The video processing boards can be used to construct the system. Therefore, the system have the ability to process nine paths videos at the same time and broadcast the real-time result on the 4K resolution screen.

The video processing algorithm is implement by Verilog HDL. After we designed and built the modules, a gate level simulation included DDR3 need to carry out. The simulation of DDR3 and multi-channel video data is shown in Fig. 6.

By using the proposed video processing system architect, we can get the nine path video processing result, which is shown in Fig. 7. Due to the limitation of the video sources, we copied the video sources and Repeated displayed the videos to describe the ability for processing multi-channel videos. The resolution of each input video source is 1280 (H) x 720 (V). The input frame rate can reach 60 frame/sec, which meets the real-time processing and display requirement. Due to the 30 HZ frame rate that the 4K screen can support, the final video frame rate is 30 HZ.

The system also have ability to process higher resolution videos. For 4K resolution screen, we can display four path 1920 (H) x 1080 (V) videos on the screen, which is shown in Fig. 8. The input frame rate can also reach 60 frame/sec, which meets the real-time processing and display requirement.

Using the ARM to control the whole system mode, the system can scale the videos according to the control words. For example, we can zoom the first channel video to 2 times magnification, which is shown in Fig. 9. The video processing is using hardware designed. Therefore, the time delay is extremely low, which is the guarantee of real-time display.

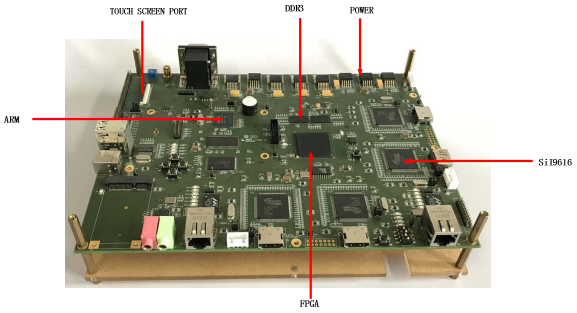


Fig. 5. Designed video processing board

Fig. 6. The simulation of DDR3 and multi-channel video processing

Fig. 7. An example of nine 720p paths videos inputs and real-time display

B. Performance Analysis

Xilinx FPGA XC6SLX150 is acceptable for the 4K real-time video processing. The system is hardware designed. So, the power consumption will be extremely low compared to the PC consumption of hundreds watt. As shown in Fig. 10, the total power consumption of the video processing board is only 1.943w. The on-chip resource utilization is also met by the FPGA. Therefore, much more arithmetic can be implement into the system.

In recent years, many research achievements have shown strongly enthusiasm for video processing with the development of VR/AR technology [15][16]. The traditional ways are using GPU and CPU to generate and process the video data. But for the fast development Virtual Reality/ Augmented Reality

Fig. 8. An example of four paths 1080p videos inputs and real-time display

Fig. 9. An example of 2 times magnification and real-time display

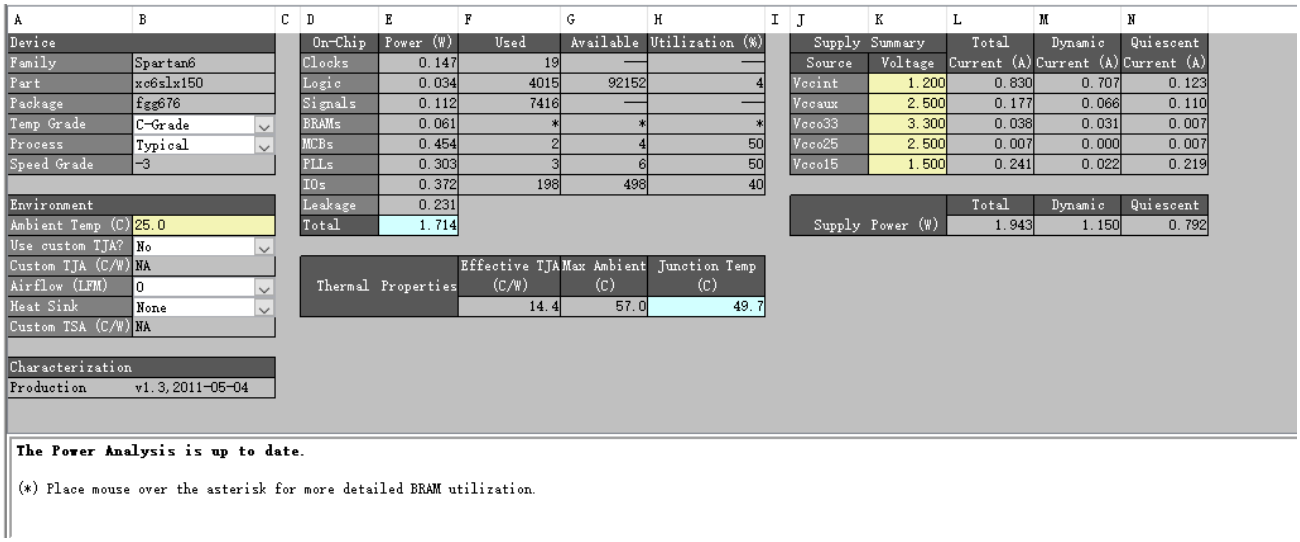
(VR/AR) areas. FPGA is suitable for building a flexible new architect to deal with the multi-channel videos and adjustable applications [17].

Multi-channel video processing and real-time 4K display are the key technology for the future display technology. There are lots of applications, such as modern surgical, patient monitoring, diagnostics, but also for office meeting, video surveillance and so on.

IV. CONCLUSION

This paper introduced an FPGA implementation to merge and process the multi-channel independent videos and reconstruct 4K real-time video. This system have ability to process full-HD (1920x1080 pixels) videos and display the costumed result on 4K UHD (3840 x 2160 pixels) screen. Specifically, it's able to process the input video frame rate at 60fps meeting the demand of real-time requirement. The hardware architecture with HDL implementation can efficiently reduce the video delay and power consumption and improve the video system robustness.

Compared to the traditional CPU + Graphics Processing Unit (GPU) architecture, the FPGA solution can deal with the fast changing of video processing development by costuming the processing structure and improve the performance of multi-channel videos processing and real-time display with lower cost. The implementation can be applied to VR/AR video processing, modern surgical, patient monitoring, diagnostics, office meeting, and video surveillance.



Device	
Family	Spartan6
Part	xc6slx150
Package	fgg676
Temp Grade	C-Grade
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Characterization	
Production	v1.3, 2011-05-04

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.147	19	—	—
Logic	0.034	4015	92152	4
Signals	0.112	7416	—	—
BRAMs	0.061	*	*	*
MCBs	0.454	2	4	50
PLLs	0.303	3	6	50
IOs	0.372	198	498	40
Leakage	0.231			
Total	1.714			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	14.4	57.0	49.7

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.830	0.707	0.123
Vccaux	2.500	0.177	0.066	0.110
Vcco33	3.300	0.038	0.031	0.007
Vcco25	2.500	0.007	0.000	0.007
Vcco15	1.500	0.241	0.022	0.219

	Total	Dynamic	Quiescent
Supply Power (W)	1.943	1.150	0.792

The Power Analysis is up to date.

(*) Place mouse over the asterisk for more detailed BRAM utilization.

Fig. 10. The utilization and power consumption of the video processing system

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