Microprocessor Unit 2

The 16-bit registers are available with their extended size of 32 bits, by adding the registers with a prefix of
a) X
b) E
c) 32
d) XX
Answer: b

In a 32-bit register, ESP, the lower 16-bits of the register can be represented by
a) LSP
b) FSP
c) SP
d) none of the mentioned
Answer: c

Which of the following is a data segment register of 80386?
a) ES
b) FS
c) GS
d) all of the mentioned
Answer: d

The register width used by the 32-bit addressing modes is
a) 8 bits
b) 16 bits
c) 32 bits
d) all of the mentioned
Answer: d

The flag that is additional in flag register of 80386, compared to that of 80286 is
a) VM flag
b) RF flag
c) VM and RF flag
d) none of the mentioned
Answer: c

The VM (virtual mode) flag is to be set, only when 80386 is in
a) virtual mode
b) protected mode
c) either virtual or protected mode
d) all of the mentioned
Answer: b

In protected mode of 80386, the VM flag is set by using
a) IRET instruction
b) task switch operation
c) IRET instruction or task switch operation
d) none of the mentioned
Answer: c

During the instruction cycle of 80386, any debug fault can be ignored if
a) VM flag is set
b) VM flag is cleared
c) RF is cleared
d) RF is set
Answer: d

The RF is not automatically reset after the execution of
a) IRET
b) POPA
c) IRET and POPF
d) IRET and PUSHF
Answer: c

The segment descriptor register is used to store
a) attributes
b) limit address of segments
c) base address of segments
d) all of the mentioned
Answer: d

The 32-bit control register, that is used to hold global machine status, independent of the executed task is
a) CR0
b) CR2
c) CR3
d) all of the mentioned
Answer: d

The descriptor table that the 80386 supports is
a) GDT (Global descriptor table)
b) IDT (Interrupt descriptor table)
c) LDT (Local descriptor table)
d) TSS (Task state segment descriptor)
e) all of the mentioned
Answer: e

The registers that are together, known as system address registers are
a) GDTR and IDTR
b) IDTR and LDTR
c) TR and GDTR
d) LDTR and TR
Answer: a

Which of the following is a system segment register?
a) GDTR
b) LDTR
c) IDTR
d) none of the mentioned
Answer: b

The test register(s) that is provided by 80386 for page cacheing is
a) test control registers
b) page cache registers
c) test control and test status registers
d) test control and page cache registers
Answer: c

Among eight debug registers, DR0-DR7, the registers that are reserved by Intel are
a) DR0, DR1, DR2
b) DR4, DR5
c) DR1, DR4
d) DR5, DR6, DR7
Answer: b

The registers that are used to store four program controllable break point addresses are
a) DR5-DR7
b) DR0-DR1
c) DR6-DR7
d) DR0-DR3
Answer: d

The register DR6 hold
a) break point status
b) break point control information
c) break point status and break point control information
d) none of the mentioned
Answer: a

The flag bits that indicate the privilege level of current IO operations are
a) virtual mode flag bits
b) IOPL flag bits
c) resume flag bits
d) none of the mentioned
Answer: b

The registers that are not available for programmers are
a) data and address registers
b) instruction pointers
c) segment descriptor registers
d) flag registers
Answer: c

Which of the following is not a newly added instruction of 80386, that are not present in 80286?
a) bit scan instructions
b) bit test instructions
c) shift double instructions
d) none of the mentioned
Answer: d

The BSF (bit scan forward) instruction scans the operand in the order
a) from left to right
b) from right to left

c) from upper nibble
d) none of the mentioned
Answer: b

The BSR (bit scan reverse) instruction scans the operand in the order
a) from left to right
b) from right to left
c) from upper nibble
d) none of the mentioned
Answer: a

If a ‘1’ is encountered when operand is scanned by BSF, then
a) zero flag is reset
b) zero flag is set
c) VM flag is set
d) RF flag is reset
Answer: b

If a ‘1’ is not encountered when operand is scanned by BSR, then
a) zero flag is reset
b) zero flag is set
c) VM flag is reset
d) RF flag is set
Answer: a

Which of the following is not a bit test instruction?
a) BTC
b) BTS
c) BSF
d) BTR
Answer: c

In case of BT instruction, if the bit position in the destination operand specified by the source operand, is ‘1’, then
a) zero flag is reset
b) carry flag is set
c) VM flag is set
d) RF flag is reset
Answer: b

Which of the following is not a conditional set byte instruction?
a) SETNP
b) SETO
c) SETNAE
d) SHRD
Answer: d

The instruction that shifts the specified number of bits in the instruction, from the upper side of the source operand into the lower side of the destination operand is
a) SHRD
b) SHLD
c) SETNS

d) none of the mentioned
Answer: b

The instruction that shifts 8 LSB bits of ECX into the MSB positions of EAX, one by one starting from LSB of ECX is
a) SHLD ECX,EAX,8
b) SHLD EAX,ECX,8
c) SHRD ECX,EAX,8
d) SHRD EAX,ECX,8
Answer: d

The instructions available in the 80386 that are not available in its real address mode is
a) addressing techniques
b) instructions for protected address mode
c) instructions for interrupt handling
d) all of the mentioned
Answer: b

The unit that is disabled in real address mode is
a) central processing unit
b) memory management unit
c) paging unit
d) bus control unit
Answer: c

To form a physical memory address, appropriate segment register contents are
a) shifted by left by 4 positions
b) added to 16-bit offset address
c) operated using one of addressing modes
d) all of the mentioned
Answer: d

The segments in 80386 real mode are
a) overlapped
b) non-overlapped
c) either overlapped or non-overlapped
d) none of the mentioned
Answer: c

The operation that can be performed on segments in 80386 real mode is
a) read
b) write
c) execute
d) all of the mentioned
Answer: d

The selectors contain the segment’s
a) segment limit
b) base address
c) access rights byte
d) all of the mentioned
Answer: d

The linear address is calculated by
a) effective address + segment base address
b) effective address – segment base address
c) effective address + physical address
d) effective address – physical address
Answer: a

If the paging unit is enabled, then it converts linear address into
a) effective address
b) physical address
c) segment base address
d) none of the mentioned
Answer: b

If the paging unit is disabled, then the linear address is used as
a) effective address
b) physical address
c) segment base address
d) none of the mentioned
Answer: b

The paging unit is enabled only in
a) virtual mode
b) addressing mode
c) protected mode
d) none of the mentioned
Answer: c

For a single task in protected mode, the 80386 can address the virtual memory of
a) 32 GB
b) 64 MB
c) 32 TB
d) 64 TB
Answer: d

The bit that indicates whether the segment has been accessed by the CPU or not is
a) base address
b) attribute bit
c) present bit
d) granulary bit
Answer: b

The TYPE field of descriptor is used to find the
a) descriptor type
b) segment type
c) descriptor and segment type
d) none
Answer: c

If the segment descriptor bit, S=0, then the descriptor is

a) data segment descriptor
b) code segment descriptor
c) system descriptor
d) all of the mentioned
Answer: c

The bit that indicates whether the segment is page addressable is
a) base address
b) attribute bit
c) present bit
d) granularity bit
Answer: d

If the Default operation size bit, D=1, the code segment operation size selected is
a) 8-bit
b) 16-bit
c) 32-bit
d) 64-bit
Answer: c

The segment descriptor contains
a) access rights
b) limit
c) base address
d) all of the mentioned
Answer: d

Which of the following is not a type of segment descriptor?
a) system descriptors
b) local descriptors
c) gate descriptors
d) none
Answer: d

The limit field of the descriptor is of
a) 10 bits
b) 8 bits
c) 16 bits
d) 20 bits
Answer: d

The starting address of the segment in physical memory is decided by
a) physical memory
b) segment descriptors
c) operating system
d) base address Answer
Answer: c

The total descriptors that the 80386 can handle is
a) 2K
b) 8K
c) 4K

d) 16K
Answer: d

The advantage of pages in paging is
a) no logical relation with program
b) no need of entire segment of task in physical memory
c) reduction of memory requirement for task
d) all of the mentioned
Answer: d

The size of the pages in paging scheme is
a) variable
b) fixed
c) both variable and fixed
d) none
Answer: b

To convert linear addresses into physical addresses, the mechanism that the paging unit uses is
a) linear conversion mechanism
b) one level table mechanism
c) physical conversion mechanism
d) two level table mechanism
Answer: d

The control register that stores the 32-bit linear address, at which the previous page fault is detected is
a) CR0
b) CR1
c) CR2
d) CR3
Answer: c

Which of the following is not a component of paging unit?
a) page directory
b) page descriptor base register
c) page table
d) page
Answer: b

The control register that is used as page directory physical base address register is
a) CR0
b) CR1
c) CR2
d) CR3
Answer: d

The bits of CR3, that are always zero are
a) higher 4 bits
b) lower 8 bits
c) higher 10 bits

d) lower 12 bits
Answer: d

Each directory entry in page directory is maximum of
a) 2 bytes
b) 4 bytes
c) 8 bytes
d) 16 bytes
Answer: b

The size of each page table is of
a) 2 Kbytes
b) 2 bytes
c) 4 Kbytes
d) 4 bytes
Answer: c

The dirty bit(D) is set, before which operation is carried out
a) write
b) read
c) initialization
d) none of the mentioned
Answer: a

The bit that is undefined for page directory entries is
a) P-bit
b) A-bit
c) D-bit
d) all of the mentioned
Answer: c

The bit that is used for providing protection is
a) User/Supervisor bit
b) Read bit
c) Write bit
d) all of the mentioned
Answer: d

The storage of 32 recently accessed page table entries to optimize the time, is known as
a) page table
b) page descriptor base register
c) page table cache
d) none of the mentioned
Answer: c

The page table cache is also known as
a) page table storage
b) storage buffer
c) translation look aside buffer
d) all of the mentioned
Answer: c