PAPER SOLUTION
WINTER 2023

Subject code : 3110016
Subject Name : Basic Electronics

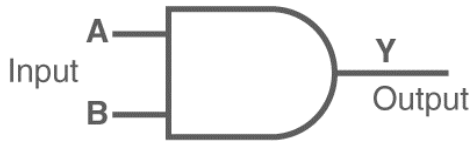
Q-1 (a) Draw symbol and truth table for AND, NOR, EX-OR logic gates.

Ans :

1. AND GATE

→ In the AND gate, the output of an AND gate attains state 1 if and only if all the inputs are in state 1.

→ Symbol



→ The Boolean expression of AND gate is Y = A.B

→ The truth table of a two-input AND basic gate is given as

→ Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. NOR GATE

→ This gate is the combination of OR and NOT gates.

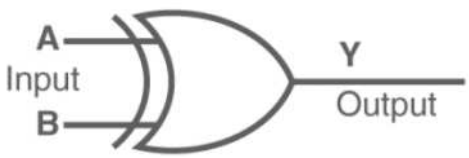
→ The Boolean expression of the NOR gate is $Y = \overline{A + B}$

→ Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

3. EX-OR GATE

→ In an XOR gate, the output of a two-input XOR gate attains state 1 if one adds only input and attains state 1.



→ The Boolean expression of the XOR gate is $A.\bar{B} + \bar{A}.B$ or $Y = A \oplus B$

→ Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b) Discuss forward and reverse bias operation of a P-N junction diode with depletion region.

Ans :

Forward Bias Operation of a P-N Junction Diode

→ Forward biasing a P-N junction diode involves applying a voltage across the diode in such a way that it reduces the potential barrier at the junction, allowing current to flow easily. Here's how it works:

1. **Voltage Application:** A positive voltage (V) is applied to the P-type material, and a negative voltage is applied to the N-type material, relative to the other terminal. This creates an electric field that opposes the potential barrier at the junction.

2. **Reduction of Barrier:** The applied voltage reduces the potential barrier height at the junction, which is the energy barrier that prevents the flow of majority carriers (electrons in the N-type and holes in the P-type) across the junction. As a result, electrons from the N-type material and holes from the P-type material are pushed towards the junction.

3. **Carrier Injection:** As the potential barrier reduces, more electrons from the N-type material and holes from the P-type material are able to cross the junction and enter the depletion region. This movement of charge carriers constitutes an electric current.

4. **Recombination:** Once the electrons and holes cross the junction, they recombine in the depletion region, releasing energy in the form of photons or heat, depending on the material. This recombination allows current to flow through the diode.

5. **Narrowing of Depletion Region:** Under forward bias, the width of the depletion region decreases. This is because the majority carriers (electrons and holes) from both sides are pushed towards the junction, reducing the region depleted of charge carriers.

6. **Conduction:** With the potential barrier reduced and a continuous flow of current, the diode behaves like a closed switch, allowing current to easily flow in the forward direction.

Reverse Bias Operation of a P-N Junction Diode

→ Reverse biasing a P-N junction diode involves applying a voltage across the diode in such a way that it increases the potential barrier at the junction, inhibiting the flow of current. Here's how it works:

1. **Voltage Application:** A negative voltage is applied to the P-type material, and a positive voltage is applied to the N-type material, relative to the other terminal. This creates an electric field that enhances the potential barrier at the junction.

2. **Increase of Barrier:** The applied voltage increases the potential barrier height at the junction, making it more difficult for majority carriers to cross the junction. Electrons in

the N-type material are pushed away from the junction, and holes in the P-type material are pushed away as well.

3. **Widening of Depletion Region:** As majority carriers are pushed away from the junction, the width of the depletion region increases. This widening of the depletion region further inhibits the flow of current through the diode.

4. **Reverse Current:** Despite the increased potential barrier, a small amount of current known as the reverse saturation current or leakage current may still flow. This current is due to minority carriers (minority carriers are electrons in the P-type material and holes in the N-type material) that are thermally generated and cross the junction.

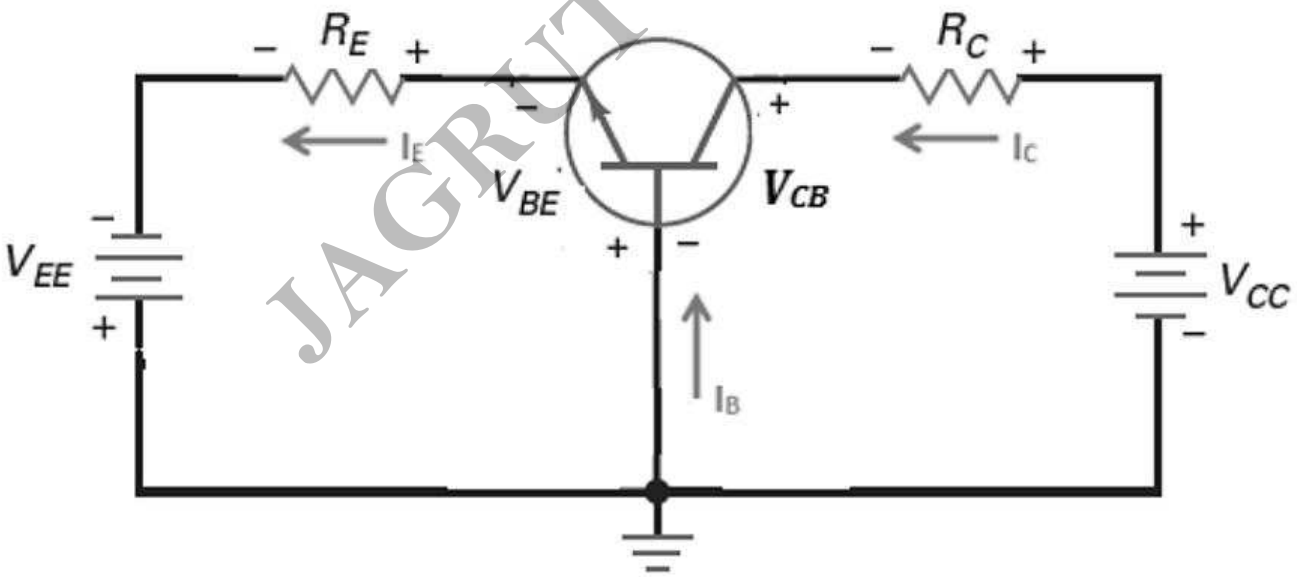
5. **Diode as an Open Switch:** In reverse bias, the diode behaves like an open switch, as the potential barrier prevents significant current flow in the reverse direction.

(c) Draw CB configuration and discuss its input and output characteristics with I_{CBO}, r_i , r_o , and current gain α.

Ans :

→ In common base configuration, emitter is the input terminal, collector is the output terminal, and base is the common terminal between input and output.

→ As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction VEE battery is connected and to reverse bias CB junction VCC battery is connected as shown in figure. Resistance RE and RC are current limiting resistors.



→ Current Gain and different current components in CB configuration:

Current Gain α_{dc} :

→ It is defined as the ration of output current I_C to Input current I_E . it is dented by α_{dc} or α . It is represented by equation

$$\alpha_{dc} = \frac{I_C(inj)}{I_E} = \frac{I_C - I_{CBO}}{I_E} \quad \text{----------(1)}$$

→ In equation (1)

→ I_C(inj) is injected charge carrier into the collector from emitter I_{CBO} is reverse leakage current between collector to base when emitter is open. Which is very small. If we neglect I_{CBO} then α_{dc} is approximated to

$$\alpha_{dc} \cong \frac{I_C}{I_E} \qquad \text{----------(2)}$$

Collector current I_C :

→ From equation (1), collector current can be written as

$$I_C = \alpha_{dc} I_E + I_{CBO} \qquad \text{----------(3)}$$

→ as I_{CBO} is very small, If we neglect I_{CBO} then collector current I_C is approximated to

$$I_C \cong \alpha_{dc} I_E$$

Emitter current I_E:

→ Emitter current is sum of Base current I_B and collector current I_C

$$I_E = I_C + I_B \qquad \text{----------(4)}$$

Base current I_B:

$$I_B = I_E - I_C \qquad \text{----------(5)}$$

→ Putting the value of IC in equation (5) from equation (3)

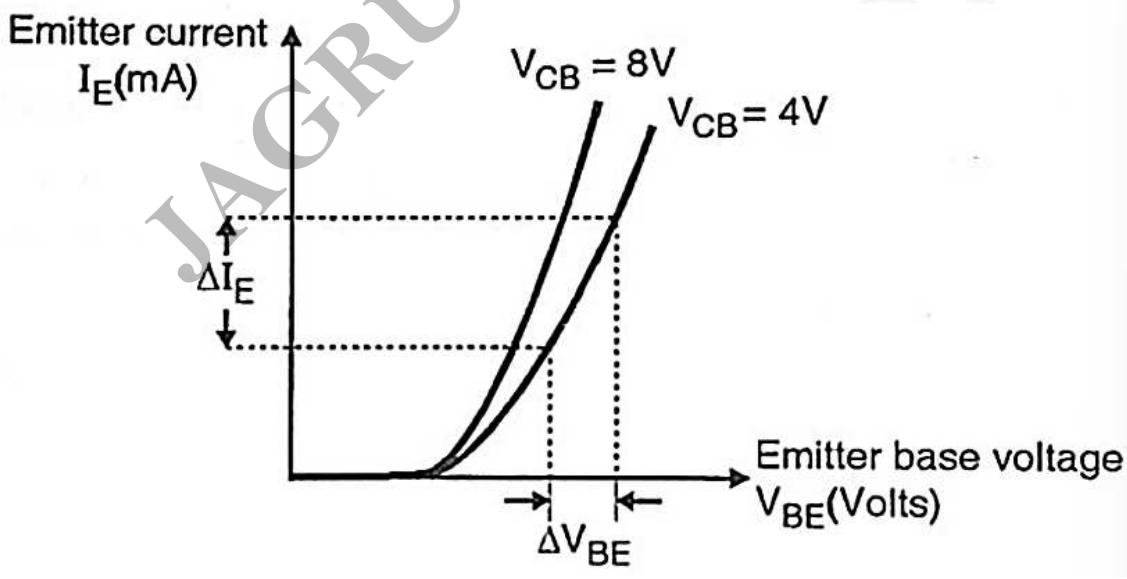
$$I_B = I_E - \alpha_{dc} I_E - I_{CBO}$$

$$I_B = I_E(1 - \alpha_{dc}) - I_{CBO} \qquad \text{----------(6)}$$

$$I_B \cong I_E(1 - \alpha_{dc})$$

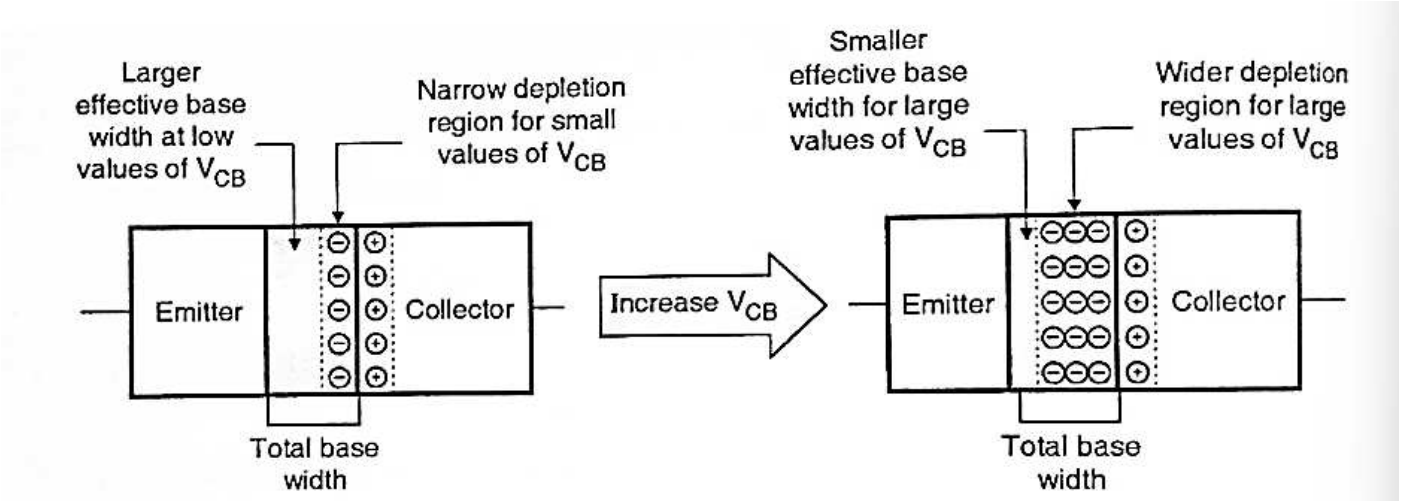
Input Characteristic of CB configuration:

→ Input characteristic is the relation between transistors input current I_E and input voltage V_{BE}, keeping the output voltage V_{CB} constant.



→ Base width modulation/Early effect:

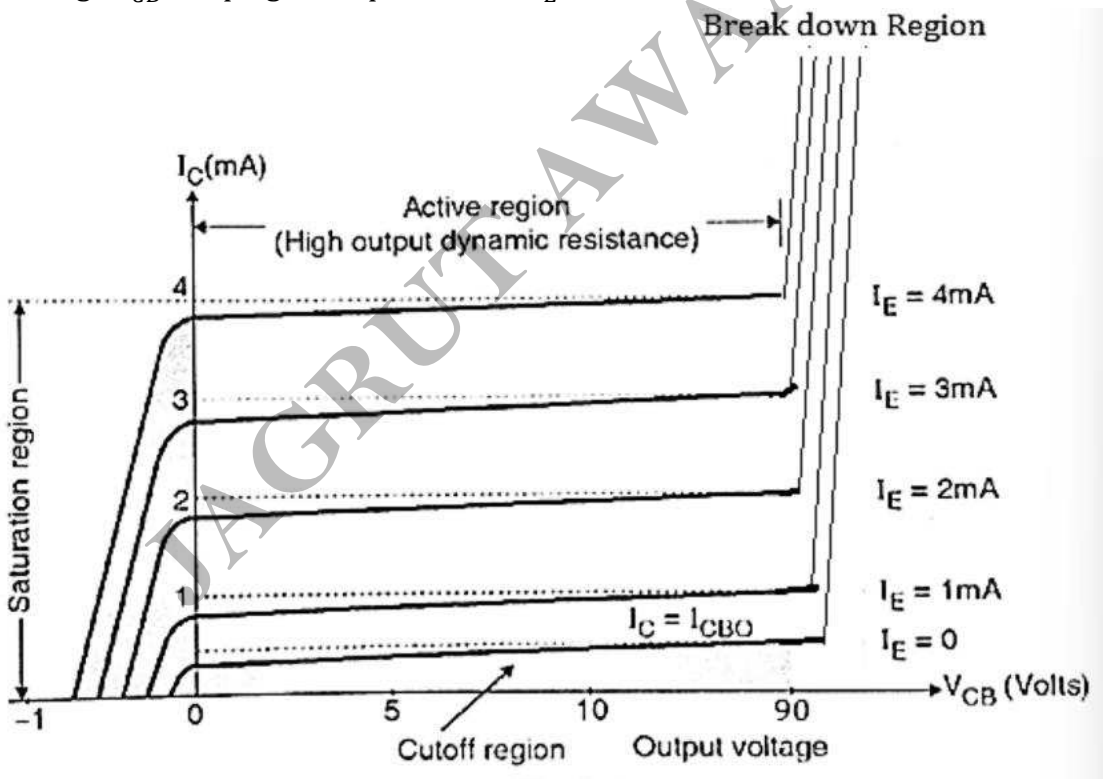
→ In CB configuration of transistor, if we increase V_{CB}, then depletion layer at CB junction will increase, which results in decrease in effective base width. Hence concentration gradient at EB junction will increase, which allows more electrons from emitter to diffuse into the base. So emitter current I_B will increase. Thus when collector base voltage V_{CB} is increases, emitter current IE will also increases.



→ The change in effective base width due to change in VCB is called Base width modulation or Early effect.

Output Characteristic of CB configuration:

→ Output characteristic is the relation between transistors output current IC and output voltage V_{CB}, keeping the input current I_E constant.



→ If an excessive reverse-bias voltage is applied to the collector-base junction, the device breakdown may occur.

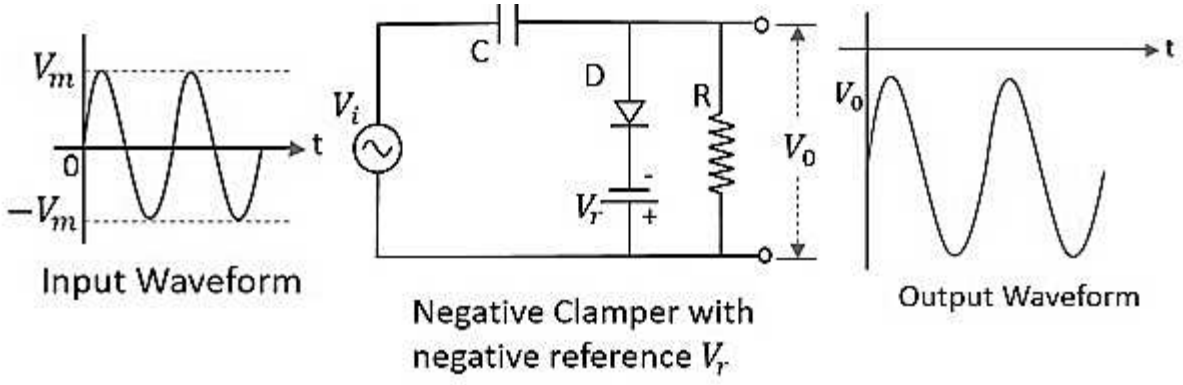
→ As reverse bias voltage V_{CB} is increases, collector-base depletion region also increases. If an excessive reverse-bias voltage is applied then collector-base depletion region penetrating into the base until it makes contact with emitter-base depletion region This condition is known as punch through or reach through effect. A Very large currents can flow when it occurs and possible destroying the device.

Q-2 (a) Describe Negative clamper circuit with necessary waveforms

Ans :

Negative Clamper circuit

→ Let's have a look at the figure shown below of negative clamper in order to understand the detailed operation-



→ At the time when positive half of the AC input is applied, the diode comes to forward bias condition that results in no-load current at the output. However, a forward current flows through the diode that charges the capacitor to the peak of the ac signal but again with inverse polarity. The capacitor here is charged up to the forward biased condition of the diode.

→ When negative half of the AC signal is applied, the diode now becomes reverse biased. This allows load current to appear at the output of the circuit. Now, this non-conducting state of the diode discharges the capacitor. So, at the output, a summation of capacitor voltage along with the input voltage is achieved.

→ Hence at the output, we have,

$$V_0 = -V_m - V_m = -2V_m$$

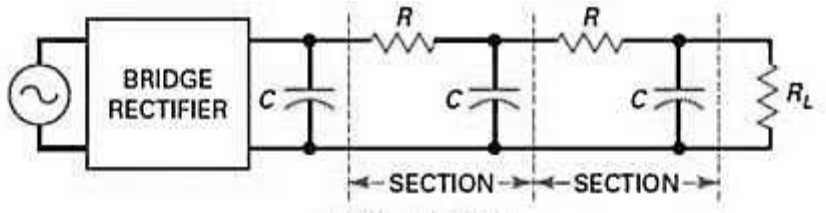
→ This results in the downward shift of the signal. Therefore, it is termed as negative clamper circuit.

(b) Describe RC filter with its limitations.

Ans :

RC Filters

→ Before the 1970s, passive filters (R, L, and C components) were often connected between the rectifier and the load resistance. Nowadays, you rarely see passive filters used in semiconductor power supplies, but there might be special applications, such as audio power amplifiers, in which you might encounter them.



→ Figure shows a bridge rectifier and a capacitor-input filter. Usually, a designer will settle for a peak-to-peak ripple of as much as 10 percent across the filter capacitor. The reason for not tryingto get even lower ripple is because the filter capacitor would become too large. Additional filtering is then done by RC sections between the filter capacitor and the load resistor.

→ The RC sections are examples of a passive filter, one that uses only R, L, or C components. By deliberate design, R is much greater than XC at the ripple frequency. Therefore, the ripple is reduced before it reaches the load resistor.

→ Typically, R is at least 10 times greater than XC. This means that each section attenuates (reduces) the ripple by a factor of at least 10.

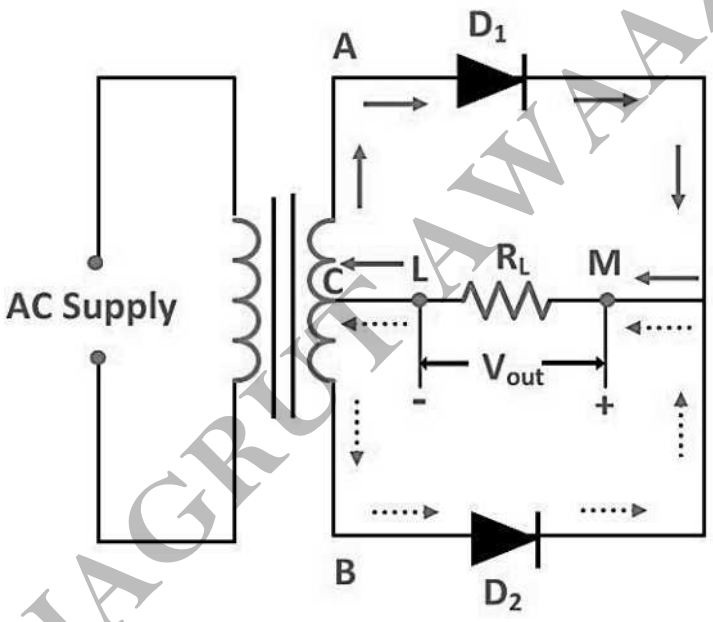
→ The disadvantage of an RC filter is the loss of dc voltage across each R. Because of this, the RC-filter is suitable only for very light loads (small load current or large load resistance).

(c) Draw circuit diagram of Center-taped full wave rectifier and explain its operation with necessary waveforms and derivation of V_{dc}.

Ans :

Center Tapped Full Wave Rectifier

→ The Center Tapped Full Wave Rectifier employs a transformer with the secondary winding AB tapped at the center point C. It converts the AC input voltage into DC voltage. The two diodes $D_1, and\ D_2$ are connected in the circuit as shown in the circuit diagram below.



→ Each diode uses a one-half cycle of the input AC voltage. The diode D_1 utilizes the AC voltage appearing across the upper half (AC) of the secondary winding for rectification. The diode D_2 uses the lower half (CB) of the secondary winding.

→ **Operation of the Center Tapped Full Wave Rectifier**

→ When AC supply is switched ON the alternating voltage, V_{in} appears across the terminals AB of the secondary winding of the transformer. During the positive half cycle of the secondary voltage, end A becomes positive, and end B becomes negative. Thus, the diode D_1 becomes forward biased, and diode D_2 becomes reverse biased.

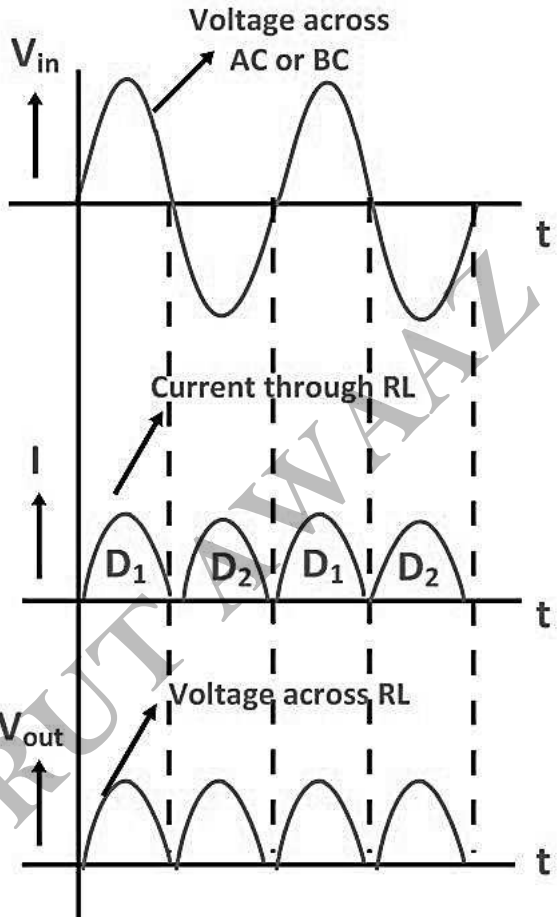
→ The two diodes conduct simultaneously. Therefore, when the diode D_1 conducts, the diode D_2 does not conduct and vice versa.

→ When the Diode D_1 is conducting, the current (i) flows through the diode D1 load resistor RL (from M to L) and the upper half of the secondary winding as shown in the circuit diagram marked by the red color arrowheads. During the negative half-cycle, the end B becomes positive, and end A becomes negative. This makes the diode D_2 forward biased, and diode D1 reverse biased.

→ When the diode D_2 conducts while the diode D_1 does not. The current (i) flows through the diode D_2 load resistor R_L (from M to L) and the lower half of the secondary winding as shown by the red dotted arrows.

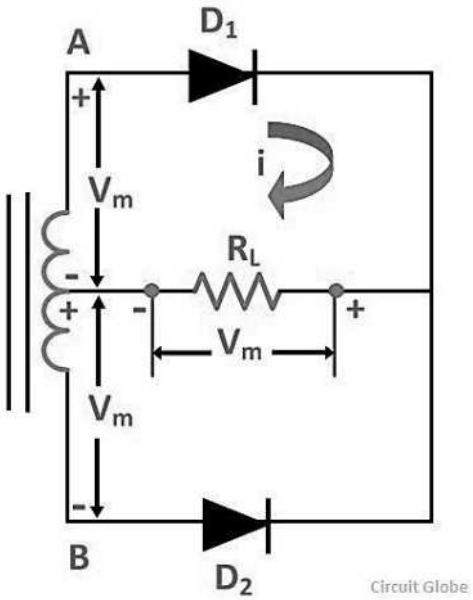
→ The current flowing through the load resistor R_L is in the same direction (i.e., from M to L) during both the positive as well as the negative half cycle of the input. Hence, the DC output voltage ($V_{out} = i R_L$) is obtained across the load resistor.

→ The wave diagram of the input voltage, the current flowing through the load, and the output voltage developed across the load is shown in the figure below:



→ **Peak Inverse Voltage of Center Tapped Full Wave Rectifier**

→ The circuit diagram given below shows the instant when the secondary voltage attains its maximum positive value.



→ At this instant, V_m developed in the upper half of the secondary winding of the transformer will forward bias the diode D_1. This diode conducts, and the current flows through R_L, developing V_m voltage across it.

→ The diode D_2 at this instant is reverse biased, and the voltage was coming across it is the sum of the maximum value of voltage developed by the lower half of the secondary winding and the voltage developed across the load. Hence, the peak inverse voltage across the diode D_2 *is* $2V_m$.

$$PIV = V_m + V_m$$

→ **Advantages and Disadvantages of Center Tapped Full Wave Rectifier**

→ The main advantage is that the output and efficiency are high because an AC supply delivers power during both half cycles.

→ **The Disadvantages of the Center tapped full wave rectifier are as follows:-**

→ Each diode utilizes only one-half of the voltage developed in the transformer secondary, and thus the DC output obtained is small.

→ It is difficult to locate the center on the secondary for the tapping.

→ The diode used must be capable of bearing high peak inverse voltage. Because the peak inverse voltage coming across each diode is twice the maximum voltage across the half of the secondary winding.

(c) Describe diode approximations in detail.

Ans :

→ Diode Approximations are how the Diodes present in the circuit gets analyzed. The diode can be considered as the basic electronic device in any type of circuit. These are of various types a design criterion is based on the requirement. The analysis of it can be done based on the Three approximations. Each approximation can be done by considering the diode as a switching element. For these basic components called Diodes, there exist three approximations. In each one, the initial and the considered stages of the diode are discussed. The motive behind this is to analyze the initial criterion considered for diodes.

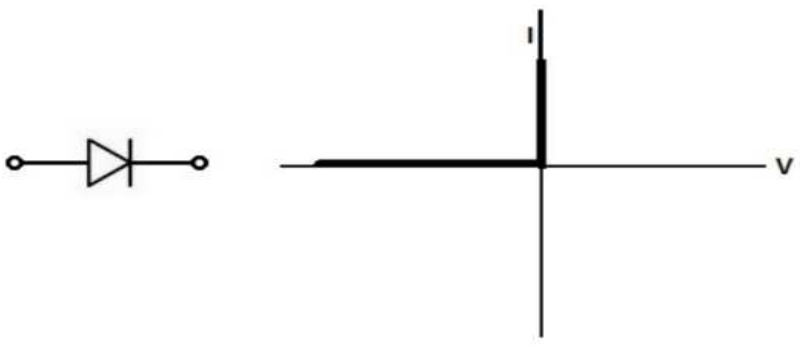
→ **Definition:** The approximation technique that helps in analyzing the various initial criteria of the diode can be defined as Diode Approximations. Each approximates relates from assuming ideal conditions to reaching practical ones.

→ **Types of Diode Approximations**

→ The diode approximation can be done in three methods using first, second, and third.

First Approximation

→ In the first situation of approximating the Diode considered to be in Ideal mode. It means there is zero Internal Resistance and doesn't have any consuming Voltage. This indicates that Diode in Ideal mode is a Perfect Version of Switch.

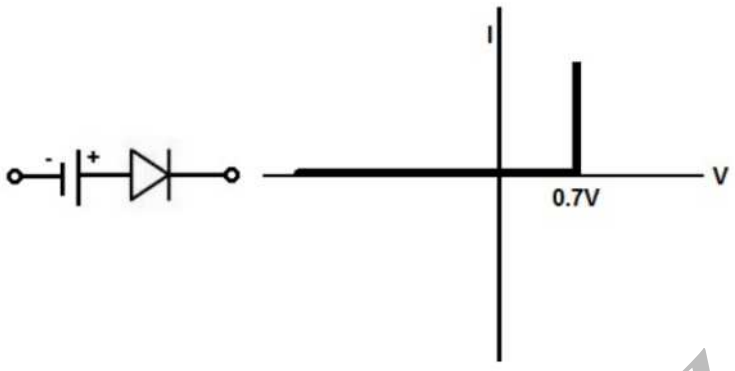


First Approximation of the Diode

→ Generally in the theoretical analysis, we can use this concept but practically this situation is impossible.

Second Approximation

→ The first condition is about the Ideal Mode of the Diode. It doesn't require any initial voltage to turn it into ON. But in the second case, it prefers a certain amount of voltage to turn the Diode ON.

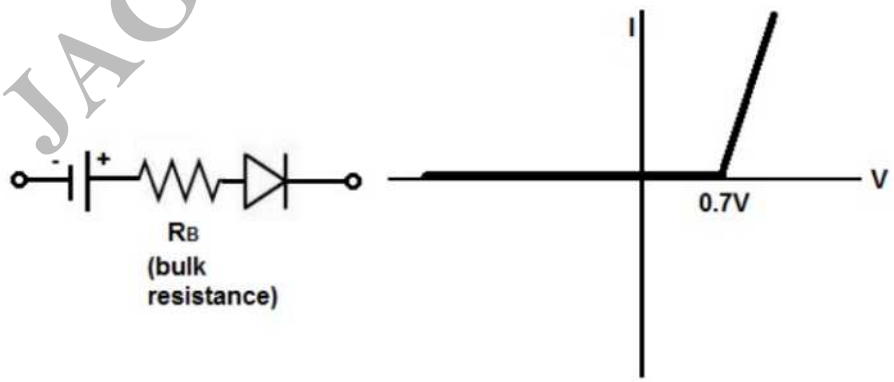


Second Approximation Diode

→ In this case of Second Approximation, the Diode can be made to function as a switch by applying the cut-off voltages. For example, if the silicon is the semiconductor material used. Then in this case, if the voltage applied exceeds 0.7 volts the Diode is in ON mode. If it is below the minimum voltage then the diode is in OFF mode. Therefore, in this way diode acts as a switch.

Third Approximation

→ In this approximation, the cut-off voltage along with some Internal Resistance across the Diode is observed. This condition exists in the practical application in the design of circuits. This type of resistance can be referred to as Bulk Resistance. It is dependent upon the amount of the Forward Voltages and Forward Currents applied to the diode.

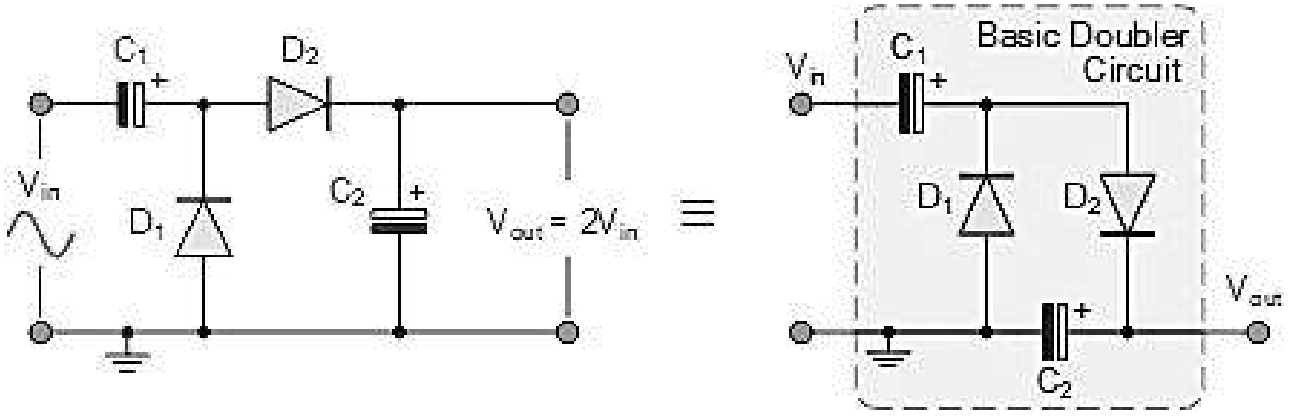


Third Approximation of the Diode

Q-3 (a) Draw circuit for Voltage doubler and explain its operation.

Ans :

→ Voltage Doubler is a voltage multiplier circuit which has a voltage multiplication factor of two. The circuit consists of only two diodes, two capacitors and an oscillating AC input voltage (a PWM waveform could also be used). This simple diode-capacitor pump circuit gives a DC output voltage equal to the peak-to-peak value of the sinusoidal input. In other words, double the peak voltage value because the diodes and the capacitors work together to effectively double the voltage.



→ So how does it work. The circuit shows a half wave voltage doubler. During the negative half cycle of the sinusoidal input waveform, diode D1 is forward biased and conducts charging up the pump capacitor, C1 to the peak value of the input voltage, (V_p). Because there is no return path for capacitor C1 to discharge into, it remains fully charged acting as a storage device in series with the voltage supply. At the same time, diode D2 conducts via D1 charging up capacitor, C2.

→ During the positive half cycle, diode D1 is reverse biased blocking the discharging of C1 while diode D2 is forward biased charging up capacitor C2. But because there is a voltage across capacitor C1 already equal to the peak input voltage, capacitor C2 charges to twice the peak voltage value of the input signal.

→ In other words, V(positive peak) + V(negative peak), so on the negative half-cycle, D1 charges C1 to V_p and on the positive half-cycle D2 adds the AC peak voltage to V_p onC1 and transfers it all to C2. The voltage across capacitor, C2 discharges through the load ready for the next half cycle.

→ Then the voltage across capacitor, C2 can be calculated as: $V_{out} = 2V_p$, (minus of course the voltage drops across the diodes used) where V_p is the peak value of the input voltage. Note that this double output voltage is not instantaneous but increases slowly on each input cycle, eventually settling to $2V_p$.

→ As capacitor C2 only charges up during one half cycle of the input waveform, the resulting output voltage discharged into the load has a ripple frequency equal to the supply frequency, hence the name half wave voltage doubler. The disadvantage of this is that it can be difficult to smooth out this large ripple frequency in much the same way as for a half wave rectifier circuit. Also, capacitor C2 must have a DC voltage rating at least twice the value of the peak input voltage.

→ The advantage of "Voltage Multiplier Circuits" is that it allows higher voltages to be created from a low voltage power source without a need for an expensive high voltage transformer as the voltage doubler circuit makes it possible to use a transformer with a lower step up ratio than would be need if an ordinary full wave supply were used. However, while voltage multipliers can boost the voltage, they can only supply low currents to a high-resistance (+100kΩ) load because the generated output voltage quickly drops-off as load current increases By reversing the direction of the diodes and capacitors in the circuit we can also reverse the direction of the output voltage creating a negative voltage output. Also, if we connected the output of one

multiplying circuit onto the input of another (cascading), we can continue to increase the DC output voltage in integer steps to produce voltage triplers, or voltage quadruplers circuits, etc, as shown.

(b) Briefly explain the effect of coupling capacitor and bypass capacitor on small signal transistor amplifier.

Ans :

→ Coupling capacitors and bypass capacitors play crucial roles in small-signal transistor amplifiers.

1. Coupling Capacitors:

→ **Function:** These capacitors block the DC component of a signal, allowing only the AC component to pass through. This is important because transistors typically operate with DC biasing, and coupling capacitors prevent this bias from affecting subsequent stages or the amplifier output.

→ **Effect on Amplifier:** By blocking DC, coupling capacitors help maintain the desired operating point (Q-point) of the transistor, ensuring that it remains in the active region where it can amplify signals effectively.

→ **Frequency Response:** The choice of coupling capacitor affects the lower cutoff frequency of the amplifier. Larger capacitors allow lower frequencies to pass, impacting the amplifier's bandwidth.

2.Bypass Capacitors:

→ **Function:** Bypass capacitors provide a low-impedance path to ground for AC signals. They effectively bypass AC signals around a certain component (usually a resistor) in the circuit.

→ **Effect on Amplifier:** Bypass capacitors help improve the gain of the amplifier at higher frequencies. This is because they reduce the effective impedance of the resistor they are bypassing, minimizing the voltage drop across the resistor at high frequencies.

→ **Frequency Response:** Bypass capacitors impact the upper cutoff frequency of the amplifier. Properly chosen bypass capacitors can extend the frequency response of the amplifier.

→ In summary, coupling capacitors block DC, allowing only AC signals to pass and ensuring proper biasing and signal integrity, while bypass capacitors provide a low-impedance path for AC signals, improving gain at higher frequencies and extending the frequency response of the amplifier. Together, these capacitors are essential for maintaining the desired performance characteristics of a small-signal transistor amplifier.

(c) Draw circuit for Emitter feedback bias and explain in detail with its advantages and disadvantages.

Ans :

Advantages:

1. **Improved Stability:** Emitter feedback bias helps stabilize the DC operating point (Q-point) of the transistor against variations in temperature and transistor parameters. This is because the feedback resistor (Rf) introduces negative feedback, which tends to oppose changes in the base-emitter voltage.
2. **Reduced Distortion:** The negative feedback introduced by Rf reduces distortion in the amplifier's output signal by stabilizing the Q-point and linearizing the amplifier's response.

3. **Better Linearity:** Emitter feedback bias improves the linearity of the amplifier by reducing the gain variations with signal level.

4. **Improved Input and Output Impedance:** The feedback resistor Rf increases the input impedance of the amplifier and reduces the output impedance, which can be beneficial for matching with other stages in a multi-stage amplifier.

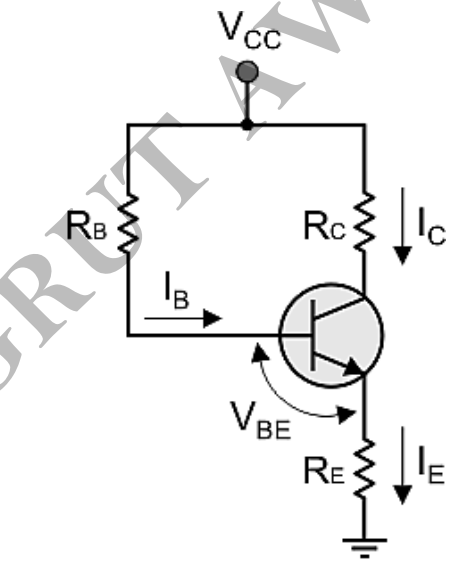
Disadvantages:

1. **Reduced Gain:** The negative feedback introduced by Rf reduces the overall voltage gain of the amplifier. This can be a disadvantage if high gain is required.

2. **Complexity:** Adding feedback components like Rf increases the complexity of the amplifier circuit and may require careful design to ensure stability.

3. **Sensitivity to Component Variations:** The performance of the amplifier can be sensitive to variations in component values, especially Rf, which can affect the biasing and stability of the circuit.

→ In summary, emitter feedback bias can improve stability, reduce distortion, and improve linearity in a transistor amplifier, but it comes at the cost of reduced gain and increased complexity. Careful design and consideration of trade-offs are necessary when implementing this biasing scheme.



Q-3 (a) State the difference between Avalanche breakdown and Zener breakdown.

Ans :

Parameters	Avalanche breakdown	Zener breakdown
Definition	Avalanche breakdown is breakdown which occurs due to current produced by high electric field caused by applying high reverse voltage across the diode.	Zener breakdown is breakdown which occurs due to reverse saturation current obtained from free electrons produced by reverse biased junction.
Junction Doping	Junction doping is light.	Junction doping is high.
Depletion layer	Its depletion layer is thick.	Its depletion layer is thin.
Electric field	Electric field produced is weak.	Electric field produced is strong.

Zener voltage	It is greater than 8V.	It ranges from 5 to 8V.
VI Curve	It has less sharp VI curve.	It has sharp VI curve.
Temperature	Increased breakdown voltage increases temperature.	Decreased breakdown voltage increases temperature.

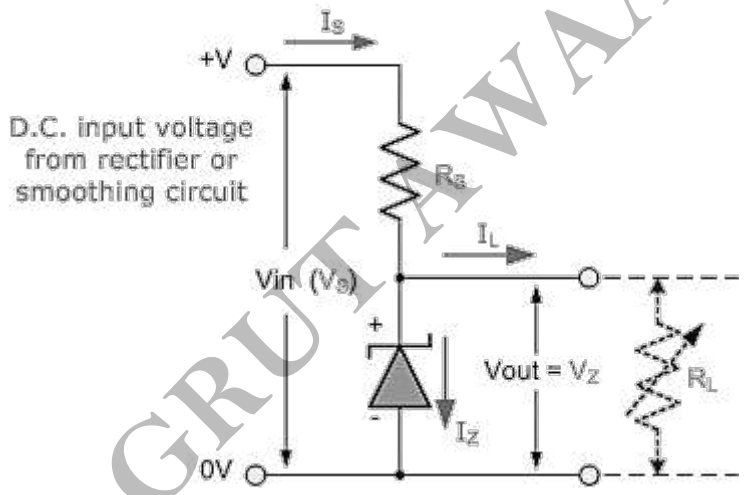
(b) Discuss Zener diode as voltage regulator.

Ans :

→ There is a series resistor connected to the circuit in order to limit the current into the diode. It is connected to the positive terminal of the d.c. It works in such a way the reverse-biased can also work in breakdown conditions. We do not use ordinary junction diode because the low power rating diode can get damaged when we apply reverse bias above its breakdown voltage. When the minimum input voltage and the maximum load current is applied, the Zener diode current should always be minimum.

→ Since the input voltage and the required output voltage is known, it is easier to choose a Zener diode with a voltage approximately equal to the load voltage, i.e. $V_Z = V_L$.

→ The circuit diagram of a voltage regulator using a Zener diode is shown:



→ The value of the series resistor is written as $RS = (V_L - V_Z)I_L$.

→ Current through the diode increases when the voltage across the diode tends to increase which results in the voltage drop across the resistor. Similarly, the current through the diode decreases when the voltage across the diode tends to decrease. Here, the voltage drop across the resistor is very less, and the output voltage results normally.

(c) Discuss load line, Q point, DC & AC load lines for BJT.

Ans :

Load line

→ A load line is a line drawn on a graph that shows the current and voltage relationship for a nonlinear device. It's usually a straight line drawn on a graph that compares current and voltage.

→ A load line represents the constraint on current and voltage in a nonlinear device by the external circuit.

→ A load line is used to find the best operating point or biasing of a nonlinear device, such as a FET or bipolar transistor.

→ A load line is also known as a waterline mark or Plimsoll line.

Q-point

→ The Q point or operating point is a fixed DC voltage and current level at which a transistor functions. It plays a significant role in determining the power consumption and amplification capacity of the transistor. Setting the Q point precisely is critical for safe operation and optimal performance of the transistor.

→ **Q point or Operating Point**

→ The point on a transistor's DC load line where the transistor is biased to operate for a specific application is known as the Q point of the transistor (also known as the operating point or bias point). The DC supply voltage and DC load resistance values determine the Q point.

→ (Operating Point) Q point →Quiescent Point

→ The term "quiescent point" refers to an electrical circuit's steady state of operation when it is not being driven by an input signal. It is a crucial idea in circuit design since it enables engineers to make sure the circuit functions correctly and dependably under typical circumstances. The Zero signal of I_C *and* V_{CE} of the transistor is known as the operating point. It is called the operating point because the variations of I_C *and* V_{CE} take place at this point when the signal is applied. It is also called quiescent (silent) point or Q-point because it is the point on $I_C - V_{CE}$ characteristic when the transistor is silent i.e., in the absence of the signal.

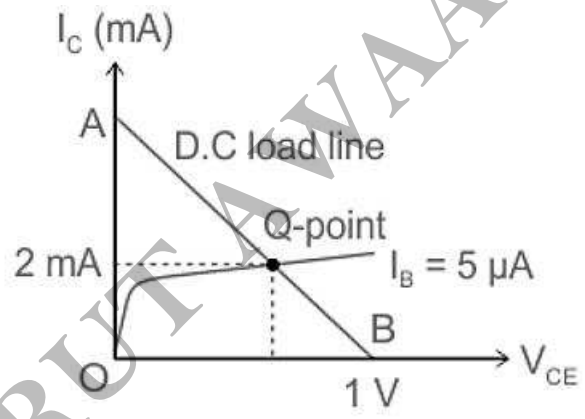


Fig: Operating Point

→ The formula for calculating a device or circuit's Q point depends on the details and properties of the object being studied. For instance, the following formula can be used to find the Q-point in a transistor circuit:

$$Q = \frac{V_{CC} - V_{CE}}{I_C}$$

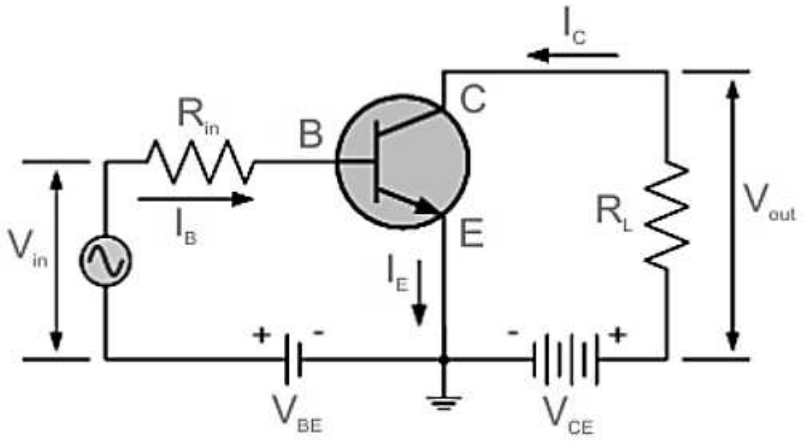
→ Where I_C is the collector current at Q point
V_{CE} is the Collector-Emitter voltage at Q point
And V_{CC} is the supply voltage

→ It's important to maintain a stable Q point in a transistor amplifier circuit to ensure proper operation and prevent distortion or other problems. Careful design and selection of components, as well as appropriate thermal management, can help to minimize fluctuations in the Q point.

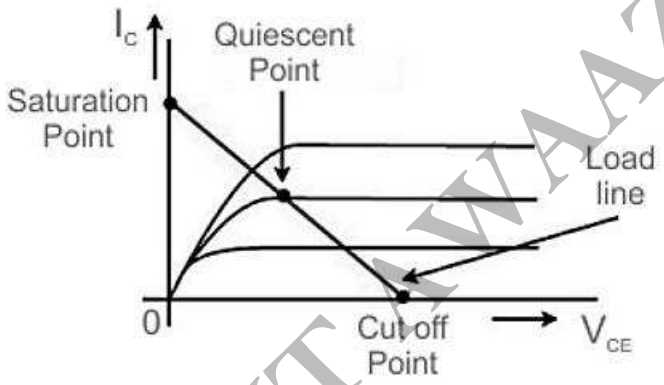
→ A transistor can function as an amplifier by receiving a weak signal through its base connection and increasing its strength. The amplified signal is then transmitted through the collector connection.

Concept of DC Load Line:

→ The DC load line of a transistor shows the relationship between the current and voltage of the circuit under consideration for a given load. The load line method is quite easy and is frequently used in the analysis of transistor applications.



→ Consider a common emitter transistor circuit shown in the figure above. Where no signal is applied to its input. Therefore D.C. conditions prevail in the circuit.



→ The output characteristics of this circuit are shown in the figure above.

→ By Applying Kirchoff's voltage law to the collector circuit, we get

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + V_{CC} R_C$$

$$y = mx + C$$

→ The equation (2) is in the form of $y = mx + C$ which represents a straight line on the output characteristics. This is known as the D.C. load line. It determines the curve between V_{CE} and I_C points for any given R_C. The two endpoints of the load line are located below.

→ When the collector current $IC = 0$, collector-emitter voltage V_{CE} is given by,

$$V_{CE} = V_{CC}$$

The first point B is $(VCC, 0)$

→ When collector-emitter voltage $V_{CE} = 0$, the collector current is given by,

$$I_C = \frac{V_{CC}}{R_C}$$

The second point A is $\left(0, \frac{V_{CC}}{R_C}\right)$

→ By joining those points A and B, the D.C load line is constructed as shown in the figure,

Concept of AC Load Line:

→ A.C. load line is the line along which Q-point shifts up and down when changes in output voltage and current of an amplifier are caused by an AC signal. The D.C. load line is drawn between output voltage V_{CE} and output current I_C . When there is no input signal applied to the transistor amplifier. After drawing the D.C. load line. The A.C. load line is drawn when an input weak signal is applied to the amplifier. After this amplification process is done.

→ The output is taken across load resistance R_L .The resistance across the collector is now equal to a parallel combination of R_C *and* R_L. Under A.C conditions capacitor C_C can be considered as a short at the frequency of operation. As a result, a new load line needs to be drawn on the output characteristics to be able to determine collector current and collector voltage for given input excitation. This line is called the A.C. load line, is drawn passing through the operating point.

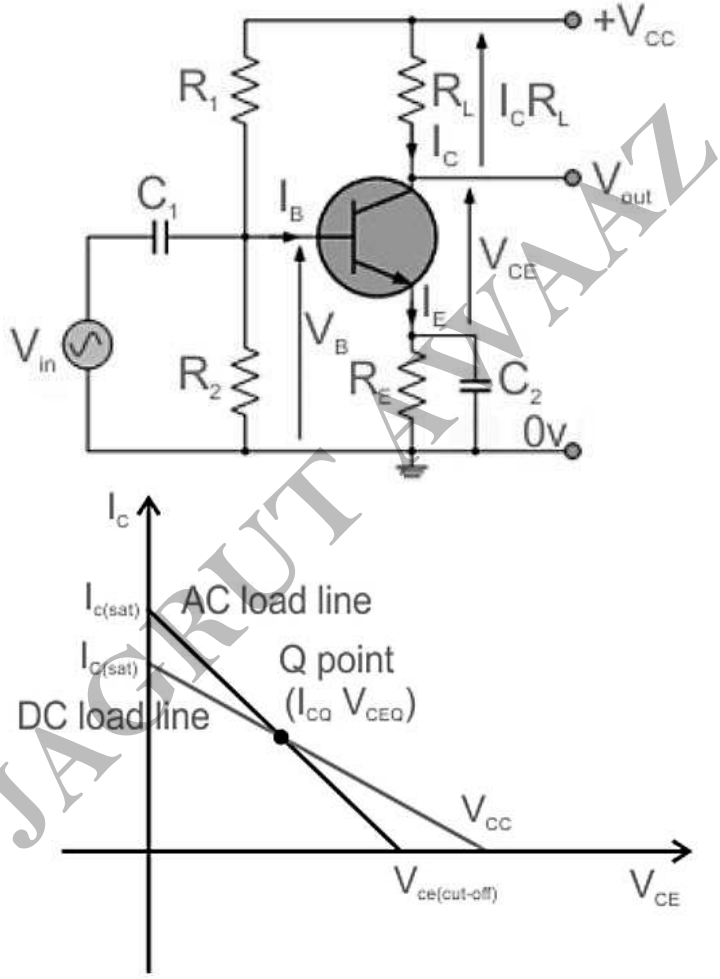


Fig: AC Load line and transistor load line

→ 1.D.C. Load Line: D.C. load line is drawn between Point A and Point B
1.Point A $(V_{CC}, 0)$ 2. Point B $\left(0, \frac{V_{CC}}{R_C}\right)$ Where, $V_{CE} = V_{CC}$ Where, $I_C == \frac{V_{CC}}{R_C}$

→ 2.A.C Load Line:
1.Point C $(V_{CE}, 0)$
Where, $V_{CE} = (V_{CEQ} + I_{CQ}R_{ac})$
R_{ac} = Load resistance
R_{ac}=$R_c||R_L$
2.Point $D(0, I_C)$ Where, $I_C = I_{CQ} + V_{CEQ}R_{ac}$ A.C load line is drawn between point C and Point D.

Q-4 (a) Derive relation between α & β for BJT.

Ans :

→ The de common-base current ratio or current gain (α_{dc}) is defined as the ratio of the collector current to emitter current.

$$\alpha_{dc} = \frac{I_C}{I_E}$$

→ The de common-emitter current ratio or current gain (β_{dc}) is defined as the ratio of the collector current to base current.

$$\beta_{dc} = \frac{I_C}{I_B}$$

→ Since the emitter current $I_E = I_B + I_C$

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$$

→ Therefore, the common-base current gain in terms of the common-emitter current gain is

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}$$

→ and the common-emitter current gain in terms of the common-base current gain is

$$\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

→ For a transistor, α_{dc} is dose to but always less than 1 (about 0.92 to 0.98) and β_{dc} ranges from 20 to 200 for most general-purpose transistors.

(b) Compare different BJT configurations.

Ans :

Characteristic	Common base(CB)	Common emitter	Common collector(CC)
Input Dynamic Resistance	Very Low(less than 100 ohm)	Low(less than 1K)	Very High(750K)
Output Dynamic Resistance	Very High	High	High
Current Gain	Less than 1	High	Very High
Voltage gain	Greater than CC but less than CE	Highest	Lowest(less than 1)

(c) Describe working principle and applications of PIN Photo diode and Solar cell.

Ans :

PIN Photodiode:

→ **Working Principle:**

→ A PIN photodiode is a type of photodetector that converts light into current. It consists of three layers: P-type (positive), intrinsic, and N-type (negative). The intrinsic layer is a high-resistivity material, which reduces the dark current (current in the absence of light). When light enters the intrinsic layer, it generates electron-hole pairs. The electric field created by the P-N junction separates these carriers, causing them to flow as current.

→ **Applications:**

1. **Optical Communications:** PIN photodiodes are used in fiber optic communication systems to convert optical signals into electrical signals for transmission.

2. **Remote Sensing:** They are used in remote sensing applications, such as LiDAR (Light Detection and Ranging), where they detect reflected light to measure distances.

3. **Medical Imaging:** In X-ray detectors, PIN photodiodes convert X-rays into electrical signals for imaging purposes.

4. **Barcode Readers:** PIN photodiodes are used in barcode scanners to detect the reflected light from the barcode lines.

5. **Flame Detection:** They are used in flame detectors to sense the presence of flames by detecting the light emitted by the flame

Solar Cell:

→ **Working Principle:**

→ A solar cell, or photovoltaic cell, converts sunlight directly into electricity through the photovoltaic effect. It is typically made of silicon and consists of two layers: P-type and N-type. When sunlight strikes the solar cell, it excites electrons in the silicon, creating electron-hole pairs. The built-in electric field at the P-N junction separates these carriers, generating a voltage and current flow.

→ **Applications:**

1. **Residential and Commercial Power:** Solar cells are used in photovoltaic systems to generate electricity for homes, businesses, and other buildings.

2. **Remote Power Systems:** They are used in remote areas where traditional power sources are not available, such as in rural electrification and off-grid applications

3. **Spacecraft and Satellites** Solar cells are used in spacecraft and satellites to provide power for various systems and instruments.

4. **Portable Chargers:** Solar cells are used in portable chargers for electronic devices, such as smartphones and laptops, to charge them using solar energy.

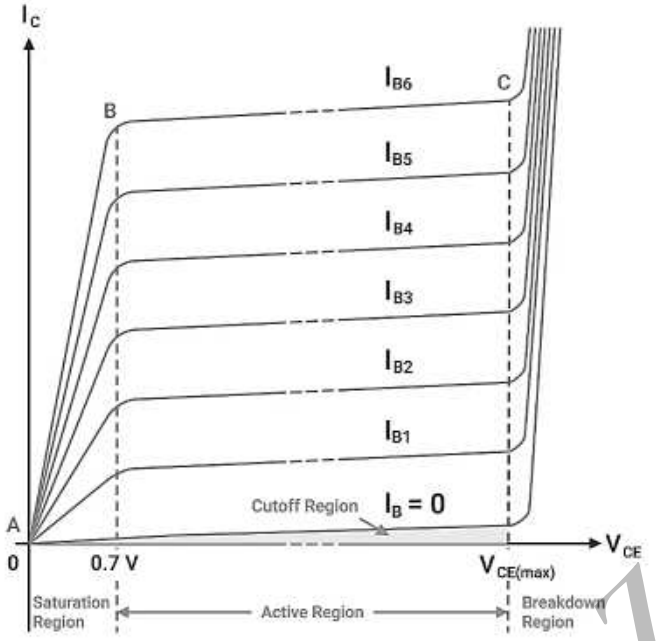
5. **Street Lights:** Solar cells are used in solar street lights to convert sunlight into electricity for powering the lights.

Q-4 (a) Briefly explain regions of operation for BJT.

Ans :

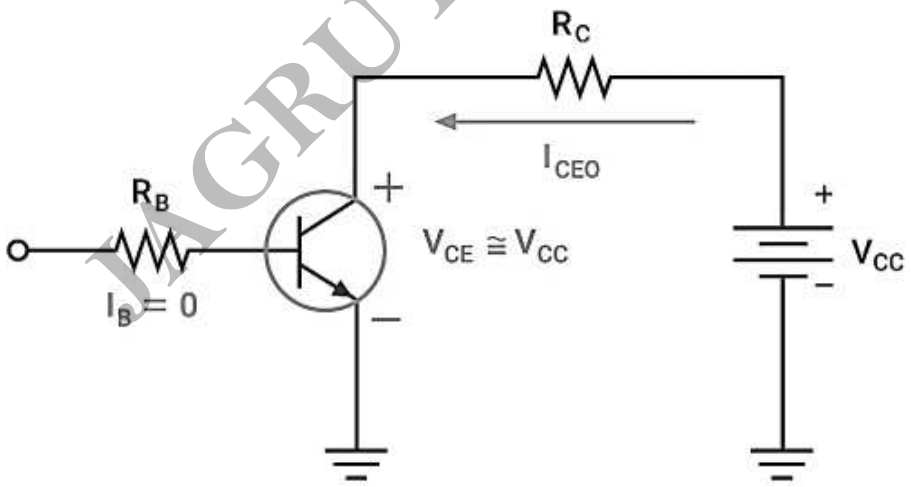
→ Now we're done with the BJT parameters and basic BJT circuit analysis, let's proceed to the operating regions of the BJT. As you can see in figure , there are three operating regions of a BJT,

cutoff region, saturation region, and active region. The breakdown region is not included as it is not recommended for BJTs to operate in this region.



→ **Cutoff Region**

→ So let's start with the cutoff region as it is the easiest one to understand. The nonconducting state of the BJT falls under the cutoff region. As shown again in figure , the BJT operates in the cutoff region when I_B is equal to zero. In this case, there should be no current that will flow through the collector. However, in reality, there will be a very small collector leakage current that will flow due to the thermally produced carriers. But since this collector leakage current is very small, it can be neglected and V_{CE} will be considered as approximately equal to V_{CC} as shown in figure .

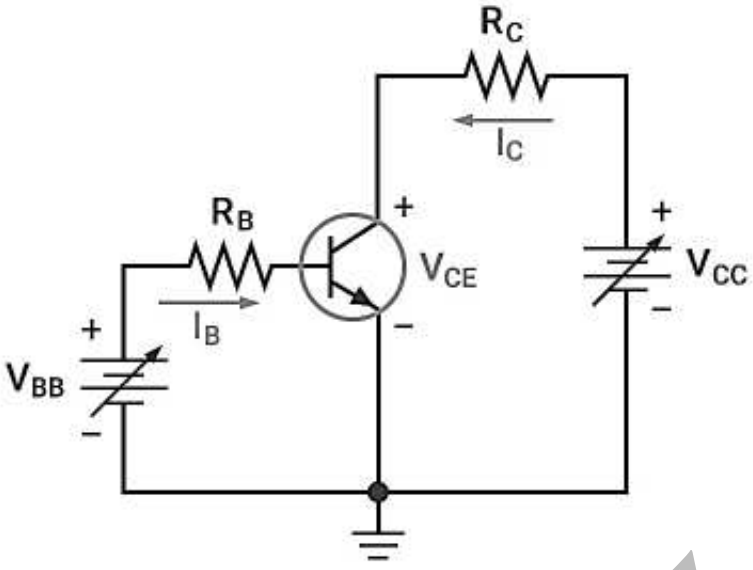


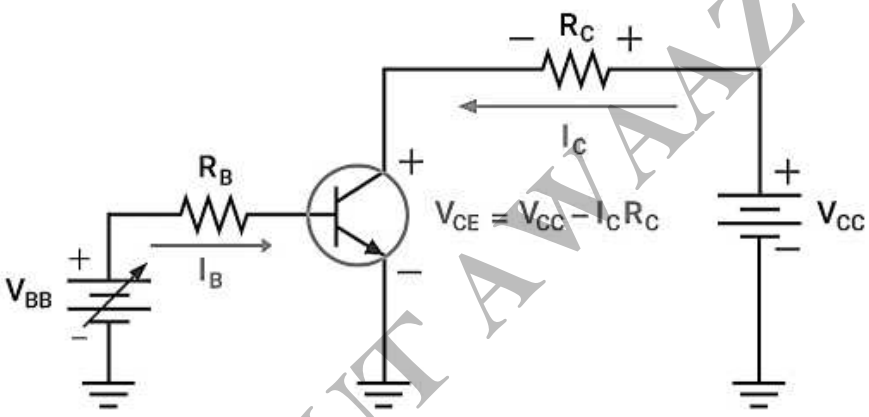
→ **Saturation Region of BJT**

→ The BJT operates in the saturation region when its collector current is not dependent on the base current and has reached a maximum. The condition for this to happen is that both the base-emitter and the base-collector junctions should be forward-biased. For example, in figure we have a BJT circuit which is similar to the circuit that we've analyzed recently though their difference is that the external bias voltages here are variable.

→ Let's say that the circuit is configured in this condition, V_{BB} will forward-bias the base-emitter junction and produce a certain value of I_B *while* V_{CC} is zero. In this case, V_{BE} will be approximately equal to 0.7V while the emitter and the collector are at 0V. As we've analyzed the basic BJT circuit recently, remember we've mentioned that if the collector is at a lower voltage than the base, then the collector-base junction will be forward-biased. Since the base voltage

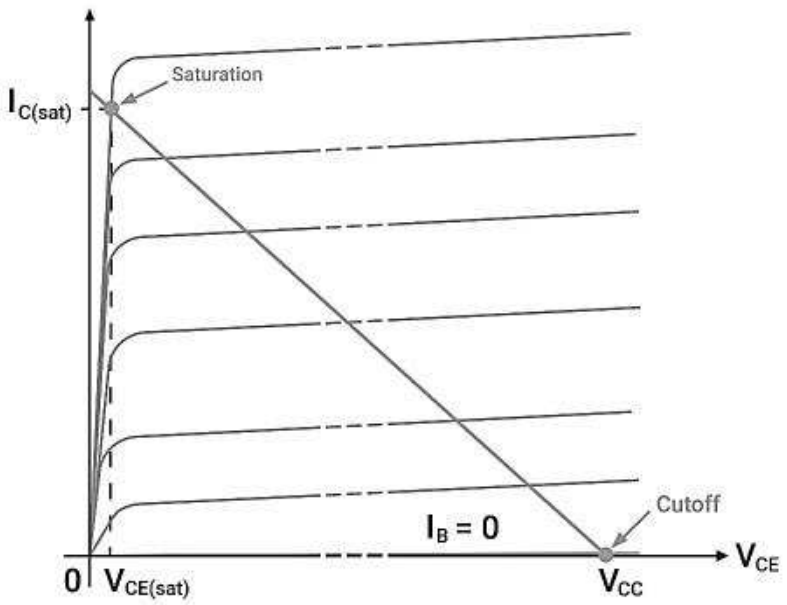
here, which is approximately 0.7V, is higher than the collector voltage which is 0V, then the base-collector junction is forward-biased.





→ Now, in figure we set V_{CC} to a non-zero value then increase the base current by increasing V_{BB}. In this case, I_C increases while VCE decreases since the voltage drop across RC also increases. As we further increase IB, IC also increases until VCE will reach the saturation voltage (VCE(sat)). This time, the BJT reaches saturation and IC can no longer increase regardless of the increase in IB.

→ **Active Region**



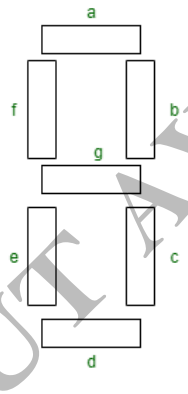
→ By using a load line, we can see that the cutoff point is at the bottom of the load line where IC is zero and VCE is equal to VCC while at the top of the load line is the saturation point where IC is equal to IC(sat) and VCE is equal to VCE(sat). Between cutoff and saturation along the load line is the active region of the BJT or also known as linear region. For the BJT to operate in the active region, the condition is that the base-emitter junction should be forward-biased while the base-collector junction is reverse-biased. In this region, IC almost remains constant for a given value of IB. But as VCE increases, IC increases slightly since the base-collector depletion region widens. When a BJT operates in the active region, ideally its output is a linear reproduction of the input signal.

(b) Discuss seven segment displays with its types.

Ans :

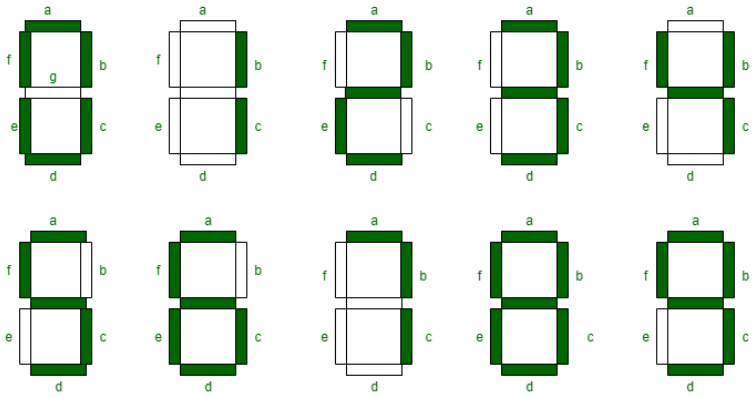
Seven Segment Display:

→ Seven segment displays are the output display device that provides a way to display information in the form of images or text or decimal numbers which is an alternative to the more complex dot matrix displays. It is widely used in digital clocks, basic calculators, electronic meters, and other electronic devices that display numerical information. It consists of seven segments of light-emitting diodes (LEDs) which are assembled like numerical 8.



→ **Working of Seven Segment Displays:**

→ The number 8 is displayed when the power is given to all the segments and if you disconnect the power for 'g', then it displays the number 0. In a seven-segment display, power (or voltage) at different pins can be applied at the same time, so we can form combinations of display numerical from 0 to 9. Since seven-segment displays can not form alphabets like X and Z, so it can not be used for the alphabet and they can be used only for displaying decimal numerical magnitudes. However, seven-segment displays can form alphabets A, B, C, D, E, and F, so they can also be used for representing each display unit is usually has a dot point (DP). The display point could be located either towards the left or towards the right of the display pattern. This type of pattern can be used to display numerals from 0 to 9 and letters from to F hexadecimal digits.



→ **Truth Table:**

→ We can produce a truth table for each decimal digit

Decimal Digit	Individual Segments Illuminated						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

→ Therefore, Boolean expressions for each decimal digit that requires respective light-emitting diodes (LEDs) are ON or OFF. The number of segments used by digit: 0, 1, 2, 3, 4, 5, 6, 7, 8, and 9 are 6, 2, 5, 5, 4, 5, 6, 3, 7, and 6 respectively. Seven segment displays must be controlled by other external devices where different types of microcontrollers are useful to communicate with these external devices, like switches, keypads, and memory.

→ **Types of Seven Segment Displays:**

→ According to the type of application, there are two types of configurations of seven-segment displays: common anode display and common cathode display.

1. In common cathode seven segment displays, all the cathode connections of LED segments are connected together to logic 0 or ground. We use logic 1 through a current limiting resistor to forward bias the individual anode terminals a to g.
2. Whereas all the anode connections of the LED segments are connected together to logic 1 in a common anode seven segment display. We use logic 0 through a current limiting resistor to the cathode of a particular segment a to g.

→ Common anode seven segment displays are more popular than cathode seven segment displays because logic circuits can sink more current than they can source and it is the same as connecting LEDs in reverse. Applications of Seven Segment Displays: Common applications of seven-segment displays are:

1. Digital clocks
2. Clock radios
3. Calculators
4. Wristwatches
5. Speedometers
6. Motor-vehicle odometers
7. Radiofrequency indicators

→ Advantages and disadvantages of Seven Segment Displays:

→ **Advantages of Seven Segment Displays:**

1. **Simplicity:** Seven Section Presentations are straightforward and simple to use since they just showcase mathematical digits (0-9) and a couple of characters like A-F for hexadecimal numbers.
2. **Cost-viable:** Seven Section Presentations are generally modest and require less parts to work than different sorts of showcases like LCDs or OLEDs.
3. **High perceivability:** Seven Portion Presentations have high perceivability even in low light circumstances as they are intended to emanate splendid, high-contrast light in a particular example that is not difficult to peruse.
4. **Durability:** Seven Section Presentations are strong and sturdy since they are produced using materials that are impervious to temperature changes and mechanical pressure.

→ **Disadvantages of Seven Segment Displays:**

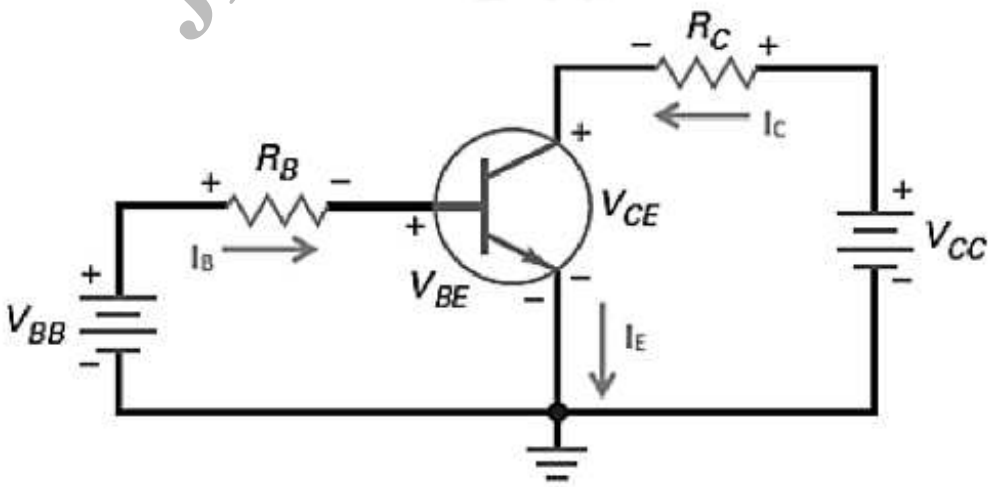
1. **Limited usefulness:** Seven Section Presentations are restricted to showing mathematical digits and a couple of characters, which can be a disservice in applications that require more mind boggling shows like designs or message.
2. **Limited review points:** Seven Fragment Showcases have restricted survey points, and that implies that the presentation might be hard to peruse from specific points or in splendid daylight.
3. **Power utilization:** Seven Portion Presentations consume more power than different sorts of showcases since they produce light constantly, which can be a burden in battery-worked gadgets.
4. **Limited customization:** Seven Portion Showcases are not effectively adaptable since they are intended to show just unambiguous examples of digits and characters, making it hard to show custom images or illustrations.

(c) Draw CE configuration and discuss its input and output characteristics with I_{CEO}, r_i, r_o, and current gain β.

Ans :

→ In common emitter configuration, base is the input terminal, collector is the output terminal, and emitter is the common terminal between input and output.

→ As shown in figure EB junction is forward biased and CB junction is reverse biased. To forward bias EB junction V_{BB} battery is connected and to reverse bias CB junction V_{CC} battery is connected as shown in figure. Resistance R_B *and* R_C are current limiting resistors.



→ Current Gain and different current components in CE configuration:

Current Gain β_{dc}:

→ It is defined as the ration of output current IC to Input current IB. it is dented by βdc or β. It is represented by equation

$\beta_{dc} = \frac{I_c(inj)}{I_B} = \frac{I_C - I_{CEO}}{I_B}$ ----------(1)

→ In equation (1)

→ I_C (inj)is injected charge carrier into the collector from emitter I_{CEO} is reverse leakage current between collector to emitter when base is open. Which is very small. If we neglect I_{CEO} *then* β_{dc} is approximated to

$\beta_{dc} \cong \frac{I_C}{I_B}$ ----------(2)

Collector current I_C :

→ From equation (1), collector current can be written as

$I_C = \beta_{dc} I_B + I_{CEO}$ ----------(3)

→ as I_{CEO} is very small, If we neglect I_{CEO} then collector current I_C is approximated to

$I_C \cong \beta_{dc} I_B$

Emitter current I_E :

→ Emitter current is sum of Base current I_B and collector current I_C

$I_E = I_C + I_B$ ----------(4)

→ Putting the value of IC in equation (4) from equation (3)

$I_E = \beta_{dc} I_B + I_{CEO} + I_B$

$I_E = I_B(1 + \beta_{dc}) + I_{CEO}$ ----------(5)

$I_E \cong I_B(1 + \beta_{dc}) + I_{CEO}$

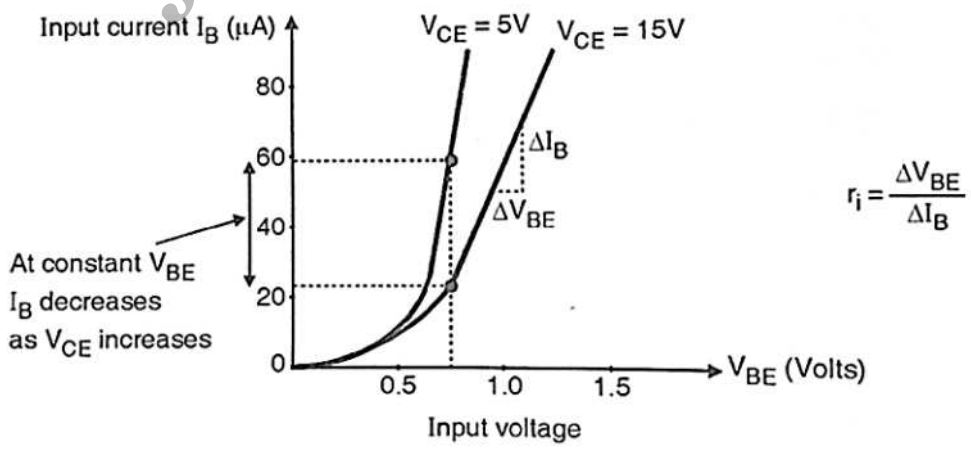
Base current I_B :

→ Base current I_B is

$I_B = I_E - I_C$ ----------(6)

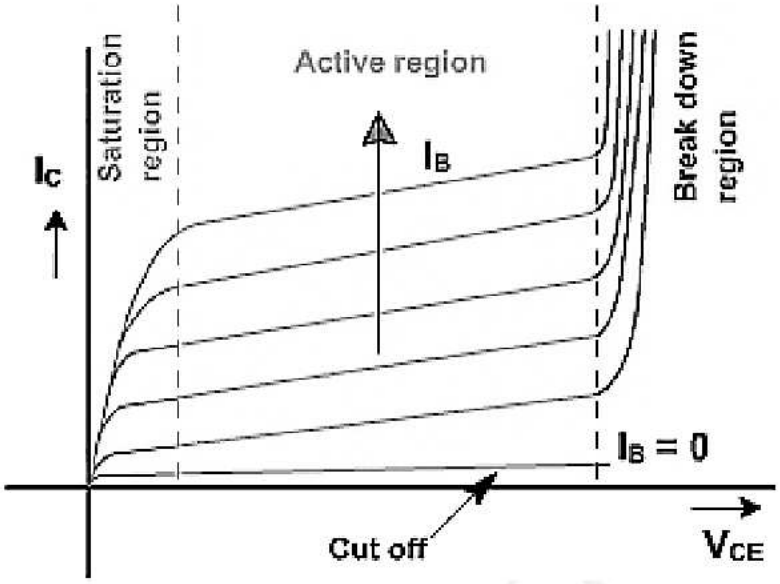
Input Characteristic of CE configuration:

→ Input characteristic is the relation between transistors input current IB and input voltage V_{BE}, keeping the output voltage V_{CE} constant.



Output Characteristic of CE configuration:

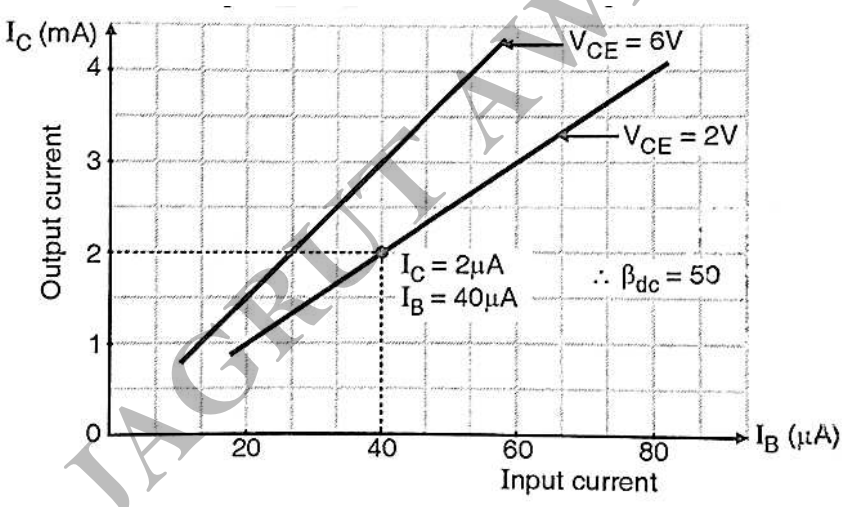
→ Output characteristic is the relation between transistors output current I_C and output voltage V_{CE}, keeping the input current I_B constant.



→ If an excessive reverse-bias voltage is applied to the collector-emitter junction, the device breakdown may occur.

Transfer Characteristic of CE configuration

→ Transfer characteristic is the relation between transistors output current IC and input current I_B for constant V_{CB} voltage. It is linear as shown in figure.



Q-5 (a) Compare FET with BJT.

Ans :

Sr. No.	FET	BJT
1.	It is unipolar device.	It is a bipolar device.
2.	Its input resistance is very high.	Its input resistance is very low.
3.	It is a voltage-controlled device.	It is a current controlled device.
4.	It has negative temperature coefficient at high current level.	It has positive temperature coefficient at high current level.
5.	It does not suffer from minority carrier storage effects.	It suffers from minority carrier storage effects.

6.	It has higher switching speed and cut off frequencies.	It has lower switching speed and cut off frequencies.
7.	It is much simpler to fabricate as an integrated circuit.	It is more complicated to fabricate as an integrated circuit.
8.	It is less noisy.	It is more noisy.
9.	It is relatively immune to radiation.	It is susceptible to radiation.
10.	It has lower gain bandwidth product.	It has higher gain bandwidth product..
11.	It requires special handling during installation.	It does not require special handling during installation.

(b) Explain FET as a switch.

Ans :

→ Field Effect Transistors (FETs) can be used as switches in electronic circuits due to their ability to control the flow of current between the source and drain terminals. Here's how an FET operates as a switch:

1. Operating Principle:

→ FETs are voltage-controlled devices, where the voltage applied to the gate terminal controls the flow of current between the source and drain terminals.

→ In a simplified view, an FET can be considered as a voltage-controlled resistor. When a voltage is applied to the gate terminal, it creates an electric field that controls the resistance between the source and drain terminals.

2. Switching Operation:

→ OFF State: When the gate-source voltage V_{GS} is below a certain threshold voltage V_{th} , the FET is in the OFF state, and only a very small leakage current flows between the source and drain (similar to an open switch).

→ -ON State: When V_{GS} is above V_{th} the FET is in the ON state, and it behaves like a closed switch, allowing a larger current to flow between the source and drain terminals.

3. Advantages of FET as a Switch:

→ High Input Impedance: FETs have a very high input impedance, which means they require very little input current to control the switching action, making them suitable for use in high-impedance circuits.

→ Fast Switching Speed: FETs can switch on and off very quickly, making them suitable for applications requiring high-speed switching.

→ Low Drive Power: FETs require very low power to drive them, which can be advantageous in low-power applications.

4. Applications:

→ FETs are commonly used as switches in digital circuits, where they can be used to control the flow of digital signals.

→ They are also used in power electronics as switches to control the flow of high-power electrical currents in devices such as motor drives, inverters, and power supplies.

(c) State different logic families and compare them in terms of fan in, fan out, propagation delay, noise margin, power dissipation.

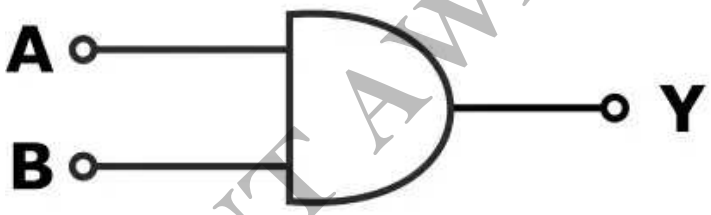
Ans :

S.N.	Parameter	DTL	HTL	TTL	RTL	ECL	MOS	CMOS
1.	Basic Gates (Positive Logic)	NAND	NAND	NAND	NOR	OR-NOR	NAND	NOR or NAND
2.	Fan out (Minimum)	8	10	10	5	24	20	>50
3.	Typical power dissipation per gate, mW	8-12	55	12-22	12	40-55	0.2-10	0.01 static 1 at 3 MHz
4.	Noise immunity	Good	Excellent	Very good	Medium	Good	Medium	Very good
5.	Typical propagation delay/gate, ns	30	90	12-6	12	4-1	300	70
6.	Clock rate (minimum frequency at which flip-flops operate), MHZ	12-30	4	15-60	8	60-400	2	5
7.	Number of functions	Fairy High	Medium	Very high	high	High	Low	Low

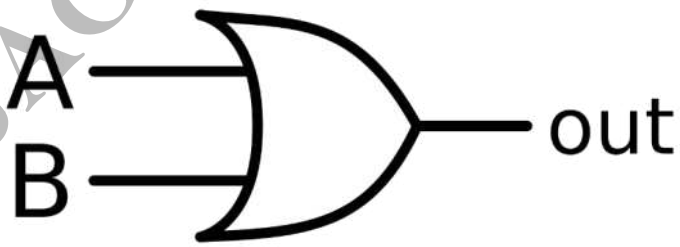
Q-5 (a) Construct AND & OR gates with diodes.

Ans :

→ AND GATE:



→ OR GATE :



(b) Explain FET as an amplifier.

Ans :

Field Effect Transistors (FETs) can be used as amplifiers in electronic circuits due to their ability to control the flow of current between the source and drain terminals. Here's how an FET operates as an amplifier:

1. Operating Principle:

→ FETs are voltage-controlled devices, where the voltage applied to the gate terminal controls the flow of current between the source and drain terminals.

→ In the amplification process, a small input voltage signal applied to the gate terminal controls a much larger output current flowing between the source and drain terminals.

2. Amplification Operation:

→ Common Source Configuration: The most common configuration for using an FET as an amplifier is the common source configuration.

→ Small Signal Amplification: In this configuration, a small AC input voltage signal applied to the gate terminal causes a corresponding AC current to flow between the source and drain terminals.

→ Voltage Gain: The ratio of the output voltage to the input voltage is the voltage gain of the amplifier. FETs can provide voltage gains ranging from a few to several hundred, depending on the circuit design and FET characteristics.

3. Advantages of FET as a Amplifier:

→ High Input Impedance: FETs have a very high input impedance, which means they draw very little current from the input signal source, minimizing loading effects.

→ Low Noise: FETs exhibit low noise characteristics, making them suitable for use in low-noise amplifier applications.

→ Wide Frequency Response: FETs can operate over a wide range of frequencies, making them suitable for use in high-frequency amplifiers.

4. Applications:

→ FETs are used in audio amplifiers, where they can amplify small audio signals to drive speakers or headphones.

→ They are used in radio frequency (RF) amplifiers to amplify RF signals in communication systems.

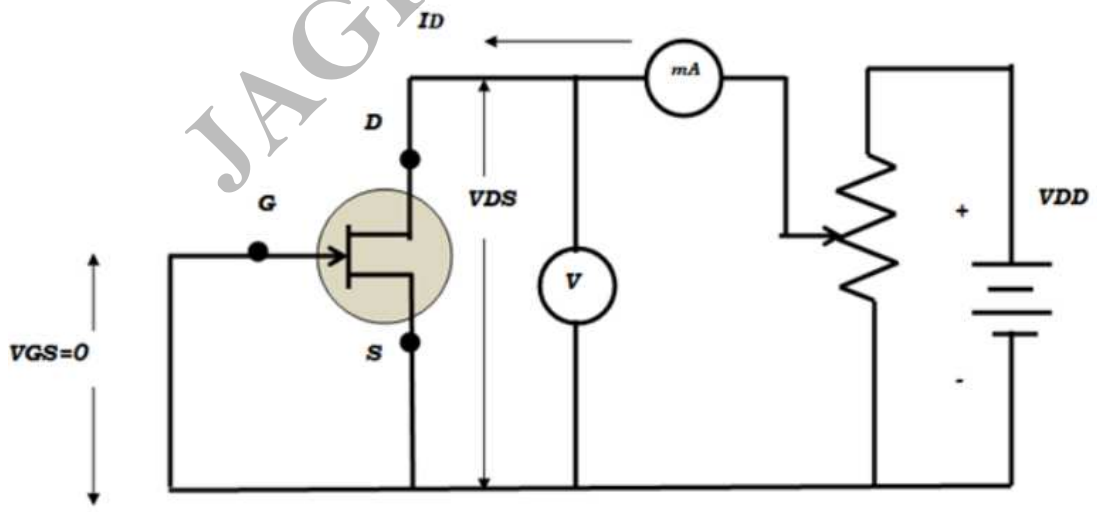
→ FETs are also used in instrumentation amplifiers and other specialized amplifier circuits.

(c) Explain Drain characteristics and Transfer characteristics of JFET in detail with all related terms as Transconductance g_m, drain resistance r_d, and amplification factor μ.

Ans :

Drain and transfer Characteristics of JFET:

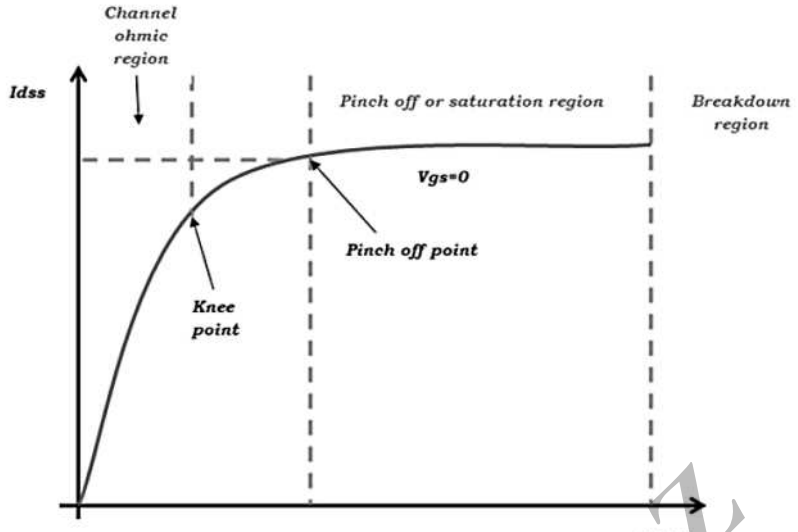
1) With no external bias:



Shorted Gate for N channel JFET to determine drain characteristics

→ Initially external voltage is not applied between gate and the source. It acts as the short circuit. The current is formed when majority charge carriers move from to source to drain. So when no external voltage is applied, there is no potential to attract the majority carries at the drain and thus initially current is zero when input voltage is zero.

→ Very small gate source voltage VGS is applied and the JFET acts as a simple resistor. The drain current ID increases gradually and reaches the knee point. Then it enters into pinch off region where the drain current ID is almost constant for the increase in the drain source voltage VDS.



Output characteristics of JFET with shorted gate

→ **Knee point:** Till this knee point the variation of drain current to the drain source voltage is linear. After this point it looks like a curve.

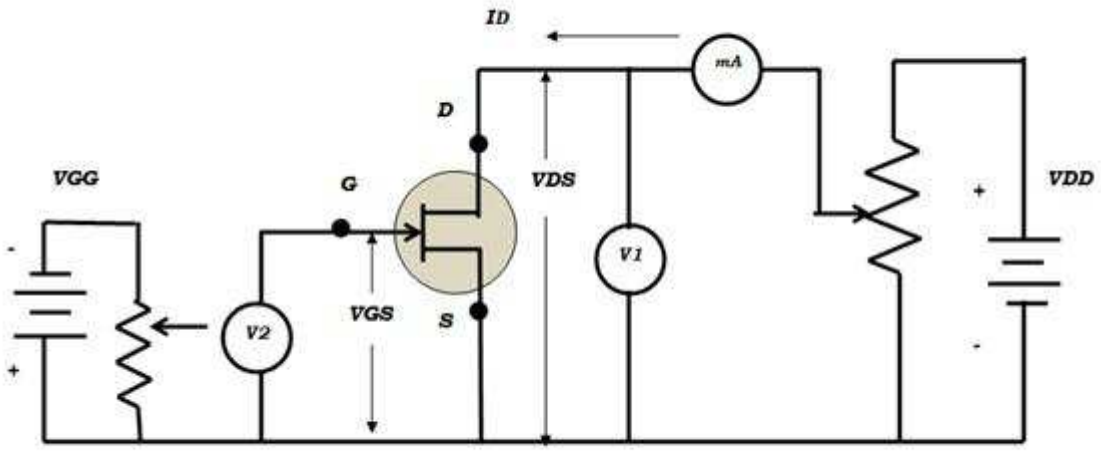
→ **Pinch off point:** Above this point the drain current does not increase even though the drain source voltage is increased.

→ **Channel Ohmic region:** The region left to the knee point is called channel Ohmic region. Because in this region JFET acts like an ordinary resistor.

→ **Pinch off or saturation region:** In this region the drain current is totally constant for the increase in the drain source voltage and it enters the saturation region.

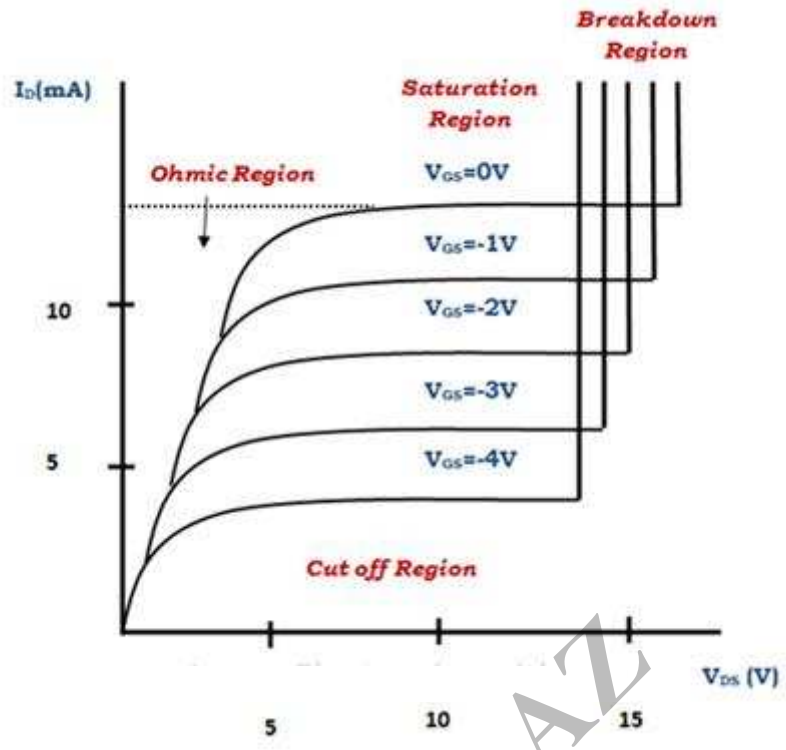
→ **Breakdown region:** when the drain and source voltage is increased further the device enters into the breakdown voltage.

2) With external bias:



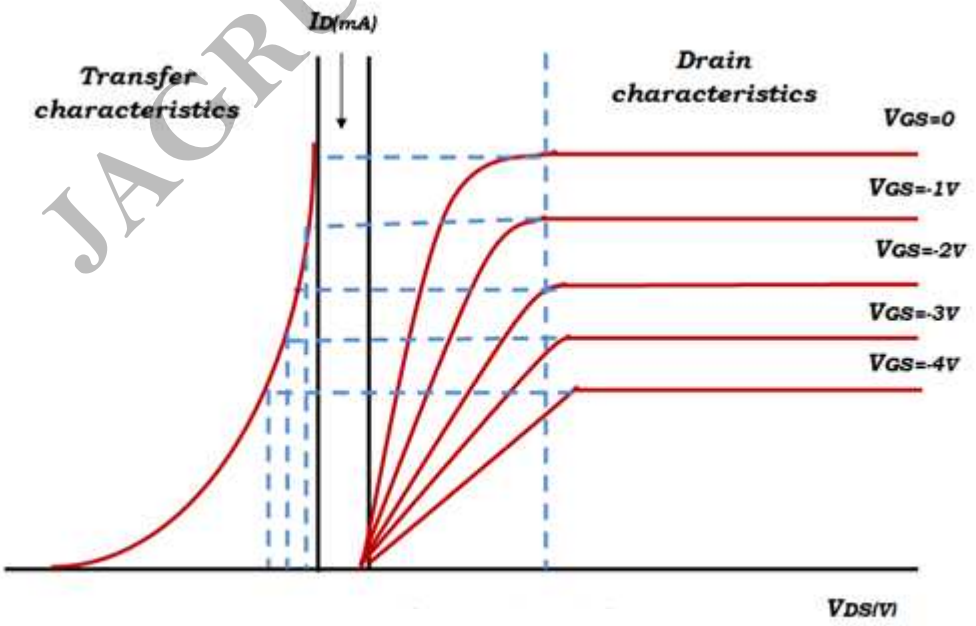
N channel JFET with external bias to determine drain characteristics

→ When the gate source voltage VGS is applied, it is reversely biased. The pinch off voltage is reached earlier when external bias is applied than when no external bias is applied.



→ The input gate source voltage VGS is increased and kept at constant and the output drain source voltage VDS is gradually increased and the output current ID is observed. Initially the current increases linearly and after it reaches knee voltage it enters the saturation region where the current is almost constant. When the applied voltage is increased further breakdown occurs and it enters into the breakdown region. In Ohmic region it acts as a resistor.

Transfer Characteristics of JFET:



JFET Transfer characteristics from Drain characteristics

→ The transfer characteristics can be determined by keeping the drain source voltage VDS constant, drain current ID is observed by changing the gate source voltage. So it is observed that when the gate source voltage VGS is increased in the negative region the drain current ID decreases.

→ During purchasing a JFET for a particular application we need to check the specifications of the device. These specifications are provided by manufacturers. The followings are the parameters used to specify a JFET and these are

→ Gate Cut Off Voltage ($V_{GS(off)}$)

→ Gate Drain Current (I_{DSS})

→ Transconductance (g_{mo})

→ Dynamic Output Resistance (r_d)

→ Amplification Factor (μ)

Transconductance

→ Transconductance is the ratio of change in drain current (δI_D) to change in the gate to source voltage (δV_{GS}) at a constant drain to source voltage (V_{DS} = Constant).

$$g_m = \frac{\delta I_D}{\delta V_{GS}} \quad at\ constant\ \ V_{DS}$$

→ This value is maximum at VGS = 0. This is denoted by g_{mo}. This maximum value (g_{mo}) is specified in a JFET data sheet. The transconductance at any other value of gate to source voltage (gm) can be determined as follows. The expression of drain current (ID) is

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

→

→ By partial differentiating the expression of drain current (I_D) in respect of gate to source voltage (V_{GS})

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{2I_{DSS}}{V_{GS(off)}}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

→ At V_{GS} = 0, the transconductance gets its maximum value and that is

$$g_{mo} = \frac{2I_{DSS}}{V_{GS(off)}}$$

→ Therefore, we can write,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$$

Dynamic Output Resistance

→ This is the ratio of change of drain to source voltage (δV_{DS}) to the change of drain current (δI_D) at a constant gate to source voltage (V_{GS} = Constant). The ratio is denoted as r_d .

$$r_d = \frac{\delta V_{DS}}{\delta I_D} \quad at\ constant\ \ V_{GS}$$

Amplification Factor

→ The amplification factor is defined as the ratio of change of drain voltage (δV_{DS}) to change of gate voltage (δV_{GS} = Constant).

$$\mu = \frac{\delta V_{DS}}{\delta V_{GS}} \quad at\ constant\ \ I_D$$

→ There is a relation between transconductance (gm) and dynamic output resistance (rd) and that can be established in the following way.

$$\mu = \frac{\delta V_{DS}}{\delta V_{GS}} = \frac{\delta V_{DS}}{\delta I_D} \times \frac{\delta I_D}{\delta V_{GS}}$$

$$\Rightarrow \mu = r_d \times g_m$$

******