Roll No. .....

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CBA-252-T

MCA First Semester

(End Semester)

Examination, Dec., 2018

COMPUTER SCIENCE AND APPLICATION

Paper - CSA-CC-122

(Digital System Design)

Time : Three Hours] [Maximum Marks : 60

Note :– Attempt all sections A, B, C. Follow the instructions given in each sections.

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Section-A

(Objective Type Questions) 10×1=10

Note :– Choose the correct option.

1. The output of a logic gate is 1 when all its inputs are at logic 0, the gate is either

   (a) a NAND or an EX-OR

   (b) an OR or EX-NOR

   (c) an AND or an EX-OR

   (d) NOR or an EX-NOR

2. How many two-input AND and OR gates are required to realize $Y = CD + EF + G$?

   (a) 2, 2

   (b) 2, 3

   (c) 3, 3

   (d) None of these

3. How is a J-K flip flop made to toggle?

   (a) J = 0, K = 0

   (b) J = 1, K = 0

   (c) J = 0, K = 1

   (d) J = 1, K = 1

4. Complement of complement of A'B + AB' is

   (a) A.B + A'.B'

   (b) (A'+B). (A+B')

   (c) A'.B + A.B'

   (d) None of these.

5. The output of full adder sum is equal to

   (a) x.y.z

   (b) x+y+z

   (c) $X \cdot Y \cdot Z$

   (d) $x \oplus y \oplus z$

6. What is the difference between a full-adder and a half-adder?

   (a) Half-adder has a carry-in

   (b) Full-adder has a carry-in

   (c) Half-adder does not have a carry-out

   (d) Full-adder does not have a carry-out

7. How many 1 of 16 decoders are required for decoding a 7-bit binary number?

   (a) 5

   (b) 6

   (c) 7

   (d) 8

8. On a master-slave flip flop, when is the master enabled?

   (a) When the gate is Low

   (b) When the gate is High

   (c) Both of the above

   (d) Neither of the above

9. ..... is used to implement virtual memory organization.

   (a) Page table

   (b) Frame table

   (c) MMU

   (d) None of these

10. The techniques which move the program blocks to or from the physical memory is called as .....

    (a) Paging

    (b) Virtual memory organisation

    (c) Overlays

    (d) Framing.

Section 'B'

(Short Answer Type Questions) 4×5=20

Note : Attempt any **four** questions.

2. Convert the following decimal numbers to the bases indicated :

   (i) 7562 to Octal

   (ii) 1938 to Hexadecimal

   (iii) 175 to binary

3. Solve the expression : $Z(A,B,C,D) = \sum (0, 1, 3, 5, 8, 9, 10, 13, 14, 15)$ using k-map.

4. Design a digital circuit that perform the four logic operation of exclusive OR, exclusive-NOR, NOR and NAND. Use two selection variable. Show the logic diagram of one typical stage.

5. Construct a 16×1 multiplexer with two 8×1 multiplexer and one 2×1 multiplexers. Show the block diagram.

6. A sequential circuit has two D flip flop A and B, two inputs x and y and one output z. The flip flop input equations and the circuit outputs are as follows :

   $D_A = x'y + xA$

   $D_B = x'B + xA$

   $z = B$

   Draw the logic diagram of the circuit.

7. A 2-way set associative cache memory uses blocks of four words? The cache can accomodate a total of 2048 words from main memory.

   The main memory size is 128K × 32 :

   (i) Formulate all pertinent information required to construct the cache memory.

   (ii) What is the size of cache memory?

Section 'C'

(Long Answer Type Questions) 3×10=30

Note :– Attempt any **three** questions.

8. State the De Morgan's theorm for three variables in both the forms and give the proof for one by the method of perfect Induction.

9. Explain using diagram how NOR and NAND gates are Universal Gate. Using De Morgan's theorem, express the function

$$F = \bar{A} + BC + \bar{B}\bar{C} + A\bar{B}$$

   with only OR and complement operations

10. Draw a 4 to 16 decoder using 2 to 4 decoders. Indicate the select lines and address lines clearly.

11. Design a 2 bit count down counter. This is a sequential circuit with two flip-flop and one out input x. When x = 0, the state of the flip-flop does not change. When x = 1, the state sequence is 11, 10, 01, 00, 11 and repeat.

12. Discuss in brief the working of an associative memory. Derive the match-logic expression for the associate memory.

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