Shrikanth Ganapathy

Summary of Research Experience

The design of embedded memories has garnered significant importance over the last decade as they now account for more than 80% of silicon real estate in modern day processors. In deep sub-micron technologies, the task of design is compounded with new challenges introduced by parametric variations of process and environmental parameters. Such variations introduce non-uniform characteristics in memory components leading to indeterministic behaviour post-manufacturing. Towards this end, our goal at ARCO has been to develop novel mechanisms at different levels of abstraction to counter the negative effects of parameter variations in embedded memories.

Sep. 2008 - Mar. 2010 **Regression-Based Energy-Delay Modelling**.
In order to optimize memory design under the effects of variability, it is important to model global figures of merit such as performance and power for early-stage estimation. Choices made at the design-stage ensure conflicting requirements from higher-levels are decoupled. A multivariate regression based modelling technique for estimating energy/delay has been proposed. The models rely extensively on circuit-level simulations for gathering empirical data. These statistical models can then help in analysing circuit optimizations like dual-V_{dd}, dual-V_{th}, standby supply voltage minimization etc The median error between generated and simulated data for delay and energy was 1.75% & 0.8%. When combined with architecture-level specifics, the models can then guide large-scale design space exploration. [DATE'10, ISLPED'10]

Apr. 2010 - May. 2011 **Post-Silicon Adaptivity for Embedded Memories**.
In order to take full-advantage of constant feature minimization, it is important to provide runtime support to complement design-level optimizations. Post-silicon adaptivity involves detecting changes in low-level circuit parameters (delay & leakage currents) post-manufacturing using on-chip canary structures and providing recovery circuits for effective repair. We have proposed a novel three-transistor one-diode (3T1D)DRAM based on-chip sensor for obtaining run-time latency/leakage profiles of memories. The profiles are stored in a lookup table that is referenced by dynamic fine-grain body-bias generator to generate an optimal body-bias that trades-off leakage power for cache latency . Our technique reduces leakage energy consumption and access latency of the cache on an average by 20% & 18% respectively. [ICCD'11]

Aug. 2011 - May. 2012 **Hybrid Techniques for Improving Yield in Caches**.
While voltage scaling can appease the negative effects of process variations to an extent, there is a maximum bound to voltage scaling beyond which reliability and yield becomes a critical design constraint. We propose a new class of hybrid techniques in improving memory yield through failure prevention and correction. Proactive read/write assist techniques like body-biasing (BB) and wordline boosting (WLB) when combined with reactive techniques like ECC and redundancy are shown to offer better quality-energy-area trade-offs when compared to their standalone configurations. Proactive techniques can help lower Vdd_{min} (improving functional margin) for significant power savings and reactive techniques ensure that the resulting large number of failures are corrected (improving functional yield). Our results in 22nm technology indicate that at scaled supply voltages, hybrid techniques can improve parametric yield by atleast 28% when considering worst-case process variations. [ISQED'13]

Sep. 2011 - May.2012 **Variation and Soft-Error Tolerant eDRAM**.
Another growing concern at low voltages is the increasing impact of soft-errors (SE) in 6T-SRAM based memories. Alternative design styles (8T/10T) while offering better robustness, result in large area-overheads reducing memory density. In light of such technology scaling issues, semiconductor companies have started embracing embedded DRAM (eDRAM) technology for on-chip memories. Memory cells designed using eDRAM technology in addition to being logic compatible, are variation tolerant and immune to noise present at low supply voltages. However, two major causes of concern are the data retention capability which is worsened by parameter variations leading to frequent data refreshes (resulting in large dynamic power overhead) and the transient reduction of stored charge increasing soft-error (SE) susceptibility. We have designed a novel 4T-DRAM cell that when compared to a similar sized eDRAM cell improves retention by 204% while incurring a minimum performance loss of 3.2%. Using a soft-error rate analysis tool we have confirmed that the sensitivity to SE is reduced by 56% in a natural working environment. [ICCD'12]

ELG 031, Station 11 – EPFL, Lausanne, 1015
☎ *+41216931027* • ✉ *shrikanth.ganapathy@epfl.ch* • *people.ac.upc.edu/sg/*

May. 2012 - Aug.2013 **CAD Tool for Memory Robustness Analysis**.
Adopting a variation-aware design paradigm requires a holistic perspective of memory-wide metrics such as yield, power and performance. However, accurate estimation of such metrics is largely dependent on circuit implementation styles, technology parameters and architecture-level specifics. In line with the requirements, we designed a prototype tool (INFORMER) that helps high-level designers estimate memory reliability metrics rapidly and accurately for a given SRAM cell design, technology, topology, working environment and memory architecture. The tool relies on accurate circuit-level simulations to capture multiple failure mechanisms (ageing, soft-errors and parametric failures) and helps couple low-level statistics with higher-level design choices. Additionally, to estimate the failure probability of rare events (low probability) where traditional monte-carlo based sampling techniques suffer, we have developed a novel algorithm that leverages SRAM transistor dimensions and importance sampling (by norm minimization) to estimate memory-wide yield accurately and rapidly. [DATE'14]

Jan. 2013 - Sep.2013 **Degradation Tolerant Cache Design**.
Negative bias temperature instability (NBTI) is a major cause of concern for chip designers because of its inherent ability to drastically reduce silicon reliability over the lifetime of the processor. Coupled with statistical variations of process parameters, it can potentially render systems dysfunctional in certain scenarios. Data caches suffer the most from such phenomenon because of the unbalanced duty cycle ratio of SRAM cells and maximum intrinsic susceptibility to process variations. We propose a modified read-modify-write (rmw) scheme to improve cache performance under degradation by frequently modifying the data stored in the cache based on access patterns. This reduces the total amount of time the memory cell is under stress by balancing the duty cycle. The highly transient nature of the data stored in L1 data cache aides this process of recovery when using our proposed write back scheme. Our technique is self-contained, in that the changing bit patterns are hidden from program execution wherein data modifications are always effected after a *write* access and before a *read* access. Our experiments conducted using SPEC2006 and PhysicsBench workloads show that on-average, the cache failure probability is reduced by 22%, 33% and 36% after two, four and eight years of processor usage respectively. Further, delay due to additional logic is small enough to not incur any system-wide performance penalty. [ICCD'14]

Publications

DATE'10 Circuit Propagation Delay Modeling using Multivariate Regression-Based Modeling, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of Design, Automation & Test in Europe Conference*, 2010 (Paper)

ISLPED'10 MODEST: A Model For Energy Estimation under Spatio - Temporal Variability, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Symposium on Low Power Electronic Design*, 2010 (Paper)

ICCD'11 Dynamic Fine-Grain Body Biasing of Caches with Latency & Leakage 3T1D-DRAM based Monitors **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Conference on Computer Design*, 2011 (Paper)

ICCD'12 A Novel Variation-Tolerant 4T-DRAM Cell with Enhanced Soft-Error Tolerance, **S.Ganapathy**, R.Canal, D.Alexandrescu, E.Costenaro, A.González & A.Rubio, *In Proceedings of International Conference on Computer Design*, 2012 (Paper)

ISQED'13 Effectiveness of Hybrid Recovery Techniques on Parametric Failures, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Symposium on Quality Electronic Design*, 2013 (Paper)

ISCA'13 An Energy-Efficient and Scalable eDRAM-Based Register File Architecture for GPGPU, N.Jing, Y.Shen, Y.Lu, **S.Ganapathy**, Z.Mao, M.Guo, R.Canal, & X.Liang, *In Proceedings of the International Symposium on Computer Architecture*, 2013 (Paper)

DATE'14 INFORMER: An Integrated Framework for Early-Stage Memory Robustness Analysis, **S.Ganapathy**, R.Canal, D.Alexandrescu, E.Costenaro, A.González & A.Rubio, *In Proceedings of the Design, Automation & Test in Europe Conference*, 2014 (Paper)

ICCD'14 iRMW: A Low-Cost Technique to Reduce NBTI-Dependent Parametric Failures in L1 Caches, **S.Ganapathy**, R.Canal, A.González & A.Rubio *In Proceedings of International Conference on Computer Design*, 2014

ELG 031, Station 11 – EPFL, Lausanne, 1015
☎ *+41216931027* • ✉ *shrikanth.ganapathy@epfl.ch* • *people.ac.upc.edu/sg/*