ELG 031, Station 11
EPFL, Lausanne, 1015
☎ +41216931027
✉ shrikanth.ganapathy@epfl.ch
people.ac.upc.edu/sg/

Shrikanth Ganapathy

Research Interests

My research is at the intersection of systems design and fault-tolerance. I am interested in exploiting novel techniques across different levels of design abstraction to enable development of ultra low-power resilient microprocessors for use in next generation computing platforms.

Education

2009 - 2014 **Doctor of Philosophy**, *Universitat Politècnica de Catalunya*, Spain.
Advisors: Ramon Canal, Antonio González (Intel) & Antonio Rubio

2008 - 2009 **Master of Science**, *Universitat Politècnica de Catalunya*, Spain.
Advisors: Ramon Canal, Antonio González (Intel) & Antonio Rubio

2004 - 2008 **Bachelor Of Engineering**, *Anna University*, India.
Advisor: Nagarajan Venkateswaran

Research Experience

May 2014 - Present **Post-Doctoral Researcher**, *École Polytechnique Fédérale de Lausanne*, Switzerland.

Sep. 2008 - April 2014 **Graduate Student**, *Universitat Politècnica de Catalunya*, Spain.
Ph.D. thesis: Reliability in the face of variability in nanometer caches
Master thesis: Effect of spatio-temporal variations on memory systems

Sep. 2011 - Dec. 2011 **Research Intern**, *iRoC Technologies*, France.
Project: Hardening of 3T1D-DRAM against neutron induced soft-errors

Honours & Awards

2012 - 2013 **Intel Doctoral Student Honor Programme**, *Awarded annually to outstanding PhD students in select EU and Swiss universities performing leading-edge innovation in their respective fields of research.*

2010 - 2013 **FI-DGR**, *Recipient of the FI-DGR grant awarded by the Generalitat de Catalunya for the entire course of PhD studies.*

2009, 2011 **Highest Grades**, *Master thesis (9.5/10) and doctoral thesis proposal (10/10).*

2011 ***Recerca Jove***, *Featured in this initiative of UPC for outstanding research in the area of information communication and technology (ICT).*

Publications

Journal

VLSI'12 Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells, N.Aymerich, **S.Ganapathy**, A.Rubio, R.Canal & A.González, *Appears in Integration, the VLSI Journal*, 2012 (Paper)

Conferences/Workshops

ICCD'14 iRMW: A Low-Cost Technique to Reduce NBTI-Dependent Parametric Failures in L1 Data Caches, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of the International Conference on Computer Design*, 2014

DATE'14 INFORMER: An Integrated Framework for Early-Stage Memory Robustness Analysis, **S.Ganapathy**, R.Canal, D.Alexandrescu, E.Costenaro, A.González & A.Rubio, *In Proceedings of the Design, Automation & Test in Europe Conference*, 2014 (Paper)

ISCA'13 An Energy-Efficient and Scalable eDRAM-Based Register File Architecture for GPGPU, N.Jing, Y.Shen, Y.Lu, **S.Ganapathy**, Z.Mao, M.Guo, R.Canal, & X.Liang, *In Proceedings of the International Symposium on Computer Architecture*, 2013 (Paper)

ISQED'13 Effectiveness of Hybrid Recovery Techniques on Parametric Failures, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Symposium on Quality Electronic Design*, 2013 (Paper)

ICCD'12 A Novel Variation-Tolerant 4T-DRAM Cell with Enhanced Soft-Error Tolerance, **S.Ganapathy**, R.Canal, D.Alexandrescu, E.Costenaro, A.González & A.Rubio, *In Proceedings of International Conference on Computer Design*, 2012 (Paper)

ICCD'11 Dynamic Fine-Grain Body Biasing of Caches with Latency & Leakage 3T1D-DRAM based Monitors **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Conference on Computer Design*, 2011 (Paper)

GLSVLSI'11 Impact of Positive Bias Temperature Instability (PBTI) on 3T1D-DRAM Cells, N.Aymerich, **S.Ganapathy**, A.Rubio, R.Canal & A.González, *In Proceedings of Great Lakes Symposium on VLSI*, 2011 (Paper)

ISLPED'10 MODEST: A Model For Energy Estimation under Spatio - Temporal Variability, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of International Symposium on Low Power Electronic Design*, 2010 (Paper)

DATE'10 Circuit Propagation Delay Modeling using Multivariate Regression-Based Modeling, **S.Ganapathy**, R.Canal, A.González & A.Rubio, *In Proceedings of Design, Automation & Test in Europe Conference*, 2010 (Paper)

DELTA'08 Design for Testability of Functional Cores in High Performance Node Architectures, N.Venkateswaran, K.Chandrasekar & **S.Ganapathy**, *In Proceedings of Electronic Design, Testing & Application*, 2008 (Paper)

IPDPS'08 On the Concept of Simultaneous Execution of Multiple Applications on Hierarchically Based Cluster and the Silicon Operating System, N.Venkateswaran, **S.Ganapathy** *et.al.*, *Large Scale Parallel Processing Workshop held in Conjunction with International Parallel and Distributed Processing Symposium*, 2008 (Paper)

Technical Proficiency

Programming	C, Matlab	Scripting	Perl, Python, Shell
Design & Simulation	HSPICE, Spectre, iRoC TFIT, ModelSim, Xilinx	Statistical Tools	CVXOPT, pyOpt, R, XLStat
Operating Systems	Unix, Linux		

References

Will be provided upon request