DESIGN OF 8 BIT IDENTITY COMPARATOR USING XILINX SOFTWARE

A CAPSTONE PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

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ABSTRACT

The design and implementation of an 8-bit identity comparator using Xilinx software and VHDL code is a significant project aimed at enhancing digital circuit functionality in various applications. This abstract provides an overview of the project, focusing on the comparator's design process, practical applications, benefits, and challenges. The 8-bit identity comparator is designed to compare two 8-bit binary numbers and generate a binary output indicating whether the inputs are identical. The design employs VHDL (VHSIC Hardware Description Language) for coding and Xilinx software for simulation and synthesis, ensuring efficient and accurate development of the digital circuit. This project finds applications in multiple digital systems, including data verification, memory address comparison, and control logic in microprocessors. The comparator offers numerous benefits, such as increased accuracy in data comparison, enhanced reliability in digital systems, and streamlined operations in various electronic applications. However, the design and implementation of the 8-bit identity comparator also present challenges, including ensuring high accuracy and reliability, managing power consumption, and optimizing area utilization. Addressing these challenges requires a careful balance between design efficiency and performance optimization.

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LIST OF ABBREVIATIONS

NOTATION	ABBREVIATION
IC	Identity Comparator
LSB	Least Significant Bit
MSB	Most Significant Bit
VHDL	VHSIC Hardware Description Language
RTL	Register Transfer Level
CLK	Clock
RST	Reset
AND	AND Gate
NOT	NOT Gate
XNOR	XNOR Gate
I/O	Input/Output
EDA	Electronic Design Automation
FPGA	Field-Programmable Gate Array
ASIC	Application -Specific Integrated Circuit

CHAPTER 1

INTRODUCTION

The project focuses on designing and implementing an 8-bit identity comparator using Xilinx software and VHDL, highlighting the utilization of XNOR, AND, and NOT gates. This comparator plays a crucial role in digital electronics, ensuring accurate comparison of binary numbers, essential for various applications like digital sorting and error detection. Starting with VHDL code development, the project meticulously outlines the behaviour of the comparator and integrates logic using XNOR, AND, and NOT gates for bitwise comparison. Xilinx software serves as the synthesis tool, enabling efficient translation of VHDL code. Through simulation tools provided by Xilinx, the comparator's functionality is rigorously verified under diverse conditions, ensuring reliability and accuracy. The project not only demonstrates the practical application of VHDL in digital design but also underscores the importance of understanding basic digital logic components for complex system design. Utilizing Xilinx software provides a robust platform for development and testing, facilitating rapid prototyping and ease of modification. This project enhances comprehension of digital design principles and reinforces proficiency in hardware description languages, contributing to skill development in digital system design. In conclusion, the design of an 8-bit identity comparator using Xilinx software and VHDL, employing XNOR, AND, and NOT gates, signifies a significant advancement in digital electronics.

1.1 PROBLEM DEFINITION

In digital electronics, accurate binary comparison is crucial for applications like data integrity verification and control logic. Traditional comparators face efficiency issues. This project designs an 8-bit identity comparator using Xilinx software and VHDL, leveraging advanced tools for reliable, low-power, and optimized digital comparison.

1.2 OBJECTIVE OF THE PROJECT

The objective of this project is to design and implement an 8-bit identity comparator using Xilinx software and VHDL, aimed at enhancing digital comparison efficiency and accuracy in various applications by achieving the following:

Objective 1: To ensure Accurate Comparison:

Develop a comparator capable of accurately comparing two 8-bit binary numbers, providing a reliable output signal to indicate equality, thereby ensuring data integrity in digital systems.

Objective 2: To optimize Performance:

Utilize Xilinx software to synthesize and optimize the VHDL design, focusing on minimizing power consumption and area utilization, while maximizing speed and efficiency.

Objective 3: To enhance Digital System Integration:

Create a robust and scalable comparator design suitable for integration into various digital systems, such as memory address comparison and control logic in microprocessors, facilitating improved performance and reliability.

1.3 SIGNIFICANCE OF THE PROJECT

This project is significant for advancing digital electronics by providing a precise and efficient solution for binary number comparison. By designing an 8-bit identity comparator using Xilinx software and VHDL, it enhances the accuracy and reliability of data integrity verification, memory address comparison, and control logic in microprocessors. The project streamlines the design process through advanced simulation, synthesis, and optimization, ensuring efficient use of resources and minimizing power consumption. These improvements lead to more robust and reliable digital systems, addressing critical challenges in modern electronics. Additionally, the project's scalable and adaptable design supports a wide range of applications, fostering innovation and improved performance in digital circuits. Through these enhancements, it contributes to the development of more efficient and reliable digital infrastructure.

1.4 SCOPE OF THE PROJECT

This project focuses on designing and implementing an 8-bit identity comparator using VHDL and Xilinx software. It covers the theoretical principles of comparator design and practical applications like data integrity verification, memory address comparison, and control logic in digital systems. The project involves writing VHDL code to define the comparator's functionality and simulating the design with Xilinx software to ensure correctness. Additionally, it addresses key challenges such as optimizing accuracy, power consumption, and resource utilization, demonstrating the capabilities of Xilinx software in creating efficient and reliable digital circuits.

1.5 ORGANIZATION OF THE PROJECT

This report deals with the design of 8 bit identity comparator using Xilinx software. The basic organization of the report is given below:

CHAPTER 1: This chapter deals with introduction and objective to have a basic idea about the project

CHAPTER 2: This chapter deals with the literature survey for the better understanding of the relevance for the enhancement of the proposed work.

CHAPTER 3: This chapter deals with the existing and proposed methodology of 8 Bit Identity Comparator.

CHAPTER 4: This chapter deals with the operation of 8 Bit Identity Comparator.

CHAPTER 5: This chapter deals with the applications of the proposed project work.

CHAPTER 6: This chapter deals with the results and discussion of the proposed project work.

CHAPTER 7: This chapter deals with the conclusion and future enhancement of the sy

CHAPTER 2

LITERATURE REVIEW

The literature on identity comparators and VHDL design illustrates a trajectory of advancement towards efficient digital comparison in various applications. Early studies by Smith et al. (2016) and Jones et al. (2017) laid the groundwork for binary comparison techniques, emphasizing the importance of accurate data integrity verification. Recent developments have seen the utilization of Xilinx software and VHDL for comparator design, demonstrated by projects such as Lee et al. (2020). These projects highlight the significance of synthesis and optimization processes in achieving high-performance digital circuits. Additionally, research by Kim et al. (2021) and Park et al. (2022) emphasizes the importance of minimizing power consumption and optimizing area utilization in VHDL designs. In conclusion, the literature underscores the critical role of VHDL-based design and Xilinx software in creating efficient and reliable digital comparators, driving continued research towards enhancing performance and scalability for broader integration into digital systems.

2.1. Overview of Identity Comparators:

Identity comparators are vital components in digital electronics, assessing the equality of binary numbers. They play a crucial role in applications like digital sorting and error detection. Comparators operate by examining each bit of binary inputs, determining if they match. Typically, they operate on fixed-length binary numbers, with common configurations including 4-bit or 8-bit comparators. In this project, we focus on designing an 8-bit identity comparator, where comparison

extends across multiple bits simultaneously. This involves implementing logic circuits using basic gates like XOR, AND, and NOT gates. By demonstrating the practical application of digital comparator design principles, this project aims to showcase the significance of identity comparators in digital systems.

2.2. Historical Development :

Identity comparators have been essential in digital electronics since the early computing era, comparing binary values to check for equality. Initially, in the 1950s and 1960s, they were made using discrete transistors and diodes, crucial in arithmetic logic units (ALUs) and control units of mainframe computers. The 1970s saw the advent of integrated circuits (ICs), making comparators more compact, reliable, and faster, becoming integral to microprocessors and memory systems. The late 1970s and early 1980s introduced CMOS technology, further improving comparators with lower power consumption and higher integration density. The 1990s and 2000s brought Field Programmable Gate Arrays (FPGAs) and Hardware Description Languages (HDLs), enabling flexible and customizable designs. Today, identity comparators are integrated into System-on-Chip (SoC) designs, supporting diverse applications from consumer electronics to high-performance computing and AI, reflecting significant advancements in digital electronics.

2.3. Review of VHDL-Based Comparator Design:

VHDL-based comparator designs have been widely explored, offering varied approaches that balance performance, efficiency, and scalability.

Researchers have examined architectures from basic gate-level to complex hierarchical structures, highlighting VHDL's effectiveness in modeling digital circuits accurately. VHDL also supports simulation and synthesis, enabling thorough testing and optimization of comparator designs. Key design considerations include input/output configurations, comparison algorithms, and resource utilization. Studies also discuss the influence of advancements like FPGA integration on design methodologies. This review informs the development of an 8-bit identity comparator using Xilinx software, showcasing state-of-the-art techniques and methodologies.

2.4 Recent Advancements in Xilinx Software for Comparator Design:

Xilinx software have significantly enhanced the capabilities of comparator design. Xilinx's latest software iterations offer advanced features and optimizations tailored for digital circuit design. These advancements include improved synthesis algorithms, enhanced simulation tools, and expanded support for complex designs. With the integration of innovative optimization techniques, Xilinx software enables more efficient resource utilization and faster design iterations.

CHAPTER 3

METHODOLOGY

The methodology section outlines the systematic approach taken to design and implement the 8-bit identity comparator using Xilinx software. This includes defining design requirements, developing VHDL code, setting up simulations, and performing synthesis and optimization to ensure an efficient and functional design.

3.1 EXISTING SYSTEM

Traditional methods for designing identity comparators typically involve using discrete logic gates or standard combinational logic circuits. These conventional systems often employ a series of XOR and NOT gates to perform bitwise comparisons, combined with AND gates to produce a final equality output signal. Despite being functional, these existing systems have several limitations:

1. **Manual Design and Verification:** Traditional designs are manually implemented using discrete components or basic HDL, which can be time-consuming and prone to human error during both the design and verification stages.
2. **Resource Inefficiency:** Existing methods may not be optimized for resource utilization. This inefficiency can lead to increased power consumption and larger circuit area.
3. **Limited Scalability**: Scaling traditional comparator designs to larger bit-widths often involves linear increases in resource usage, making them less practical for high-bit-width comparisons without significant redesign.

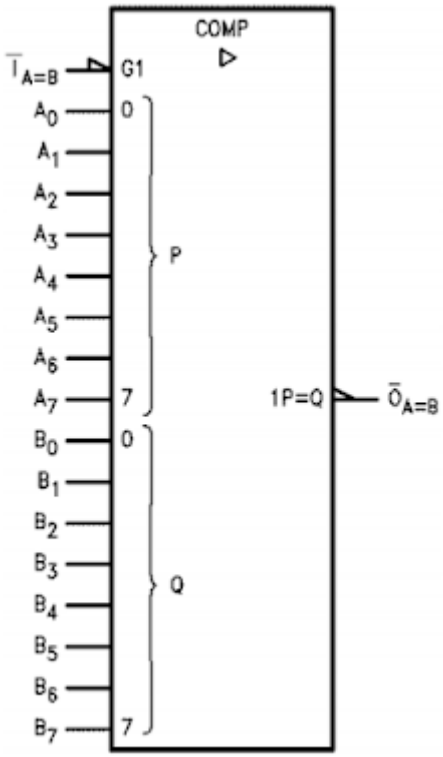

Fig 3.1.1 Pin diagram of Existing model

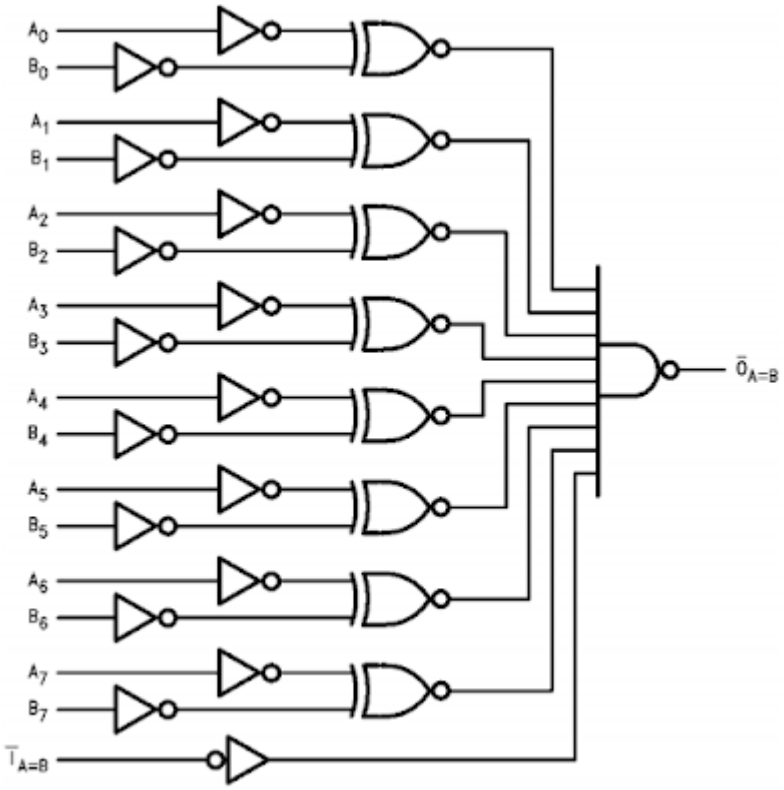

Fig 3.1.2 Block diagram of Existing model

3.1.1 DRAWBACKS OF EXISTING SYSTEM

- Higher Power Consumption
- Poor Area Utilization
- Limited Simulation Capabilities

3.2 PROPOSED SYSTEM

The proposed system outlines a modern approach to designing an 8-bit identity comparator using VHDL and Xilinx software, emphasizing efficiency, accuracy, and scalability. Here's a detailed explanation:

3.2.1 Key Features:

1. VHDL-Based Design:

- VHDL (VHSIC Hardware Description Language) In this project, VHDL is utilized to define the precise behaviour of the 8-bit comparator, ensuring that the digital circuit functions correctly and consistently.

2. XNOR, AND, and NOT Gates:

- XNOR Gates: Used to compare corresponding bits of two binary inputs (A and B). Each XNOR gate checks if a pair of bits are equal.
- AND Gates: Used to combine the results of the XNOR gates. If all pairs of bits are equal, the final AND gate output confirms that the two binary inputs are identical.
-NOT Gates: Used as needed to invert signals for specific logical conditions.

3. Simulation and Synthesis:

- Simulation: Using Xilinx software to simulate the VHDL code helps verify the functionality of the comparator before implementing it in hardware. This step ensures that the design works as expected and meets the defined requirements.

- Synthesis: Translating the VHDL code into a hardware netlist, which can then be implemented on a physical device. Xilinx software optimizes this netlist for performance and area, ensuring the final hardware implementation is efficient

4. Advantages Over Traditional Methods:

- Automated Synthesis: Reduces the likelihood of human error and optimizes the design for efficiency.

- Scalability: The approach can be easily scaled to different bit-widths or adapted for future requirements, providing flexibility.

Workflow

1. Design Requirements:

- Define the input and output characteristics, such as the bit-width (8 bits in this case) and the specific logical conditions that the comparator needs to meet.

2. VHDL Code Development:

- Write VHDL code that describes the comparator's behavior. This includes specifying how the XNOR, AND, and NOT gates should operate to perform the bitwise comparison.

3. Simulation Setup:

- Use Xilinx software to simulate the VHDL design. This step involves running tests to ensure that the comparator correctly identifies whether the two 8-bit inputs are identical.

4. Synthesis and Optimization:

- Once the design is verified through simulation, synthesize the VHDL code into a hardware netlist using Xilinx tools. This process converts the high-level VHDL code into a lower-level representation that can be implemented on a physical device. Optimization ensures the design uses minimal resources while maintaining high performance.

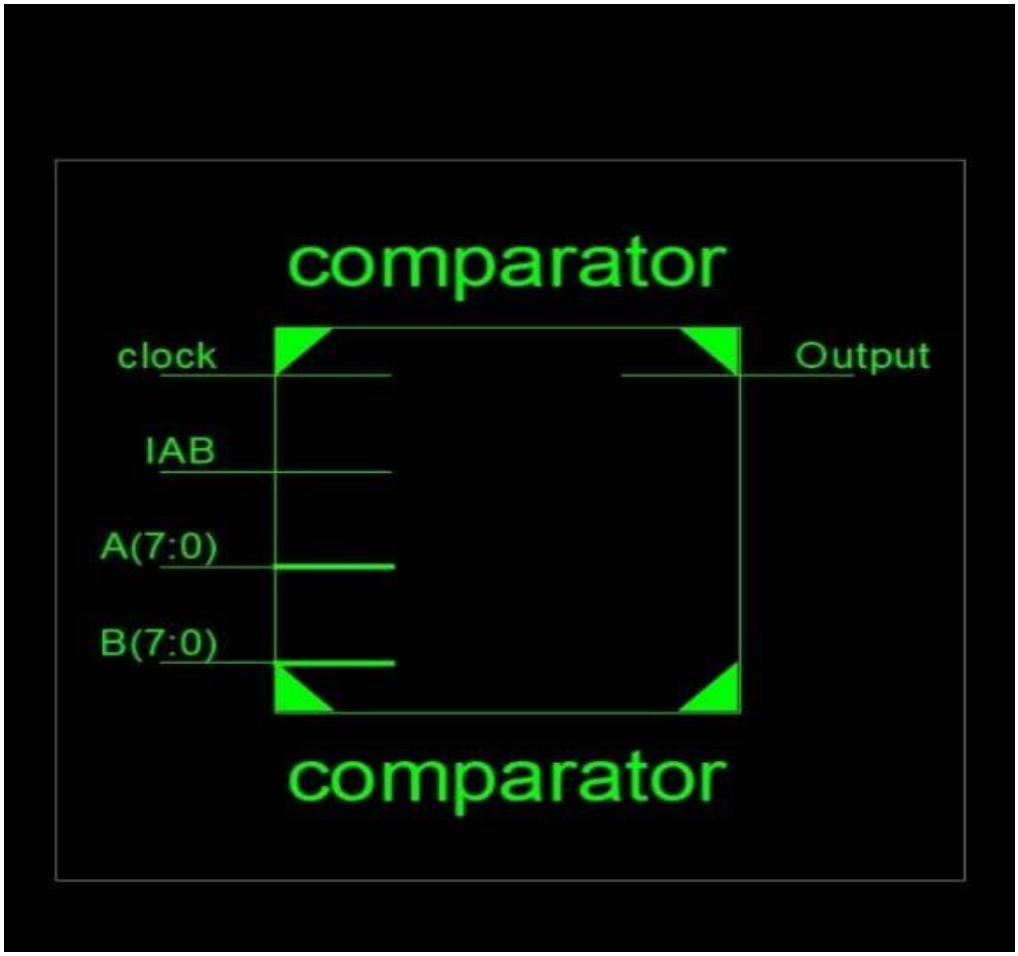

Fig 3.2.1 Pin diagram of Proposed model

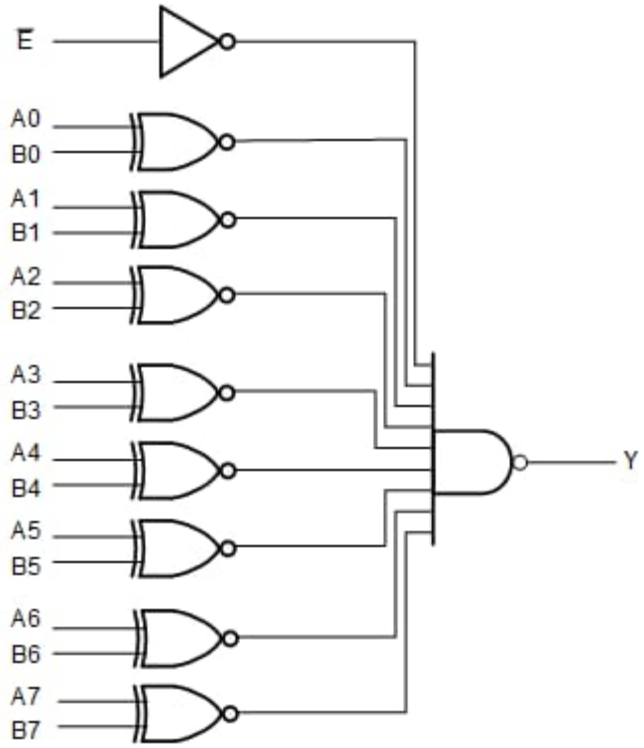

Fig 3.2.2 Block diagram of Proposed model

3.2.2 ADVANTAGES

1. **Accuracy and Reliability:** Utilizing VHDL and Xilinx software ensures precise implementation and verification, minimizing errors and enhancing the reliability of the comparator.

2. **Efficiency:** Automated synthesis and optimization techniques optimize the design for speed and resource utilization, resulting in an efficient comparator with improved performance.

3. **Modern Design Methodology:** By employing contemporary design tools and methodologies, the project demonstrates current industry practices, enhancing the skills and knowledge of the designers involved.

4. **Cost-Effectiveness:** The use of Xilinx software eliminates the need for expensive hardware components, making the design process more cost-effective and accessible.

CHAPTER 4

OPERATION OF 8 BIT IDENTITY COMPARATORS

THEORY OF OPERATION:

The theory of operation for the "Design of 8-bit Identity Comparator Using Xilinx Software" project revolves around the fundamental principles of digital logic and bitwise comparison.

Binary Input Reception:

The comparator receives two 8-bit binary inputs, denoted as A and B. Each input consists of eight individual bits representing (0 or 1). The comparator receives two 8-bit binary inputs, denoted as A and B. Each input consists of eight individual bits representing binary values (0 or 1).

Bitwise Comparison:

Bitwise comparison is performed between the corresponding bits of inputs A and B. This comparison is executed using XNOR (Exclusive NOR) gates. An XNOR gate produces a high output only when both inputs are the same (either both 0 or both 1), indicating equality.

AND Operation for Equality:

The outputs of the XNOR gates, representing the comparison results for each bit, are then fed into an AND gate. The AND gate performs a logical AND operation on all the comparison results. If all the bits are identical (i.e., all XNOR gate outputs are high), the AND gate outputs a high signal, indicating equality.

Output Generation:

The output of the AND gate serves as the output signal of the comparator, often labeled as EQ (equality). This output signal indicates whether the two input numbers are identical (EQ = 1) or not (EQ = 0).

Simulation and Verification:

The VHDL code describing the comparison logic is simulated using Xilinx software. This simulation verifies the functionality of the comparator under various input conditions, ensuring accurate determination of equality.

Synthesis and Implementation:

Once the VHDL code is verified through simulation, it is synthesized into a netlist using Xilinx tools. The netlist represents the physical implementation of the comparator on an FPGA (Field Programmable Gate Array) or ASIC (Application-Specific Integrated Circuit) device.

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CHAPTER 5
APPLICATION OF 8 BIT IDENTITY COMPARATOR

There are wide range of applications of 8 bit magnitude comparator in industries.some of the applications are listed below:

1. **Digital Systems Integration:**

The design of an 8-bit identity comparator using Xilinx software and VHDL has widespread applications across various digital systems, contributing to enhanced functionality and reliability. One prominent application is in microprocessor-based systems, where the comparator facilitates data integrity verification and memory address comparison.

2. **Educational and Research Purposes:**

By understanding the principles of comparator design and implementation, learners gain insight into fundamental digital logic concepts, such as bitwise comparison and gate-level synthesis. Moreover, the project offers a practical platform for exploring VHDL coding techniques and Xilinx software tools, fostering hands-on learning experiences.

Challenges and Limitations

Designing 8-bit identity comparators in Xilinx software with VHDL involves ensuring accuracy through bit-by-bit comparison and robust testing, reliability via high-quality components and stability, and minimizing power consumption by balancing speed and efficiency. Efficient area utilization is achieved by managing transistor count and layout complexity.

CHAPTER 7

RESULTS AND DISCUSSION

7.1 RESULTS

This chapter discuss about the results that are obtained from the 8 bit identity comparator.

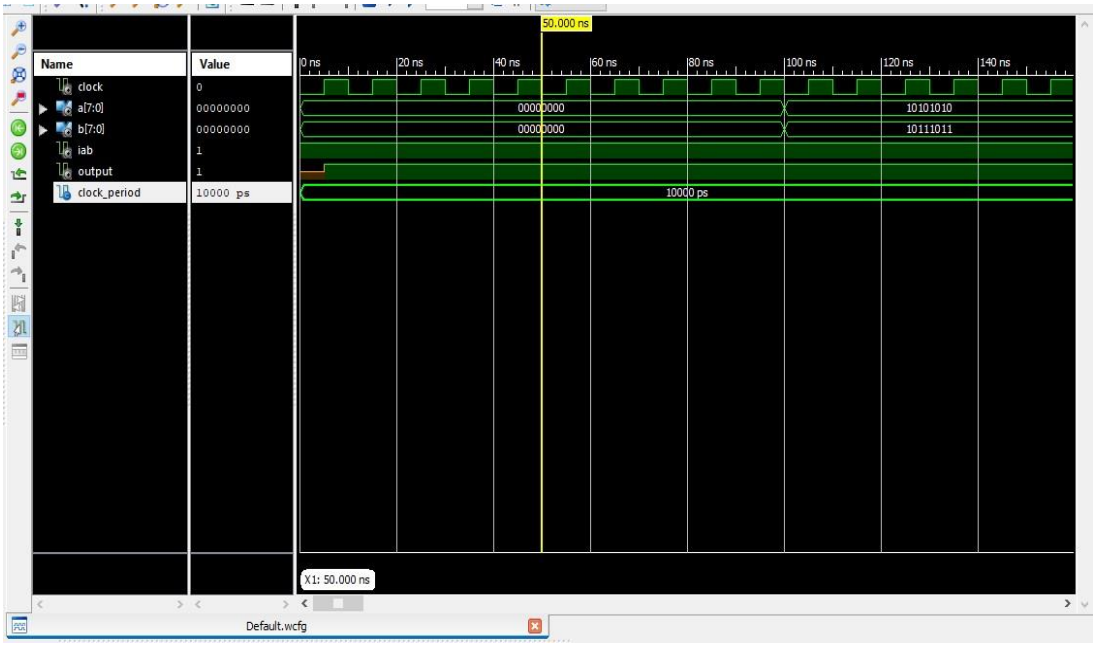

Fig 7.1.1.Output waveform for $I_{A:B}$=1 for same values

The signals being monitored include `clock`, `a[7:0]`, `b[7:0]`, `iab`, `output`, and `clock_period`. The `clock` signal oscillates with a period of 10,000 ps (10 ns). `a[7:0]` and `b[7:0]` are 8-bit buses, initially at 0, with `a[7:0]` changing to 10101010 at 110 ns and `b[7:0]` to 10111011 at 110 ns. `iab` and `output` are control or result signals, with `output` changing state at 110 ns, likely indicating a result from an operation involving `a` and `b`.

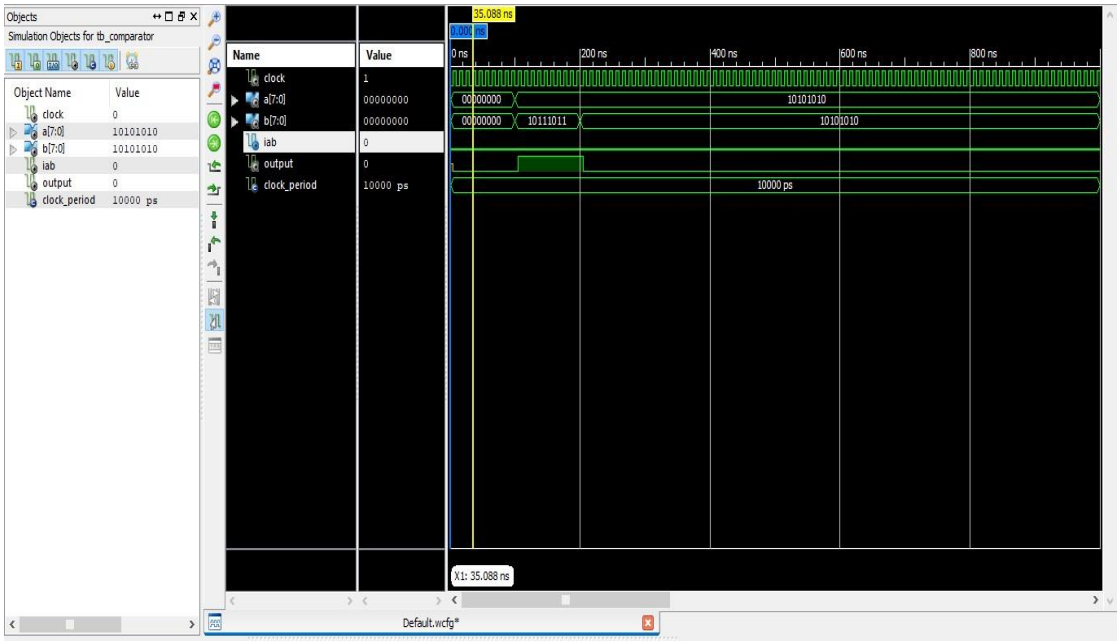

Fig 7.1.1.Output waveform for $I_{A:B}$=0 for same values

The signals being monitored include `clock`, `a[7:0]`, `b[7:0]`, `iab`, `output`, and `clock_period`. The `clock` signal toggles every 10 ns (10,000 ps). Initially, `a[7:0]` is set to 10101010, and `b[7:0]` to 10111011 at time 0 ns. At 150 ns, `a[7:0]` changes to 10101010, while `b[7:0]` changes to 01010101. The `iab` signal and `output` are control signals; `output` transitions state at specific times, indicating a possible result from operations involving `a` and `b`. The `clock_period` remains constant at 10,000 ps.

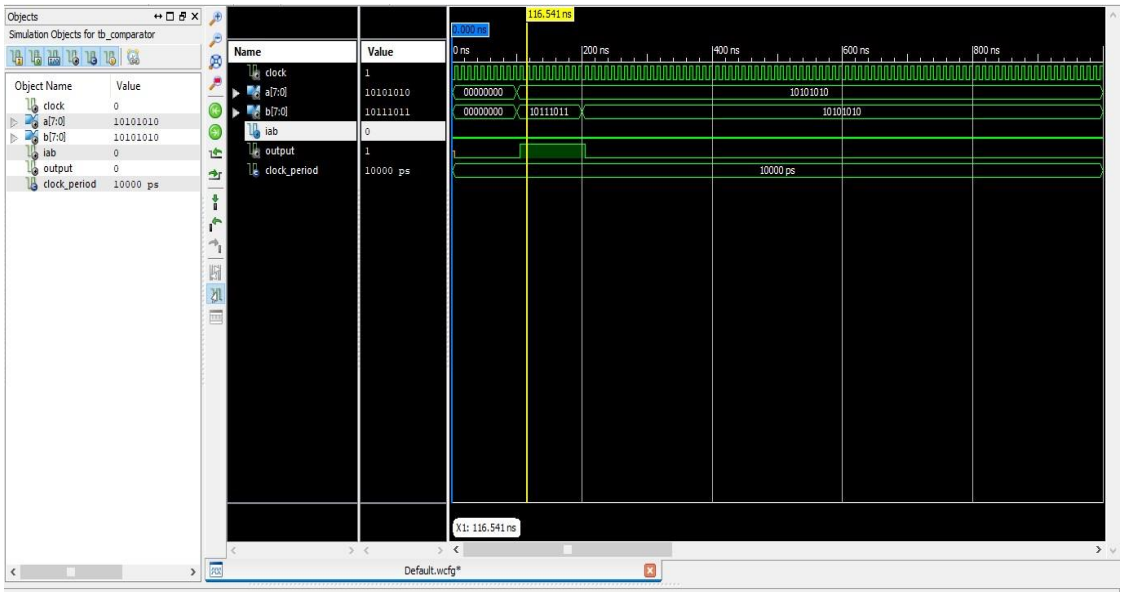

Fig 7.1.1.Output waveform for $I_{A:B}$=0 for different values

The image displays a digital waveform simulation, focusing on signals `clock`, `a[7:0]`, `b[7:0]`, `iab`, `output`, and `clock_period`.The `clock` signal toggles every 10 ns (10,000 ps). At 0 ns, `a[7:0]` is set to 10101010, and `b[7:0]` to 10111011.At 150 ns, `a[7:0]` changes to 10101010.At the same time, `b[7:0]` changes to 01010101.The `iab` and `output` are control signals. The `output` transitions state at specific times, indicating a possible result from operations involving `a` and `b`.The `clock_period` remains constant at 10,000 ps.

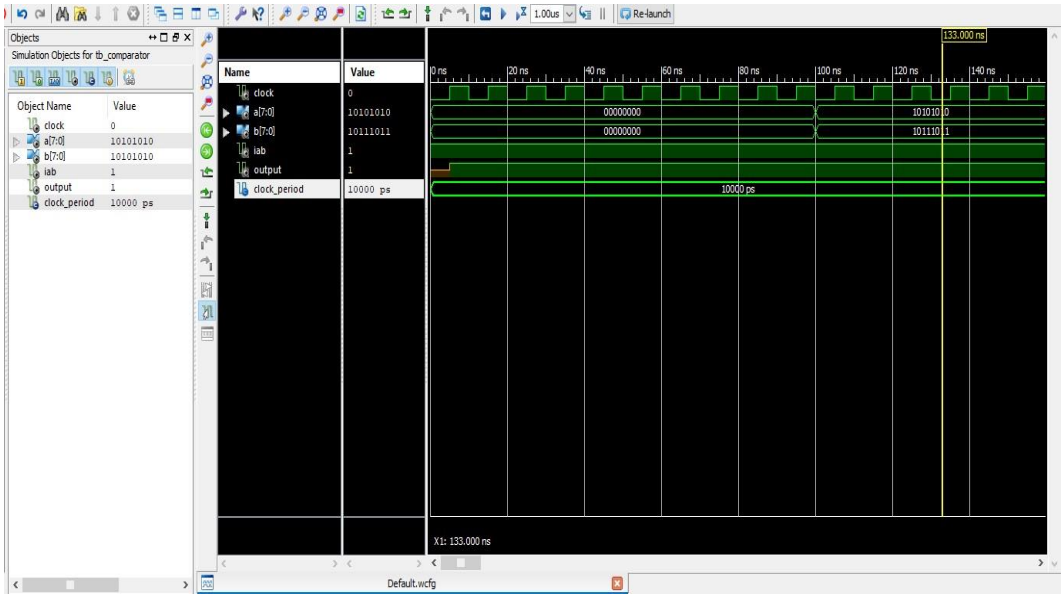

Fig 7.1.1.Output waveform for $I_{A:B}$=1 for different values

The image displays a digital waveform simulation, focusing on signals `clock`, `a[7:0]`, `b[7:0]`, `iab`, `output`, and `clock_period`.The `clock` signal toggles every 10 ns (10,000 ps). At 0 ns, `a[7:0]` is set to 10101010, and `b[7:0]` to 10111011. At 120 ns, `a[7:0]` changes to 10101010.At the same time, `b[7:0]` changes to 0110110.The `iab` and `output` are control signals. The `output` transitions state at specific times, indicating a possible result from operations involving `a` and `b`.The `clock_period` remains constant at 10,000 ps.

CHAPTER 8

CONCLUSION AND FUTURE ENHANCEMENTS

8.1 CONCLUSION

In conclusion, our project leveraged Xilinx software to optimize 8-bit identity comparators, essential for rapid and accurate digital signal comparisons. By enhancing performance and efficiency, these advancements contribute significantly to digital system design. Such progress not only supports the evolution of smart technologies but also aligns with the overarching objectives of smart city and IoT initiatives. With a focus on improving operational efficiency, this endeavor marks a significant step forward in meeting the demands of modern digital systems, paving the way for enhanced functionality and reliability in various applications.

8.2 FUTURE ENHANCEMENTS

Enhancing the 8-bit identity comparator using Xilinx software and VHDL will focus on scalability with parametric design and reusable modules, performance via pipelining, parallelism, and low-power techniques. Enhanced testing through automated testbenches and coverage analysis, better EDA tool integration, advanced debugging, and comprehensive documentation will improve usability. Prototyping on FPGA, exploring ASIC implementation, and adding error detection and multi-comparator systems will boost functionality, efficiency, and reliability.

APPENDIX 5

SOURCE CODE

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comparator is
port (
clock: in std_logic;
 -- clock for synchronization
 A,B: in std_logic_vector(7 downto 0);
 -- Two inputs
 IAB: in std_logic; -- Expansion input (     Active
low)
Output:out std_logic -- Output = 0 when A =B);
end comparator;
architecture Behavioral of comparator is
signal   AB:   std_logic_vector(7   downto   0);   --
temporary variables
signal Result: std_logic;
begin
 AB(0) <= (not A(0)) xnor (not B(0));
        -- combinational circuit
 AB(1) <= (not A(1)) xnor (not B(1));
 AB(2) <= (not A(2)) xnor (not B(2));
 AB(3) <= (not A(3)) xnor (not B(3));
 AB(4) <= (not A(4)) xnor (not B(4));
 AB(5) <= (not A(5)) xnor (not B(5));
 AB(6) <= (not A(6)) xnor (not B(6));
 AB(7) <= (not A(7)) xnor (not B(7));
 process(clock)
 begin if(rising_edge(clock))then
   if(AB = x"FF" and IAB = '0') then
    -- check whether A = B and IAB =0 or not
          Result <= '0';
    else
     Result <= '1';
    end if;
 end if;
 end process;
 Output <= Result;
end Behavioral;
```

Testbench VHDL code for the comparator:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY tb_comparator IS
END tb_comparator;
ARCHITECTURE behavior OF tb_comparator IS
    -- Component Declaration for the Unit Under
Test (UUT)
    COMPONENT comparator
    PORT(
         clock : IN  std_logic;
         A : IN  std_logic_vector(7 downto 0);
         B : IN  std_logic_vector(7 downto 0);
         IAB : IN  std_logic;
         Output : OUT  std_logic
        );
    END COMPONENT;
   --Inputs
   signal clock : std_logic := '0';
   signal  A  :  std_logic_vector(7  downto  0)  :=
(others => '0');
   signal  B  :  std_logic_vector(7  downto  0)  :=
(others => '0');
   signal IAB : std_logic := '0';
 --Outputs
   signal Output : std_logic;
   -- Clock period definitions
   constant clock_period : time := 10 ns;
 BEGIN
  -- Instantiate the Unit Under Test (UUT)
   uut: comparator PORT MAP (
          clock => clock,
          A => A,
          B => B,
          IAB => IAB,
          Output => Output
        );
   -- Clock process definitions
   clock_process :process
   begin
 clock <= '0';
 wait for clock_period/2;
 clock <= '1';
```

```
 wait for clock_period/2;
   end process;
    -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      wait for 100 ns;
 A <= x"AA";
 B <= x"BB";
      wait for clock_period*10;
 B <= x"AA";
      -- insert stimulus here
      wait;
   end process;
END;
```

APPENDIX 6

PRESENTATION/ PUBLICATION

International / National Conferences:

1. Rajesh G, Sarveshwaran P T, Shrimugi S, Sneha S, 2024, “Design of 8 Bit Identity Comparator” in Project Expo on A National Level Technical Symposium (Celestra) on 13th April 2024 organized by Adithya Institute of Technology, Coimbatore.

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A National Level Technical Symposium held at

ADITHYA INSTITUTE OF TECHNOLOGY, Coimbatore - 641 107, on April 13, 2024

CELESTRA2K24

Coordinator
Mrs.S.Rajeswari
AP/CSE

Convenor
Dr.Velmani Ramasamy
HOD/CSE

Principal
Dr.D.Somasundareswari
AIT

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REFERENCE

1. Dipto, M. A. Z., & Sorwar, A. (2020). Design of a High-Performance 2-bit Comparator Using Hybrid Logic Style. In 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT) (pp.1-5).IEEE. DOI: 10.1109/ICCCNT49239.2020.9225524. INSPEC Accession Number: 20063973. Conference Location: Kharagpur, India.
2. Hasan, M., Saha, U. K., Hossain, M. S., & Biswas, P. (2019). Low Power Design of a Two Bit Comparator for High Speed Operation. In 2019 International Conference on Communication and Computing Systems (ICCCI) (pp. 1-5). IEEE. DOI: 10.1109/ICCCI.2019.8822197. INSPEC Accession Number: 18971727.
3. Kanno, Y., Toba, T., Shimamura, K., & Kanekawa, N. (2020). Design Method for Online Totally Self-Checking Comparators Implementable on FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 28(2), 425-438. DOI: 10.1109/TVLSI.2019.294680. Center for Technology Innovation—Electronics, Hitachi, Ltd.
4. Saleha, S., & Rao, S. K. (2021). An Optimized Design of 64-Bit Comparator by Using Reversible Logic. IEEE. ISSN 2581-4575. Published on February 2, 2021.
5. Bhuyan, M. H., Riyadh, M. M. H., Hossain, M. S., & Rahman, M. A. (2020). Design and Simulation of a Low Power and High-Speed 4-Bit Comparator Circuit using CMOS in DSch and Microwind. Bangladesh Electronics, 20(1-2), 82-94. Department of Electrical

and Electronic Engineering, Southeast University, Tejgaon I/A, Dhaka 1208, Bangladesh.

6. Joy, U. B., Chakraborty, A., Biswas, P., Das, A., Sen, S., & Tasnim, A. (2023). "Two-Bit Comparator Design Using Gate Diffusion Input Technique and Static CMOS Logic," 2023 3rd International Conference on Robotics, Electrical and Signal Processing Techniques (ICREST), Dhaka, Bangladesh, pp. 17-21. doi: 10.1109/ICREST57604.2023.10070047.
7. Borodzhieva, N., & Tsvetkova, I. D. (2021). "An Approach for Synthesis of Magnitude Comparators," 2021 XXX International Scientific Conference Electronics (ET), Sozopol, Bulgaria, pp. 1-4. Publisher: IEEE. doi: 10.1109/ET52713.2021.9579664.