I2C MASTER SLAVE COMMUNICATION USING VERILOG

SAKSHI K V

SAMRUDDHI S KAGE

SANJANA VEERANGOUDAR

SHRINIDHI ANGADI

UNDER THE GUIDANCE OF

PROF. SUNIL MATHAD

Communication Protocols

	UART	**CAN**	**USB**	**SPI**	**I2C**
PROS	Well known simple	Secure fast	Secure ,fast, plug and play	Fast, low cost, universally accepted, large portfolio	Simple, plug and play, cost efficient, universally accepted
CONS	Limited, functionally, point to point	Complex, limited portfolio, automotive oriented	Powerful master required, no plug and play software, extra drivers required	No plug and play hardware, no fixed standard	Limited no. of components due to capacitance effect

Comparison of different protocols [3]

I2C COMMUNICATION PROTOCOL

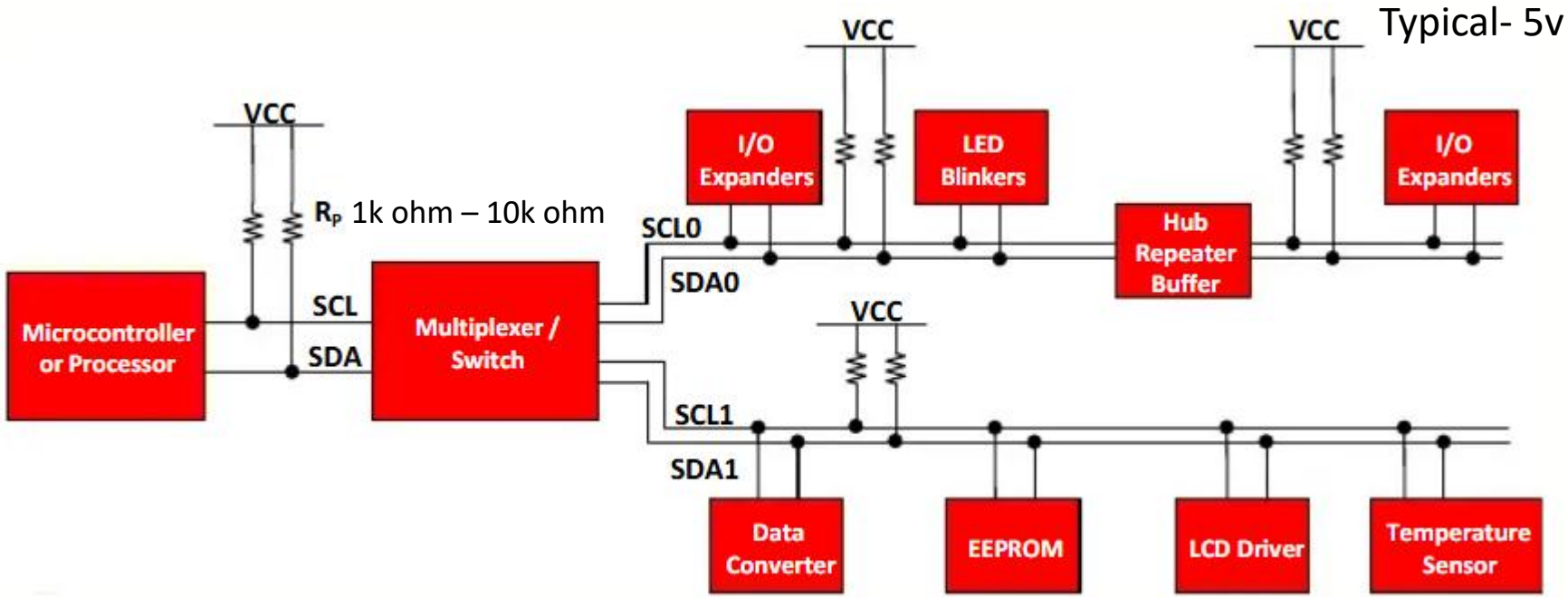
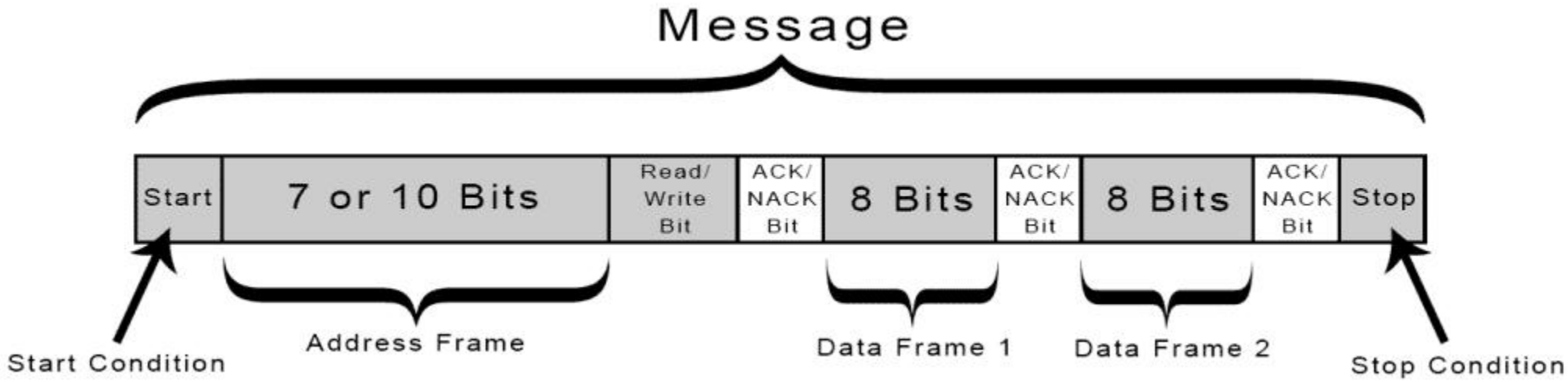


Figure 1. Example I^2C Bus [5]

Normally speed of device is 400kbps

Byte Diagram



How I2C Works [6]

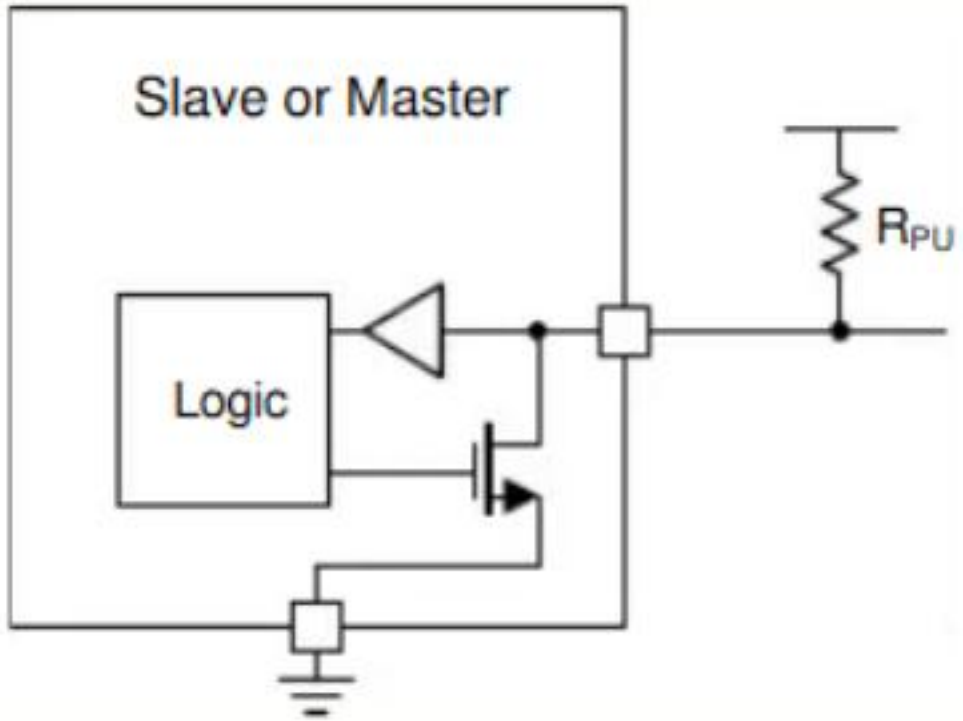


Figure 2. Basic Internal Structure of SDA/SCL Line [5]

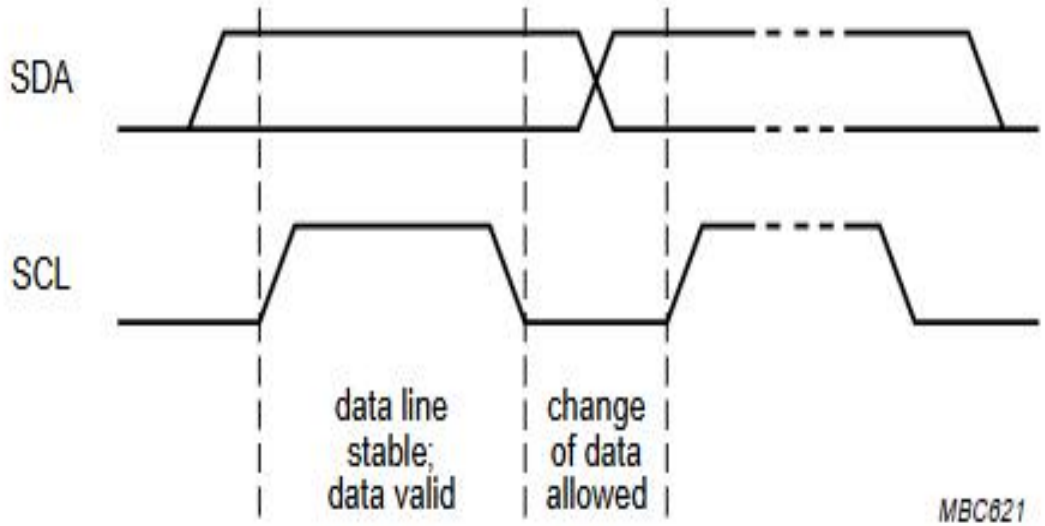
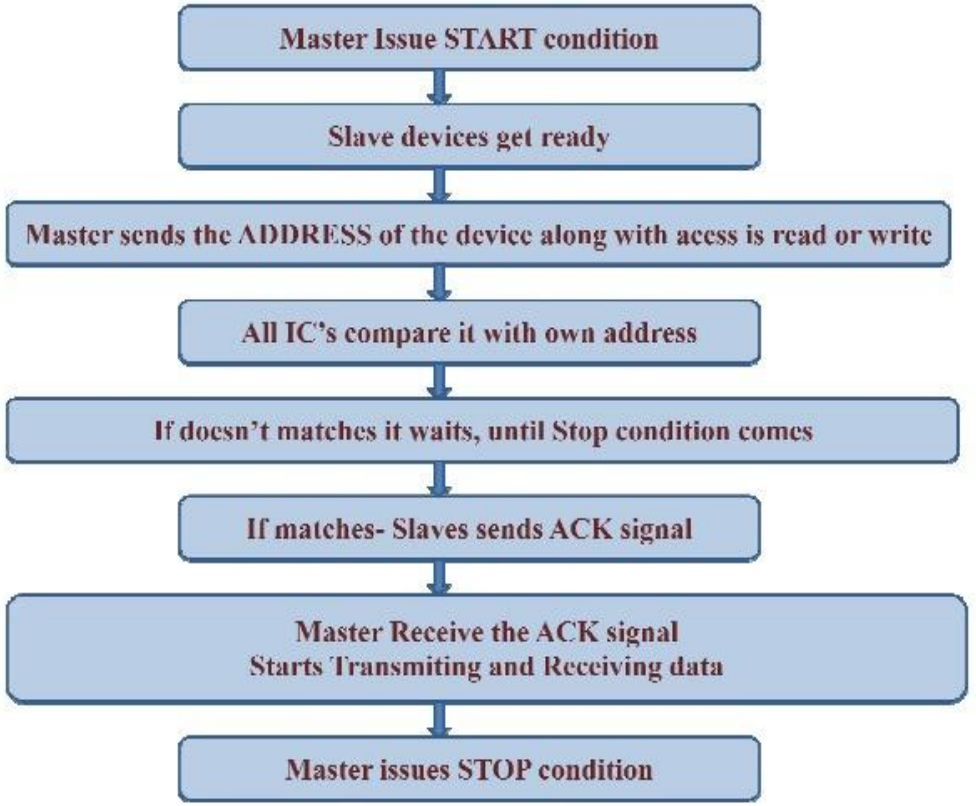


Fig.4 Bit transfer on the I^2C-bus. [5]

Process Algorithm

4.6. Process Algorithm: [3]



I^2C Arbitration and Clock Synchronization

Introduction to I^2C Arbitration.

Arbitration Mechanism.

- Arbitration occurs on the SDA line while the *SCL line* is high.
- Each master monitors the SDA line and compares the sent and actual data on the bus.
- If a master sends a HIGH but reads a LOW, it loses arbitration and stops transmitting.
- Arbitration continues bit-by-bit until one master remains (the winner).
- This process ensures no data loss because the winning master continues its transmission seamlessly.

Clock Synchronization.

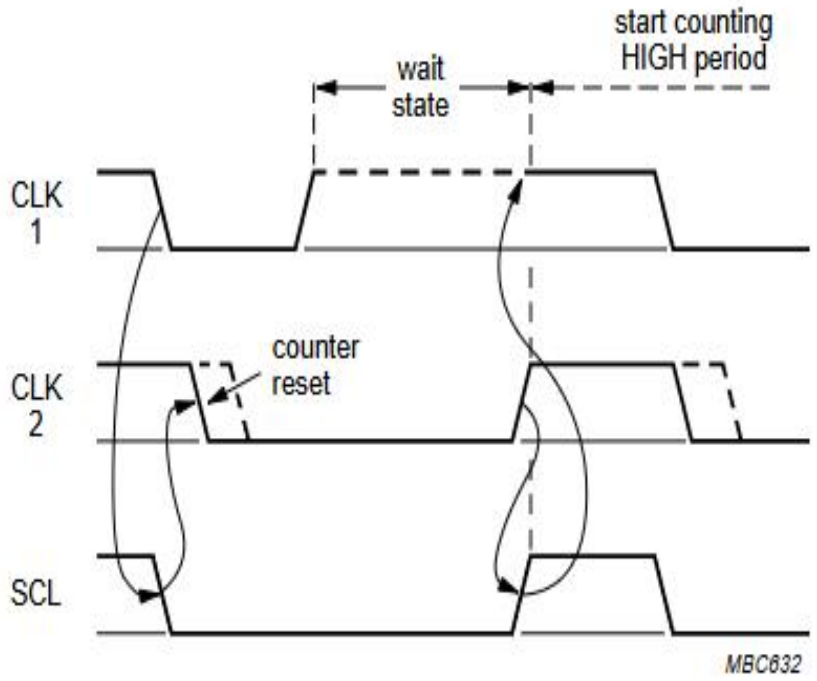
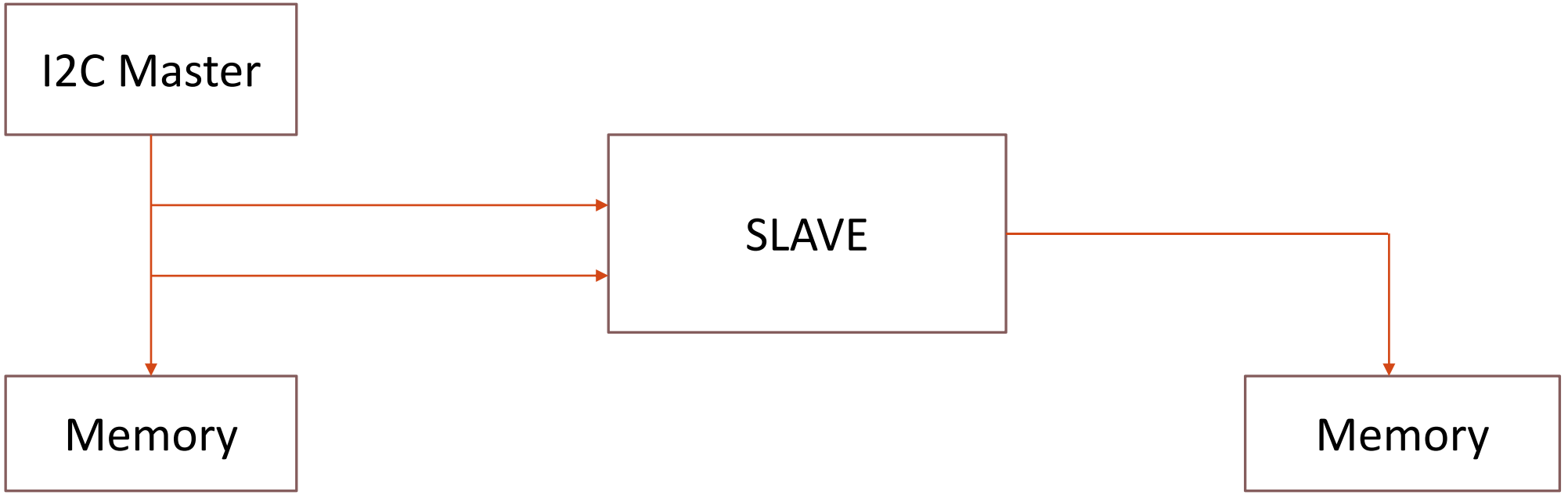


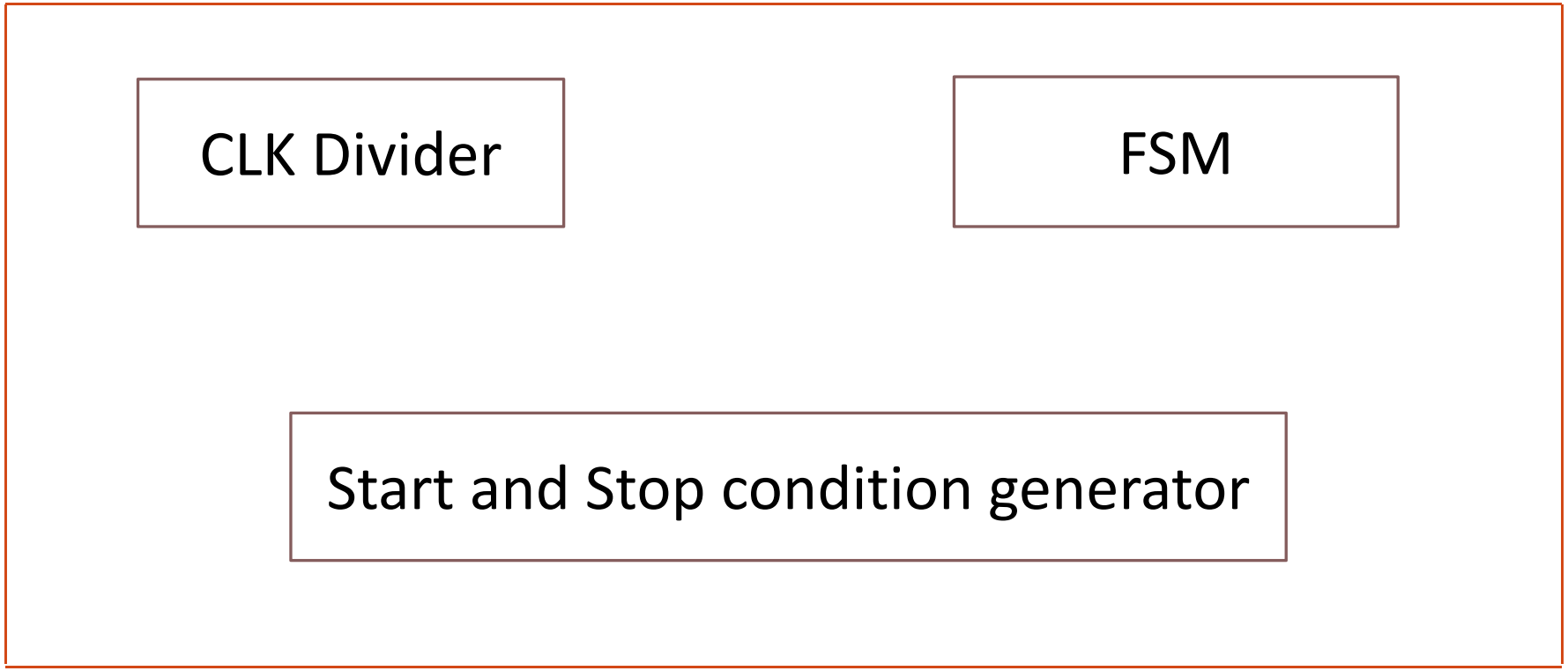
Fig.8 Clock synchronization during the arbitration procedure. [3]

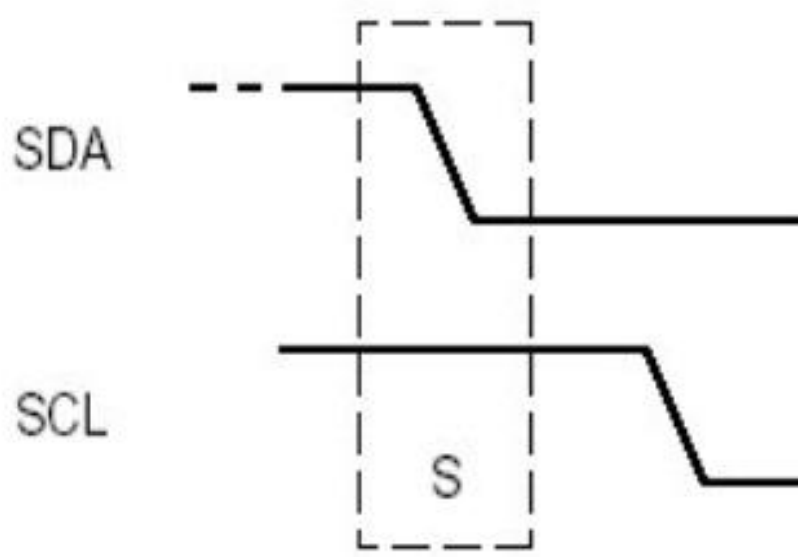
I2C Using Verilog

Block Diagram:

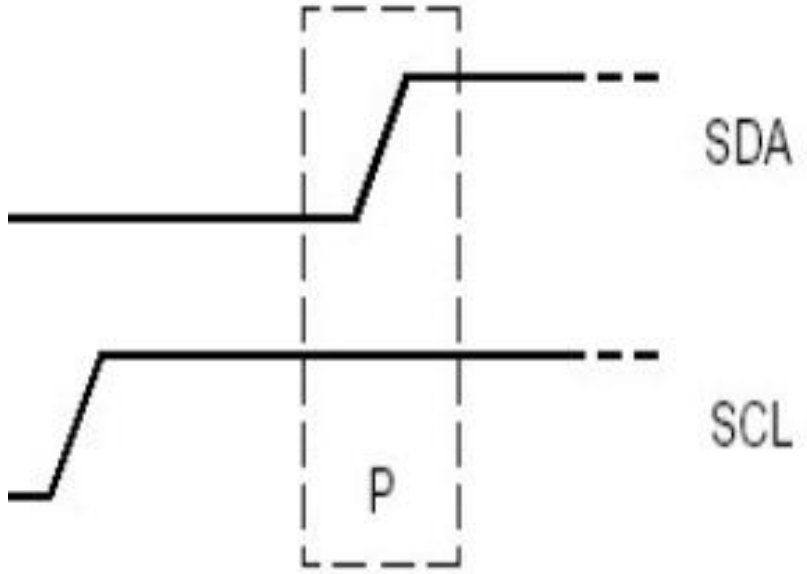


Master:





START condition



STOP condition

State Diagram:

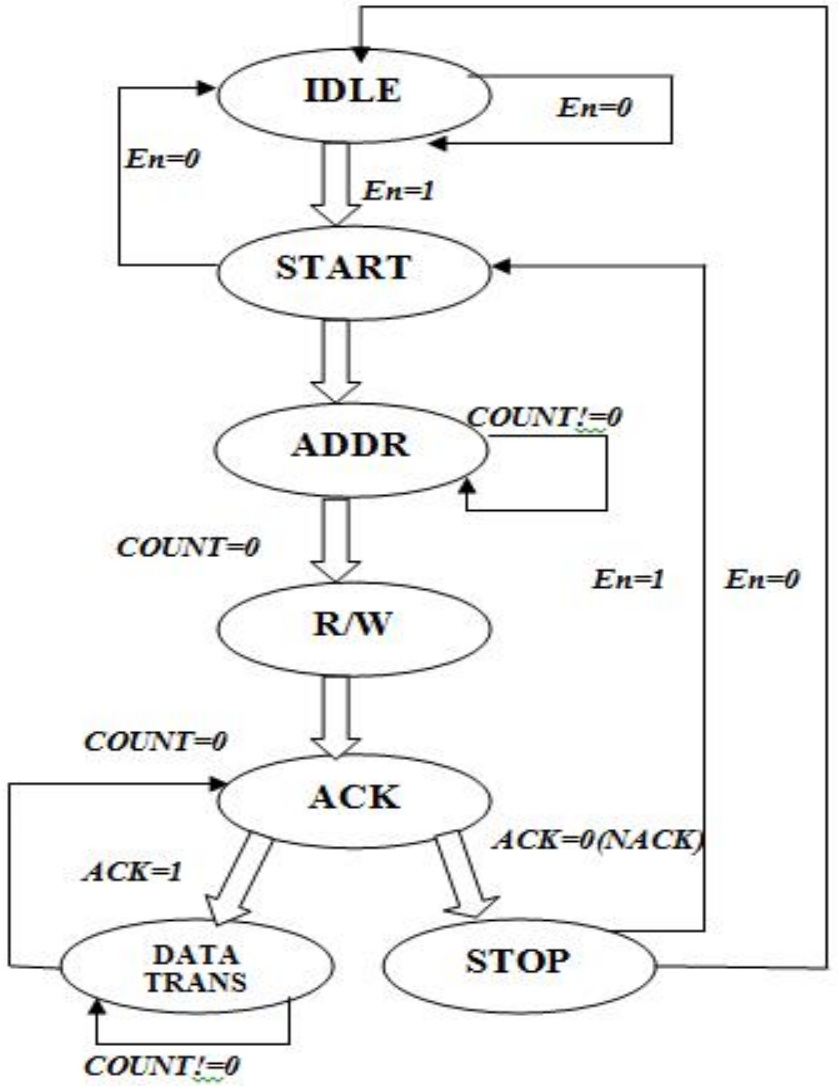
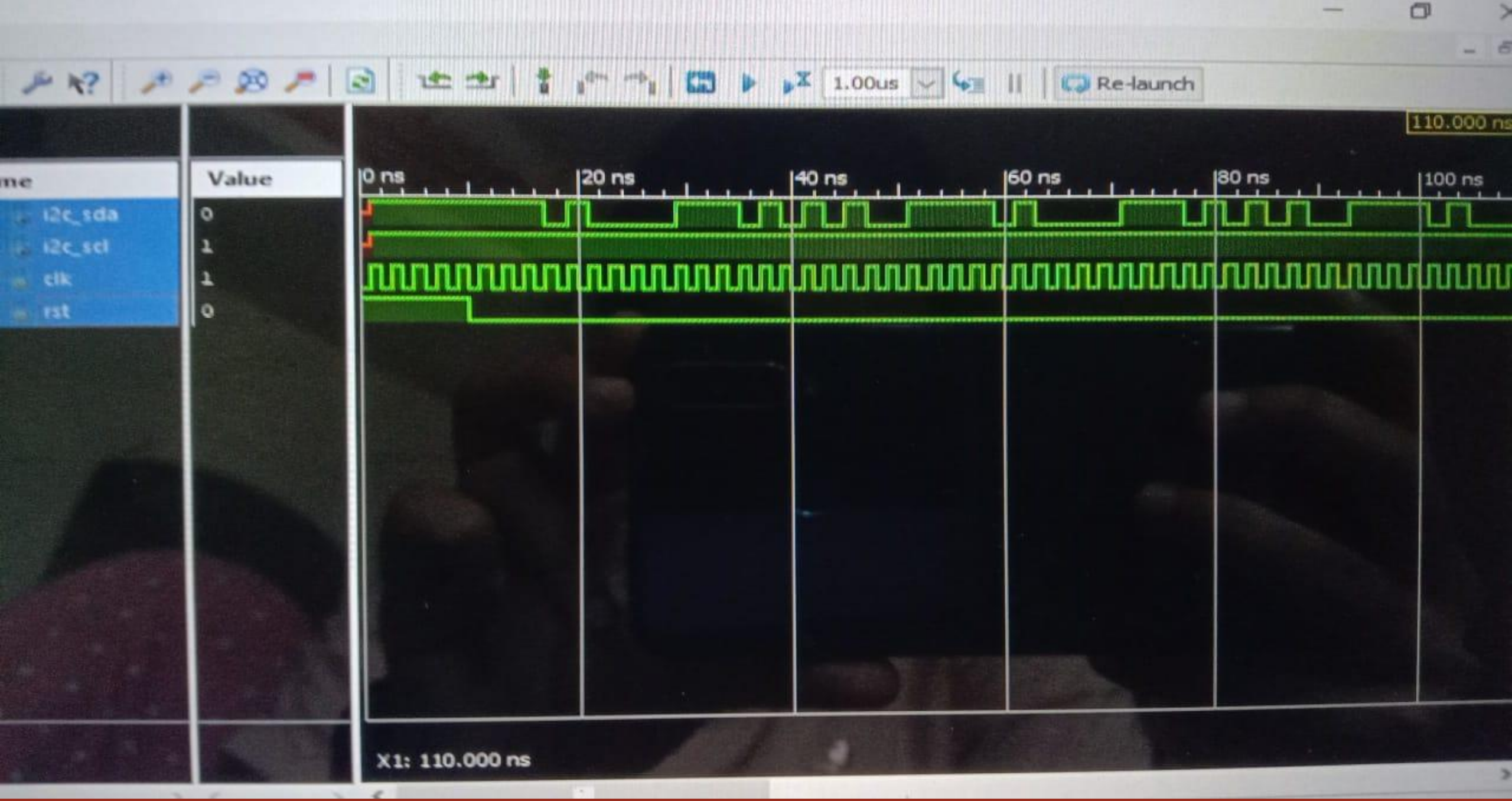
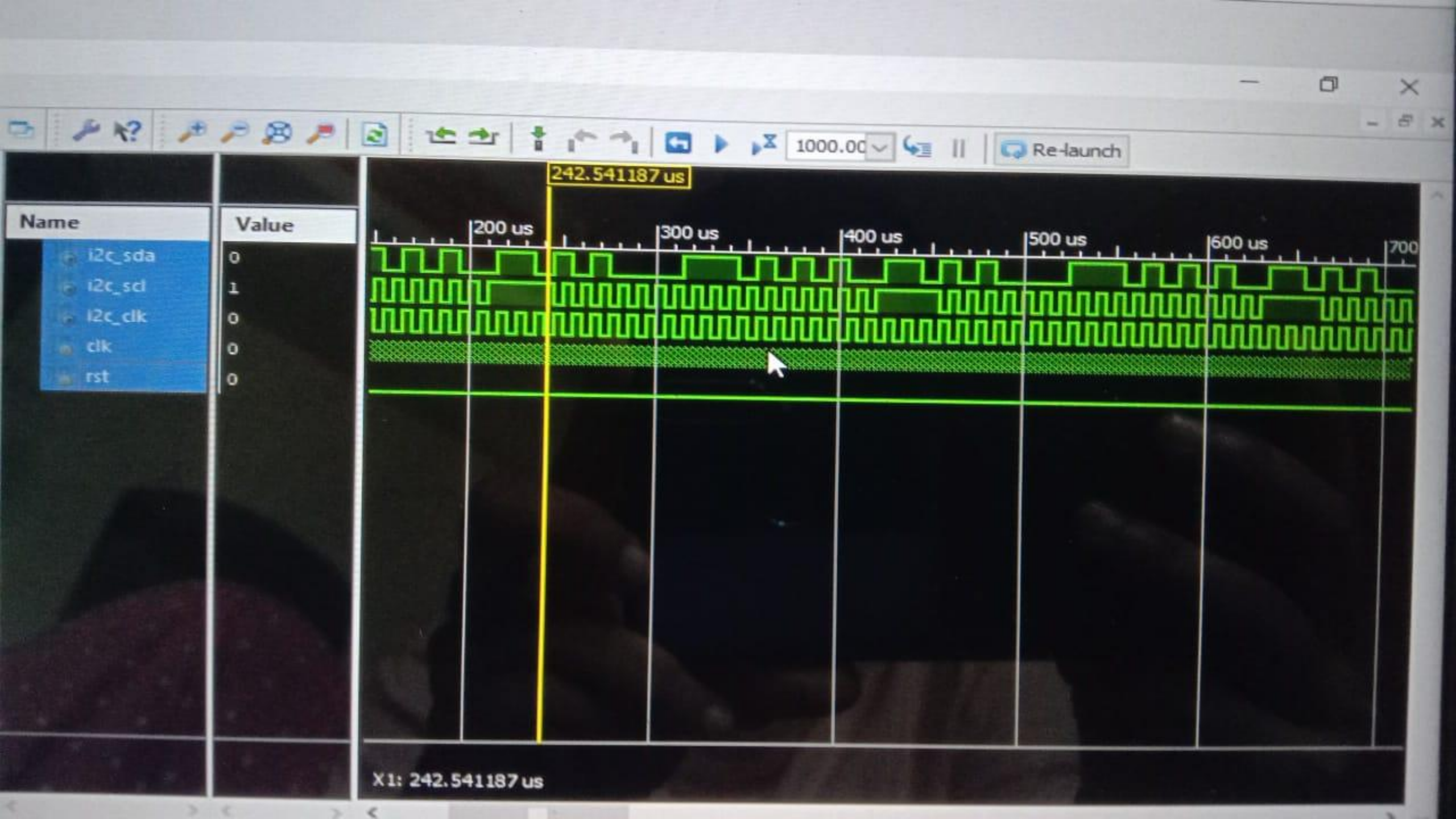


Fig [4]


1.00us
Re-launch
110.000 ns
me
Value
i2c_sda
i2c_scl
clk
rst
0
1
1
0
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
X1: 110.000 ns


1000.00
Re-launch
242.541187 us
Name
Value
i2c_sda
i2c_scl
i2c_clk
clk
rst
0
1
0
0
0
200 us
300 us
400 us
500 us
600 us
700
X1: 242.541187 us

References:

[1] EVALUATION OF I2C COMMUNICATION PROTOCOL IN DEVELOPMENT OF MODULAR CONTROLLER BOARDS Alvin Jacob, Wan Nurshazwani Wan Zakaria, and Mohd Razali Bin Md Tomari, Advanced Mechatronics Research Group, Faculty of Electrical & Electronic Engineering, University Tun Hussein Onn Malaysia, Parit Raja, Batu Pahat, Johor, Malaysia.

[2] FSM implementation of I2C protocol and its verification using Verilog Tapaswi SJ1, Dr Kiran V2.

[3] Volume 2, Issue 1, January 2014 International Journal of Research in Advent Technology, Available Online at: http://www.ijrat.org

[4] I2C BUS PROTOCOL USING VERILOG 2019 JETIR June 2019, Volume 6, Issue 6

[5] Texas Instrumentation, “Understanding I2C Bus”, June 2015.

[6] https://www.circuitbasics.com/basics-of-the-i2c-communication-protocol