DS 255 - System Virtualization
Assignment IV - System Virtual Machines

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1. It is important for VMM to handle the timer interrupt as it provides an opportunity for gaining control of the system to enable the time sharing of resources among different guest VMs. When a timer interrupt occurs, the VMM executes a code which performs the following operations

   (a) Save the architected state of running VM and determine the next VM to be activated

   (b) Restore the architected state for next VM and set timer interval and enable interrupts

   (c) Set PC to timer interrupt handler of OS in next VM

   The guest OS must be denied direct access to timer interrupt to ensure a fair scheme of time sharing of resources to work. Otherwise, the guest will have access to reschedule the next timer interrupt which can degrade performance of other running VMs. This is why the guest OS is provided with virtual emulated timer interrupt by the VMM.

   Also, it might not be feasible to ensure transparency by VMM if the guest is allowed to read the real timer interrupt value set by the VMM. Lack of transparency might cause the guest OS to behave differently when running under a VMM than a real machine.

2.

3. There are different variants for the standard time-sharing CPU scheduler as implemented in *Xen* hypervisor. They are: (a) Borrowed Virtual Time (BVT) scheduler, (b) Simple Earliest Deadline First (SEDF) scheduler and (c) Credit Scheduler.

   For the given scenario of three VMs on top of a single CPU, SEDF scheduler can be used. The goals of this scheduler is to increase *fairness* which is the time interval over which the scheduler provides fair CPU allocation and decrease *allocation error* which is the relative difference between requested CPU use percentage and the actual/observed CPU use percentage for a given VM.

   The SEDF scheduler achieves these goals as follows:

   (a) For each VM, it maintains a domain Dom_i, slice s_i, period p_i and a flag x_i. These indicates that the Dom_i will receive at least s_i units of CPU in period p_i. If x_i is true, scheduler follows *work-conserving* policy or else *non-work-conserving*

   (b) For each Dom_i, scheduler maintains deadline d_i which is the time at which the current period ends and r_i which is the remaining time of Dom_i in current period. The runnable domain with earliest deadline is picked to be scheduled next

   (c) The fairness and allocation error are calibrated by the time granularity in the definition of period p_i. E.g. 10ms, 100ms etc. Lower granularity will achieve better fair share allocation with larger period leading to "burstier" CPU allocation

   (d) In general, this scheduler can achieve consistently low allocation error for different target CPU allocation while maintaining fairness of allocation

4. The TLB consists of guest virtual address (GVA) to host physical address (HPA) mapping irrespective of whether the page table or the TLB is architected.

   The shadow page tables increase the memory access latency though it reduces one level of indirection since there is a significant overhead in intercepting and emulating the guest's modification of page table by the hypervisor. Also, note that the shadow page tables are maintained by hypervisor causing multiple VM exits and intervention of hypervisor in case of page table writes.

   Nested page table support is needed at the hardware level to reduce this latency caused by shadow paging. It uses a second page table to translate Guest Physical Address (GPA) to HPA. The page walking now becomes two dimensional with two page tables: Guest page table with GVA to GPA and host page table with GPA to HPA.

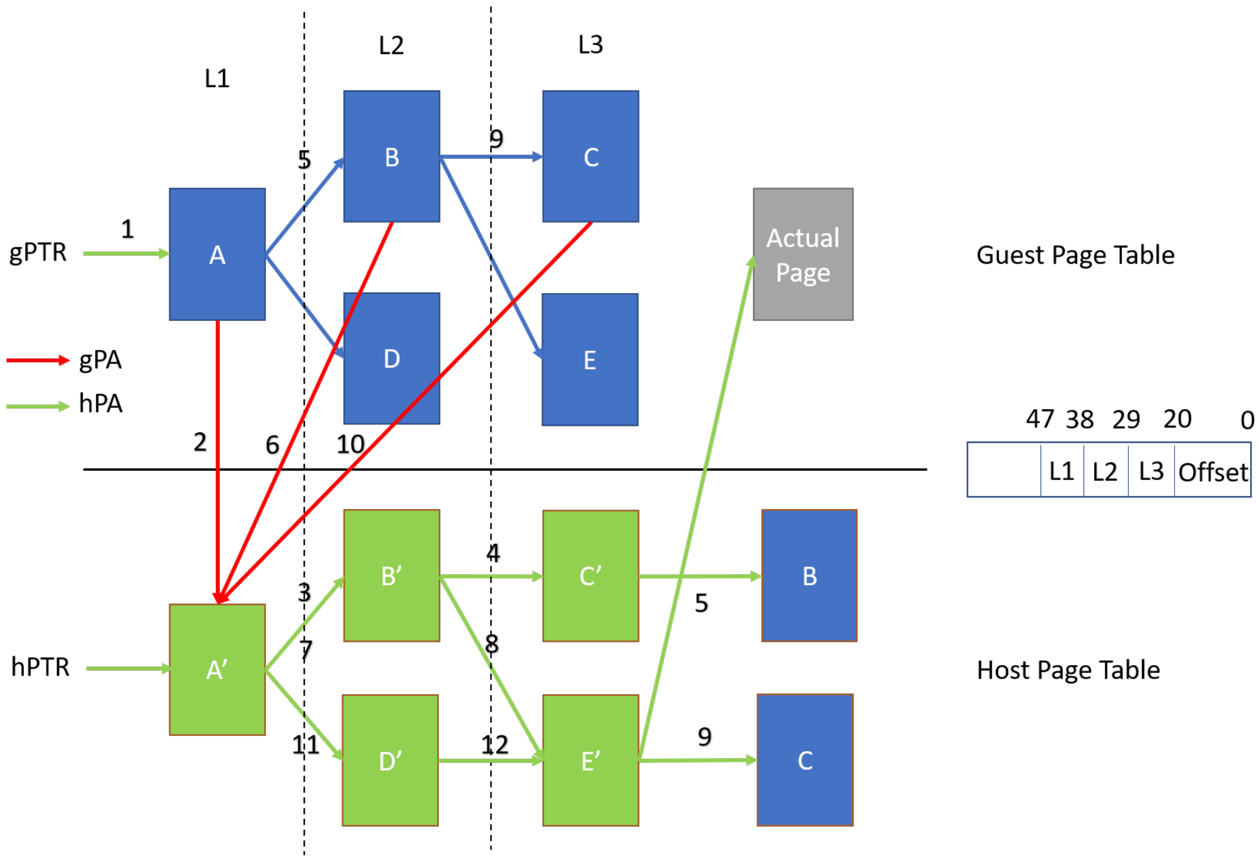
   The nested paging is already available with AMD and Intel architectures (VT-X) as part of their hardware virtualization support.

5.

6. The TLB Reach is defined as the product of page size and TLB size. Given page size = 4KB and TLB size = 1024. Therefore the TLB Reach = 4MB.

   If the program has large working set size (2GB in this case), the TLB reach can be increased by using large pages. For example, Intel x86-64 supports large page size of 2MB and Linux kernel manages these pages using the HugePages feature. With this increased page size, the TLB reach grows to 2GB and can cover the entire program memory.

7. The 2-D page walk diagram for 2MB page size using 48-bit virtual address is given below,



   The numbers on top of arrows indicate the sequence of page table walk. It requires 12 memory accesses to get the frame number of the desired physical page. Large page sizes help in reducing the latencies by increasing the TLB reach and reducing the no. of levels in a page table.

8.

References

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