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COA Assignment.

Que 9.2

segments	1	2	3	4	5	6	7	8	9	10	11	12
1.	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8				
2.		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8			
3.			T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8		
4.				T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	
5.					T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
6.						T_1	T_2	T_3	T_4	T_5	T_6	T_7

→ $(k+n-1)\,t_p$

$6+1-8$

13 cycles.

Que 9.3 $k = 6$ segments $\quad n = 200$

$(k+n-1) \Rightarrow 6+200-1 = 205$ cycles.

Que 9.4 $t_n = 50\,ns$

$k = 6$

$t_p = 100\,nm$

$n = 100$

$$S = \frac{n t_n}{(5-99)\times 10} = \frac{100 \times 50}{(5-99)\times 10} = 4.76.$$

$$S_{max} \quad \frac{t_n}{t_p} = \frac{50}{10} = 5.$$

Que 12.1 (a) $\frac{2048}{128} = 16$ chips

(b) $2048 = 2^{11} = 11$ address lines

$128 = 2^7 = 7$ lines to address each chip.

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(c) 4 x 16 decoder.

Que 12.2 (a) 8 chips are needed with address lines connected in parallel.

(b) 16 x 8 = 128 chips.

Use 14 address lines (16K = 2^14) 10 lines specify the chip address 4 lines are decoded into 16 chip selected inputs.

Que 12.5 128K = 2^17

For a set of size of 2, the index address has 10 bits of words of cache. accomdate $\frac{2048}{2} = 1024$

(a)

Tag	Index
7 bits	10 bits

(b) Size of cache memory = $1024 \times 2(7+32)$

$= 1024 \times 78$

$= 79872$

Que 12.21

4 2 0 1 2 6 1 4 0 1 0

2 3 5 7

COA Assignment

	FirstIn		LRU	
Initial	Page in main memory	Content of FIFO	Pages in main memory	Most recent used
2	0124	4201	0124	4012
6	0126	2016	0126	0126
1	0126	2016	0126	0261
4	0146	0164	1246	2614
0	0146	0164	0146	6140
1	0146	0164	0146	6401
0	0146	0164	0146	6401
2	1246	1642	0124	4102
3	2346	6423	0123	1023
5	2345	4235	0235	0235
7	2357	2357	2357	2357