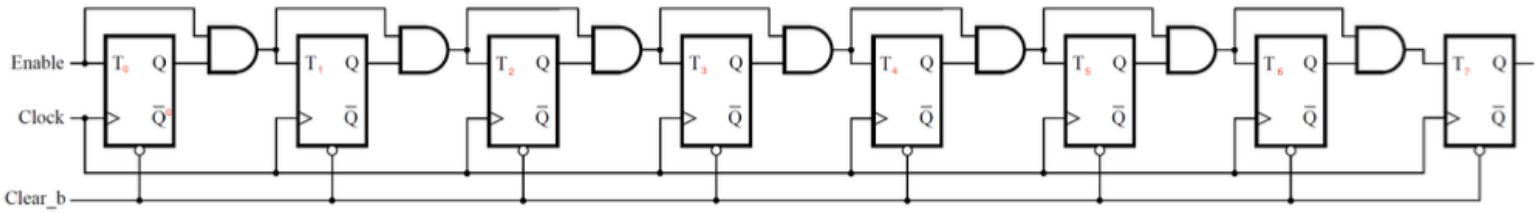
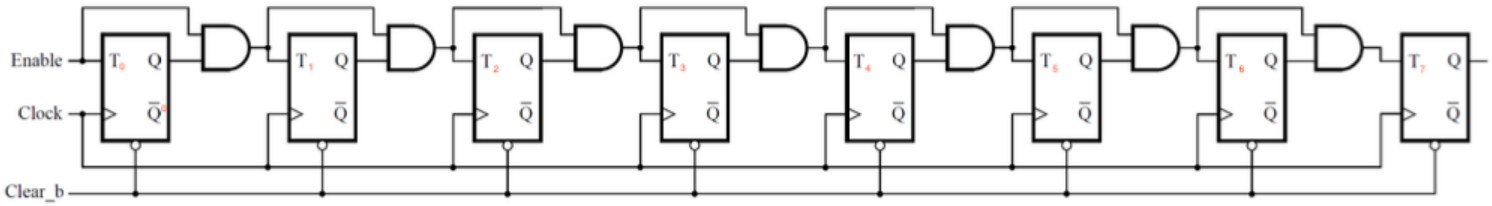
Csc258 prelab 5

4 Part I

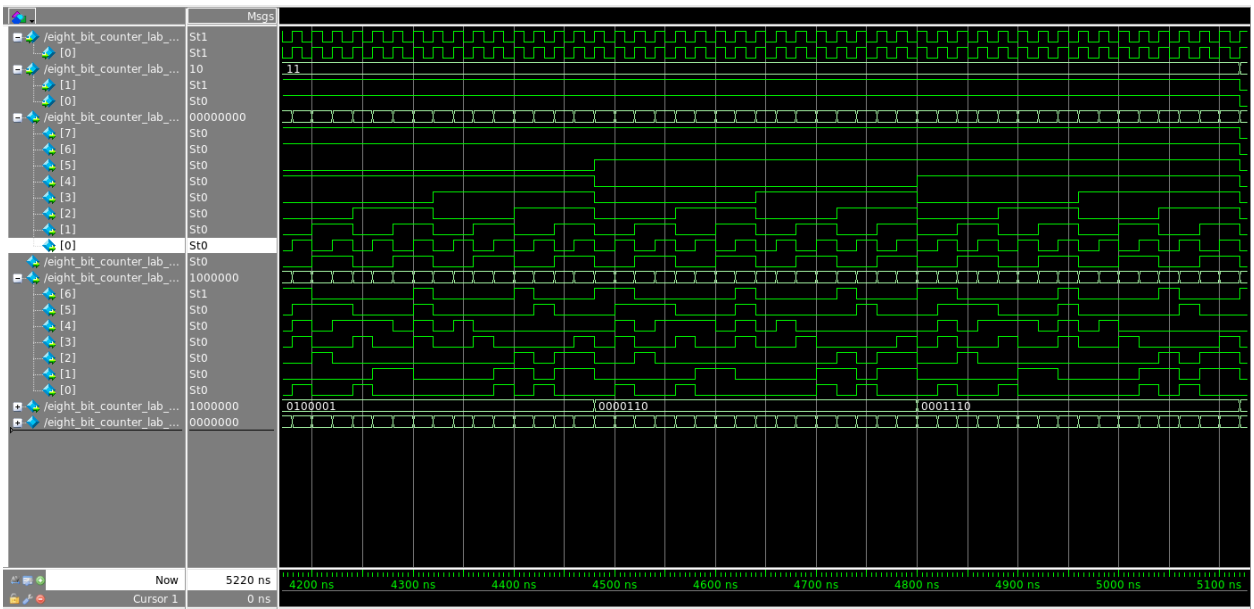
1.



2.



4.



6.

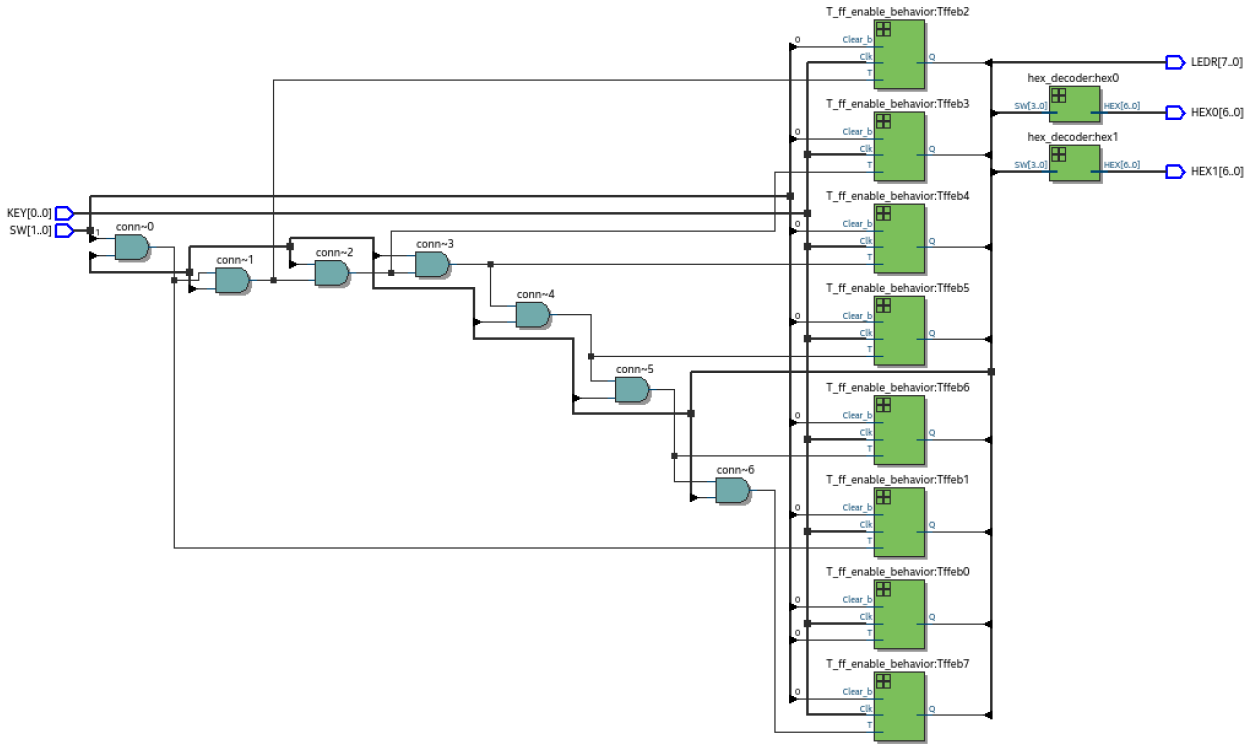
a)

Logic utilization (in ALMs)	13 / 32,070 (< 1 %)

b)

Slow 1100mV 85C Model				
	Fmax	Restricted Fmax	Clock Name	Note
1	606.8 MHz	606.8 MHz	KEY[0]	

7.

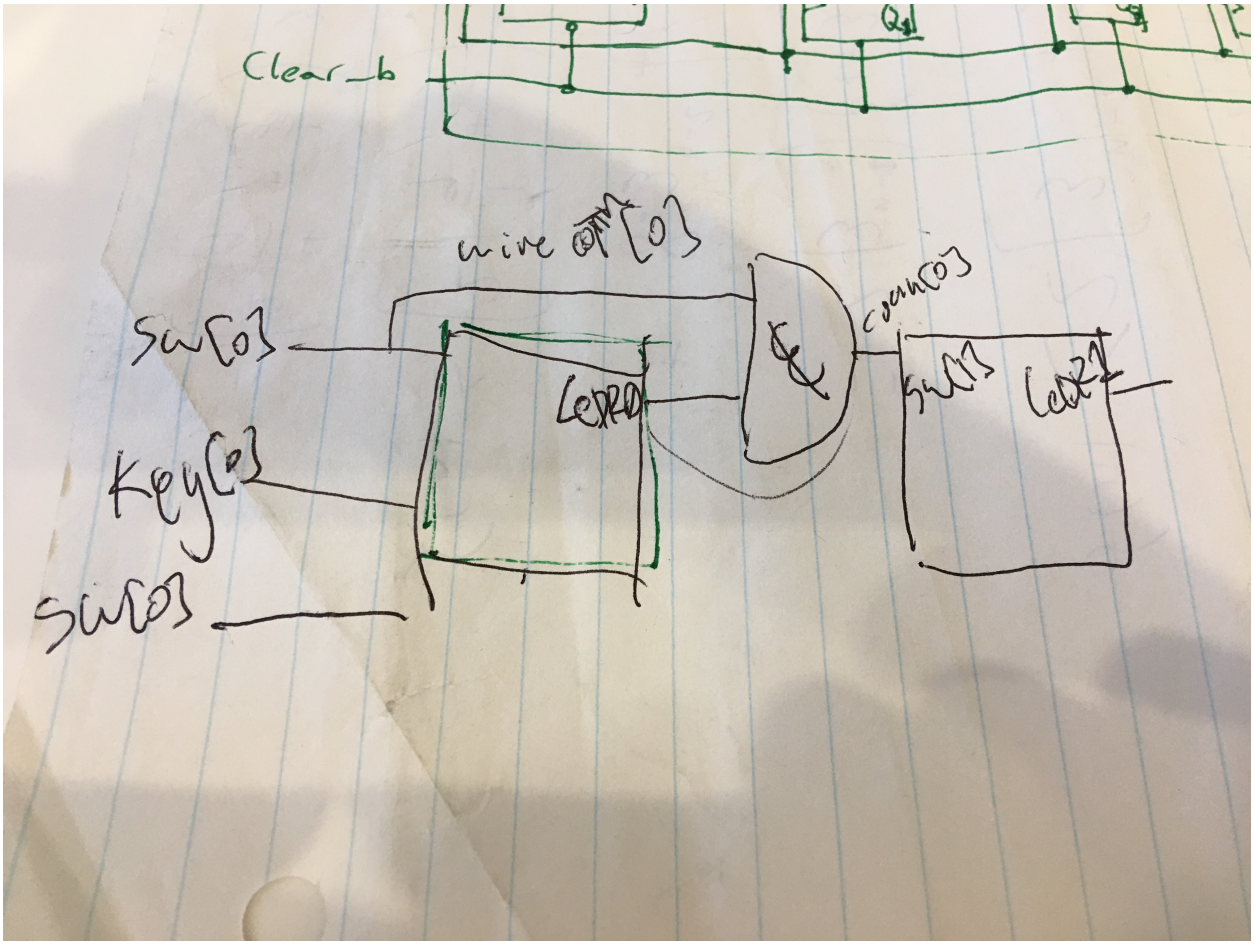


5 Part II

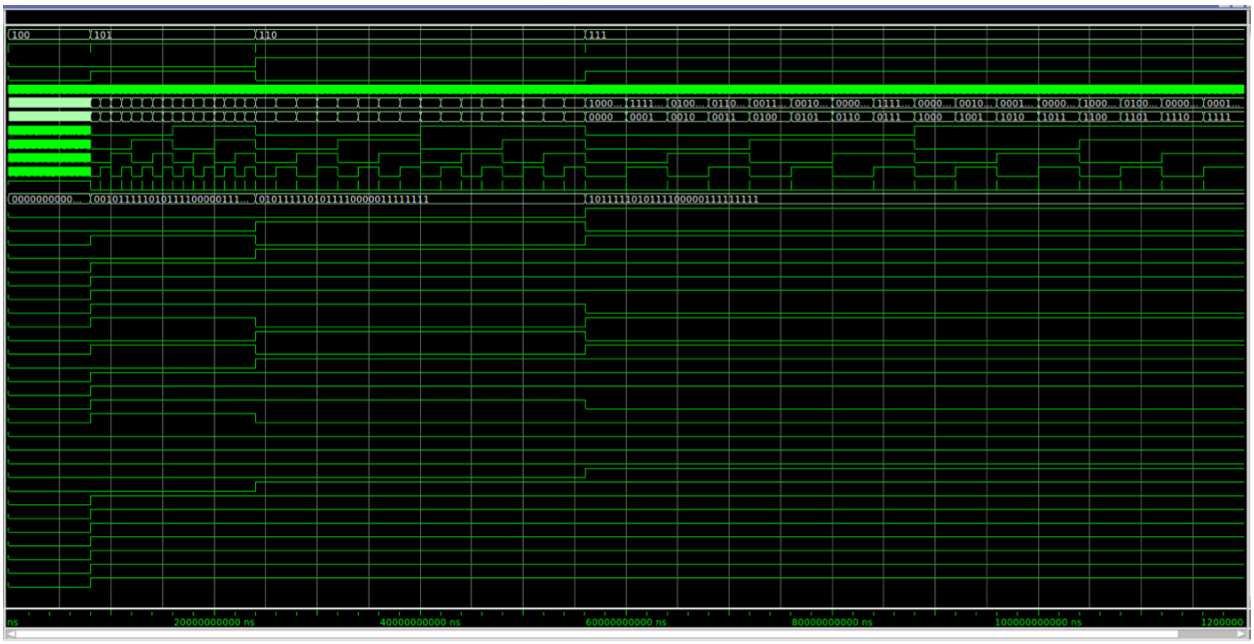
- Since this is a 4-bit counter the largest value we need is the largest 4-bit value. A larger value is not possible in a 4-bit array.

- Change if (q == 4'b1111) to (q == 4'b1001).
- 1/50*(10^6) = 0.00000002 seconds. Too fast to see.
- two 50 million counters combined
- 2^{26}, so 26 bits.

1.



3.


100
101
110
111
20000000000 ns
40000000000 ns
60000000000 ns
80000000000 ns
100000000000 ns
1200000

6 Part III

1.

Letter	Morse Code	Pattern Representation (pattern length is 14 bits)
S	• • •	10100000000000
T	—	11100000000000
U	• • —	10101110000000
V	• • • —	10101011100000
W	• — —	11101010111000
X	— • • —	11101010111000
Y	— • — —	11101011101110
Z	— — • •	11101110101000

2.