Ain Shams University
Faculty of Computer & Information Sciences
Computer Systems Department
Final Exam
Date: 21/5/2019

CHW-362 Computer Architecture & Org.
Dr. Karim Emara
3rd Year, 2nd Semester
Allowed Time: 3 hours

Answer the following 4 questions. **(Total marks: 65)**

Question 1: **marks: 20**

A. Choose the BEST answer for the following questions **[15 marks]**

1. The _____ determines how many tasks done per unit time.
   a) response rate
   b) CPU frequency
   c) throughput
   d) execution time
2. CPU performance can be improved by _____ the average cycles per instruction and _____ the clock rate.
   a) increasing, increasing
   b) decreasing, increasing
   c) increasing, decreasing
   d) decreasing, decreasing
3. In _____, the instruction format is variable-length, while in _____ the instructions are fixed-length.
   a) CISC, RISC
   b) RISC, CISC
   c) ISA, MIPS
   d) None of the above
4. In MIPS, the $a0 - $a3 registers are conventionally used as _____.
   a) return values
   b) local variables
   c) temporary variables
   d) function arguments
5. The _____ component allows reading from any two registers and writing to a third.
   a) ALU
   b) register file
   c) register bank
   d) stack
6. In MIPS, ALU performs _____ operation while executing load or store instructions.
   a) AND
   b) Subtract
   c) Add
   d) OR
7. The _____ hazard occurs when an instruction must wait for a pervious instruction to complete its data read/write.
   a) control
   b) data
   c) structure
   d) forward
8. The unexpected events arise within the CPU are called ____, while they are called ____ when they come from external sources.
   a) exceptions, interrupts
   b) interrupts, exceptions
   c) interrupts, errors
   d) errors, interrupts
9. In the _____ cache, any memory block has only one choice in the cache.
   a) fully associative
   b) 1-way associative
   c) 2-way associative
   d) None of the above
10. Upon writing, the _____ policy updates the cache block only, while updating the memory block when this block is replaced.
    a) write-through
    b) write-allocate
    c) write-forward
    d) write-back

B. [5 marks] Consider a program of 1 million instructions divided into four categories: ALU, Load, Store and Branch. The percentage of each category and its CPI are shown in the table below.

Category	P_i	CPI_i
ALU	50 %	1
Load	20 %	3
Store	16 %	2
Branch	14 %	1

1) Calculate the average CPI for this program.
2) Assume a cache is used while running this program of the following characteristics: Instruction cache miss rate = 2%, data cache miss rate = 4% and miss penalty = 100 cycles. Calculate the actual CPI when this cache used.
3) Assume a clock of 2 GHz rate is used, calculate the CPU time in these cases:
   a. The ideal CPI case (*no* cache misses and CPI calculated in 1) is used)
   b. The actual CPI case (with cache misses and CPI calculated in 2) is used).

Question 2: **marks: 15**

A. Convert the following MIPS code into its machine code **in decimal** assuming the first instruction is located at address 300 (decimal). Copy the following table into your answer sheet and fill it. Register codes and opcodes can be found in the last page. **[8 marks]**

MIPS Code	*Type*	*Machine Code*					
		opcode	rs	rt	rd	shamt	funct
		Address/Immediate					
`add $t2, $zero, $zero`							
`addi $s0, $zero, 3`							
`L1: slt $t1, $t0, $s0`							
`beq $t1, $zero, L2`							
`lw $t2, 8($s1)`							
`sll $t2, $t2, 2`							
`sw $t2, 4($s1)`							
`j L1`							
`L2:`							

B. Complete the following MIPS code to sum items of an integer array **arr1** and put the sum in **$s2**. Assume **$s0** contains the base address of arr1, **$s1** contains number of items in arr1 and **$t0** is a loop counter. **[7 marks]**

```
and $s2, $zero, $zero
and $t0, $zero, $zero
L1: ..[1].. $t1, $t0, $s1
..[2].. $t1, ..[3].., L2
sll $t2, $t0, ..[4]..
..[5].. $t2, $t2, $s0
lw $t2, ..[6]..($t2)
add $s2, $s2, $t2
..[7].. $t0, $t0, 1
j L1
L2:
```

Sub
beq $zero
2
add
$s0
addi

Question 3: **marks: 18**

A. Assume a single-cycle MIPS datapath and registers $s0 = 10, $s1 = 15, $s2 = 20, answer the following questions, given the following instructions:

I. `add $s0, $s1, $s2`
II. `beq $s0, $s1, L1` `# Assume L1 - (PC + 4) = 12`
III. `sw $s0, 32 ($s2)`

1. Convert the above instructions into its corresponding machine code **in decimal. [1 mark]**
2. Fill the following table by the **data** inputs of the register file, ALU and data memory **in decimal** while executing each instruction. Treat each instruction separately and independent on other instructions. If the input is unknown, write X. **[6 marks]**

Data input		add $s0, $s1, $s2	beq $s0, $s1, L1	sw $s0, 32 ($s2)
Register File	Read Register 1			
	Read Register 2			
	Write Register			
ALU	input 1			
	input 2			
Data Memory	Address			
	Write Data			

3. Fill the following table by the **control** signals while executing each instruction. **[3 marks]**

Control Signal	add $s0, $s1, $s2	beq $s0, $s1, L1	sw $s0, 32 ($s2)
RegDst			
MemtoReg			
ALUop (2 bits)			
MemWrite			
ALUSrc			
RegWrite			

B. Assume a pipelined processor of 5 stages IF, ID, EX, MEM and WB and the following sequence of instructions:

I1 lw r1, 40 (r6)
I2 add r6, r2, r2
I3 sw r6, 50 (r1)

1. Decide whether the following sentences are true or false. If a sentence is true, write the register name(s) which cause(s) the data dependency. **[2 marks]**

	True or false?	Register(s)
a) I2 depends on I1	/	
b) I3 depends on I1	✓	r1
c) I3 depends on I2	✓	r6

2. Assume there is **no forwarding** in this pipelined processor, rewrite the above code and add **nop** instructions to eliminate any data hazards, if any. **[2 marks]**

2 nop

3. Assume there is **full forwarding** in this pipelined processor, rewrite the above code and add **nop** instructions to eliminate any data hazards, if any. **[2 marks]**

4. Assume the cycle time equals 350ps with forwarding and 300ps without forwarding, what is the total execution time of the above code in both cases? **[2 marks]**

Question 4: **marks: 12**

Given the 16-bit memory address references below, as BYTE addresses in hex format:
0030, 00E8, 0031, 00EC, 0029, 0040, 003A, 0042, 00E8

a) For each of these references, identify the binary address. **[1 Mark]**
b) Given a direct-mapped cache with a total of 16 words organized as 1 word/block, what is the length of the tag, the index and byte offset? For each memory reference, list the index, the tag and if each reference is a hit or miss. **[3 Marks]**
c) Repeat (b), but with 2 words/block for a cache with a total of 16 words. **[3 Marks]**
d) Repeat (b) for a two-way set associative cache with 1 word/block, and a total size of 16 words. **[3 Marks]**
e) Repeat (b) for a fully associative cache with 1 word/block, and a total size of 8 words. **[2 Marks]**

Hint:

For b) and c), use a table of the following header:

Address (binary)	Index (hex)	Tag (hex)	Hit or Miss

For d), use a table of the following header:

Address (binary)	Index (hex)	Tag (hex)	Way	Hit or Miss

Good Luck

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Q 1)

A)

1- c

2- b

3- a

4- d

5- b

6- c

7- b

8- a ⇒ Lecture 9

9- Mais oui

10- " "

B)

1) $C = 1$ mil.

$\frac{C_i}{C}$

$$CPI_{av} = \sum CPI_i \times P_i$$

$$= (1 \times 0.5) + (3 \times 0.2) + (2 \times 0.16) + (1 \times 0.14)$$

$$= 1.56 \text{ Cycles}$$

2)
3) } مش عايزنا

Q2)

A)

code	type	opcode	rs	rt	Address / Imm: rd	Shamt	Funct
add t_2, $2, $2	R	0	0	0	10	0	32
addi s_0, $2, 3	I	8	0	16	3		
L1: slt t_1, t_0, s_0	R	0	8	16	9	0	42
beq t_1, $2, L_2	I	4	9	0	300 + (4 × 8) = 332		
lw t_2, 8(s_1)	I	35	17	10	8		
sll t_2, t_2, 2	R	0	10	?	10	2	0
sw t_2, 4(s_1)	I	43	17	10	4		
J L_1	J	2	300 + (4 × 2) = 308				
L2:							

B) arr1 ⇒ s_0 , sum ⇒ s_2 , no items ⇒ s_1

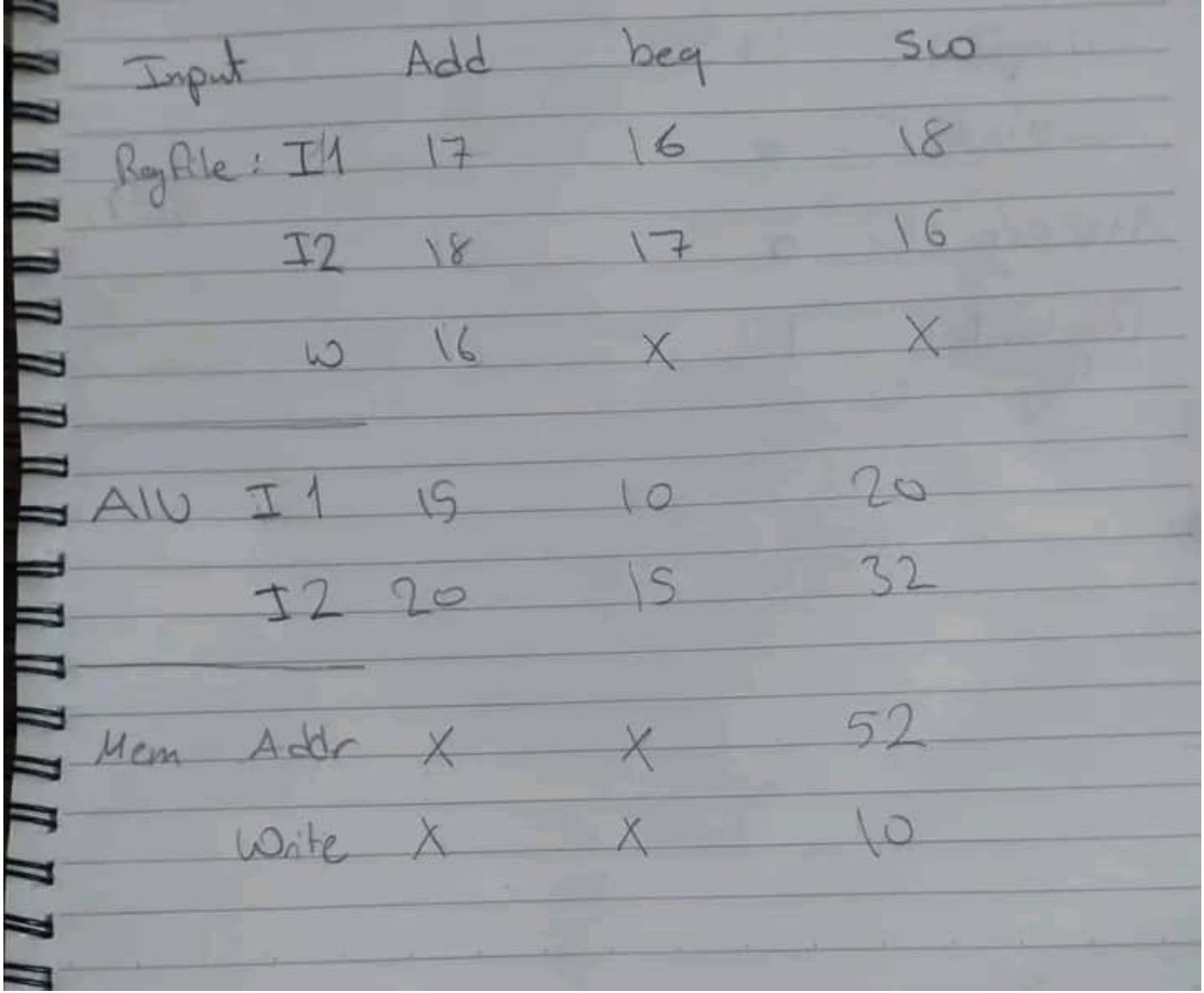
counter ⇒ t_0

1- sub

2- beq
3- $zero } if loop counter equals no. items

4- 2
5- add } multiply counter by 4 Then add it to base address
6- 0 Then load element in That position

7- addi ;increment loop counter by 1



Input		Add	beq	sw
RegFile :	I1	17	16	18
	I2	18	17	16
	W	16	X	X
ALU	I1	15	10	20
	I2	20	15	32
Mem	Addr	X	X	52
	Write	X	X	10

MemWrite		X	X

Q3:

ALU	add	beq	sw
RegDst	1	X	X
MemtoReg	0	X	X
ALUop	10	01	00
MemWrite	0	0	1
ALUSrc	0	0	1
Reg write	1	0	0

Q3 [1]

(B) (a) False

(b) True, r_1

(c) True, r_6

---

[2] 1- lw r1, 40(r6)

2- add r_6, r_2, r_2

3- nop

4- nop

5- sw r_6, 50(r_1)

[3] same code (No data hazard

[4] case (1) {forwarding}

First instruction → (2,3)

5.350 + 2.350 = 2450

case (2) {no forwarding} the (2 nop) instructions

5.300 + 2.300 + 2.300 = 2700