ECEN 5613 Fall 2023	Embedded System Design Lab #1 Signoff Sheet – Part 1&2 Elements	Week #1 8/28/2023

You will need to obtain the signature of your TA on the following items in order to receive credit.

The Part 1 & Part 2 Elements of Lab #1 should be completed and signed off by **Friday, Sept. 15, 2023** in order to give you time to complete the Part 3 Elements upon receipt of your parts kit. All signoffs are due by **Friday, Sept. 22, 2023.** You need to submit both of your signoff sheets and other required elements by **11:59pm Sunday, Sept. 24, 2023**. Labs completed after the signature due date or submitted after the submission due date will usually receive grade reductions, but there is leniency on Lab #1.

Print your name below and then demonstrate your working hardware/firmware in order to obtain the necessary signatures. All items must be completed to get a signature, but partial credit is given for incomplete labs. Receiving a signature on this signoff sheet does not mean that your work is eligible for any particular grade; it merely indicates that you have completed the work at an acceptable level.

Student Name: SHRUTHI THALLAPALLY

Checklist

- ☑ Student demonstrates detailed knowledge of an 8051 simulator or debugger (including changing register values, editing data memory, using breakpoints, single stepping, uses /overlay option, etc.)
- ☑ Student assembly program works correctly
- ☑ Student demonstrates detailed knowledge of WinCUPL and WinSim, logic equations correct
- ☑ Student demonstrates detailed knowledge of the final project assignment and discusses any questions with the TAs.

Student Answers to Lab Questions

1. **How many bytes of code space does your program require?**
   (Show how you arrived at your answer.)
   Code Size? 56 bytes.

2. **How long did your program take to execute for X=0x93 and Y=0x0A? Assume an 11.0592 MHz clock and include the instructions executed from the beginning until you reach the ENDLOOP label. Show the TA your detailed calculations on the code listing during your signoff.**
   Execution Time? 59.64 µs

09/15/2023
TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
SPLD code	☐	☐	☐	☑	☐
Assembly Language Code Style	☐	☐	☐	☑	☐
Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐	☑	☐
Overall Demo Quality	☐	☐	☐	☑	☐

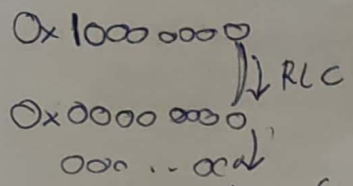
Comments:

NOTE: This submission sheet should be the top/first sheet of your submission.

[+] Folder structure correct

[+] Assembly is well-commented

[+] All cases work correctly except for address 0x23 and B >= 80H



[+] WinCUPL/WinSim correct.

ECEN 5613 Fall 2023	Embedded System Design Lab #1 Signoff Sheet – Part 3 Elements	Week #1 8/28/2023

Print your name below, answer the questions, and then demonstrate your working hardware in order to obtain the necessary signatures. All items must be completed to get a signature.

Student Name: SHRUTHI THALLAPALLY

Checklist

- ☑ Schematic of acceptable quality, Student name on board in permanent ink
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board:
- ☑ Mounting hardware present (e.g. standoffs or an enclosure)
- ☑ Power switch and LED, voltage regulator functional, power jack present
- ☑ Power-on Reset (RC) and Run-time Reset (pushbutton), 8051 bypass cap is present
- ☑ RS-232 connector mounted, 74LS373 transparent latch wired
- ☑ Logic outputs correct (e.g. SPLD generation of /READ and /CSPERIPH; view SPLD code)
- ☑ Student displays good knowledge of oscilloscope
- ☑ Peak to peak noise measured across processor VCC and GND is < 800mV
- ☑ Oscillator functional (check for correct ALE/XTAL2 signals after power on-off cycles)
- ☑ EFM8 & ARM development boards functional, student can demonstrate the basic software.

Student Answers to Lab Questions

1. **What voltage is present at the regulator input?** Use a digital multimeter. 7.6 V
2. **What voltage is present at the regulator output?** Use a digital multimeter. 4.99 V
3. **What peak to peak noise is present across the processor VCC and GND?** Use an oscilloscope.

   Measured value at processor package pins on top side of board: 284 mV

   Measured value at wire wrap socket pins on bottom side of board: 275 mV
4. **How long is the processor held in reset after the run-time reset pushbutton is released?** Use an oscilloscope and try to measure the time between the release of the pushbutton and the time when noise from ALE is observed on the RST signal.

   Measured value: 276 ms
5. **What frequency is present at the ALE pin?** Use an oscilloscope. 1.842 MHz

09/29/2023

TA signature and date

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐ ✓	☐	☐
Overall Demo Quality	☐	☐	☑	☐	☐

Comments:

NOTE: This submission sheet should be the second sheet of your submission.

Part 3 Comments

[+] Hardware Implementation

- [+] Decoupling capacitors added
- [-] Label not present for IC

[+] Good knowledge of oscilloscope & logic analyzer.

[+] STM32 code

Submission Sheet

Instructions: Print your name below and sign the honor code pledge. Separate the signoff and submission sheets from the rest of the lab and turn in a scan (or clear picture) of these signed forms, the items in the checklist below, and the answers to any applicable lab questions in order to receive credit for your work. No cover sheet please. **Submit all items electronically via Canvas to reduce paper usage. Canvas is https://canvas.colorado.edu .**

Remember, in addition to the items listed on the signoff checklist, be sure to review the lab for additional requirements for submission, including:

- ☑ Scan of signed and dated Part 1 & 2 Elements signoff sheet as the top sheet (No cover sheet please)
- ☑ Scan of signed and dated Part 3 Elements signoff sheet as the second sheet
- ☑ Scan of submission sheet with signed honor code pledge as the third sheet
- ☑ PDF of complete and accurate final schematic of acceptable quality (all components shown).
- ☑ Fully, neatly, and clearly commented assembly code.
- ☑ Clear high-resolution pictures of the top and bottom sides of your 8051 board. Must be able to read any silkscreen/labels on the board as well as zoom in and see the solder joints and wire wraps.

Make copies of your code, SPLD code, and schematic files and save them as an archive.

Student Name: Shruthi Thallapally

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: T. Shruthi

1. **How much power is dissipated in the regulator, assuming a load current of 210mA?** Assume that the regulator is drawing the max quiescent current shown in the data sheet (use the correct data sheet for the regulator you have on your board). Neatly show all your work.

$P_{dissi} = (V_{in} - V_{out}) I_{load}$; $V_{in} = 7.6V$ $V_{out} = 4.99V$ $I_Q = 6mA$

with load:

$P_{di} = (7.6 - 4.99) \times 210mA$

$= 2.61 \times 210m$

$= 548.1mW$

without load

$P_{di} = (7.6) I_Q = 7.6 \times 6m$

$= 45.6mW$

Total $P_{di} = 548.1m + 45.6m = 593.7mW$

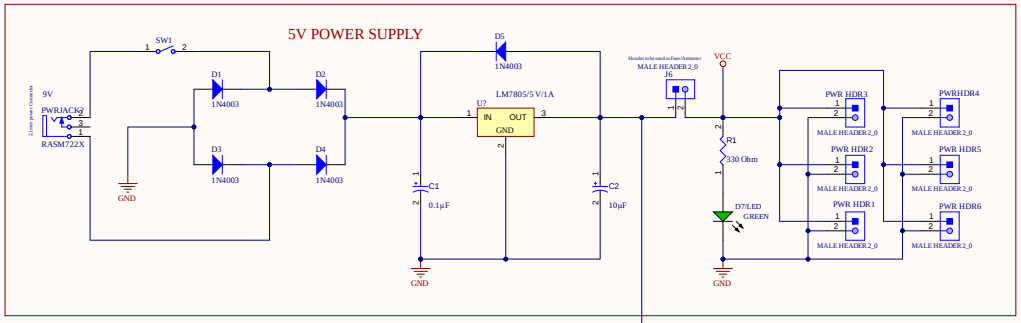
Calculated value: 593.7mW

Comments:

NOTE: This submission sheet should be the third sheet of your submission.

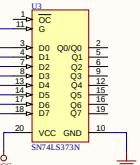
REVISION	DESCRIPTION	DATE	APPROVED

5V POWER SUPPLY

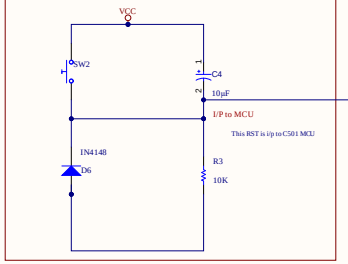


5V to MCU

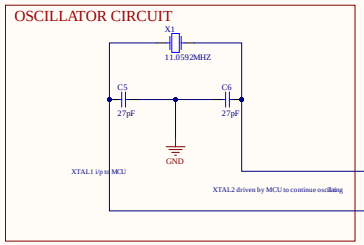
Transparent Latch

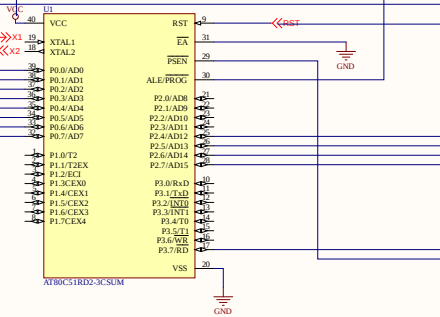


Power on RESET/Run time Reset

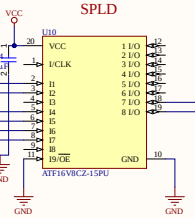


OSCILLATOR CIRCUIT





SPLD



8051 MCU

GND

Shruthi Thallapally

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: Altium

PROJECT REVISION: Not in version control | DOCUMENT REVISION: Not in version control | DESIGN ITEM: Item not interpreted

TITLE: *

SIZE: A2 | CAGE CODE: | DWG NO. | REV

SCALE: | FILE NAME: ESDLabSchematics.SchDoc | SHEET * OF

ItemRevision not interp

ASSEMBLY CODE

```
ORG 0000H
MOV B,#0AH          //storing divisor value in B
MOV A,#93H          //storing dividend value in A
MOV 20H,A           //storing A value in internal memory
MOV 21H,A           //storing A value in internal memory
MOV 22H,B           //storing B value in internal memory
MOV A,B             //storing B value in A
JZ ERROR_DIVISOR_ZERO         //checking if the value in A is ZERO if it is,
jump to error_divisor_zero
RLC A               //left shifting value in A(multiply by 2)
JC ERROR_8BIT_EXCEED          //checking if the value is overflowing if it
is, jumping to exceed_8bit_exceed
RLC A               //left shifting value in A(multiply by 2)
JC ERROR_8BIT_EXCEED          //checking if the value is overflowing if it
is, jumping to exceed_8bit_exceed
CLR C               //clearing carry flag
MOV B,A             //storing divisor value in B
MOV R0,#0H          //Initiating R0 register to zero to store quotient
MOV A,20H           //storing dividend value in A

DIVISIONLOOP:       //loop to divide
MOV R1,A            //storing A value in R1 for future reference
SUBB A,B            //subtracting B from A
JC DIVISIONEND      //Jump to DIVISIONEND if A becomes negative
INC R0                    //Incrementing R0 to store quotient
SJMP DIVISIONLOOP //Jump to DIVISIONLOOP to continue the division

DIVISIONEND:        //Loop to end the division

MOV 24H,R0          //Storing R0 in memory address 24H
MOV 25H,R1          //Storing R1 in memory address 25H
MOV 30H,#00H        //Storing 0 in memory address 30H
SJMP ENDLOOP        //Jump to ENDLOOP


ERROR_DIVISOR_ZERO:           //error when the divisor is zero
MOV 30H,#01H        // Storing 1 in memory address 30H
SJMP ENDLOOP        // Jump to ENDLOOP

ERROR_8BIT_EXCEED:            //error when bits overflows
MOV 30H,#02H        // Storing 2 in memory address 30H
SJMP ENDLOOP        // Jump to ENDLOOP

ENDLOOP:
SJMP ENDLOOP        // Jump to ENDLOOP, creates an infinite loop

END
```

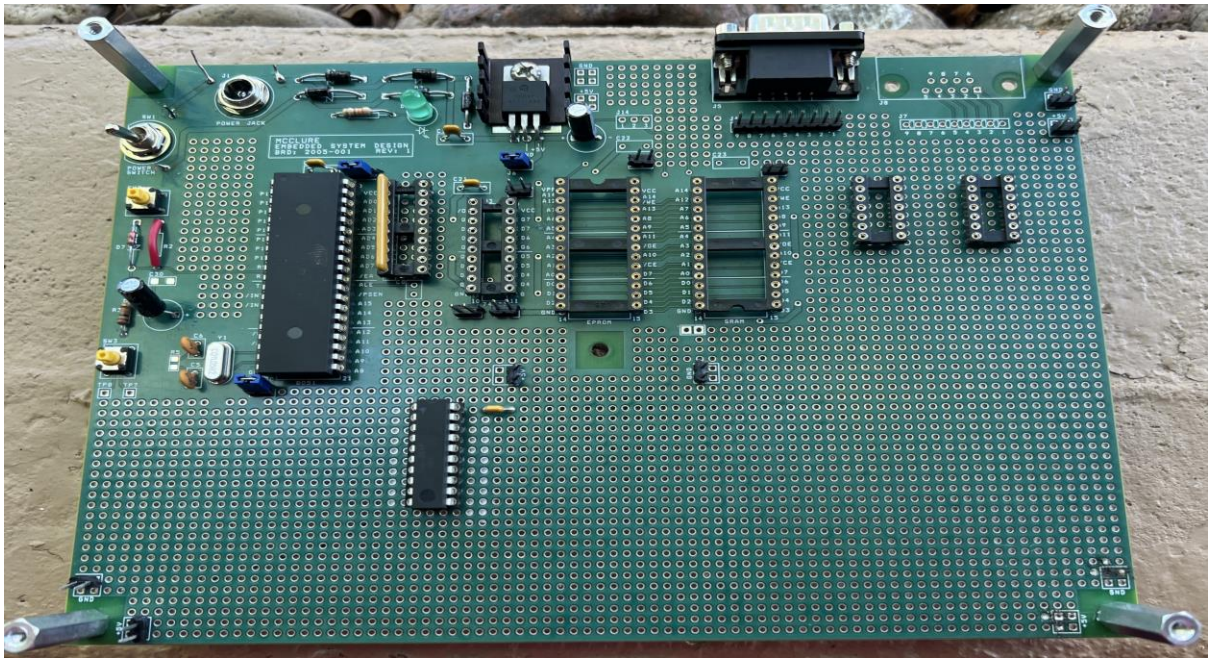


Fig. a: Top side of the Board

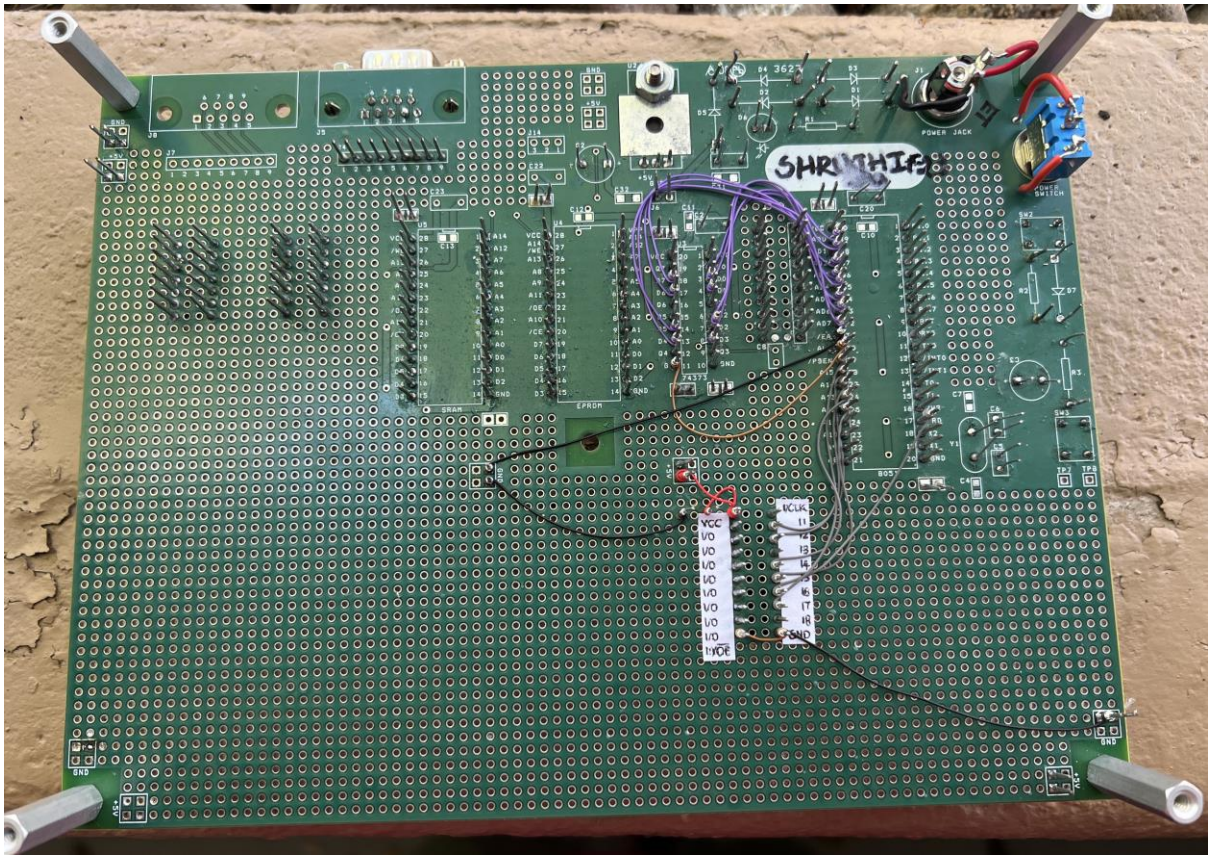


Fig. b. Back side of the Board

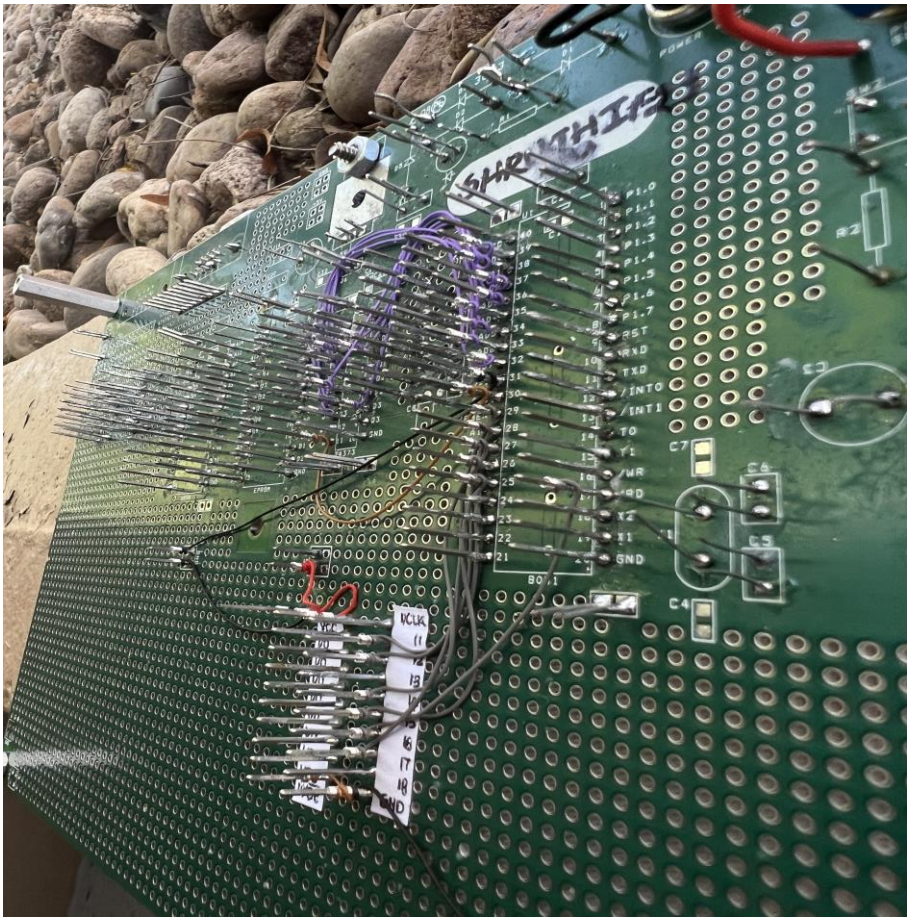


Fig. c: Back side of the board with the view of wire wrapping