Embedded System Design Lab #2 Signoff Sheet

Fall 2023

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by Friday, September 29, 2023 (Part 1 Elements) and Friday, October 6, 2023 (Part 2 Elements).

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: SHRUTHI THALLAPALLY Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own." Student Signature: T Shnithi Signoff Checklist Part 1 Required Elements Schematic of acceptable quality, correct memory map, SPLD .PLD file Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board NVRAM (as EPROM substitute), decode logic, and LED functional Understands device programmer. Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display. Shows and discusses logic analyzer screen captures: Assembly program and timer ISR functional: TA signature and date Part 2 Required and Supplemental Elements AT89C51RC2, RS-232, and FLIP functional □ 74LS374 debug port functional Understands timing analysis, setup/hold/propagation ARM code build process, LED program, version control TA signature and date FOR INSTRUCTOR USE ONLY Poor/Not Meets Not Exceeds Outstanding Part 1 Elements Applicable Complete Requirements Requirements Schematics, SPLD code 昌 Hardware physical implementation Part 1 Required Elements functionality Sign-off done without excessive retries Student understanding and skills

Overall Demo Quality (Fait 1 Elements)					
FOR INSTRUCTOR USE ONLY Part 2 Elements	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code Hardware physical implementation Part 2 Required Elements functionality Supplemental Elements functionality					0000
Sign-off done without excessive retries Student understanding and skills		H			
Overall Demo Quality (Part 2 Elements)			0		

NOTE: This signoff sheet should be the top/first sheet of your submission.

I.F. Schematic is chear and cornect. SPLD cosmock C+3 Functionality of the Enlarging in correct. OAD 53 Temer Door not make (ED blank out correct [+] Correct use of the Logic Anolyger, EZ MSRAM doe con missing. Good Schematics This functional ARM part c functional, part

SUBMISSION QUESTIONS:

a) What operating system (including revision) did you use for your 8051-code development?

Ans: Windows OS

b) What assembler(s) (including revision) did you use?

Ans: Keil uVision 5

c) What ARM development tools did you use?

Ans: STM Cube IDE

- d) Did you install and use any other software tools to complete your lab assignment?

 Ans: I have used the above software and LogicPort to complete these lab assignments.
- e) Did you experience any problems or challenges with this lab assignment or any of the software tools? If so, describe the issues.

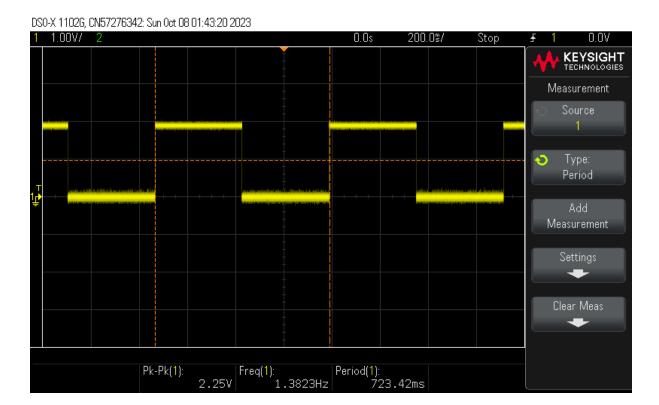
Ans: I found some difficulty in the beginning in using a new software/IDE and working in it.

f) If you have any suggestions for changes to this lab assignment for the future, please include those ideas in your submission.

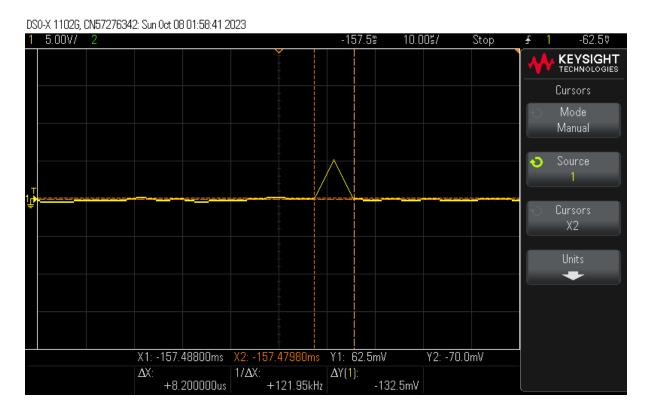
Ans: It would be helpful if demo sessions are conducted when new software is required to be installed/used. It would be helpful if more clarity is given on the things that is expected from us.

TIMING DIAGRAMS:

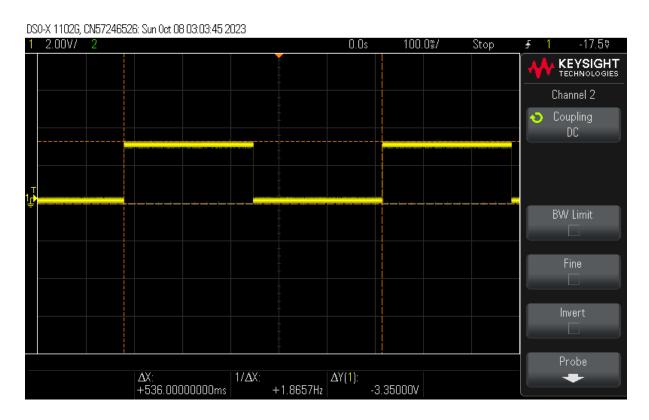
1. Oscilloscope screenshot of Part 1 Toggling LED with the frequency of 1.38 Hz.



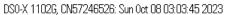
2. Oscilloscope screenshot of Part 1: Toggling another unused pin when entering and exiting ISR.

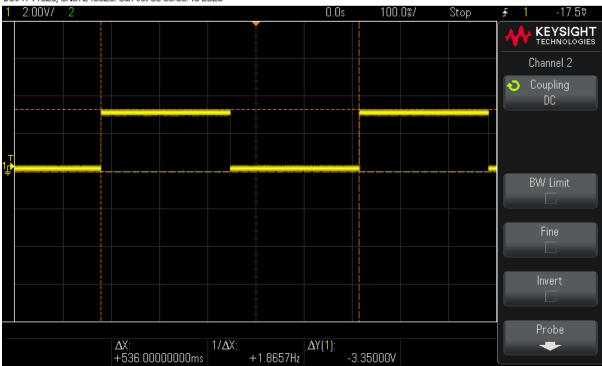


3. Oscilloscope screenshot of Part 2: Toggling LED using STMCube IDE



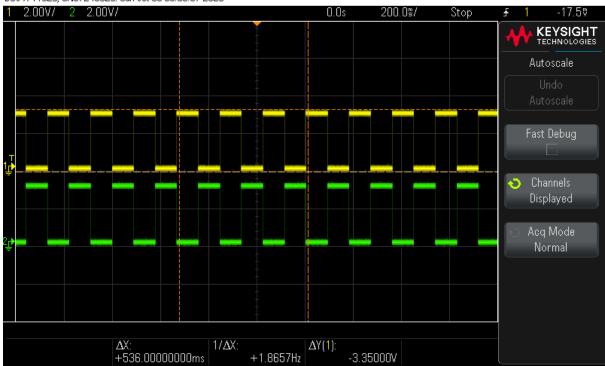
4. Oscilloscope screenshot of Part 2: Turning on the on-board LED for 270ms and turning it off for 270ms.



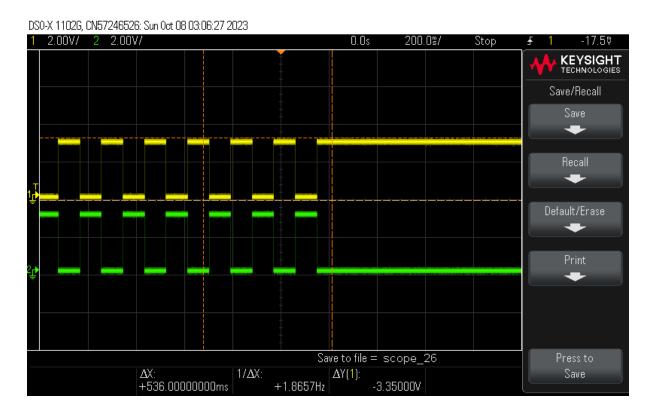


5. Oscilloscope screenshot of Toggling on-board green and blue LEDs.

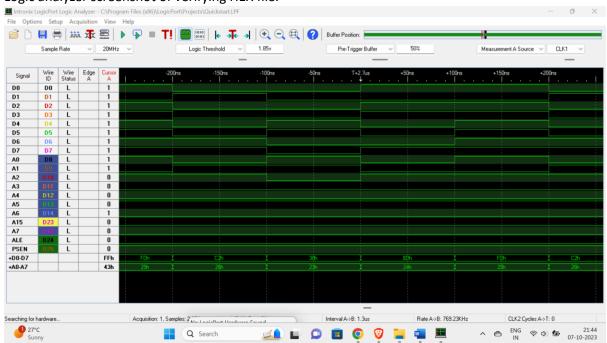
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Oscilloscope screenshot of When the push button is pressed, toggling is stopped.



6. Logic analyzer screenshot of verifying HEX file.



CALCULATIONS: (2) & 1 Propos of a site of 12201 1020 12. Time taken by ISR Time period of IIR obtained by the time period of pin Pl.O = 8.2 usec [From oscilloscope] LIMP -2 clock cycles (208 to promise formation) CLR - 1 clock cycle SETB - 1 clock Cycle 10000 11 24p CPL -1 clock cycle sunt and ton bloods SJMP - 2 clock cycles Total clock cycles = 7 Time taken for each clock cycle = 1.085 ulee Time taken by IIR = 7x 1.085 wee
= 7.895 = 8 wee
= 7.895 = 8 wee Delay of 0.362 see for LED ON and OFFT OUT OUT Freq. of 8051 ucontroller = 11.0592 MHz Machine cycle = 12 clock cycles Each clock cycle = 11.0592 = 0.9216 MHz Time period of each clock cycle = 1.085 mec For 0.362 sec of delay $Count(x) = \frac{0.362}{1.085 \times 10^{-6}} = 333640$ Timer can hold max value of FFFFH= 65536D 333640 = 5.0909

Timer should run tortill its max value 5 times and to obtain the remaining delay the timer should be loaded with 5963D => F8 B9 H

that is

TH = E8H TL=B9H

18.6) Delay of 270ms for RED LED ON and OFF

Required delay = 270ms; timer clock = 48MH2
= 3.7Hz

Reg foreg = timer clock

(PSCH) X (ARRHI)

(PSCH) (ARRH) = $\frac{48 \times 10^6}{3.7}$ = 12972972.9 Hz

tets Cowider PSC = FFH = 256

ARRH1 = 12972972.9 256 = 50675

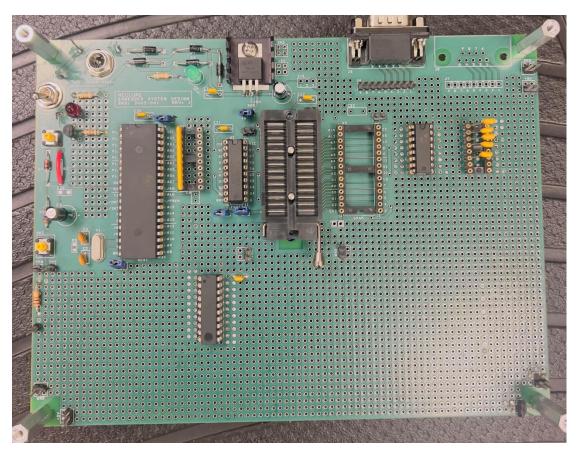
ARR = 50674

for reg delay of 270 ms

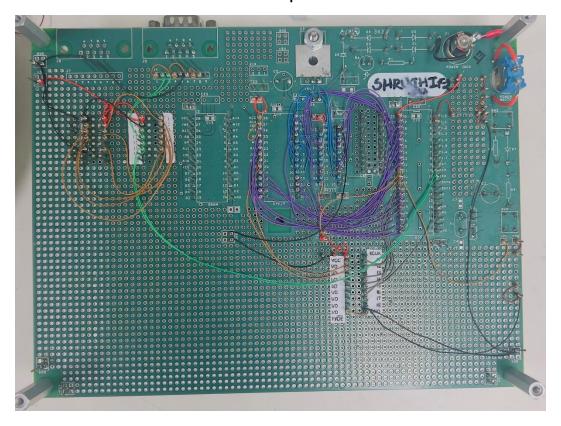
PSC = FFH

ARR = 50675D = C5F3H

BOARD PICTURES



a. Top side of the Board



b. Bottom side of the Board