Basys 3 Board
FPGA Pin Assignments
for On-Board I/O

function	FPGA pin
LEDs	
LD0	U16
LD1	E19
LD2	U19
LD3	V19
LD4	W18
LD5	U15
LD6	U14
LD7	V14
LD8	V13
LD9	V3
LD10	W3
LD11	U3
LD12	P3
LD13	N3
LD14	P1
LD15	L1

DISPLAY	
(4 digit 7-segment display)	
CA	W7
CB	W6
CC	U8
CD	V8
CE	U5
CF	V5
CG	U7
CDP	V7
AN0	U2
AN1	U4
AN2	V4
AN3	W4

function	FPGA pin
BUTTONS	
BTNL	W19
BTNR	T17
BTNU	T18
BTND	U17
BTNC	U18

SWITCHES	
SW0	V17
SW1	V16
SW2	W16
SW3	W17
SW4	W15
SW5	V15
SW6	W14
SW7	W13
SW8	V2
SW9	T3
SW10	T2
SW11	R3
SW12	W2
SW13	U1
SW14	T1
SW15	R2

CLOCKS	
system (100 MHz)	W5

reverse look-up	
FPGA pin	function
E19	LD1
L1	LD15
N3	LD13
P1	LD14
P3	LD12
R2	SW15
R3	SW11
T1	SW14
T2	SW10
T3	SW9
T17	BTNR
T18	BTNU
U1	SW13
U2	AN0
U3	LD11
U4	AN1
U5	CE
U7	CG
U8	CC
U14	LD6
U15	LD5
U16	LD0
U17	BTND
U18	BTNC
U19	LD2

reverse look-up	
FPGA pin	function
V13	LD8
V14	LD7
V15	SW5
V16	SW1
V17	SW0
V19	LD3
V2	SW8
V3	LD9
V4	AN2
V5	CF
V7	CDP
V8	CD
W2	SW12
W3	LD10
W4	AN3
W5	Sys Clock
W6	CB
W7	CA
W13	SW7
W14	SW6
W15	SW4
W16	SW2
W17	SW3
W18	LD4
W19	BTNL