Shriya Shukla

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Education

University of Michigan, Ann Arbor **August 2024 – December 2025**

Master's in Electrical Engineering and Computer Science (Integrated Circuits and VLSI track)

Relevant Coursework: Computer Architecture, VLSI for ML, Parallel Computer Architecture, Microarchitecture, VLSI Design (Fall'25), Advance Operation Systems (Fall'25)

Vellore Institute of Technology, Chennai **July 2016 – June 2020**

Bachelors of Technology in Electronics and Communication Engineering

Relevant Coursework: Semiconductor Devices and Circuits, Digital Logic Design, Applied Linear Algebra, Digital Signal Processing, VLSI System Design, Computer Organization and Architecture

Projects

- **2-Way Superscalar Out-of-Order R10K RISC-V Processor** **Fall 2024**
  - Engineered a 2-way superscalar R10K RISC-V processor with write-back DCache, Dual-Ported ICache, Store Queue and PAg branch predictor using SystemVerilog and Verilog (CPI: 3.96)
  - Tested modules with Synopsys VCS and debugged signals in Verdi
- **Adaptive Resource Allocation in Hybrid CPU-GPU Systems for Optimizing TSP** **Winter 2025**
  - Developed a dynamic scheduler to split metaheuristic Travelling Salesman Problem solvers across CPU and GPU using CUDA and C++
  - Profiled execution with Nsight and VTune, achieving 30× speedup and 9× error reduction via dynamic workload reallocation.
- **Hardware Accelerator for Sequence-to-Graph Alignment** **Winter 2025**
  - Designed a systolic-array accelerator for Smith-Waterman alignment over genome graphs using SystemVerilog
  - Implemented and verified control and memory modules, achieving 30× speedup on short reads

Professional Experience

Rivian Automotive, Palo Alto

Design Verification Intern **May 2025 – August 2025**

- Contributing to UVM-based design verification under the Electrical Hardware team

Qualcomm, Bangalore

Senior Performance Verification Engineer **June 2020 – August 2024**

- Verified performance for 10+ DSP cores using RTL simulation and emulation, and addressed critical design issues early in the development process
- Developed micro-benchmarks in C++ and Assembly by adapting real application kernels to identify and resolve performance bottlenecks in RTL simulation and emulation
- Debugged RTL setups and automation scripts, identifying key performance bottlenecks and reducing workflow interruptions by over 30%
- Designed and documented performance experiments in a pre-silicon environment, providing design feedback for next-generation cores based on observed results
- Monitored performance measuring data to identify and interpret performance changes based on input workloads
- Diagnosed and resolved correlation issues between RTL-ISS and emulation-silicon platforms, reducing correlation error to under 5% and improving performance prediction accuracy for next-gen cores
- Built end-to-end workflows with Python scripts to run ML applications for monitoring power and performance across simulation platforms

Qualcomm, Bangalore

Interim Engineering Intern **January 2020 – June 2020**

- Automated DSP core snapshot generation using Python, cutting processing time and speeding up test creation
- Solved RTL-ISS snapshot mismatches by identifying root causes and ensuring output consistency

Skills

Languages: C/C++, Verilog/SystemVerilog, MATLAB, Assembly, Python, Bash
Verification: UVM, Synopsys VCS, Verdi, Emulation, Performance Monitoring Tools
Tools: Intel VTune, NVIDIA Nsight, Synopsys Design Compiler, Git, Makefile