

# JEDEC STANDARD

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**LPDDR6 Standard**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## LPDDR6 Standard

(From JEDEC Board Ballot number JCB-25-45, formulated under the cognizance of the JC-42.6 subcommittee on Low Power Memories, item 1891.99B).

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### 1 Scope

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This standard defines the LPDDR6 standard, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this standard is to define the minimum set of requirements for a JEDEC compliant x24 one channel SDRAM device. LPDDR6 device density ranges from 4 Gb to 64 Gb. This standard was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), DDR5 (JESD79-5), LPDDR (JESD209), LPDDR2 (JESD209-2), LPDDR3 (JESD209-3), LPDDR4 (JESD209-4), and LPDDR5 (JESD209-5).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated to prepare the LPDDR6 standard<sup>1</sup>.

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<sup>1</sup> Strikethroughs were intentionally added to the contents of a few tables to indicate that these are pending committee approval; i.e., place holders.

## 2 Overview

---

### 2.1 Features

TBD

### 2.2 Functional Description

LPDDR6 SDRAM is a high-speed synchronous SDRAM device internally configured with two sub-channels containing 24 DQ signals, two pairs of differential data clock (WCK) and two pairs of differential Read Data Strobe (RDQS). The bank architecture is four banks with four bank groups per sub-channel for LPDDR6 SDRAM. See 2.2.2 for more information.

Density can range from 4 Gb to 64 Gb. These LPDDR6 SDRAM devices contain the following number of bits:

- 4 Gb has 4,294,967,296 bits
- 6 Gb has 6,442,450,944 bits
- 8 Gb has 8,589,934,592 bits
- 12 Gb has 12,884,901,888 bits
- 16 Gb has 17,179,869,184 bits
- 24 Gb has 25,769,803,776 bits
- 32 Gb has 34,359,738,368 bits
- 48 Gb has 51,539,607,552 bits
- 64 Gb has 68,719,477,736 bits

LPDDR6 SDRAM devices use a command clock (CK) that operates at a reduced rate from per 12-DQ data clock (WCK). There are four (DDR) command/address (CA) pins that the memory controller uses to transmit command, address, bank, configuration, and training information to the SDRAM. CA signals are latched on both the rising and falling CK edges when indicated by a high signal on the single (SDR) CS pin. Most commands are 2nCK in duration. See Table 254 for details.

The WCK:CK ratio is 2:1 for all frequency. For low-power operation the WCK is generally designed to operate only when read or write data needs to be transmitted on the bus. Due to the high speeds required for WCK, the LPDDR6 SDRAM generally implements circuitry to divide the WCK frequency immediately after the WCK receiver. This leads to a requirement to synchronize WCK to CK when the WCK needs to be re-started from an idle time. See Table 254 for details.

The double-data-rate I/O signaling in high-speed modes is designed to operate with on-die termination on both the memory controller and the LPDDR6 SDRAM. The high-speed I/O was designed to operate with a VDDQ of 0.5 V nominal. Signals from the memory controller to the SDRAM were designed assuming a Voh of 0.5\*VDDQ, or 250 mV. Signals from the SDRAM to the memory controller are calibrated to 0.5\*VDDQ, or 250 mV nominal. In low-speed modes the signaling may operate unterminated with nominal VDDQ in a range from 0.3 V – 0.5 V both to and from the SDRAM, with some limitations.

Data access size depends on the burst length, with 12n and 24n prefetches supported. A single BL24 Read or Write access for a 12-DQ Sub-Channel LPDDR6 SDRAM, typically consists of a single 288-bit (256-bit data and 32-bit non-data) transfer at the internal SDRAM core, and twelve corresponding 12-bit wide, one half-WCK-clock-cycle data transfers at the I/O pins.

## 2.2 Functional Description (cont'd)

Read and Write accesses to LPDDR6 SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command. When issuing a Read or Write, WCK must be synchronized to CK by issuing a WCK2CK SYNC operand (WS="H") in a Read (RD) or Write (WR) or Mode Register Read(MRR) or Write FIFO (WFF) or Read FIFO (RFF) or Read DQ Calibration (RDC) command.

The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR6 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure sections provide detailed information covering device initialization.

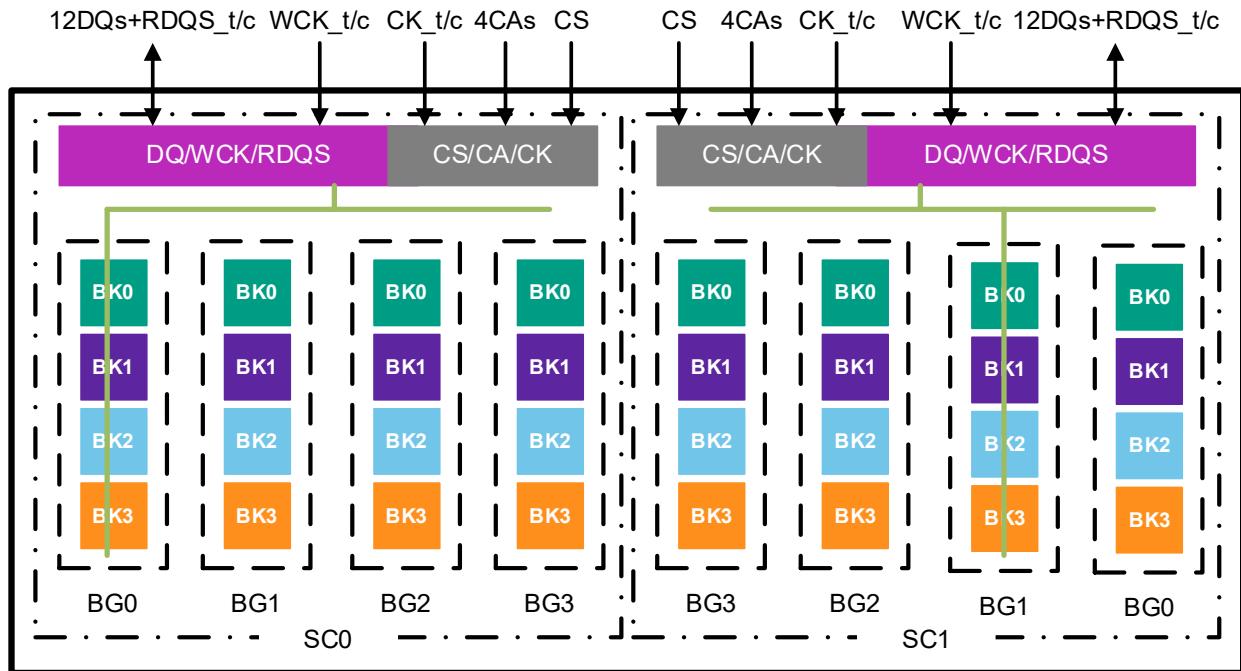
## 2.2.1 Pad Definition and Description

Table 1 – Pad Definition and Description

Symbol	Type	Description	Note
CK0_t, CK0_c CK1_t, CK1_c	Input	<b>Clock:</b> CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c). One pair for each sub-channel.	
CS0, CS1	Input	<b>Chip Select:</b> CS is part of the command code, and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down mode where it becomes an asynchronous signal.	1
CA0[3:0], CA1[3:0]	Input	<b>Command/Address Inputs:</b> CA signals provide the Command and Address input according to the Command Truth Table	1
DQ0[11:0], DQ1[11:0]	I/O	<b>Data Input/Output:</b> Bi-direction data bus.	1, 2
WCK0_t, WCK0_c, WCK1_t, WCK1_c	Input	<b>Data Clocks:</b> WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output. One pair for each sub-channel.	1
RDQS0_t , RDQS0_c , RDQS1_t , RDQS1_c	Output	<b>Read Data Strobe:</b> RDQS_t and RDQS_c are the differential output clock signals used to strobe data during a READ operation. One pair for each sub-channel.	1
ZQ	Reference	<b>ZQ:</b> ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor.	
VDDQ, VDD1, VDD2C, VDD2D	Supply	<b>Power Supplies:</b> Isolated on the die for improved noise immunity.	
VSS	GND	<b>Ground Reference:</b> Power supply ground reference	
RESET_n	Input	<b>RESET:</b> When asserted LOW, the RESET_n signal resets the die. Reset_n is an asynchronous signal.	
ALERT	Output	<b>ALERT:</b> If error is detected and reported to fault register, ALERT goes HIGH for a time interval and goes back LOW. If the ALERT is not used, the ALERT pin must be pulled to VSS on the board.	
NOTE 1 Sub-channel 0 and Sub-channel 1 have independent pads.			
NOTE 2 There is no DMI in LPDDR6.			

## 2.2.2 Block Diagram

### 2.2.2.1 x24 DQs Normal Mode Configuration



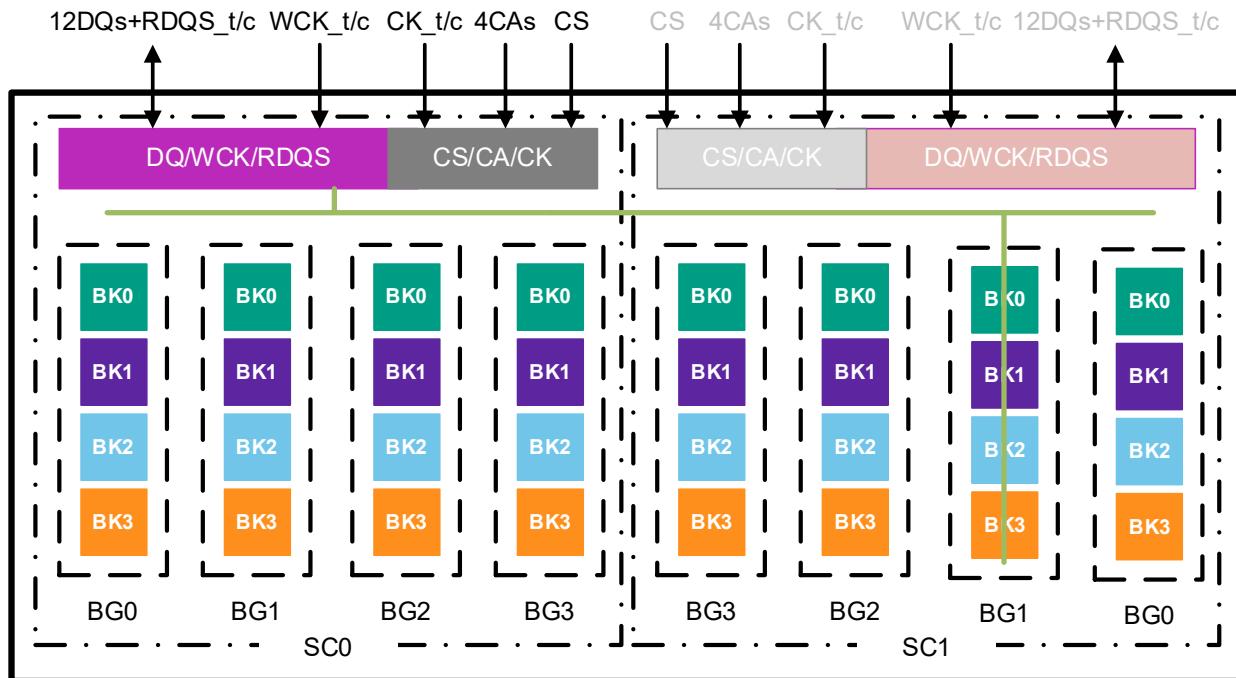
NOTE 1 Meaning of abbreviation is below.

- SC: Sub-Channel
- BG: Bank Group
- BK: Bank

NOTE 2 MR0 OP[2]=0<sub>B</sub>: Device is switchable both normal and Dynamic Efficiency mode  
MR1 OP[6]=0<sub>B</sub>: Normal

**Figure 1 – x24 Mode Configuration (Normal Mode) Example**

### 2.2.2.2 x12 DQs Dynamic Efficiency Mode Configuration



NOTE 1 Meaning of abbreviation is below.

- SC: Sub-Channel
- BG: Bank Group
- BK: Bank

NOTE 2 SC0/SC1 of sub-channel is indicated each sub-channel's MR0 OP[3].

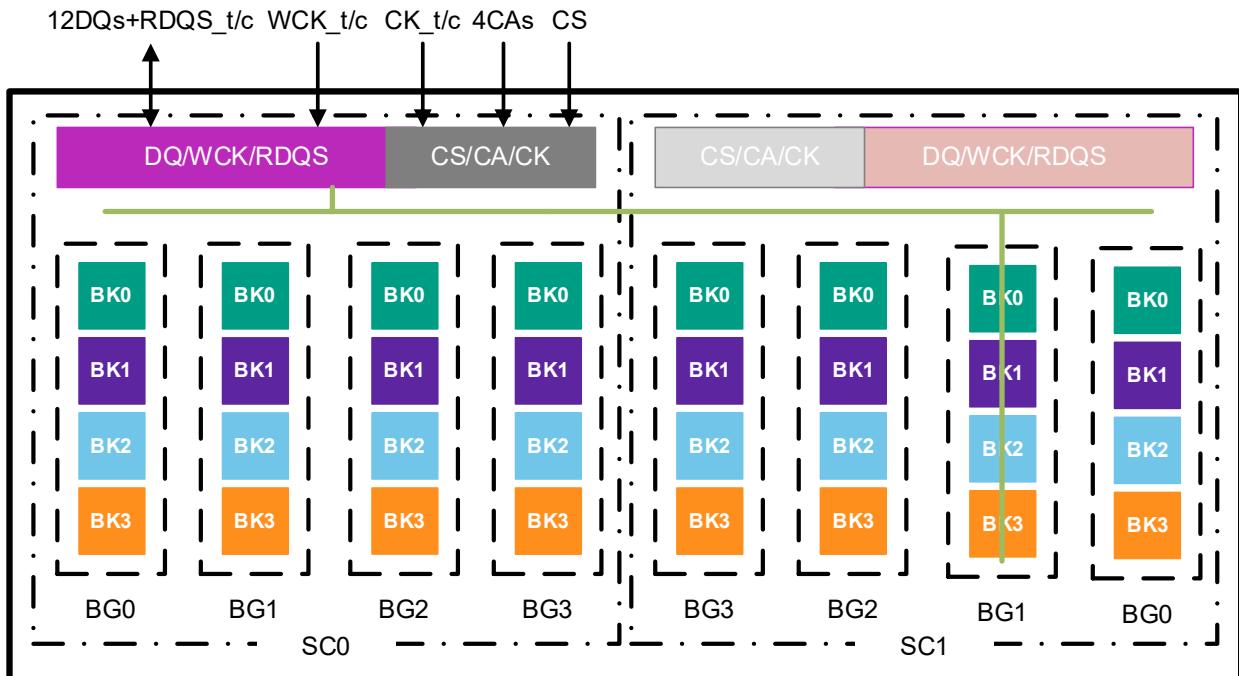
NOTE 3 CS, CK, CA, WCK, DQ and RDQS for SC1 is in-active during Dynamic Efficiency mode.

NOTE 4 MR0 OP[2]=0<sub>b</sub>: Device is switchable both normal and Dynamic Efficiency mode

MR1 OP[6]=1<sub>b</sub>: Dynamic Efficiency mode

**Figure 2 – x12 Mode Configuration (Dynamic Efficiency Mode) Example**

### 2.2.2.3 x12 DQs Static Efficiency Mode Configuration



NOTE 1 Meaning of abbreviation is below.

- SC: Sub-Channel
- BG: Bank Group
- BK: Bank

NOTE 2 SC0/SC1 of sub-channel is indicated each sub-channel's MR0 OP[3].

NOTE 4 MR0 OP[2]=1<sub>B</sub>: Device supports Efficiency mode only (Static Efficiency mode)  
MR1 OP[6]=Don't Care

**Figure 3 – x12 mode Configuration (Static Efficiency Mode) Example**

### 2.2.3 LPDDR6 SDRAM Addressing

**Table 2 – LPDDR6 SDRAM x12 Addressing for Normal (No-Efficiency) Mode**

Sub-Channel Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Number of Banks in BG	4	4	4	4	4	4	4	4	4
Number of Bank Groups	4	4	4	4	4	4	4	4	4
Array Pre-Fetch	256	256	256	256	256	256	256	256	256
Number of Rows	8,192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns	64	64	64	64	64	64	64	64	64
Page Size (Bytes)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
Density	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1
Bank Group Addresses	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1
Row Addresses	R0 - R12	R0 - R13 (R12=0 when R13=1)	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Native Burst Length	24	24	24	24	24	24	24	24	24

NOTE 1 Die density is twice as sub-channel density.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

### 2.2.3 LPDDR6 SDRAM Addressing (cont'd)

**Table 3 – LPDDR6 SDRAM x12 Addressing for Efficiency Mode**

Die Density	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb	48Gb	64Gb
Number of Sub-Channel	2	2	2	2	2	2	2	2	2
Number of Banks in BG	4	4	4	4	4	4	4	4	4
Number of Bank Groups	4	4	4	4	4	4	4	4	4
Array Pre-Fetch	256	256	256	256	256	256	256	256	256
Number of Rows	8,192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns	64	64	64	64	64	64	64	64	64
Page Size (Bytes)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
Density	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368	51539607552	68719476736
Bank Address	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1
Bank Group Addresses	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1
Row Addresses	R0 - R12	R0 - R13 (R12=0 when R13=1)	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Native Burst Length	24	24	24	24	24	24	24	24	24

NOTE 1 Sub-Channel is selected by SC flag. See Command Truth table: Table 254 for detail.

NOTE 2 Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

NOTE 3 For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

NOTE 4 A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

## 2.3 Speed Grade

**Table 4 — LPDDR6 Speed Grade and Support Function**

## 2.4 Data Packet Format

LPDDR6 SDRAM Data packet format consists of 12 DQ pins and 24 beat length, and has 256 data fields and 32 metadata fields. The metadata fields are divided into two segments, and each segment can contain two bytes. The contents of the metadata depend on the enabled features.

### 2.4.1 Features Related to the Metadata Contents

LPDDR6 SDRAM features that modifies metadata contents and their mutual relationship are summarized in Table 5.

**Table 5 – Features Related to Metadata Contents**

Features			Combined function	Note
Link-protection	DBI	System-meta		
Disabled	Disabled	<b>Enabled</b>	System-meta	
Disabled	<b>Enabled</b>	Disabled	DBI	
Disabled	<b>Enabled</b>	<b>Enabled</b>	DBI & System-meta	Two-byte-base DBI only for data bits (not cover System metadata bits)
<b>Enabled</b>	Disabled	Disabled	Link-protection	
<b>Enabled</b>	Disabled	<b>Enabled</b>	Link-protection & System-meta	Link-protection covers system-meta bits
<b>Enabled</b>	<b>Enabled</b>	Disabled	Prohibited setting	Link-protection and DBI are exclusive function
<b>Enabled</b>	<b>Enabled</b>	<b>Enabled</b>	Prohibited setting	All features cannot be enabled together

### 2.4.2 Data Packet Format

Data packet field assignment for each function are defined following tables.

**Table 6 – Normal Mode Data Packet Field Assignment**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	FIXL	FIXL	FIXL	FIXL	D144	D145	D146	D147	D192	D193	D194	D195	FIXL	FIXL	FIXL	FIXL
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	FIXL	FIXL	FIXL	FIXL	D148	D149	D150	D151	D196	D197	D198	D199	FIXL	FIXL	FIXL	FIXL
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	FIXL	FIXL	FIXL	FIXL	D168	D169	D170	D171	D216	D217	D218	D219	FIXL	FIXL	FIXL	FIXL
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	FIXL	FIXL	FIXL	FIXL	D172	D173	D174	D175	D220	D221	D222	D223	FIXL	FIXL	FIXL	FIXL

## 2.4.2 Data Packet Format (cont'd)

**Table 7 – Data Packet Field Assignment when System-Meta is Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	M0	M1	M2	M3	D144	D145	D146	D147	D192	D193	D194	D195	FIXL	FIXL	FIXL	FIXL
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	M4	M5	M6	M7	D148	D149	D150	D151	D196	D197	D198	D199	FIXL	FIXL	FIXL	FIXL
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	M8	M9	M10	M11	D168	D169	D170	D171	D216	D217	D218	D219	FIXL	FIXL	FIXL	FIXL
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	M12	M13	M14	M15	D172	D173	D174	D175	D220	D221	D222	D223	FIXL	FIXL	FIXL	FIXL

**Table 8 – Data Packet Field Assignment when DBI is Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	FIXL	FIXL	FIXL	FIXL	D144	D145	D146	D147	D192	D193	D194	D195	I0	I1	I2	I3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	FIXL	FIXL	FIXL	FIXL	D148	D149	D150	D151	D196	D197	D198	D199	I4	I5	I6	I7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	FIXL	FIXL	FIXL	FIXL	D168	D169	D170	D171	D216	D217	D218	D219	I8	I9	I10	I11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	FIXL	FIXL	FIXL	FIXL	D172	D173	D174	D175	D220	D221	D222	D223	I12	I13	I14	I15

NOTE 1 I\* fields are for DBI control bits. I0 associates:D0:D15, I1 associates:D16:D31, I2 associates:D32:D47, I3 associates:D48:D63, I4 associates:D64:D79, I5 associates:D80:D95, I6 associates:D96:D111, I7 associates:D112:D127, I8 associates:D128:D143, I9 associates:D144:D159, I10 associates:D160:D175, I11 associates:D176:D191, I12 associates:D192:D207, I13 associates:D208:D223, I14 associates:D224:D239, I15 associates:D240:D255

## 2.4.2 Data Packet Format (cont'd)

**Table 9 – Data Packet Field Assignment when Link-Protection is Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	FIXL	FIXL	FIXL	FIXL	D144	D145	D146	D147	D192	D193	D194	D195	L0	L1	L2	L3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	FIXL	FIXL	FIXL	FIXL	D148	D149	D150	D151	D196	D197	D198	D199	L4	L5	L6	L7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	FIXL	FIXL	FIXL	FIXL	D168	D169	D170	D171	D216	D217	D218	D219	L8	L9	L10	L11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	FIXL	FIXL	FIXL	FIXL	D172	D173	D174	D175	D220	D221	D222	D223	L12	L13	L14	L15

NOTE 1 L\* fields are for Link-protection data bits.

**Table 10 – Data Packet Field Assignment when System-Meta and DBI are Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	M0	M1	M2	M3	D144	D145	D146	D147	D192	D193	D194	D195	I0	I1	I2	I3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	M4	M5	M6	M7	D148	D149	D150	D151	D196	D197	D198	D199	I4	I5	I6	I7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	M8	M9	M10	M11	D168	D169	D170	D171	D216	D217	D218	D219	I8	I9	I10	I11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	M12	M13	M14	M15	D172	D173	D174	D175	D220	D221	D222	D223	I12	I13	I14	I15

NOTE 1 M\* fields are for system metadata bits, Note 1: I\* fields are for DBI control bits (refer to Table 8 Note 1).

NOTE 2 system metadata bits (M[0:15]) are not scope of DBI calculations.

## 2.4.2 Data Packet Format (cont'd)

**Table 11 – Data Packet Field Assignment when System-Meta and Link-Protection are Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	M0	M1	M2	M3	D144	D145	D146	D147	D192	D193	D194	D195	L0	L1	L2	L3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	M4	M5	M6	M7	D148	D149	D150	D151	D196	D197	D198	D199	L4	L5	L6	L7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	M8	M9	M10	M11	D168	D169	D170	D171	D216	D217	D218	D219	L8	L9	L10	L11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	M12	M13	M14	M15	D172	D173	D174	D175	D220	D221	D222	D223	L12	L13	L14	L15

NOTE 1 M\* fields are for system metadata bits, L\* fields are for Link-protection data bits.

### 2.4.3 Read Burst Chunk and Order

### 2.4.3.1 Read Data and Meta Data

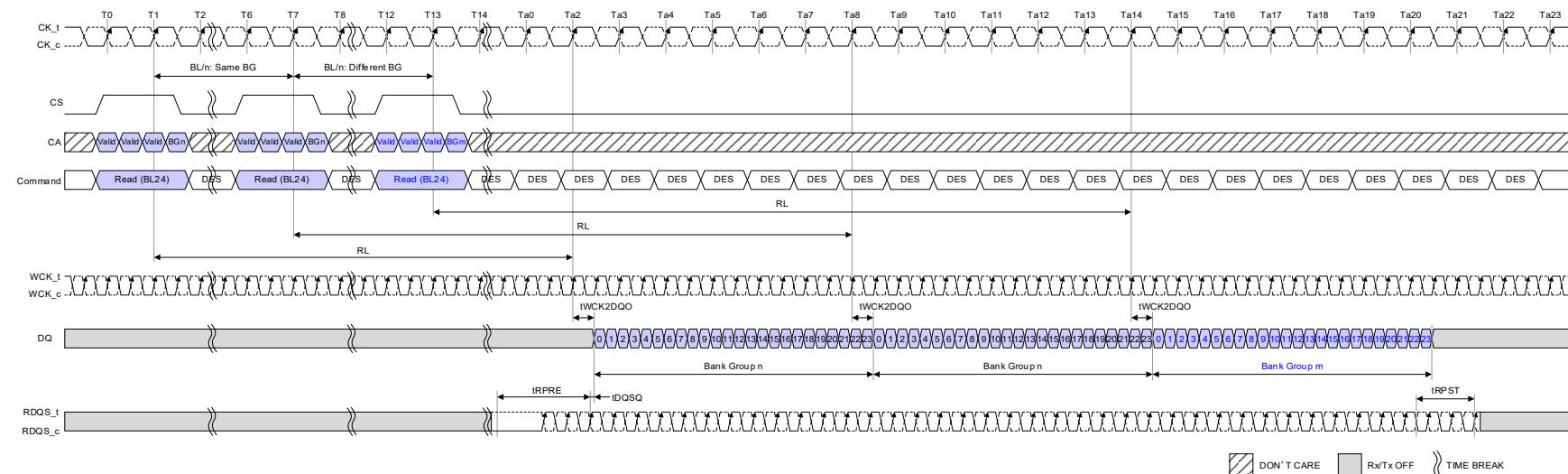
Read operation uses 12 DQs per sub channel to output Data. Read meta data includes Link Protection and system Meta.

### 2.4.3.2 Read Burst Chunk and Sequence

LPDDR6 SDRAM supports 32byte (BL24) and 64byte (BL48) chunk. Details are shown below.

#### 2.4.3.2.1 Read BL24 Operation: 32byte Access

LPDDR6 Read burst chunk is defined 32byte data, Data bus Inversion flag and Meta data mapped to 24beats as unit. There is no Read burst start address selectable within 24beats access. It means that LPDDR6 Read BL24 operation supports only fixed burst order.



NOTE 1 tWCK2CK is 0 ps in this instance.

**NOTE 2** WCK Always On mode

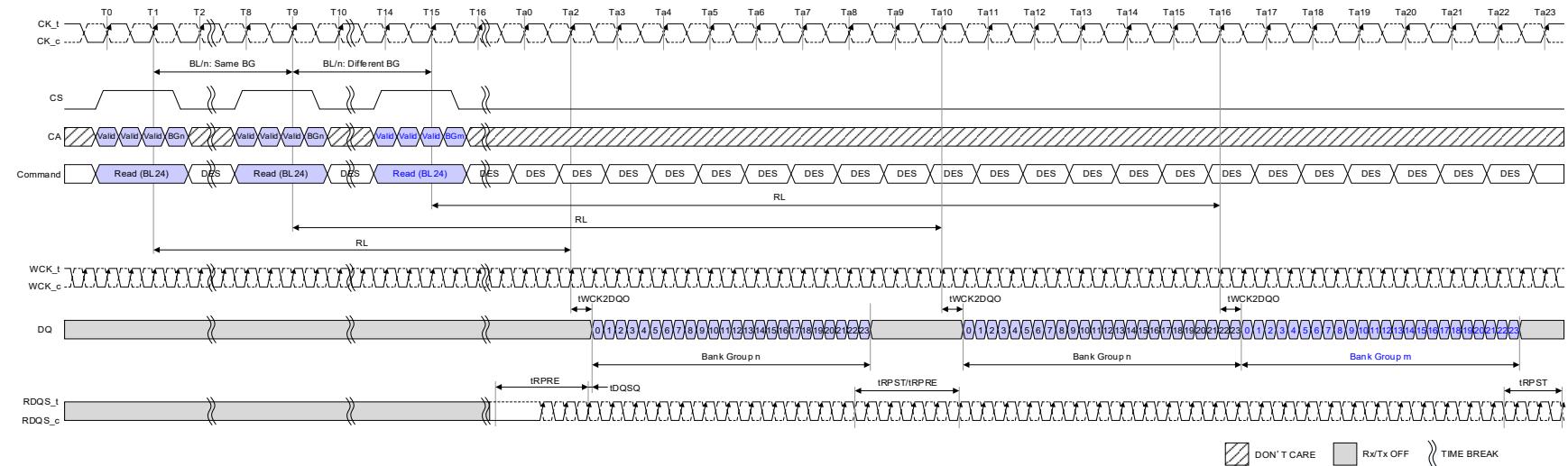
NOTE 3 BL/n: Same BG varies depending on Data Rate. Refer to Table 382- Same BG tCCD Timing Definition for detail.

NOTE 4 BL/n: Same BG=6nCK. BL/n: Different BG=6nCK.

**NOTE 5** DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 4 – Read Operation, BL24, BL/n: Same BG=6nCK**

### 2.4.3.2.1 Read BL24 Operation: 32byte Access (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK Always On mode

NOTE 3 BL/n: Same BG varies depending on Data Rate, Refer to Table 382 - Same BG tCCD Timing Definition for detail.

NOTE 4 Refer to the Table 282 — RDQS Pattern Definition for the behavior of tRPST/tRPRE during the period when RDQS Preamble and Postamble are in conflict.

NOTE 5 BL/n: Same BG=8nCK, BL/n: Different BG=6nCK,

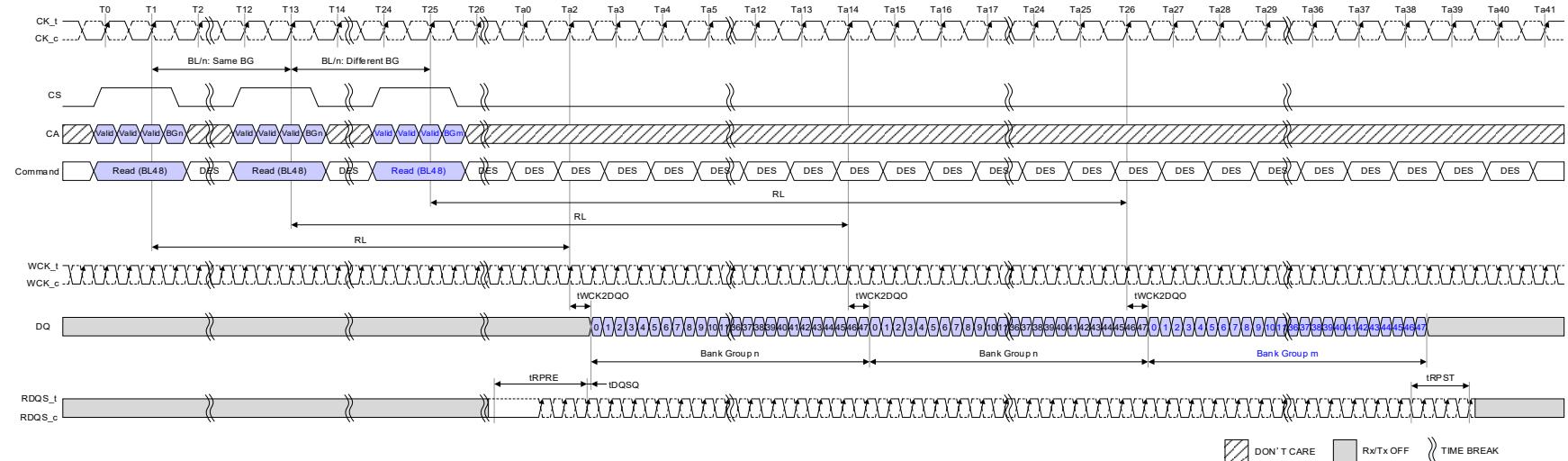
NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 5 – Read Operation, BL24, BL/n: Same BG=8nCK

### 2.4.3.2.2 Read Operation: 64byte Access

LPDDR6 Read burst chunk is defined 64byte data, Data bus Inversion flag and Meta data mapped to each 24beats as unit and Read 64byte command can select burst start order by C0.

When Data Rate is equal or less than 6400 Mbps ( $\leq$  6400 Mbps), LPDDR6 supports gapless 64byte. When data rate is higher than 6400 Mbps ( $>$  6400 Mbps), LPDDR6 supports interleaved 64byte access with 24beat gap.



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK Always On mode

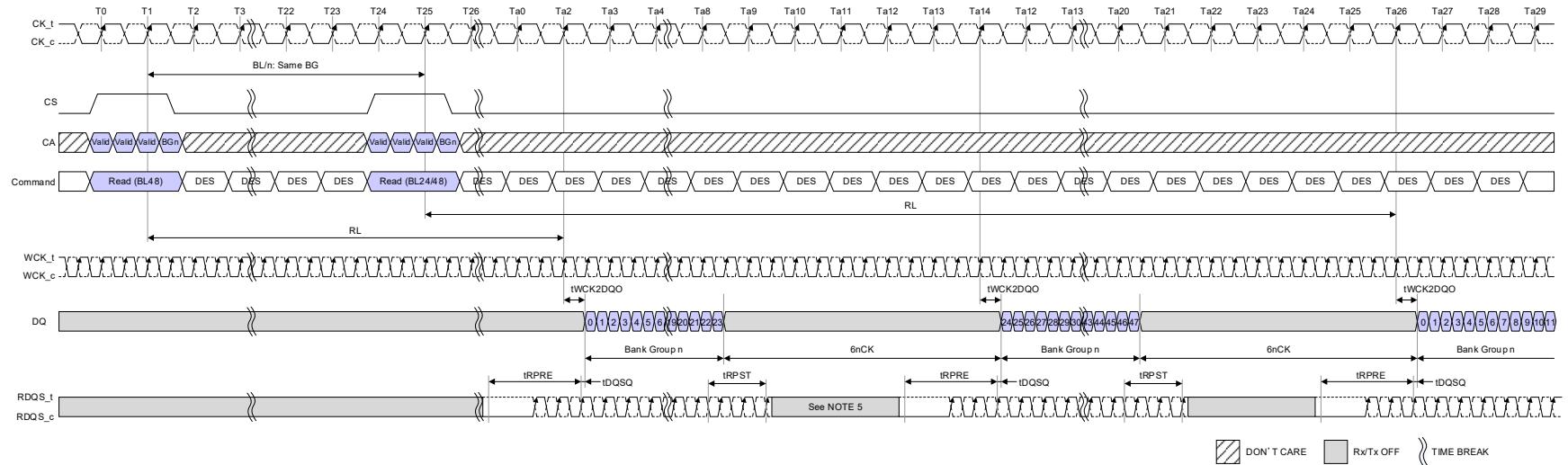
NOTE 3 BL/n: Same BG varies depending on Data Rate, Refer to Table 382- Same BG tCCD Timing Definition for detail.

NOTE 4 BL/n: Same BG=12nCK, BL/n: Different BG=12nCK,

NOTE 5 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 6 – Read Operation, BL48, BL/n: Same BG=12nCK, Non-Interleave**

### 2.4.3.2.2 Read Operation: 64byte Access (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK Always On mode

NOTE 3 BL/n: Same BG varies depending on Data Rate, Refer to Table 382 - Same BG tCCD Timing Definition for detail.

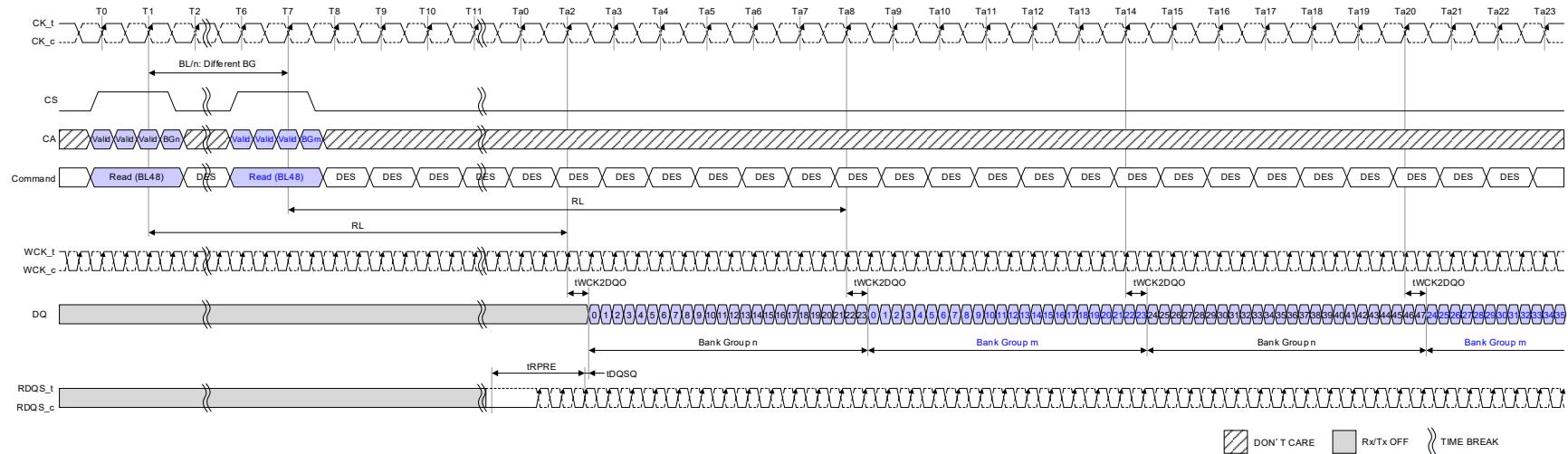
NOTE 4 BL/n: Same BG=24nCK

NOTE 5 RDQS output between Beat23 and Beat24 is disabled.

NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 7 – Read Operation followed by Read Command to Same BG, BL48, BL/n: Same BG=24nCK, Interleave**

#### **2.4.3.2.2 Read Operation: 64byte Access (cont'd)**



NOTE 1 tWCK2CK is 0 ps in this instance.

## NOTE 2 WCK Always On mode

NOTE 3 BL/n: Different BG=6nCK

**NOTE 4** DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 8 – Read Operation followed by Read Command to Different BG, BL48, Interleave**

## **2.4.4 Write Burst Chunk and Order**

### **2.4.4.1 Write Data and Meta Data**

Write data burst assigned the same as Read operation. Write meta data includes Link Protection and system Meta.

### **2.4.4.2 Write Burst Chunk and Sequence**

LPDDR6 SDRAM supports 32byte (BL24) and 64byte (BL48) chunk. Details are shown below.

#### **2.4.4.2.1 Write BL24 Operation: 32byte Access**

LPDDR6 Write burst chunk is defined 32byte data, Enhanced Data bus Inversion flag and Meta data mapped to 24beats as unit. There is no write burst start address selectable with in 24beats access. It means that LPDDR6 Write BL24 operation supports only fixed burst order.

Write data input scheme is the same as Read operation.

#### **2.4.4.2.2 Write Operation: 64byte Access**

LPDDR6 Write burst chunk is defined 64byte data, Enhanced Data bus Inversion flag and Meta data mapped to each 24beats as unit. Write 64byte command support only fixed Write burst sequence.

When Data Rate is equal or less than 6400 Mbps ( $\leq$  6400 Mbps), LPDDR6 supports gapless 64byte. When data rate is higher than 6400 Mbps ( $>$  6400 Mbps), LPDDR6 supports interleaved 64byte access with 24beat gap.

Write data input scheme is the same as Read operation too.

## 2.4.5 Burst Sequence

Refer to clause 2.4.2 Data Packet Format for Read/Write burst sequence of BL24.

**Table 12 – Burst Sequence (BL48) for READ: C0=0**

		Beat																							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0		D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1		D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2		D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3		D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4		D16	D17	D18	D19	D64	D65	D66	D67	FIXL/ M0	FIXL/ M1	FIXL/ M2	FIXL/ M3	D144	D145	D146	D147	D192	D193	D194	D195	FIXL/ L0/ I0	FIXL/ L1/ I1	FIXL/ L2/ I2	FIXL/ L3/ I3
DQ5		D20	D21	D22	D23	D68	D69	D70	D71	FIXL/ M4	FIXL/ M5	FIXL/ M6	FIXL/ M7	D148	D149	D150	D151	D196	D197	D198	D199	FIXL/ L4/ I4	FIXL/ L5/ I5	FIXL/ L6/ I6	FIXL/ L7/ I7
DQ6		D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7		D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8		D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9		D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10		D40	D41	D42	D43	D88	D89	D90	D91	FIXL/ M8	FIXL/ M9	FIXL/ M10	FIXL/ M11	D168	D169	D170	D171	D216	D217	D218	D219	FIXL/ L8/ I8	FIXL/ L9/ I9	FIXL/ L10/ I10	FIXL/ L11/ I11
DQ11		D44	D45	D46	D47	D92	D93	D94	D95	FIXL/ M12	FIXL/ M13	FIXL/ M14	FIXL/ M15	D172	D173	D174	D175	D220	D221	D222	D223	FIXL/ L12/ I12	FIXL/ L13/ I13	FIXL/ L14/ I14	FIXL/ L15/ I15
		Beat																							
		24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DQ0		D256	D257	D258	D259	D304	D305	D306	D307	D352	D353	D354	D355	D384	D385	D386	D387	D432	D433	D434	D435	D480	D481	D482	D483
DQ1		D260	D261	D262	D263	D308	D309	D310	D311	D356	D357	D358	D359	D388	D389	D390	D391	D436	D437	D438	D439	D484	D485	D486	D487
DQ2		D264	D265	D266	D267	D312	D313	D314	D315	D360	D361	D362	D363	D392	D393	D394	D395	D440	D441	D442	D443	D488	D489	D490	D491
DQ3		D268	D269	D270	D271	D316	D317	D318	D319	D364	D365	D366	D367	D396	D397	D398	D399	D444	D445	D446	D447	D492	D493	D494	D495
DQ4		D272	D273	D274	D275	D320	D321	D322	D323	FIXL/ M16	FIXL/ M17	FIXL/ M18	FIXL/ M19	D400	D401	D402	D403	D448	D449	D450	D451	FIXL/ L16/ I16	FIXL/ L17/ I17	FIXL/ L18/ I18	FIXL/ L19/ I19
DQ5		D276	D277	D278	D279	D324	D325	D326	D327	FIXL/ M20	FIXL/ M21	FIXL/ M22	FIXL/ M23	D404	D405	D406	D407	D452	D453	D454	D455	FIXL/ L20/ I20	FIXL/ L21/ I21	FIXL/ L22/ I22	FIXL/ L23/ I23
DQ6		D280	D281	D282	D283	D328	D329	D330	D331	D368	D369	D370	D371	D408	D409	D410	D411	D456	D457	D458	D459	D496	D497	D498	D499
DQ7		D284	D285	D286	D287	D332	D333	D334	D335	D372	D373	D374	D375	D412	D413	D414	D415	D460	D461	D462	D463	D500	D501	D502	D503
DQ8		D288	D289	D290	D291	D336	D337	D338	D339	D376	D377	D378	D379	D416	D417	D418	D419	D464	D465	D466	D467	D504	D505	D506	D507
DQ9		D292	D293	D294	D295	D340	D341	D342	D343	D380	D381	D382	D383	D420	D421	D422	D423	D468	D469	D470	D471	D508	D509	D510	D511
DQ10		D296	D297	D298	D299	D344	D345	D346	D347	FIXL/ M24	FIXL/ M25	FIXL/ M26	FIXL/ M27	D424	D425	D426	D427	D472	D473	D474	D475	FIXL/ L24/ I24	FIXL/ L25/ I25	FIXL/ L26/ I26	FIXL/ L27/ I27
DQ11		D300	D301	D302	D303	D348	D349	D350	D351	FIXL/ M28	FIXL/ M29	FIXL/ M30	FIXL/ M31	D428	D429	D430	D431	D476	D477	D478	D479	FIXL/ L28/ I28	FIXL/ L29/ I29	FIXL/ L30/ I30	FIXL/ L31/ I31

NOTE 1 Data assigned “FIXL/ Mx” and “FIXL/ Lx/ Ix” uses Meta, Link Protection and Data Bus Inversion.

## 2.4.5 Burst Sequence (cont'd)

**Table 13 – Burst Sequence (BL48) for READ: C0=1**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
<b>DQ0</b>	D256	D257	D258	D259	D304	D305	D306	D307	D352	D353	D354	D355	D384	D385	D386	D387	D432	D433	D434	D435	D480	D481	D482	D483
<b>DQ1</b>	D260	D261	D262	D263	D308	D309	D310	D311	D356	D357	D358	D359	D388	D389	D390	D391	D436	D437	D438	D439	D484	D485	D486	D487
<b>DQ2</b>	D264	D265	D266	D267	D312	D313	D314	D315	D360	D361	D362	D363	D392	D393	D394	D395	D440	D441	D442	D443	D488	D489	D490	D491
<b>DQ3</b>	D268	D269	D270	D271	D316	D317	D318	D319	D364	D365	D366	D367	D396	D397	D398	D399	D444	D445	D446	D447	D492	D493	D494	D495
<b>DQ4</b>	D272	D273	D274	D275	D320	D321	D322	D323	FIXL/ M16	FIXL/ M17	FIXL/ M18	FIXL/ M19	D400	D401	D402	D403	D448	D449	D450	D451	FIXL/ L16/L16	FIXL/ L17/L17	FIXL/ L18/L18	FIXL/ L19/L19
<b>DQ5</b>	D276	D277	D278	D279	D324	D325	D326	D327	FIXL/ M20	FIXL/ M21	FIXL/ M22	FIXL/ M23	D404	D405	D406	D407	D452	D453	D454	D455	FIXL/ L20/L20	FIXL/ L21/L21	FIXL/ L22/L22	FIXL/ L23/L23
<b>DQ6</b>	D280	D281	D282	D283	D328	D329	D330	D331	D368	D369	D370	D371	D408	D409	D410	D411	D456	D457	D458	D459	D496	D497	D498	D499
<b>DQ7</b>	D284	D285	D286	D287	D332	D333	D334	D335	D372	D373	D374	D375	D412	D413	D414	D415	D460	D461	D462	D463	D500	D501	D502	D503
<b>DQ8</b>	D288	D289	D290	D291	D336	D337	D338	D339	D376	D377	D378	D379	D416	D417	D418	D419	D464	D465	D466	D467	D504	D505	D506	D507
<b>DQ9</b>	D292	D293	D294	D295	D340	D341	D342	D343	D380	D381	D382	D383	D420	D421	D422	D423	D468	D469	D470	D471	D508	D509	D510	D511
<b>DQ10</b>	D296	D297	D298	D299	D344	D345	D346	D347	FIXL/ M24	FIXL/ M25	FIXL/ M26	FIXL/ M27	D424	D425	D426	D427	D472	D473	D474	D475	FIXL/ L24/L24	FIXL/ L25/L25	FIXL/ L26/L26	FIXL/ L27/L27
<b>DQ11</b>	D300	D301	D302	D303	D348	D349	D350	D351	FIXL/ M28	FIXL/ M29	FIXL/ M30	FIXL/ M31	D428	D429	D430	D431	D476	D477	D478	D479	FIXL/ L28/L28	FIXL/ L29/L29	FIXL/ L30/L30	FIXL/ L31/L31
	Beat																							
	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
<b>DQ0</b>	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
<b>DQ1</b>	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
<b>DQ2</b>	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
<b>DQ3</b>	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
<b>DQ4</b>	D16	D17	D18	D19	D64	D65	D66	D67	FIXL/ M0	FIXL/ M1	FIXL/ M2	FIXL/ M3	D144	D145	D146	D147	D192	D193	D194	D195	FIXL/ L0/L0	FIXL/ L1/L1	FIXL/ L2/L2	FIXL/ L3/L3
<b>DQ5</b>	D20	D21	D22	D23	D68	D69	D70	D71	FIXL/ M4	FIXL/ M5	FIXL/ M6	FIXL/ M7	D148	D149	D150	D151	D196	D197	D198	D199	FIXL/ L4/L4	FIXL/ L5/L5	FIXL/ L6/L6	FIXL/ L7/L7
<b>DQ6</b>	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
<b>DQ7</b>	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
<b>DQ8</b>	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
<b>DQ9</b>	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
<b>DQ10</b>	D40	D41	D42	D43	D88	D89	D90	D91	FIXL/ M8	FIXL/ M9	FIXL/ M10	FIXL/ M11	D168	D169	D170	D171	D216	D217	D218	D219	FIXL/ L8/L8	FIXL/ L9/L9	FIXL/ L10/L10	FIXL/ L11/L11
<b>DQ11</b>	D44	D45	D46	D47	D92	D93	D94	D95	FIXL/ M12	FIXL/ M13	FIXL/ M14	FIXL/ M15	D172	D173	D174	D175	D220	D221	D222	D223	FIXL/ L12/L12	FIXL/ L13/L13	FIXL/ L14/L14	FIXL/ L15/L15

NOTE 1 Data assigned "FIXL/ Mx" and "FIXL/ Lx/ Ix" uses Meta, Link Protection and Data Bus Inversion.

## 2.4.5 Burst Sequence (cont'd)

**Table 14 – Burst Sequence (BL48) for Write**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	FIXL/ M0	FIXL/ M1	FIXL/ M2	FIXL/ M3	D144	D145	D146	D147	D192	D193	D194	D195	FIXL/ L0/I0	FIXL/ L1/I1	FIXL/ L2/I2	FIXL/ L3/I3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	FIXL/ M4	FIXL/ M5	FIXL/ M6	FIXL/ M7	D148	D149	D150	D151	D196	D197	D198	D199	FIXL/ L4/I4	FIXL/ L5/I5	FIXL/ L6/I6	FIXL/ L7/I7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	FIXL/ M8	FIXL/ M9	FIXL/ M10	FIXL/ M11	D168	D169	D170	D171	D216	D217	D218	D219	FIXL/ L8/I8	FIXL/ L9/I9	FIXL/ L10/I10	FIXL/ L11/I11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	FIXL/ M12	FIXL/ M13	FIXL/ M14	FIXL/ M15	D172	D173	D174	D175	D220	D221	D222	D223	FIXL/ L12/I12	FIXL/ L13/I13	FIXL/ L14/I14	FIXL/ L15/I15
	Beat																							
	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
DQ0	D256	D257	D258	D259	D304	D305	D306	D307	D352	D353	D354	D355	D384	D385	D386	D387	D432	D433	D434	D435	D480	D481	D482	D483
DQ1	D260	D261	D262	D263	D308	D309	D310	D311	D356	D357	D358	D359	D388	D389	D390	D391	D436	D437	D438	D439	D484	D485	D486	D487
DQ2	D264	D265	D266	D267	D312	D313	D314	D315	D360	D361	D362	D363	D392	D393	D394	D395	D440	D441	D442	D443	D488	D489	D490	D491
DQ3	D268	D269	D270	D271	D316	D317	D318	D319	D364	D365	D366	D367	D396	D397	D398	D399	D444	D445	D446	D447	D492	D493	D494	D495
DQ4	D272	D273	D274	D275	D320	D321	D322	D323	FIXL/ M16	FIXL/ M17	FIXL/ M18	FIXL/ M19	D400	D401	D402	D403	D448	D449	D450	D451	FIXL/ L16/I16	FIXL/ L17/I17	FIXL/ L18/I18	FIXL/ L19/I19
DQ5	D276	D277	D278	D279	D324	D325	D326	D327	FIXL/ M20	FIXL/ M21	FIXL/ M22	FIXL/ M23	D404	D405	D406	D407	D452	D453	D454	D455	FIXL/ L20/I20	FIXL/ L21/I21	FIXL/ L22/I22	FIXL/ L23/I23
DQ6	D280	D281	D282	D283	D328	D329	D330	D331	D368	D369	D370	D371	D408	D409	D410	D411	D456	D457	D458	D459	D496	D497	D498	D499
DQ7	D284	D285	D286	D287	D332	D333	D334	D335	D372	D373	D374	D375	D412	D413	D414	D415	D460	D461	D462	D463	D500	D501	D502	D503
DQ8	D288	D289	D290	D291	D336	D337	D338	D339	D376	D377	D378	D379	D416	D417	D418	D419	D464	D465	D466	D467	D504	D505	D506	D507
DQ9	D292	D293	D294	D295	D340	D341	D342	D343	D380	D381	D382	D383	D420	D421	D422	D423	D468	D469	D470	D471	D508	D509	D510	D511
DQ10	D296	D297	D298	D299	D344	D345	D346	D347	FIXL/ M24	FIXL/ M25	FIXL/ M26	FIXL/ M27	D424	D425	D426	D427	D472	D473	D474	D475	FIXL/ L24/I24	FIXL/ L25/I25	FIXL/ L26/I26	FIXL/ L27/I27
DQ11	D300	D301	D302	D303	D348	D349	D350	D351	FIXL/ M28	FIXL/ M29	FIXL/ M30	FIXL/ M31	D428	D429	D430	D431	D476	D477	D478	D479	FIXL/ L28/I28	FIXL/ L29/I29	FIXL/ L30/I30	FIXL/ L31/I31

NOTE 1 Data assigned “FIXL/ Mx” and “FIXL/ Lx/ Ix” uses Meta, Link Protection and Enhanced Data Bus Inversion.

### 3 WCK Clocking

LPDDR6 SDRAM's command and address interface operates from a differential clock (CK\_t and CK\_c). Commands and addresses are registered double data rate (DDR) at every rising edge of CK\_t and CK\_c. CS is sampled at the every other rising edge of CK\_t and the falling edge of CK\_c.

LPDDR6 uses a DDR data interface. The data interface uses two differential forwarded clocks (WCK\_t/WCK\_c) that are source synchronous to the DQs. DDR means that the data is registered at every rising edge of WCK\_t and rising edge of WCK\_c. WCK\_t and WCK\_c operate at twice the frequency of the command/address clock (CK\_t/CK\_c).

WCK\_t/WCK\_c is used to sample DQ data for write operation and to toggle DQ data for read operation. WCK\_t/WCK\_c is required to start toggling before starting write or read DQ data bursts. Any commands that require DQ data burst initiate a WCK2CK Sync sequence in LPDDR6 SDRAM. The WCK2CK Sync sequence is illustrated in Figure 11. After WCK2CK Sync sequence, SDRAM internal WCK0 is aligned with CK to get ready for DQ data burst. This SDRAM internal WCK2CK Sync sequence is hidden from the memory controller, not requiring any extra commands. RDQS\_t and RDQS\_c are also generated from WCK clock.

### 3.1 Clocking and Interface Relationship

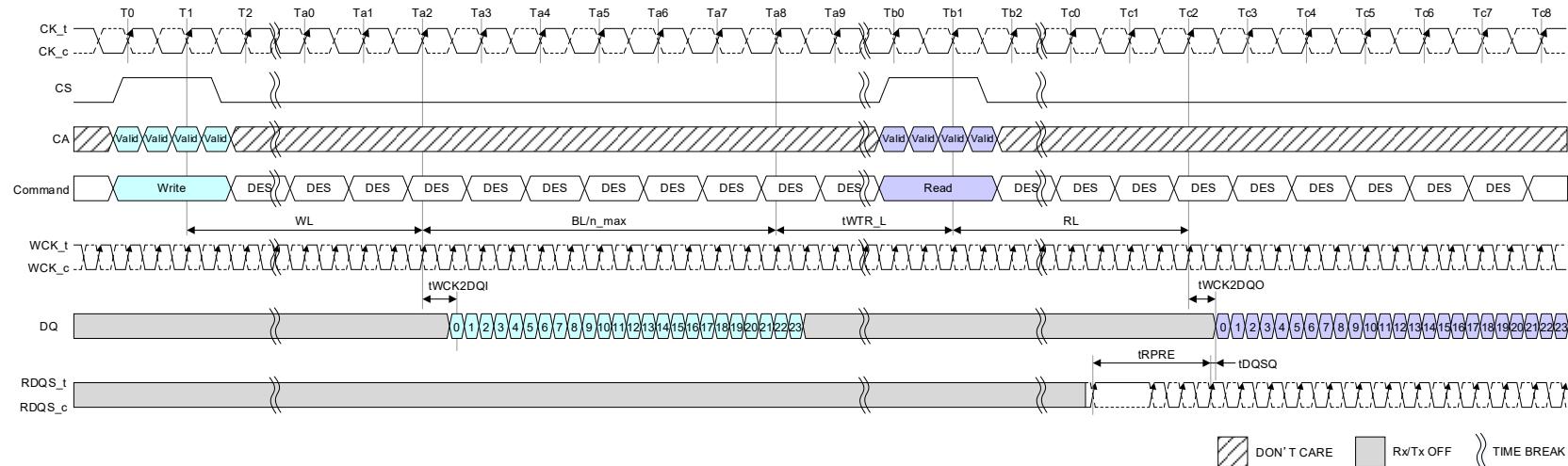


Figure 9 – Clocking and Interface Relationship: Same Bank Write to Read Timing, BL=24, WCK Always On Mode

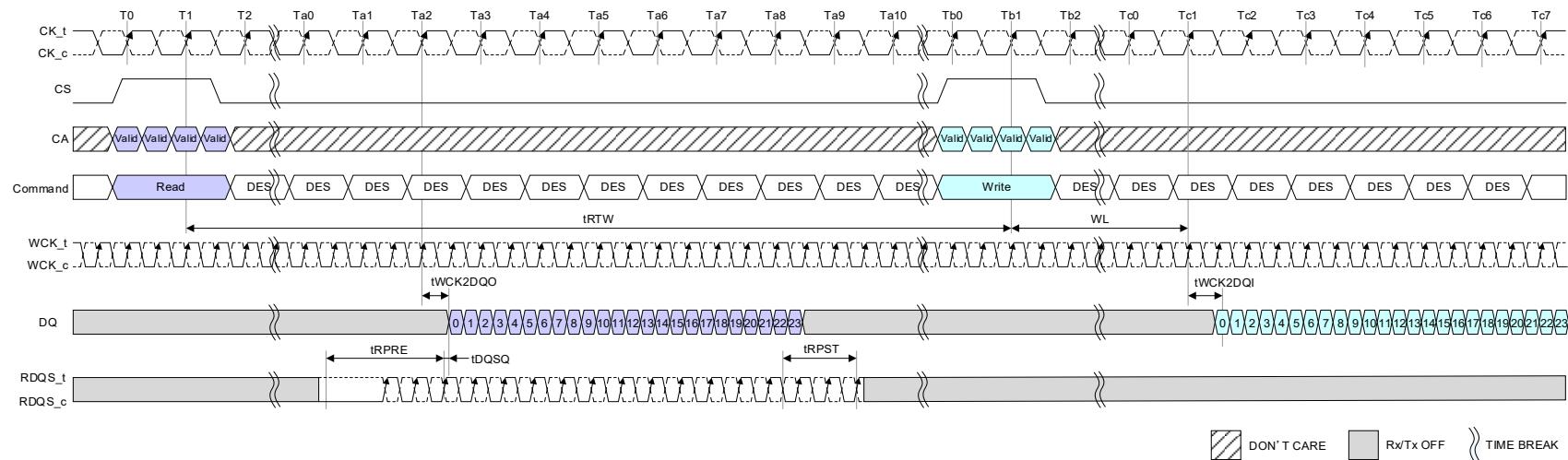
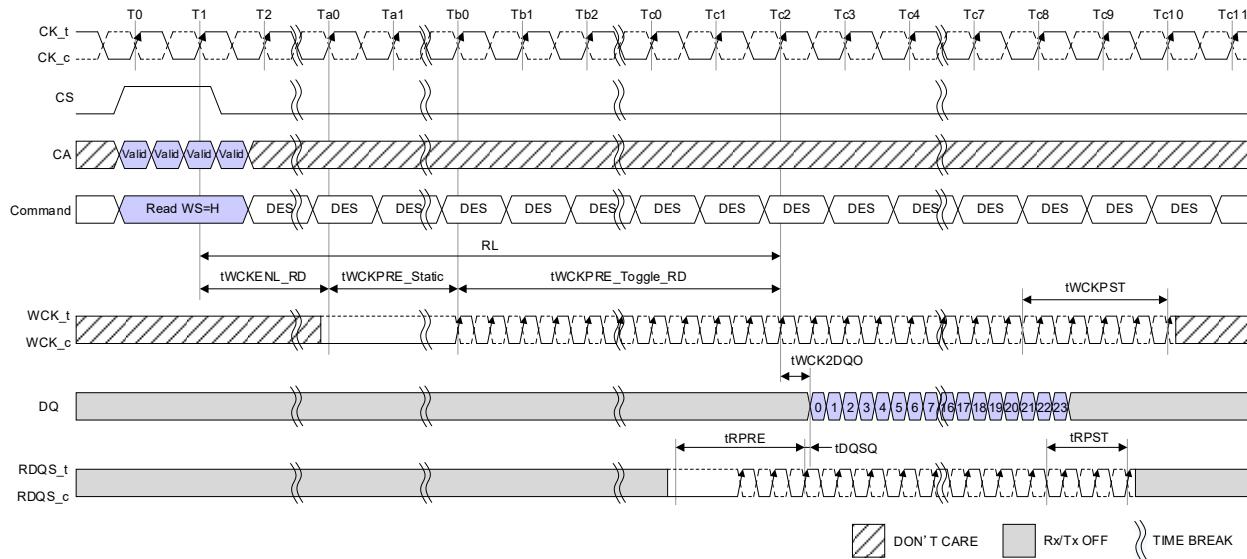


Figure 10 – Clocking and Interface Relationship: Read to Write Timing, BL=24, WCK Always On Mode

### 3.2 WCK2CK Sync Operation



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

**Figure 11 – WCK2CK Sync Operation by Read Command with WS Operand Enabled**

**Table 15 – Example Clock and Interface Signal Frequency Relationship**

Pin	Speed	Unit
CK_t, CK_c	2400	MHz
Command/Address	4800	Mbps/pin
WCK_t, WCK_c	4800	MHz
DQ	9600	Mbps/pin

### 3.3 WCK Clocking Block Diagram Example

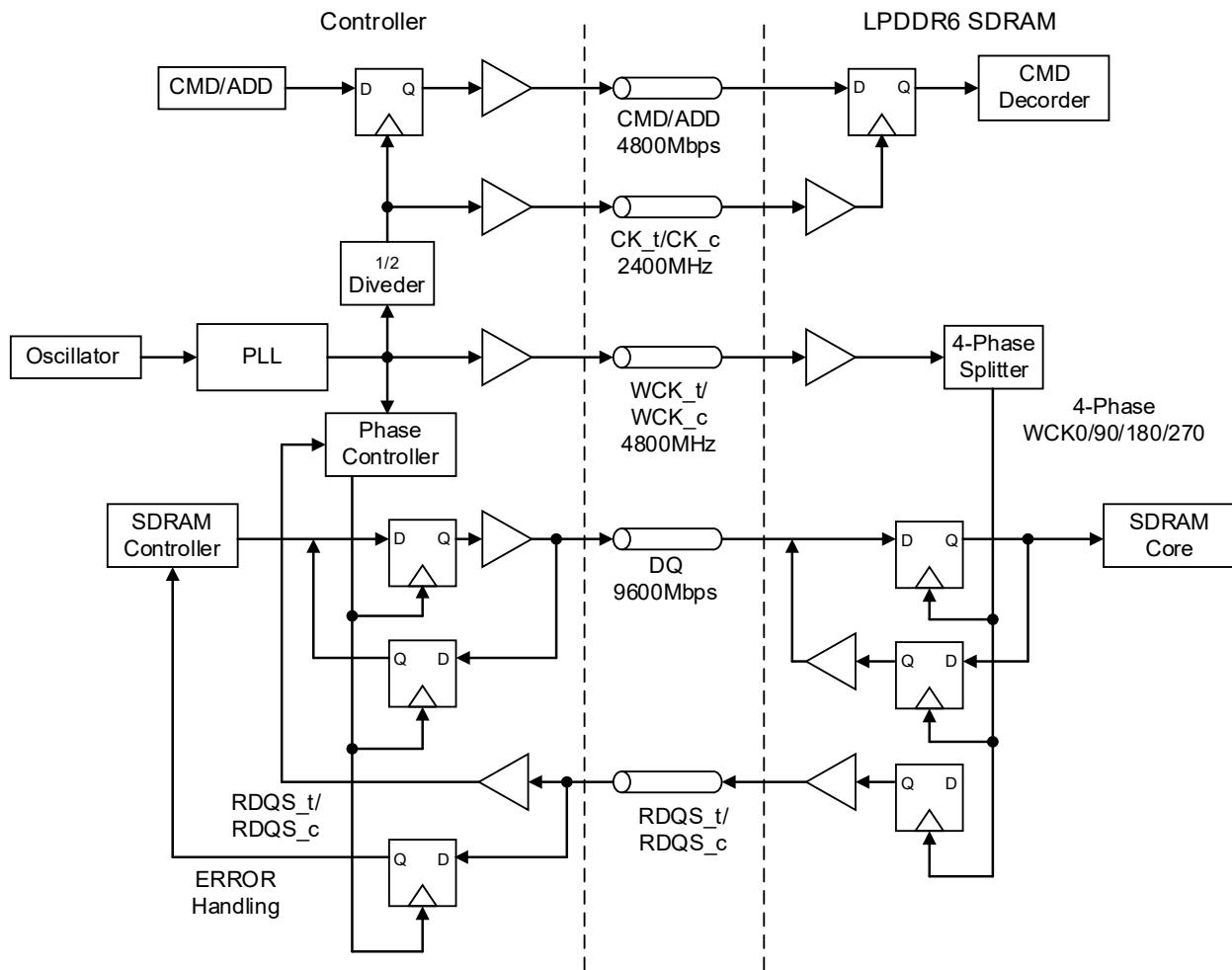


Figure 12 – Block Diagram of an Example System

## 4 Initialization and Training

### 4.1 Power-up, Initialization, and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR set in Table 16.

**Table 16 – MRS Default Setting (TBD)**

Item	MRS	Default Setting	Description
FSP_OP/WR	MR16_OP[3:0]	0000 <sub>b</sub>	FSP_OP/WR[0] is enabled
WLS	MR3_OP[5]	0B	Write Latency Set A is selected
WL	MR1_OP[7:4]	0000 <sub>b</sub>	WL = 4
RL	MR2_OP[3:0]	0000 <sub>b</sub>	RL = 6, nRBTP = 0
nWR	MR2_OP[7:4]	0000 <sub>b</sub>	nWR = 5
DBI_WR/RD	MR3_OP[7:6]	00 <sub>b</sub>	Write & Read DBI are disabled
CA_ODT	MR11_OP[6:4]	000 <sub>b</sub>	CA_ODT is disabled
DQ_ODT	MR11_OP[2:0]	000 <sub>b</sub>	DQ_ODT is disabled
Vref (CA) Value	MR12_OP[6:0]	1010000 <sub>b</sub>	VREF(CA): 50.0% of VDDQ
Vref (DQ) Value	MR14_OP[6:0] MR15_OP[6:0]	1010000 <sub>b</sub> 1010000 <sub>b</sub>	VREF(DQ): 50.0% of VDDQ
Vref (CS) Value	MR15_OP[6:0]	1010000 <sub>b</sub>	VREF(CS): 50.0% of VDDQ
ZQ Mode	MR28_OP[5]	0B	Background ZQ Calibration

#### 4.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR6 SDRAM. Unless specified otherwise, these steps are mandatory.

- 1) While applying power (after Ta), RESET\_n is recommended to be LOW ( $\leq 0.2 \times VDD2C$ ) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET\_n is held LOW. Power supply voltage ramp requirements are provided in Table 17. VDD1 must ramp at the same time or earlier than VDD2C. VDD2C must ramp at the same time or earlier than VDD2D. VDD2D must ramp at the same time or earlier than

**Table 17 – Voltage Ramp Conditions**

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2C
	VDD2C must be equal to or greater than VDD2D
	VDD2D must be greater than VDDQ
NOTE 1 Ta is the point when any power supply first reaches 300 mV. NOTE 2 Voltage ramp conditions in Table 17 apply between Ta and controlled power-off. NOTE 3 Tb is the point at which all supply voltages are within their defined ranges. NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.	

#### 4.1.1 Voltage Ramp and Device Initialization (cont'd)

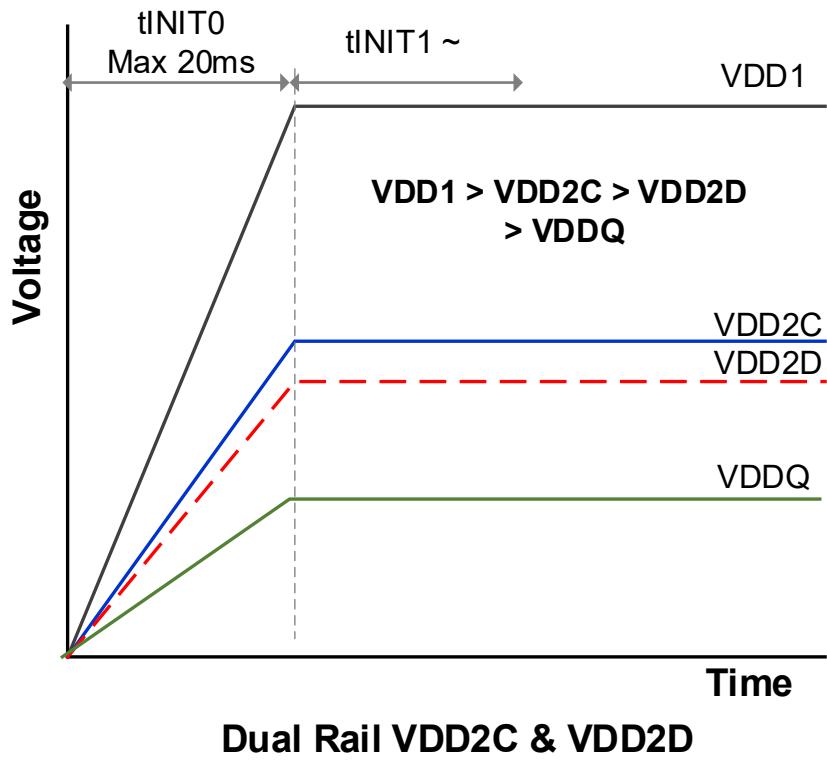
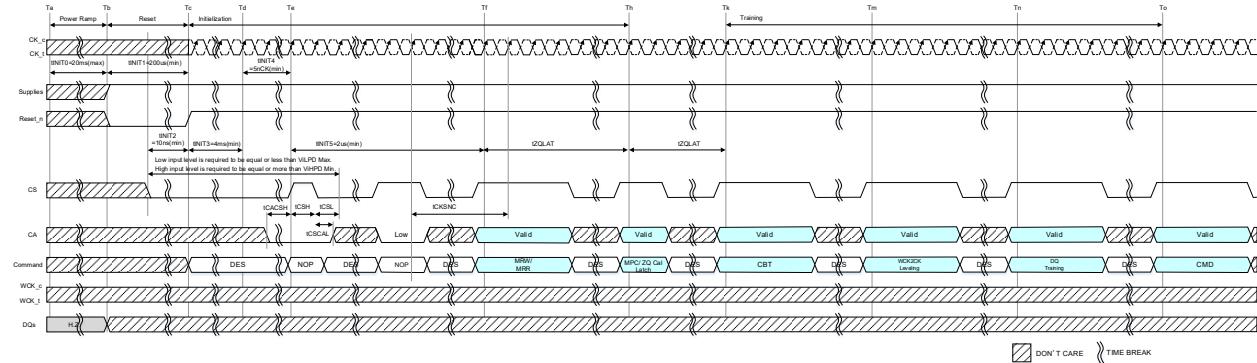


Figure 13 – Requirement for Voltage Ramp Control

- 2) Following the completion of the voltage ramp ( $T_b$ ), RESET\_n must be maintained LOW. DQ, WCK\_t and WCK\_c, CK\_t, CK\_c and CA voltage levels must be between VSS and  $V_{DDQ}$  during voltage ramp to avoid latch-up. CS level is required to be equal or less than ViLPD Max to prevent malfunction before a starting point of  $t_{INIT2}$ .
- 3) Beginning at  $T_b$ , RESET\_n must remain LOW for at least  $t_{INIT1}(T_c)$ , after which RESET\_n can be de-asserted to HIGH( $T_c$ ).

#### 4.1.1 Voltage Ramp and Device Initialization (cont'd)



NOTE 1 Training is optional and may be done at the system architect's direction. The training sequence after ZQ\_CAL latch in this figure (Th) is simplified recommendation and actual training sequence may vary depending on systems.

NOTE 2 Initial ZQ Calibration is started automatically by DRAM when RESET\_n goes high after tINIT1 and is completed before Td.

**Figure 14 – Power Ramp and Initialization Sequence**

- 4) Almost at the same time when RESET\_n is de-asserted, CK\_t and CK\_c need to be toggled or valid to be complementary level.
  - 5) CK\_t and CK\_c are required to be toggling (Td) and stabilized for tINIT4 before CS receives one toggling (Te).
  - 6) After tINIT4, wait minimum of tINIT5 to issue any MRR or MRW commands (Tf). When issuing the first command (Tf), the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tWCK2CK) could have relaxed timings (such as tWCK2CKb) before the system is appropriately configured.
  - 7) Since LPDDR6 initial ZQ calibration is done automatically after ramp up, ZQ Latch command should be issued. After tZQLAT is satisfied (Th), the command bus (internal VREF(CA), CS, and CA) should be trained for high-speed operation by issuing MRW command (Command Bus Training Mode). This command is used to calibrate the SDRAM's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR6 SDRAM will power-up with receivers configured for low-speed operations, with VREF(CA) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
- NOTE 1 The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See 4.2.3 Command Bus Training for information on how to enter/exit the training mode.
- 8) After command bus training, DRAM controller must perform WCK2CK leveling. WCK2CK leveling mode is enabled when MR16-OP[2] is high (Tk). See 4.2.4 WCK2CK Leveling Procedure and Related AC parameter for detailed description of WCK2CK leveling entry and exit sequence. After finishing WCK2CK Leveling, tWCK2CK which means CK-to-WCK relationship is determined and WCK2CK-Sync. operation will be performed with the optimized margin.

#### 4.1.1 Voltage Ramp and Device Initialization (cont'd)

- 9) After WCK2CK leveling, the DQ Bus (internal VREF(DQ), WCK, and DQ) should be trained for high-speed operation using the training commands (RD FIFO / WT FIFO / RD DQ Calibration) described in the command truth table and by issuing MRW commands to adjust VREF(DQ)(Tm). The LPDDR6 SDRAM will power-up with receivers configured for low-speed operations and VREF(DQ) set to a default factory setting. Normal SDRAM operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The Read DQ Calibration command is used together with FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See 4.2.9 WCK-DQ Training for detailed DQ Bus Training sequence.
- 10) At Tn, the LPDDR6 SDRAM is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

**Table 18 – Initialization Timing Parameters**

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Max voltage-ramp time at power-up
tINIT1	200		μs	Min Reset_n low time after completion of voltage ramp
tINIT2	10		ns	Min CS low time before RESET_n high
tINIT3	4		ms	Min CS low time after RESET_n high
tINIT4	5		tCK	Min stable clock before first CS high
tINIT5	2		μs	Min idle time before first MRW/MRR command
tZQLAT	Max(30ns, 4nCK)		ns	ZQCAL latch quiet time
tCKb	Note 1,2	Note 1,2	ns	Clock cycle time during boot

NOTE 1 Min tCKb guaranteed by DRAM test is 18 ns.  
 NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

#### 4.1.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

- 1) Assert RESET\_n below 0.2 x VDD2C anytime when reset is needed. RESET\_n needs to be maintained for minimum tPW\_RESET. CS must be pulled LOW ( $\leq$ VILPD) at least 10 ns before deasserting RESET\_n.
- 2) Repeat steps 4 to 9 in 4.1.1.

**Table 19 – Reset Timing Parameter**

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100		ns	Min RESET_n low time for Reset initialization with stable power

#### 4.1.3 Power-off Sequence

The following procedure is required to power off the SDRAM.

While powering off, CS must be held LOW (?VILPD) and all other inputs must be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while CS is held LOW. DQ, WCK\_t and WCK\_c, CK\_t, CK\_c and CA voltage levels must be between VSS and VDDQ during voltage ramp to avoid latch-up. RESET\_n input levels must be between VSS and VDD2C during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.

Tz is the point where all power supplies are below 300 mV. After Tz, the SDRAM is powered off.

**Table 20 – Power Supply Conditions**

Between	Applicable Conditions
Tx and Tz	VDD1 must be greater than VDD2C
	VDD2C must be equal to or greater than VDD2D
	VDD2D must be greater than VDDQ

## 4.2 Training

### 4.2.1 LPDDR6 CS Training

#### 4.2.1.1 Introduction

The CS Training Mode is a method to facilitate the loopback of a sampled sequence of the CS signal. In this mode, the CK is running, and the CA signals must be fixed to low. Once this mode is enabled and the DRAM devices are selected to actively sample and drive feedback, The DRAM will sample the CS signal on the rising edge of CK. Every set of 32 CK rising edge samples will be included in a logical computation to determine the CS Training mode Output result that is sent back to the host on the DQ bus.

#### 4.2.1.2 Entry and Exit for CS Training Mode

The CS Training Mode is enabled when the host sends an MRW command with the opcode for CS Training Mode Entry. When the DRAM is in this mode, commands are still actively processed. The only commands that should be sent by the host memory controller while CS Training Mode is enabled are the NOP command and the MRW to exit CS Training Mode. Any other command may produce unreliable results. To avoid the unreliable results on CA bus host drive CA [3:0] to low during CS training mode.

CSTM enters at low frequency through MRW command and switch to high frequency mode. To exit CS Training Mode, sync off require at low frequency mode using DQ [11] just like in CBT mode. After Sync off NOP command issued to CK Sync followed by an MRW command to disable CS Training Mode.

#### 4.2.1.2.1 Entering CS Training Mode

To enter CS Training mode, issue an MRW-1 command followed by an MRW-2 command to set MR16 OP [6] = 1<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> for the CS training mode selection.

The WCK ODT value is fixed at 40 ohms regardless of the MR19 setting; DQ ODT and NT-ODT states are turned off. WCK\_t and WCK\_c are input pins for capturing DQ [11], DQ [10] and DQ [9] levels by toggling, and DQ [10] is a dedicated pin for capturing the VREF(CS) setting from DQ [6:0] during CS training mode.

The WCK input is required to be at a valid level (WCK\_t = Low and WCK\_c = High), DQ [6:0] are required to be at valid levels, and DQ [11], DQ [10] and DQ [9] are required to be low before the MRW-2 command input. After tCBTWCKPRE\_static, the WCK signal can toggle, and tWCK2DQ11H must be satisfied before DQ [11] goes high. DQ [11] is driven HIGH, and when the LPDDR6 SDRAM samples the high level of DQ [11] by WCK, the LPDDR6 SDRAM switches from FSP-OP[x] to the FSP set defined by MR16 OP [5:4], completing the entry into CS training mode.

#### 4.2.1.2.2 Exiting CS Training Mode

To exit CS Training mode, change the CK frequency to the low-frequency operating point and then drive DQ [11] low after tDQ11LCK. The WCK toggle timing tWCK2DQ11H and tDQ11HWCK must be satisfied to capture the high-to-low transition of DQ [11]. The DQ [11] high-to-low transition is also used for CK sync off. After time tCKSNOFF, issue the CK Sync NOP command to perform the LPDDR6 SDRAM CK sync for low-frequency mode. After time tCKSNC, issue the CSTM exit MRW command to set MR16 OP [5:4] = 00<sub>B</sub>.

#### 4.2.1.2.2 Exiting CS Training Mode (cont'd)

After training exit, the LPDDR6 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training. DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied. After time tMRD, the LPDDR6 SDRAM is ready for normal operation.

#### 4.2.1.3 CS Training Mode (CSTM) Operation

SOC sends 101010 toggle pattern (clock-like pattern) on CS. DRAM checks the CS High pulse width on Even rising edge. DRAM checks the CS Low pulse width on Odd rising edge.

SOC can use the fix number of CS toggles (16 pulses). DRAM starts counting when CS starts to toggle to define the sample window. DRAM returns the odd and even results on separate DQs. Default output of "1" on DQ [7:6] indicates failure. If a pass is detected, the output changes to "0" and remains at "0" on DQ [7:6] until the reset pin DQ [9] is asserted. Host reads out the result before sending the next CS toggle pattern. Host can capture the CS output pass/fail results after tADR and reset the CS output results by asserting DQ [9] before sending out the next CS toggle pattern.

CK Sync operation is not required during CS training mode as CS is not trained and Host can detect the pass / fail pattern by sweeping the CS delay.

- After CSTM entry with first CS toggle, DRAM starts sampling and counts to 32nCK before sending the output results on DQ [7:6].
- DQ [6] indicates CS High PW error and DQ [7] indicates the CS Low PW error.
- DRAM keeps the DQ output (pass/fail) until DQ [9] resets the CS counter and compares results.
- SOC may stop the CK between 2 CS pattern to update the CK delay and avoid any glitch on CK.
- SOC must keep the CK in valid state when CK is stopped.

#### 4.2.1.4 Frequency Set Point (FSP) and Frequency Switching

The LPDDR6 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR6 SDRAM is initiated to FSP-OP [0] at power-up, which has the default settings to operate in unterminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP [5:4] for FSP-WR (Frequency Set Point Write/Read Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP [6] and MR16 OP [5:4] for CS Training Mode selection.

Prior to entering CS Training, the LPDDR6 SDRAM will be operating from FSP-OP[x]. Upon CS Training entry when DQ [11] is driven HIGH, the LPDDR6 SDRAM will automatically switch to the active FSP register set FSP-OP[x], FSP-OP[y] or FSP-OP[z] according to MR16 OP [5:4] and use the active register settings during training. Upon CS Training exit when DQ [11] is driven LOW, the LPDDR6 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the "known-good" state that was operating prior to training. The training values for VREF(CS) are not retained by the DRAM in FSP-OP[y] or FSP-OP[z] registers and must be written to the registers after training exit.

#### 4.2.1.5 VREF(CS) Update and DQ Bus Input/Output Control During CS Training Mode

VREF(CS) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF(CS) setting from DQ [6:0] during CS training mode. The LPDDR6 SDRAM samples the high and low level of DQ [10] using WCK.

- DQ [10] is used as a strobe pin for VREF(CS) setting updates via DQ [6:0] and serves as a DQ [7:0] output-mode-off switch.
- The LPDDR6 SDRAM samples DQ [6:0] levels at the internal DQ [10] rising edge and then updates its VREF(CS) setting. When the LOW level of DQ [10] is sampled by WCK, the DQ [7:0] output mode is turned off, and the input mode is turned on.
- DQ [7:0] becomes input pins for setting the VREF(CS) level, which is captured at the internal DQ [10] rising edge. During input mode, DQ [6:0] are used for setting the VREF(CS), while DQ [7] is not used but must remain in valid state. The input level of DQ [6:0] must remain stable during the tDStrain + tDHtrain period, and DQ [10] should be maintained "High" for tDHtrain to complete the latching of specific patterns.
- DQ [7:0] becomes output pins to feedback the CS training output results via DQ [7:6] until the low level of DQ [10] is sampled by WCK. During output mode, DQ [7:6] are used for CS training output results, while DQ [5:0] are not used and must be driven low.
- After tDQ11HWCK and tDQ112DQ from DQ [11] rising edge, the LPDDR6 SDRAM can accept its VREF(CS) value change using input signals of DQ [6:0]. The LPDDR6 SDRAM samples DQ [6:0] by the internal DQ [10] rising edge and then updates the existing value that was set via MR15 OP [6:0]. The mapping between MR15 OP code and DQ's is shown in Table 21. At least one VREF(CS) setting is required before proceeding to the next training steps.
- The new VREF(CS) value must "settle" for time tVREF\_LONG or tVREF\_SHORT before sending new CS toggle pattern.
- Refer to Table 22 for the DQ mapping function during CS training mode.

**Table 21 – Mapping of MR15 OP Code and DQ Numbers**

Mapping							
MR15 OP code	OP [6]	OP [5]	OP [4]	OP [3]	OP [2]	OP [1]	OP [0]
DQ Number	DQ [6]	DQ [5]	DQ [4]	DQ [3]	DQ [2]	DQ [1]	DQ [0]

#### 4.2.1.6 Data Bits (DQ) Function during CSTM

**Table 22 – Data Bits (DQ) Function during CSTM**

DQ Number	DQ Functions during CSTM
DQ [6:0]	Input pins for setting VREF(CS) level
DQ [7:6]	DQ [7]: pass/fail for CS Low pulse (1= fail, 0 = pass) DQ [6]: pass/fail for CS High pulse (1= fail, 0 = pass)
DQ [11]	FSP Switching and CK Sync off
DQ [10]	To latch the CS VREF settings
DQ [9]	Reset signal for CS counter & training compare output

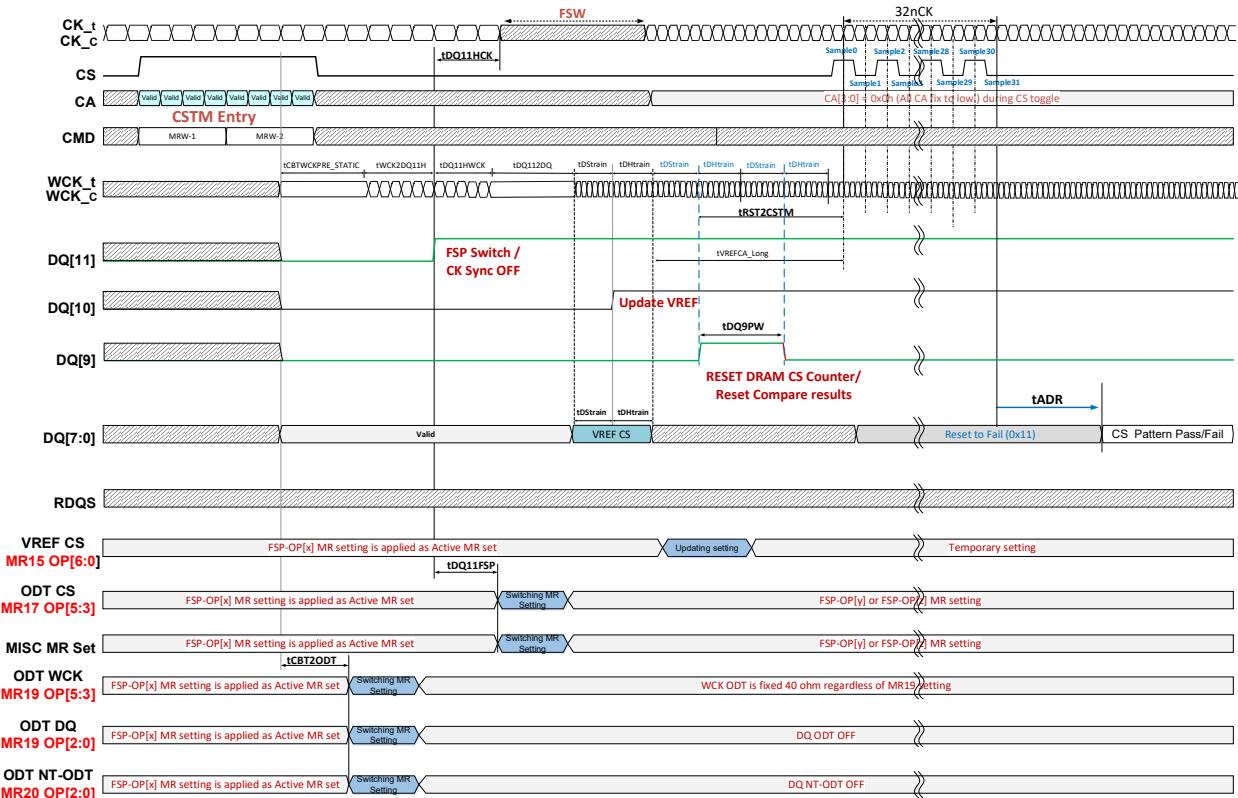
#### 4.2.1.7 CS Training Sequence Steps

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

- 1) Set MR13 OP [5:4] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP [6] = 1<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> for CS training mode (CST [y]).
- 4) Issue MRW-1 and MRW-2 commands to enter chip select Training mode.
- 5) Drive DQ [11] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Update the VREF (CS) setting if required. VREF (CS) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF (CS) setting from DQ [6:0] during CSTM.
- 7) Issue reset by asserting DQ [9] pulse signal to reset the CS counter and CS compare results. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK.
- 8) Perform CS Training (VREF(CS), CS).
  - a. Send the CS toggle pattern (101010...).
  - b. LPDDR6 SDRAM starts sampling CS toggle pattern with first CS toggle and counts to 32nCK before sending the output results on DQ [7:6]. In the 32nCK window, all CS samples must pass for the DQ [7:6] output to be a pass.
- 9) Repeat steps 6 to 8 as required to complete the CS training.
- 10) Exit training by driving DQ [11] LOW, a change CK frequency to the low frequency operating point prior to driving DQ [11] Low.
- 11) DQ [11] also performs the CK sync off at low frequency.
- 12) Issue CK Sync NOP
- 13) and then issue MRW-1 and MRW-2 commands to exit CS Training mode. When DQ [11] is driven LOW and SDRAM samples the LOW level of DQ [11] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 14) DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied. After time tMRD, the LPDDR6 SDRAM is ready for normal operation.
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.

Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination and change CK frequency to the high frequency operation point. At this point the CS is trained, and CBT training can be performed.

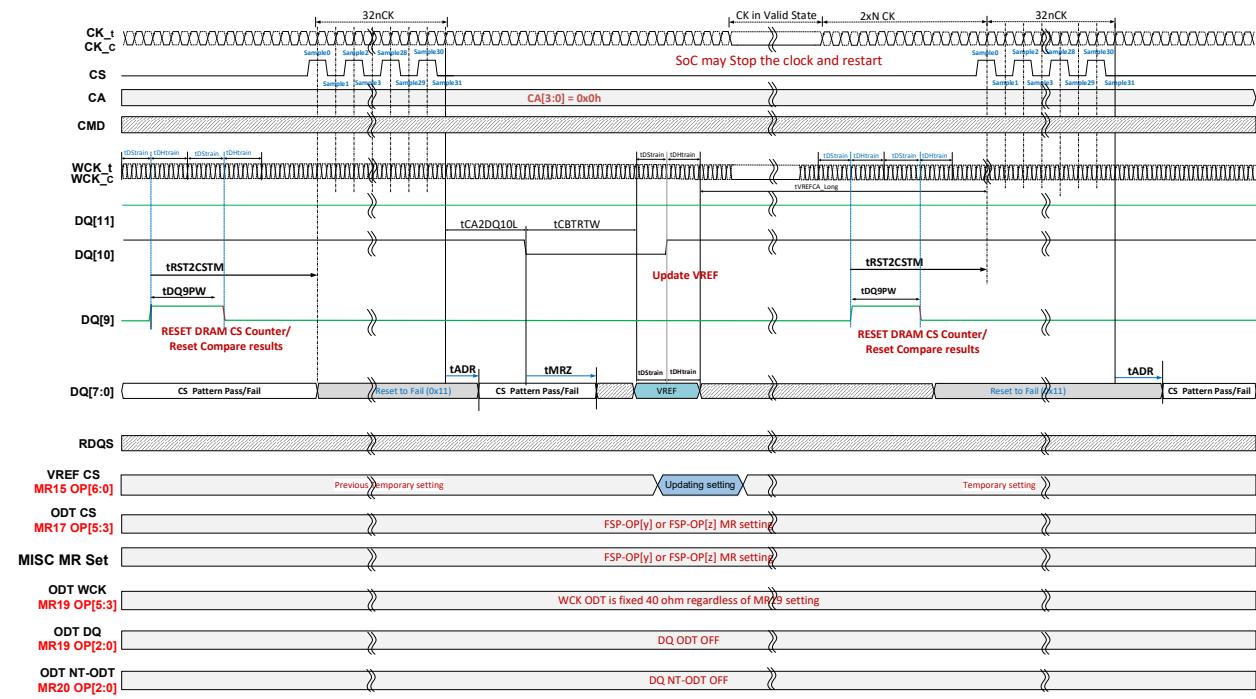
#### 4.2.1.7 CS Training Sequence Steps (cont'd)



- NOTE 1 The FSP switches and CK sync off when DQ [11] is asserted or de-asserted.
- NOTE 2 After DQ [11] is driven HIGH and the SDRAM samples the HIGH level of DQ [11] by WCK toggle in CS training mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set.
- NOTE 3 After tDQ11HCK, clock (CK) can be stopped, or frequency changed any time.
- NOTE 4 WCK\_t and WCK\_c are input pins for capturing DQ [11], DQ [10] and DQ [9] levels by toggling, and DQ [10] is a dedicated pin for capturing the VREF(CS) setting from DQ [6:0] during CS training mode.
- NOTE 5 The value of the DQ [6:0] signal level is sampled by the DQ [10] rising edge. The DRAM updates its VREFCS setting of MR15 temporarily, after time tVREFCS\_long.
- NOTE 6 tVREFCS\_long may be reduced to tVREFCS\_short.
- NOTE 7 WCK ODT state is set to a fixed value 40 ohm regardless of MR19 setting and DQ ODT/NT-ODT are turned off during CS training.
- NOTE 8 Differential WCK input is needed during CS training mode.
- NOTE 9 DQ [9] is used to reset the CS output results and CS compare logic. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK. The WCK toggle timing tDStrain + tDHtrain must be satisfied to capture the high-to-low and low-to-high transition of DQ [9].
- NOTE 10 WCK frequency is don't care during CS training as far as the frequency is within the allowed range of each frequency mode (MR11 OP [6]). WCK toggle may be stopped during tDQ112DQ and after tDHtrain, but WCK pair should be driven at static levels as WCK\_t = Low and WCK\_c = High. WCK should toggle. to satisfy tWCK2DQ11H and tDStrain before either DQ [11] or DQ [10] changes again.

Figure 15 — CSTM Entry and VREF Update

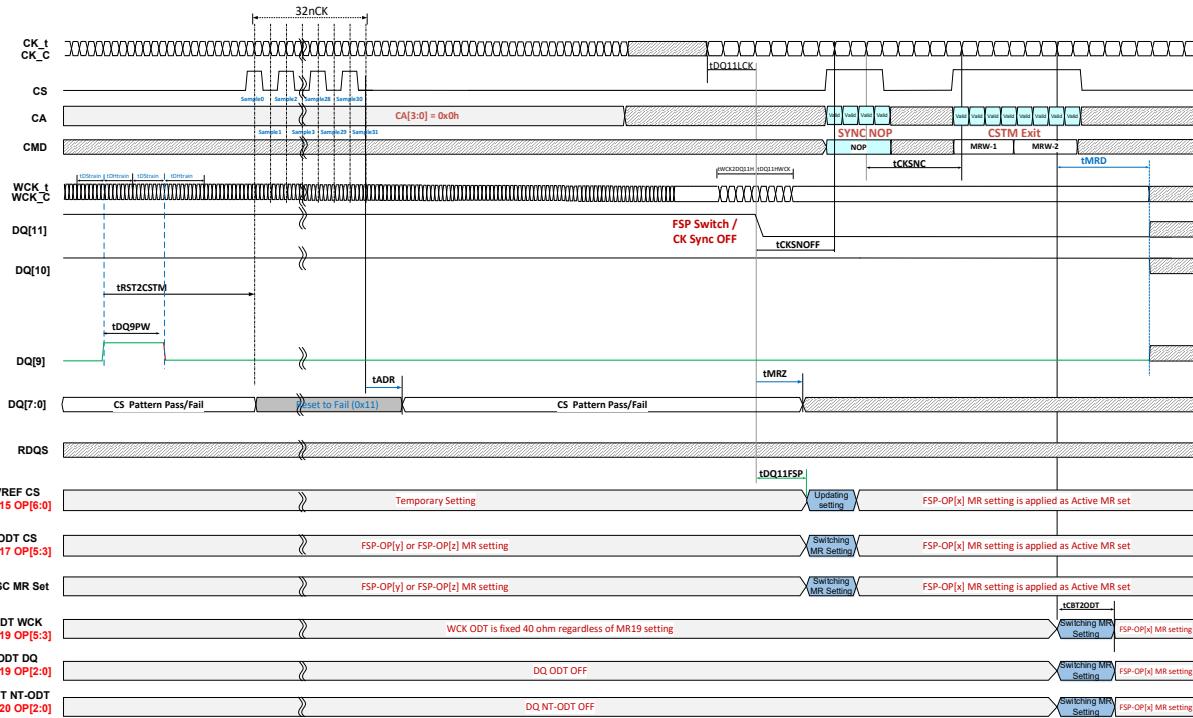
#### 4.2.1.7 CS Training Sequence Steps (cont'd)



- NOTE 1 The value of the DQ [6:0] signal level is sampled by the DQ [10] rising edge. The DRAM updates its VREFCS setting of MR15 temporarily, after time tVREFCS\_long.  
 NOTE 2 tVREFCS\_long may be reduced to tVREFCS\_short.  
 NOTE 3 To change read mode to write mode for DQ pins, DQ [10] must be driven Low.  
 NOTE 4 The host stops driving VREF on DQ [6:0] after satisfying the tDHtrain minimum and before resetting the DRAM CS counter/compare results via DQ [9].

Figure 16 – CSTM Sequence and VREF Change

#### 4.2.1.7 CS Training Sequence Steps (cont'd)



- NOTE 1 CK is required to satisfy tDQ11LCK before DQ [11] is driven low.  
 NOTE 2 DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.  
 NOTE 3 Training values are not retained by the SDRAM and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREF(CS) will return to the value programmed in the original set point.  
 NOTE 4 WCK doesn't need to synchronize with clock signal during CS training mode.

Figure 17 – CSTM Exit Sequence

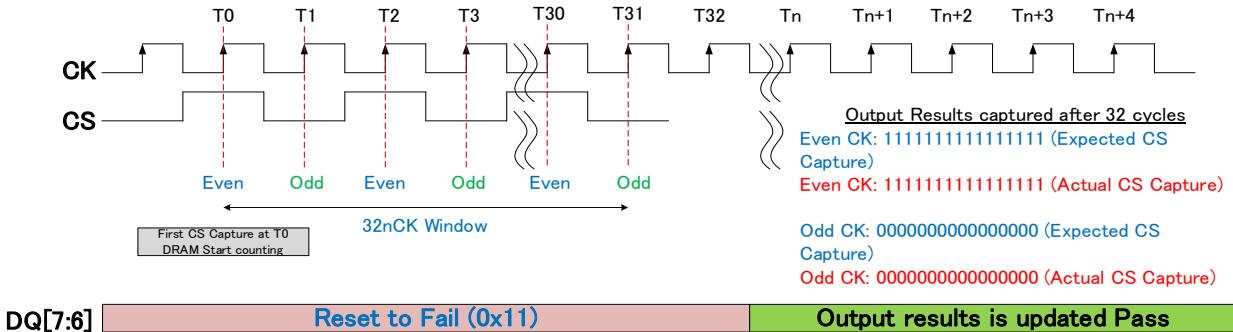
#### 4.2.1.8 CS-CK Sweeping Cases

Following are the important example cases that explain how the CS training results are expected during training mode.

##### 4.2.1.8.1 Case 0: CS-CK has 0 Skew (Ideal Condition)

First CS capture at T0, DRAM start counting the CS number of toggle (16) and output the pass/fail results.

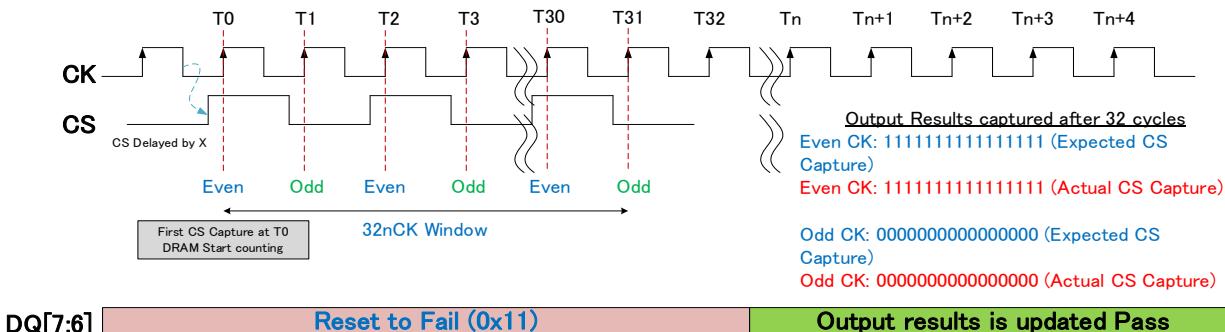
Even CK rising edge will be at T0.



##### 4.2.1.8.2 Case 1: CS-CK has x Skew (CS is Delayed by x)

First CS capture at T0, DRAM start counting the CS number of toggle (16) and output the pass/fail results.

Even CK rising edge will be at T0 as T0 captures the first CS toggle successfully.

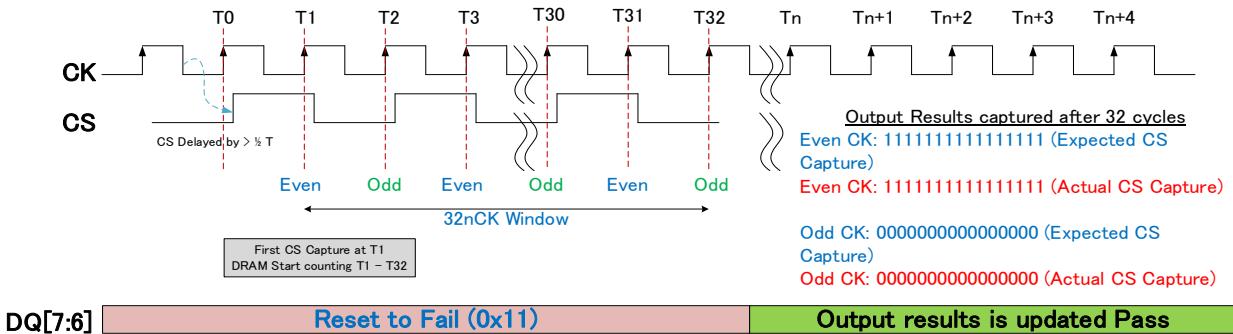


#### 4.2.1.8.3 Case 2: CS-CK has >1/2tCK Skew (CS is Delayed by >1/2tCK)

In this case first CS capture at T1, DRAM start counting the CS number of toggle (16) at T1 and output the pass/fail results.

Even CK rising edge will be at T1 as T1 capture the first CS toggle successfully.

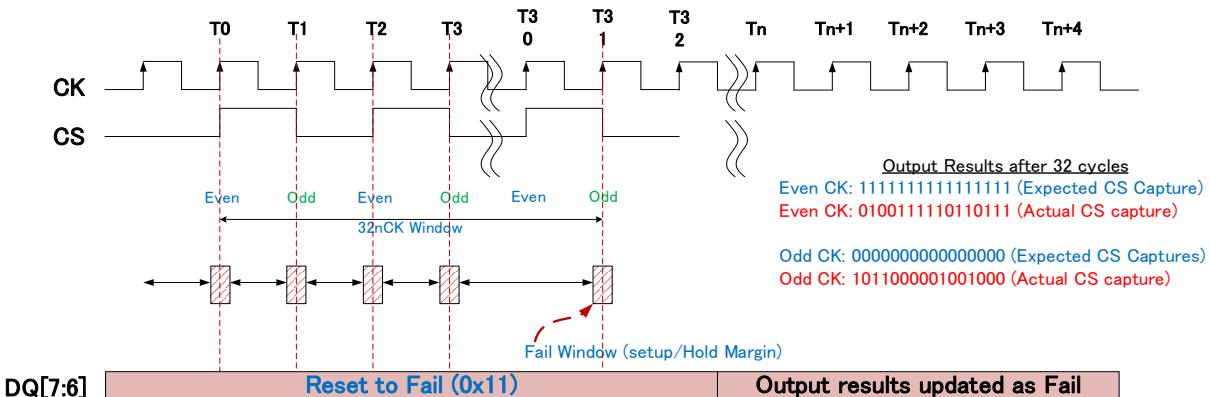
The delay between CK and CS is > 1/2tCK which shift the DRAM counting window from T1 - T32



#### 4.2.1.8.4 Case 3a: CS-CK Marginally Close (CS Rising Edge Very Close to CK Rising Edge)

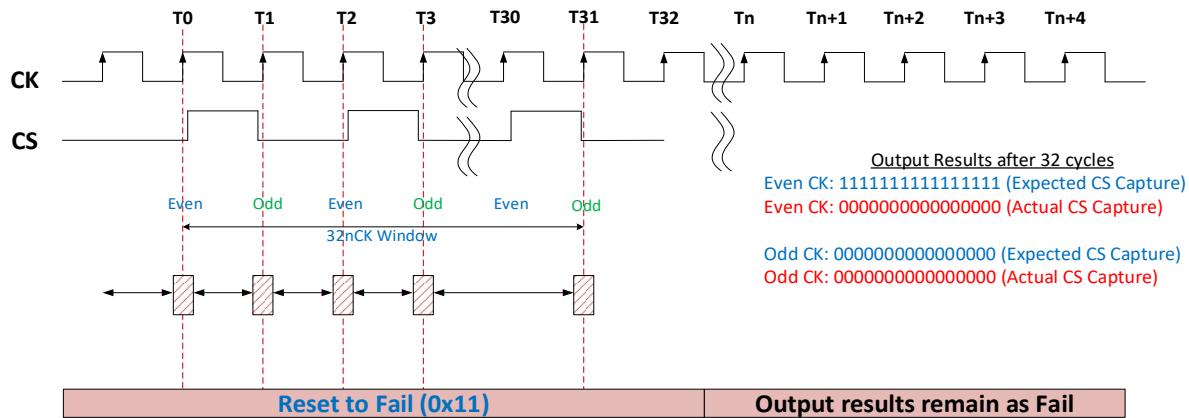
In this case CS rising edge is very close to the CK rising edge. DRAM fails to capture the CS even and odd samples and output results will not match the expected CS pattern as explained in below timing diagram.

DRAM will update the output results as fail.



#### 4.2.1.8.5 Case 3b: No CS High Capture due to DCD on High PW

In this case when CS has duty cycle distortion and high pulse width is degraded DRAM fails to capture any CS high pulse. DRAM will output the results as fail. Since default output results are fail before starting the CS pattern and remain at fail, Host will sweep the CS delay to find the correct pass/fail boundary.



#### 4.2.1.8.5 Case 3b: No CS High Capture due to DCD on High PW (cont'd)

**Table 23 – AC Parameters for CS Training Mode**

Item Description	Parameters	Min/Max	Data Rate	Unit	Note
			Up to 10667 Mbps		
Set-up margin between DQ11 and WCK	tWCK2DQ11H	Min	max (5ns, 12nWCK)	ns	
Hold margin between DQ11 and WCK	tDQ11HWCK	Min	max (5ns, 12nWCK)	ns	
Clock and Command Valid after DQ11 High	tDQ11HCK	Min	TBD	ns	
DQ11 High to valid DQ [6:0] input for VREFCS setting	tDQ11DQ	Min	250	ns	
Static WCK period (CS training entry to WCK toggling start)	tCBTWCKPRE_static	Min	max (20ns, 2nCK)	ns	
Asynchronous Data Read	tADR	Max	2nCK + 18ns	ns	
Data Setup margin between DQ and WCK	tDStrain	Min	max (5ns, 12nWCK)	ns	
Data Hold margin between DQ and WCK	tDHtrain	Min	max (5ns, 12nWCK)	ns	
Switching from DQ input to output margin	tDHtrain	Max	max (20ns, 24nWCK)	ns	3
VREF Step Time – Long	VREFCS_long	Min	250 + 0.5tCK	ns	1
VREF Step Time – short	VREFCS_short	Min	200 + 0.5tCK	ns	2
CK Sync Period	tCKSNC	Min	TBD	ns	
CK Sync Off	tCKSNOFF	Min	TBD	ns	
FSP change latency after DQ11 High or Low	tDQ11FSP	Min	20ns	ns	
DQ read out mode disable	tCBTRTW	Min	max (20ns, 24nWCK)	ns	
CS Counter reset (DQ9H) to CST	tRST2CBT	Min	max (20ns, 24nWCK)	ns	
CS counter reset (DQ9H) pulse width	tDQ9PW	Min	max (10ns, 12nWCK)	ns	
DQ10 Low to DQ driver off	tMRZ	Min	TBD	ns	
NOTE 1	VREFCS_long is for at least 2 step-size increment/decrement change including up to VREFmin to VREFmax or VREFmax to VREFmin change in VREF voltage.				
NOTE 2	VREFCS_short is for a single step-size increment/decrement change in VREF voltage.				
NOTE 3	The host stops driving VREF on DQ [6:0] after satisfying the tDHtrain minimum and before resetting the DRAM CS counter/compare results via DQ [9].				

#### 4.2.2 ZQ Calibration

Only one ZQ calibration mode is supported-Background Calibration. In Background Calibration mode, calibration of the output driver and CA/DQ ODT impedance across process, temperature, and voltage occurs in the background of device operation and is designed to eliminate any need for coordination among channels (that is, it allows for channel independence) within a single package.

ZQ re-calibration may be required as the LPDDR6 SDRAM voltage and/or temperature changes due to changes in the system environment. ZQ calibration can only be performed when the VDDQ voltage is set to nominal 0.5v DC or above (i.e., when DVFSQ is not active). In Background Calibration mode, the calibration shall be halted by the memory controller setting ZQ Stop when VDDQ is set to a nominal DC level below 0.5v or when VDDQ is being slewed between levels (i.e., when DVFSQ is active). See 4.2.2.2 for more information.

Changing CA ODT values (MR18-OP[5:3]) and/or DQ ODT values (MR19-OP[2:0]) will not alter the existing recalibration scheme, therefore there is no need for immediate recalibration.

##### 4.2.2.1 Calibration During Powerup and Initialization

ZQ calibration is automatically performed by all LPDDR6 sub-channel during the initialization/powerup sequence before Td, as shown in Figure 14. A ZQCAL Latch command shall be issued to all LPDDR6 sub-channels on or after Tg regardless of the state of ZQUF.

See Table 24 for calibration latency and timing.

Asserting ZQ Reset will set the calibration values to their default setting.

When ZQ Stop is enabled, the ZQ resource is available for use by other devices. See 4.2.2.2 for more information.

ZQ Interval MR setting is only applicable to ZQ Initiator sub-channel. These settings will be ignored by ZQ Target sub-channel.

After the power up initialization and reset sequences have been completed, ZQUF MR4 OP[5]=0B.

LPDDR6 packages with more than one ZQ pin may include more than one ZQ Initiator sub-channel.

#### 4.2.2.1.1 Background Calibration

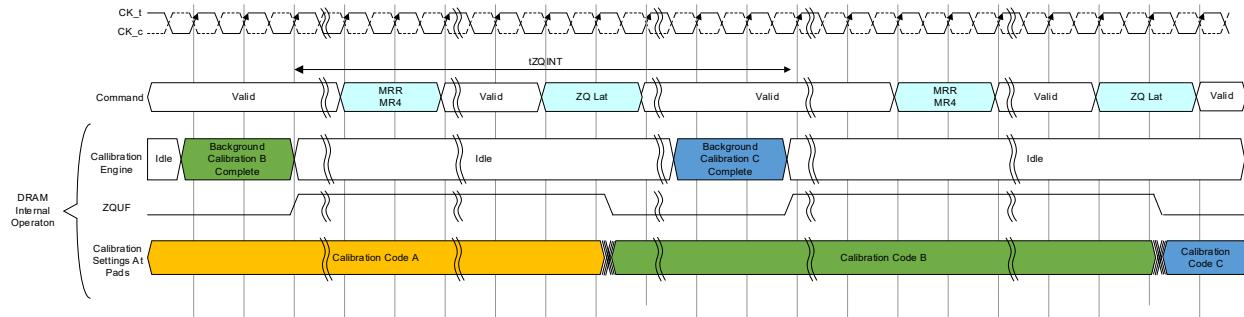
In this mode, pull-down/ODT and pull-up/Voh calibration will be performed in the background and kept up to date by the DRAM. Re-calibration will be performed by the LPDDR6 SDRAM within the time interval, tZQINT, specified in MR28 OP[3:2].

Pull-down/ODT calibration is controlled by each LPDDR6 sub-channel using an external ZQ resistor connected between VDDQ and a package ball or pin (ZQ resources). These ZQ resources may be shared among a number of LPDDR6 sub-channel up to a maximum of NZQ. Calibration will be automatically performed as part of power-up/initialization and after RESET\_n assertion. Subsequent re-calibration will be kept up to date by the DRAM. Self-arbitration by the DRAM insures that up to NZQ sub-channels within a package can share a common external ZQ resistor and avoid conflicts. Noise immunity will not be compromised when sharing the external ZQ calibration resistor.

When automatic pull-down/ODT calibration is complete, pull-up/Voh calibration will start automatically. At the completion of pull-down/ODT and pull-up/Voh calibration, MR4 OP[5] bit (ZQUF) will be set if the new calibration codes do not match the currently latched codes. An MRR of this bit will notify the system that new calibration results are available and that a ZQCal Latch command (following ZQCal Latch timing constraints) should be issued to ensure accurate calibration of Pull-down, ODT and Voh is consistently maintained. Setting of ZQUF is unique to each sub-channel regardless of configuration or sharing of the ZQ pin or pins. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCal Latch commands.

Setting the MR28 OP[1]=ZQ Stop will halt all background calibration activity. Re-setting MR28 OP[1] to zero will immediately start a calibration sequence, where all LPDDR6 sub-channels sharing the ZQ resource will recalibrate in a serial fashion. This enables rapid recalibration when exiting from DVFSQ-active mode where recalibration was not possible.

#### 4.2.2.1.1 Background Calibration (cont'd)



**Figure 18 – Background ZQ Calibration Timing**

#### 4.2.2.1.2 Latching ZQ Calibration Results in Background Calibration Mode

Latching ZQ calibration results is accomplished with the MPC ZQCal Latch command. This command loads new calibration results into the pull-down/ODT devices and pull-up drivers.

A ZQCal Latch command may be issued anytime outside of power-down when there are no DQ operations pending or in progress. The results from the most-recently completed calibration will always be latched with each ZQCal Latch command. If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQLAT to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always dis-allowed during tZQLAT.

The DQ and CA ODT calibration values will not be updated until ZQCal Latch command is performed and tZQLAT has been met, with the following exceptions:

ZQ calibration will automatically occur for each LPDDR6 sub-channel on power up/initialization and after Reset\_n pin assertion. A ZQCal Latch command shall be issued to all LPDDR6 sub-channels on or after Tg.

When a ZQCal Latch command is executed the ZQUF bit will be reset to 0 before expiration of tZQLAT.

#### 4.2.2.1.3 Maintaining Accurate Calibration - Background Calibration Mode

To maintain Pull-down/ODT calibration and Voh calibration when DVFSQ is not active:

1. Periodically, based on tZQINT, issue an MRR to MR4 to check the ZQUF OP[5] bit status for each LPDDR6 sub-channel.
2. If MR4 OP[5]=1, issue a ZQCAL Latch command.

Repeat 1-2 as needed. Alternatively, the memory controller may choose not to monitor ZQUF and periodically issue ZQCAL Latch commands. In this case the most-recently-completed calibration results will always be latched and will be no older than tZQINT.

It may be permissible for the memory controller to ignore ZQUF and not issue ZQCAL Latch commands if both of the following are true:

CA ODT is disabled

The LPDDR6 SDRAM is in an idle state, or in Self Refresh or Power Down mode

Re-calibration will still occur in the background to ensure accurate driver/ODT settings are available should they be needed. In this case, the memory controller should ensure a ZQCAL Latch command is performed prior to resuming data traffic if ZQUF is set.

When DVFSQ is active, MR28 OP[1] ZQ Stop shall be set for each LPDDR6 sub-channel to ensure recalibrations are inhibited. When DVFSQ is no longer active, ZQ Stop may be de-asserted, which will immediately begin a recalibration and enable subsequent periodic background calibrations. When the memory controller de-asserts ZQ Stop it shall reset MR28 OP[1] to zero for all sub-channels sharing the ZQ resource within 100ns as described in 4.2.2.2.2. The ZQUF will be updated and results from the recalibration can be latched after the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) has been satisfied.

#### 4.2.2.2 ZQ Stop Functionality

##### 4.2.2.2.1 ZQ Resistor Sharing in Background Calibration Mode

In Background Calibration mode, a ZQ Stop function is provided to enable another device or devices to share the ZQ resistor. This function is enabled by MR28 OP[1]=ZQ Stop. When another device needs to use the ZQ resistor, MR28 OP[1] shall be set to 1 for all LPDDR6 sub-channels that share ZQ resources. This will halt background calibration operations within delay time tZQSTOP (see Table 24) for each LPDDR6 sub-channel. Once tZQSTOP has expired for all LPDDR6 sub-channels that share the ZQ resource, other sub-channels may use the resource. When the ZQ resource is no longer needed by the other sub-channel or sub-channels the ZQ Stop MR bit should be reset to 0 to allow background calibrations to continue normally. When the ZQ Stop MR bit is reset to 0, periodic background calibrations will be re-started.

Since ZQ Stop inhibits the LPDDR6 sub-channel from recalibrating, note that changing system conditions while the ZQ Stop MR bit is set may cause the LPDDR6 ZQ calibration accuracy to deviate from specification. To ensure continued accurate calibration as discussed in 4.2.2.1.3, the ZQ Stop MR bit shall not be set for longer than tZQINT in background calibration mode.

##### 4.2.2.2.2 Stopping Background Calibration when DVFSQ is Active

In Background Calibration mode, the calibration shall be halted by setting ZQ Stop before DVFSQ is entered. ZQ Stop may be reset to 0 when DVFSQ is no longer active (when VDDQ is returned to a 0.5v nominal level). Resetting of ZQ Stop will start background calibration(s) immediately. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) from resetting of ZQ Stop on the ZQ Initiator sub-channel, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to all sub-channels sharing the ZQ resource. To guarantee recalibration of all sub-channels sharing the ZQ resource within tZQCAL, the MR28 OP[1] ZQ Stop bit shall be reset for all Target sub-channels sharing the ZQ resource either before, or no later than 100 ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ Initiator sub-channel.

#### 4.2.2.2.3 Stopping Background Calibration when VDDQ is Powered Off

In Background Calibration mode, before entering Power-down mode, the calibration shall be halted by setting ZQ Stop when VDDQ is going to be powered off. When Power-down mode is exited, ZQ Stop should be reset to 0 to re-enable background calibration. Resetting of ZQ Stop on the ZQ Initiator sub-channel will start background calibration(s) immediately. After expiration of the appropriate tZQCAL time (tZQCAL4, tZQCAL8 or tZQCAL16) from resetting of ZQ Stop, the memory controller may check the ZQUF flags, or may issue a ZQCal Latch command to each sub-channel sharing the ZQ resource. To guarantee recalibration of all sub-channels sharing the ZQ resource within tZQCAL, the MR28 OP[1] ZQ Stop bit shall be reset for all Target sub-channels sharing the ZQ resource either before, or no later than 100ns after, the MR28 OP[1] ZQ Stop bit is reset on the ZQ Initiator sub-channel.

**Table 24 – ZQ Calibration Timing Parameters**

Parameter	Symbol	Min/Max	Value	Units
From resetting ZQ Stop to Latch Time, NZQ≤4	tZQCAL4	Min	1.5	μs
From resetting ZQ Stop to Latch Time, 4<NZQ≤8	tZQCAL8	Min	3	μs
From resetting ZQ Stop to Latch Time, NZQ 8<NZQ≤16	tZQCAL16	Min	6	μs
ZQ Calibration Latch Time	tZQLAT	Min	MAX(30ns,4nCK)	Ns
ZQ Calibration Reset Time	tZQRESET	Min	MAX(50ns,3nCK)	Ns
Delay Time from ZQ Stop Bit Set to ZQ Resistor Available	tZQSTOP	Max	30	ns
Background Calibration Interval	tZQINT	Max	Programmable, 32, 64, 128, or 256	ms
Maximum Number of LPDDR6 sub-channels Connected to a Single ZQ Resistor	NZQ	Max	16	Sub-channel
Maximum Capacitive Load on ZQ Network	CZQ_N	Max	TBD	pF

#### 4.2.2.2.4 Stopping Background Calibration during VDD2C is Ramping Up or Down

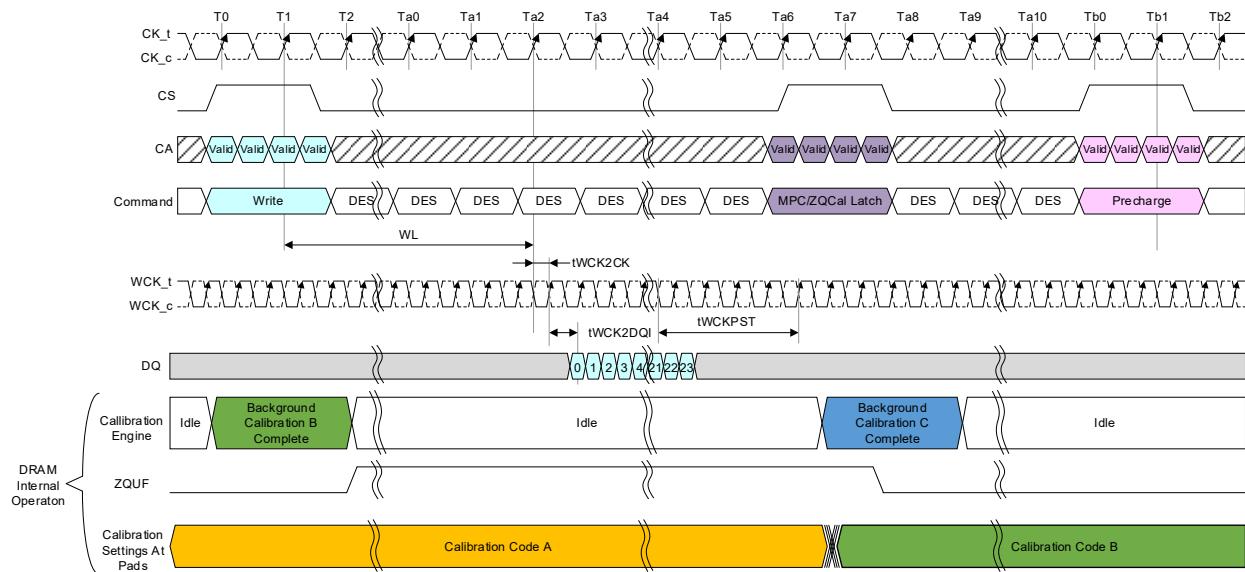
In the status of DVFSH, VDD2C is subjected to change from default range to Step-up range or vice versa. During the voltage transition is happening due to it, the calibration shall be halted by setting ZQ Stop. After VDD2C voltage transition is completed, ZQ Stop shall be reset to obtain the new ZQ calibration results appropriate to the new VDD2C condition.

#### 4.2.2.2.5 Stopping Background Calibration during VDD2D is Ramping Up or Down

In the status of DVFSL, VDD2D is subjected to change from default range to Step-down range or vice versa. During the voltage transition is happening due to it, the calibration shall be halted by setting ZQ Stop. After VDD2D voltage transition is completed, ZQ Stop shall be reset to obtain the new ZQ calibration results appropriate to the new VDD2D condition.

#### 4.2.2.3 ZQ Reset

Setting the ZQ Reset MR bit resets the output impedance calibration to a default accuracy of  $\pm 30\%$  across process, voltage, and temperature. The ZQ Reset command is executed by writing MR28 OP[0] = 1b. The ZQ Reset command will also reset the ZQ Stop MR28 OP[1] and ZQUF MR4 OP[5] bits to 0. ZQ Reset will not change the state of the ZQ Interval MR bits MR28 OP[3:2]. If CA ODT is enabled, the CA bus shall maintain a deselect state during tZQRESET to allow CA ODT calibration settings to be updated. In any case, operations that initiate DQ operations are always disallowed during tZQRESET. The ZQ Reset MR bit shall be reset to 0b by the DRAM after tZQRESET. To reset the ODT and output impedance in a multi-die package, the ZQ Reset function shall be issued to all sub-channels regardless of ZQ Initiator or ZQ Target designation.



- NOTE 1** WRITE and PRECHARGE operations are shown for illustrative purposes. Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
- NOTE 2** Before the ZQCal Latch command can be executed, any prior commands that utilize the DQ bus shall have completed.  
WRITE commands with DQ termination shall be given enough time to turn off the DQ ODT before issuing the ZQCal Latch command. See clause 7.8.4 On-Die Termination (ODT) for ODT timing.

**Figure 19 – ZQcal Timing**

#### 4.2.2.4 Multi-die Package Considerations

Up to NZQ LPDDR6 sub-channels within a single package may connect to the same ZQ resistor. ZQ stop function that is executed by writing MR28 OP[0]=1b and resetting MR28 OP[0]=0b is managed by Initiator sub-channel and may be issued to other sub-channel sharing a ZQ resource asynchronously or simultaneously. ZQCal Latch commands, when required, are necessary for each sub-channel. When multiple die share a ZQ resource and a ZQ Initiator sub-channel is managing calibration (when DVFSQ is inactive), the MR28 OP[1] ZQ Stop bit shall be set to 0B for all ZQ Target sub-channels sharing the ZQ resource. No other arbitration considerations are required.

#### 4.2.2.4.1 Other Considerations in Background Calibration Mode

Each LPDDR6 channel includes a single ZQ pin and associated ZQ calibration circuitry. Calibration values from this circuit will be generated and used according to the following protocol:

- Setting of the ZQ Stop bit always has priority over background calibration processes
- If the ZQ Stop MR bit is set to 1 while a background ZQ calibration is in progress, the background calibration will be interrupted
- A background calibration will start immediately when the ZQ Stop MR bit is reset to 0
- A background calibration will not start while the ZQ Stop MR bit is set to 1
- The ZQUF bit will not be reset by setting of the ZQ Stop bit to 1
- The ZQUF bit will be reset only by a ZQCal Latch command or ZQ Reset
- The ZQUF bit will be set if calibration codes do not match the currently latched codes even when the sub-channel is in Self-refresh or Power-down mode, providing ZQ Stop is not set

#### 4.2.2.5 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm  $\pm 1\%$  tolerance external resistor shall be connected between the ZQ pin and VDDQ.

The total capacitive loading on the ZQ pin shall be limited to CZQ\_N.

#### 4.2.2.6 Flow Chart Examples

The flow charts in Figure 20 to Figure 22 are representative only of one set of LPDDR6 sub-channel that share a single ZQ resource. These are examples only; there may be other valid methods of operation.

#### 4.2.2.6 Flow Chart Examples (cont'd)

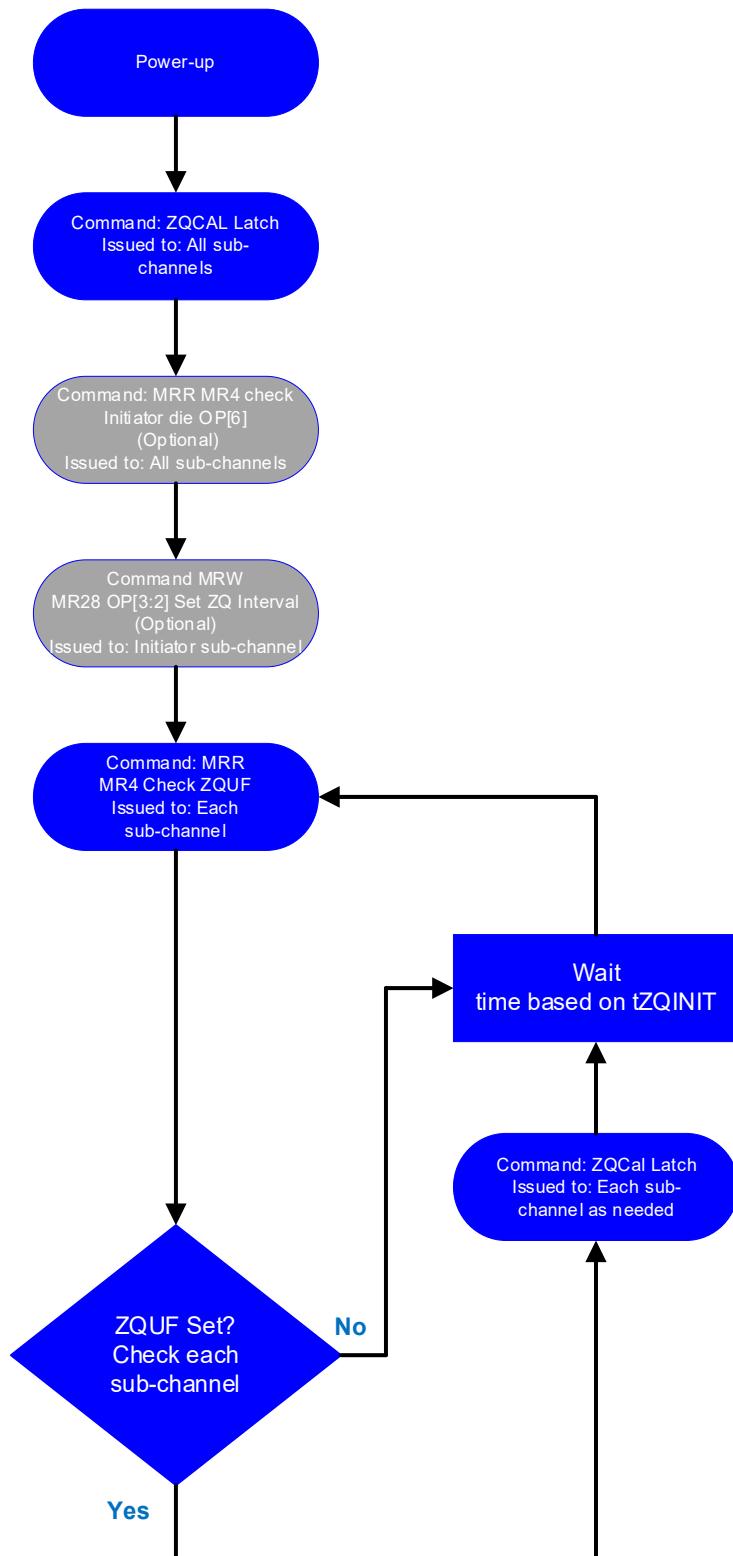


Figure 20 – Initialization to Background Calibration Flow Chart, no DVFSQ Support

#### 4.2.2.6 Flow Chart Examples (cont'd)

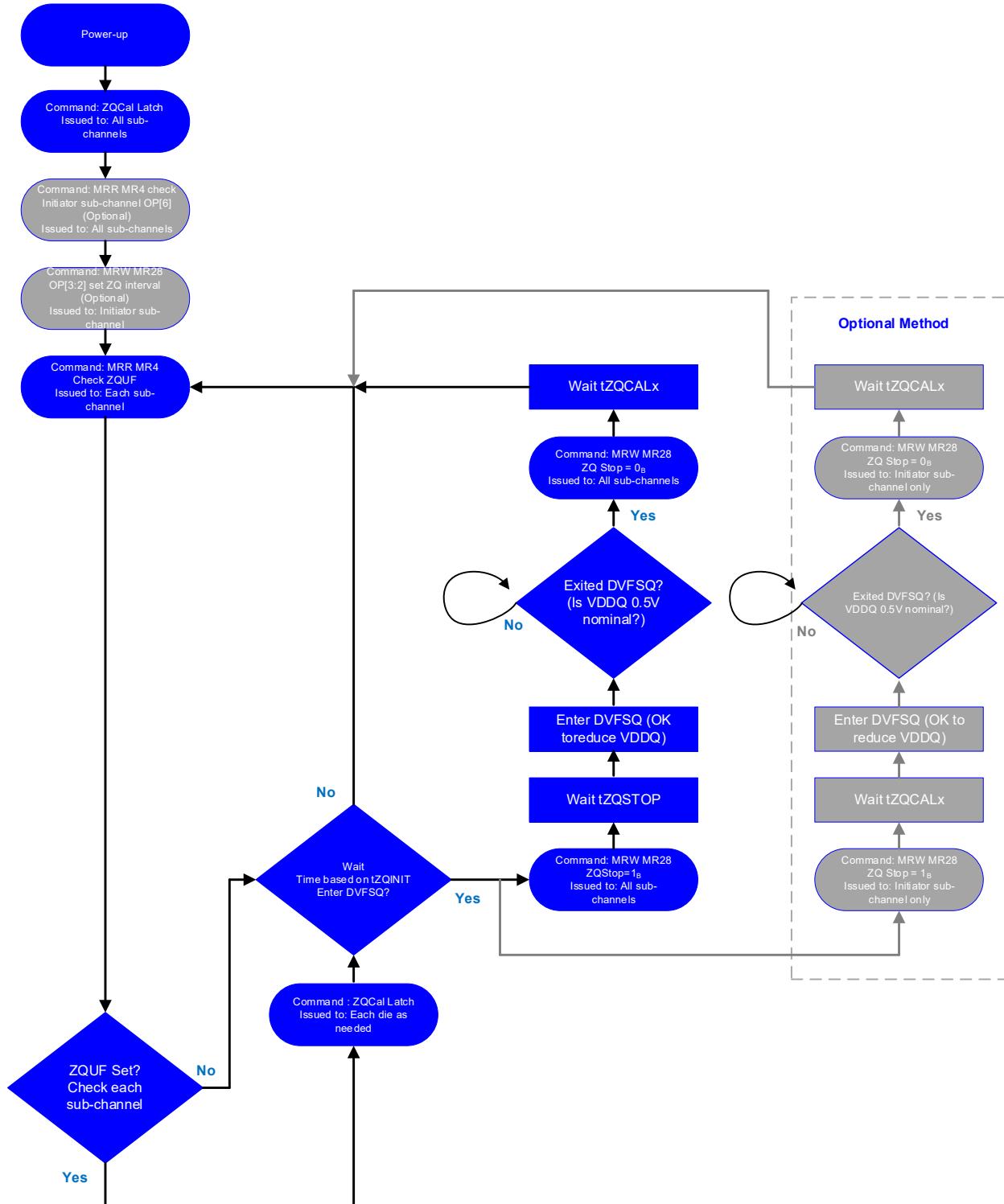


Figure 21 – Initialization to Background Calibration Flow Chart, with DVFSQ Support

#### 4.2.2.6 Flow Chart Examples (cont'd)

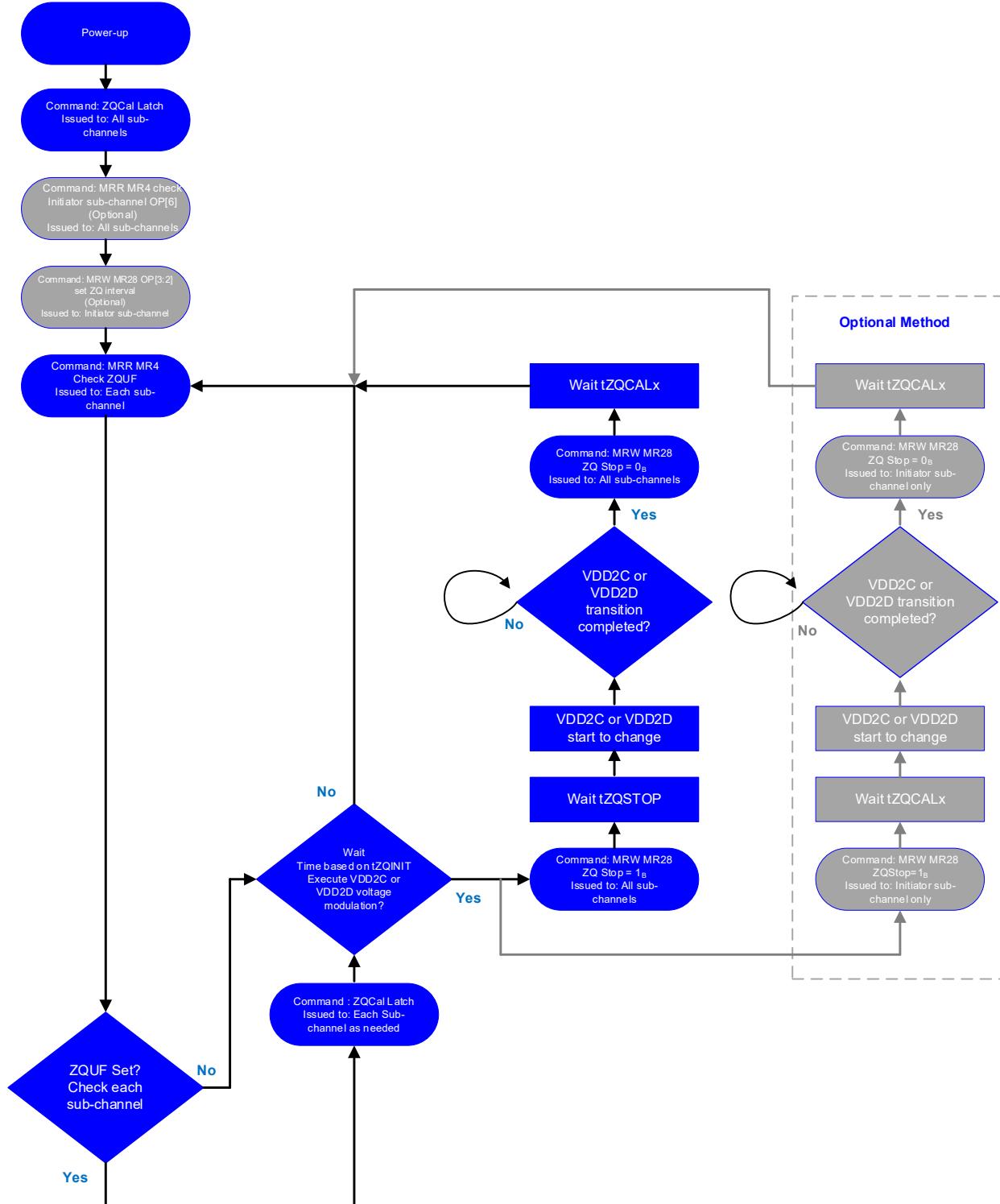


Figure 22 – Initialization to Background Calibration Flow Chart, with VDD2C/D Transition Support

### 4.2.3 LPDDR6 Command Bus Training (CBT)

#### 4.2.3.1 Introduction

The LPDDR6 SDRAM command bus must be trained before enabling termination for high-frequency or mid-frequency operation. The command bus training mode is a method to facilitate the loopback of a logical combination of the sampled CA [3:0] signals. In this mode, the CK is running, and the CS qualifies when the CK samples the CA signals. Command Bus training perform per-bit and per phase to adjust the per-bit skew and duty cycle distortion. SDRAM Controller sends the long CA burst with CS high and DRAM captures the CA pattern every rise and fall of CK cycle. SDRAM Controller and DRAM use matching PRBS generator to compare CA per phase and per-bit in parallel and return the error asynchronously on DQ bus. LPDDR6 provides an internal VREF(CA) that default level is suitable for un-terminated, low-frequency operation, but the VREF(CA) must be trained to achieve suitable receiver voltage margin for terminated, high-frequency or mid-frequency operation. The training mode described here centers the internal VREF(CA) in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements.

When the DRAM is in this mode, no functional commands are executed in the DRAM. The functional command interface is restored only after exiting this mode.

Prior to entering the CA Training Mode, the CS signal must be aligned to the CK to meet the CS to CK timing specifications. This assumes that CS Training has been completed to determine the correct CS timings on the host.

#### 4.2.3.2 Entry and Exit for CBT Mode

To enter the command bus training mode SDRAM controller switch to low frequency to issue MRW command. DQ [11] is used to perform the FSP switch and CK Sync OFF operation before entering and exiting the CBT training. DQ [11] transition from low to high or high to low trigger the FSP switch and CK Sync OFF

Command Bus Training is enabled through MRW command followed by DQ [11] is driven high to perform FSP Switch and CK Sync OFF. LPDDR6 SDRAM samples HIGH level of DQ [11] by WCK.

When DRAM enters command bus training mode Only the sampling of the CA signals, evaluation of the XOR result, and loop back to the DQ's will occur. While in CA Training Mode, the CS signal will only assert for CA long burst and CK Sync NOP command.

To exit Command Bus Training mode SDRAM controller switch to Low frequency, drive DQ [11] LOW to perform FSP switch and CK Sync OFF. After time tCKSNOFF issue Sync NOP and after tCKSNC issue the MRW command to disable command bus training mode. After time tMRD the LPDDR6 SDRAM is ready for normal operation.

#### 4.2.3.2.1 Entering CBT Mode

To enter CBT mode, issue an MRW-1 command followed by an MRW-2 command to set MR16 OP [6] = 0<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> for the CBT mode selection.

The WCK ODT value is fixed at 40 ohms regardless of the MR19 setting; DQ ODT and NT-ODT states are turned off. WCK\_t and WCK\_c are input pins for capturing DQ [11], DQ [10] and DQ [9] levels by toggling, and DQ [10] is a dedicated pin for capturing the VREF(CA) setting from DQ [6:0] during CBT mode. The WCK input is required to be at a valid level (WCK\_t = Low and WCK\_c = High), DQ [6:0] are required to be at valid levels, and DQ [11], DQ [10] and DQ [9] are required to be low before the MRW-2 command input. After tCBTWCKPRE\_static, the WCK signal can toggle, and tWCK2DQ11H must be satisfied before DQ [11] goes high. DQ [11] is driven HIGH, and when the LPDDR6 SDRAM samples the high level of DQ [11] by WCK, the LPDDR6 SDRAM switches from FSP-OP[x] to the FSP set defined by MR16 OP [5:4], completing the entry into CBT mode.

#### 4.2.3.2.2 Exiting CBT Mode

To exit CBT mode, change the CK frequency to the low-frequency operating point and then drive DQ [11] low after tDQ11LCK. The WCK toggle timing tWCK2DQ11H and tDQ11HWCK must be satisfied to capture the high-to-low transition of DQ [11]. The DQ [11] high-to-low transition is also used for CK sync off. After time tCKSNOFF, issue the CK Sync NOP command to perform the LPDDR6 SDRAM CK sync for low-frequency mode. After time tCKSNC, issue the CBT exit MRW command to set MR16 OP [5:4] = 00<sub>B</sub>.

After training exit, the LPDDR6 SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training. DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied. After time tMRD, the LPDDR6 SDRAM is ready for normal operation.

#### 4.2.3.3 Frequency Set Point (FSP) and Frequency Switching

The LPDDR6 SDRAM uses Frequency Set Points to enable multiple operating settings for the die. The LPDDR6 SDRAM is initiated to FSP-OP [0] at power-up, which has the default settings to operate in unterminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP [5:4] for FSP-WR (Frequency Set Point Write/Read Enable), setting all other mode register bits for FSP-OP (Frequency Set Point Operation Mode) to make the desired settings for high-frequency or mid-frequency operation, and setting MR16 OP [6] and MR16 OP [5:4] for CBT Mode selection.

Prior to entering Command Bus Training, the LPDDR6 SDRAM will be operating from FSP-OP[x]. Upon Command Bus Training entry when DQ [11] is driven HIGH, the LPDDR6 SDRAM will automatically switch to the active FSP register set FSP-OP[x], FSP-OP[y] or FSP-OP[z] according to MR16 OP [5:4] and use the active register settings during training. Upon Command Bus Training exit when DQ [11] is driven LOW, the LPDDR6 SDRAM will automatically switch back to the original FSP register set FSP-OP[x], returning to the “known-good” state that was operating prior to training. The training values for VREF(CA) are not retained by the DRAM in FSP-OP[y] or FSP-OP[z] registers and must be written to the registers after training exit.

#### 4.2.3.4 VREF CA and DQ Bus Input/Output Control During CBT Mode

VREF (CA) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF (CA) setting from DQ [6:0] during CBT mode. The LPDDR6 SDRAM samples the high and low level of DQ [10] using WCK.

- DQ [10] is used as a strobe pin for VREF(CA) setting updates via DQ [6:0] and serves as a DQ [7:0] output-mode-off switch.
- The LPDDR6 SDRAM samples DQ [6:0] levels at the internal DQ [10] rising edge and then updates its VREF(CA) setting. When the LOW level of DQ [10] is sampled by WCK, the DQ [7:0] output mode is turned off, and the input mode is turned on.
- DQ [7:0] becomes input pins for setting VREF(CA) level and the VREF(CA) level is captured at the internal DQ [10] rising edge which LPDDR6 SDRAM samples High level of DQ [10] by WCK. During input mode, DQ [6:0] is used for setting the VREF(CA), while DQ [7] is not used but must remain in valid state. The input level of DQ [6:0] must remain stable during the tDStrain + tDHtrain period, and DQ [10] should be maintained "High" for tDHtrain to complete the latching of specific patterns.
- DQ [7:0] becomes output pins to feedback the captured value via the command bus from the CS high signal until Low level of DQ [10] is sampled by WCK. Refer to Table 27 for CA to DQ mapping.
- After tDQ11HWCK and tDQ11DQ from DQ [11] rising edge, the LPDDR6 SDRAM can accept its VREF(CA) value change using input signals of DQ [6:0]. The LPDDR6 SDRAM samples DQ [6:0] by the internal DQ [10] rising edge and then updates the existing value that was set via MR12 OP [6:0]. The mapping between MR12 OP code and DQ's is shown in Table 25. At least one VREF(CA) setting is required before proceeding to the next training steps.
- The new VREF(CA) value must "settle" for time tVREF\_LONG or tVREF\_SHORT before sending new CA PRBS pattern.
- Refer to Table 26 for the DQ mapping function during command bus training mode.

**Table 25 – Mapping of MR12 OP Code and DQ Numbers**

<b>Mapping</b>							
MR12 OP code	OP [6]	OP [5]	OP [4]	OP [3]	OP [2]	OP [1]	OP [0]
DQ Number	DQ [6]	DQ [5]	DQ [4]	DQ [3]	DQ [2]	DQ [1]	DQ [0]

#### 4.2.3.5 CK Sync OFF and LFSR Reset

LPDDR6 requires CK sync on and sync off timing whenever there is clock stop and frequency switch. CBT mode enters with low frequency mode and switch to high frequency for command bus training which requires sync off and sync on timing. DQ [11] is used to perform the Sync off operation during CBT mode. Sync on operation is performed with NOP Command once post frequency switch.

#### 4.2.3.6 Data Bit (DQ) Function during CBT

Table 26 – Data Bit (DQ) Function during CBT

DQ Number	DQ Functions during CBT
DQ [6:0]	Input pins for setting VREF(CA) level
DQ [7:0]	Output pins to feedback the captured value via the command bus CA [3:0] from the CS HIGH signal until Low level of DQ [10] is sampled by WCK
DQ [11]	FSP Switching and CK Sync off. To Enter/Exit CBT Mode
DQ [10]	To latch the VREF settings Switch b/w input and output mode
DQ [9]	LFSR and Compare logic output Reset

#### 4.2.3.7 Mapping of CA Input Pins to DQ Output Pins

Table 27 – CA to DQ Mapping

Phase	Phase1 (CLK Falling Edge)				Phase0 (CLK Rising Edge)			
CA	CA [3]	CA [2]	CA [1]	CA [0]	CA [3]	CA [2]	CA [1]	CA [0]
DQ	DQ [7]	DQ [6]	DQ [5]	DQ [4]	DQ [3]	DQ [2]	DQ [1]	DQ [0]

#### 4.2.3.8 PRBS Generator for CBT

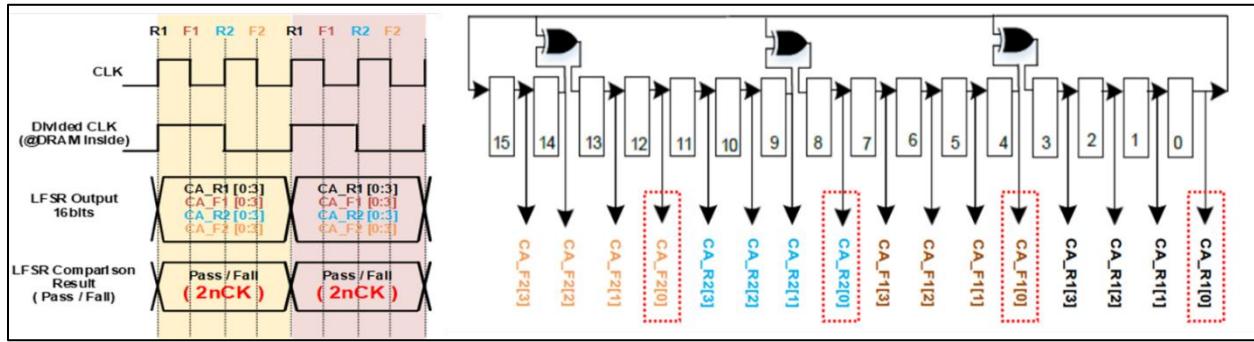
For the training of the command bus, the DRAM controller and the DRAM device will use the Pseudo Random Binary Sequence (PRBS16) with 16-bit Linear Feedback Shift Register (LFSR). This sequence generator will be used on the DRAM controller side to generate the bit stream for the training of the CA bits. The DRAM will use the same sequence generator to generate the expected data and then compare the received data with the expected data to find if the CA bits were transferred successfully from the DRAM controller to the DRAM device. The per CA lane comparison result at the DRAM will be sent back to the DRAM controller to take appropriate action.

The polynomial to be used for the PRBS is the PRBS16 polynomial  $X^{16} + X^{14} + X^9 + X^4 + 1$ . Figure 23 shows the hardware implementation of the PRBS generator on the DRAM controller side using a 16-bit shift register and XOR gates. Every fourth bit of the PRBS16 register is used to generate the data for the CA bus. Least significant bits are used for generating the CA data for rise edge and the most significant bits are used for generating CA data for the fall edge.

DRAM checks each CA pattern in 2nCK unit like normal command operation and error checking is done on each 16bit boundary which simplify the DRAM internal design. This also benefit LFSR operation at half the data rate with divided clock.

CA [3:0] capture on each R1/F1/R2/F2 edges and output 16bit CA data packet as shown in the following Diagram.

SoC has the same implementation to generate the 16bit output from matching LFSR and serialize CA packet at DRAM interface. To achieve the improved randomness across the bit sequence and CA phases, mapping of the CA bits updated with different CA pin phases are 4-clock apart.



**Figure 23 – PRBS16 Implementation**

To start the PRBS generator, it needs to be initialized with a seed. The DRAM controller and the DRAM device will use the same seed to initialize the PRBS16 generator to ensure the same pattern is generated on both sides. The default seed for Command bus training will be 16'h4411. This seed is chosen to initialize the PRBS generator such that it generates alternating 1 and 0 in the rise and fall sequence of the CA bits.

Table 28 shows the initial 8 values seen on the CA bus when the sequence generator is run with the default seed of 16'h4411.

#### 4.2.3.8 PRBS Generator for CBT (cont'd)

**Table 28 – LFSR Pattern**

PRBS state	CA_F2[3]	CA_F2[2]	CA_F2[1]	CA_F2[0]	CA_R2[3]	CA_R2[2]	CA_R2[1]	CA_R2[0]	CA_F1[3]	CA_F1[2]	CA_F1[1]	CA_F1[0]	CA_R1[3]	CA_R1[2]	CA_R1[1]	CA_R1[0]
16'h4411	0	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
16'h8300	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
16'h4180	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
16'h20c0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0
16'h1060	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0
16'h0830	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0
16'h0418	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0
16'h020c	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0
16'h0106	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0

PRBS generator will start from the default seed value, 16'h4411, whenever the generator is re-enabled. If the default seed of 16'h4411 is used, then the first data pattern seen on the CA bus from SoC will be 16'h8300 when the CS is high.

#### 4.2.3.9 Command Bus Training Sequence

In Command bus Training Mode, the CA values are sampled in the same way as for functional operation, where the CS qualifies which cycle the sampling occurs in, and the sample is captured by the rising and falling CK edge.

Sampling of the CA signals ONLY occurs when CS is asserted. Controllers send the PRBS CA pattern with CS asserted and DRAM has matching LFSR to compare each phase / bit and return the error on DQ bus.

DRAM Compare logic monitors the continuous data on every clock cycle and records the error if any of the CA bit fails. If there is no error, DRAM transmits the 0 on DQ bus and if any of the CA bit fails, DRAM transmits the 1 on mapping DQ bit.

If there is any error detected on a given CA lane from the same pattern, the corresponding DQ is driven HIGH after tADR, and it remains driven HIGH until next Sync NOP and LFSR Reset. If no error is detected from the same pattern from a given CA lane, the corresponding DQ is driven LOW after tADR, and it remains driven LOW.

During CA Training Mode the CA ODT is enabled for functional operation. The VREF (CA) is Group according to the functional setting. The timing requirements for the CA bus, CK\_t, CK\_c, and CS are the same as for functional operation. The following timing Diagram describes the CA training mode operation.

#### 4.2.3.10 Training Sequence Steps for Single-Rank Systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation.

- 1) Set MR13 OP [5:4] to enable writing to Frequency Set Point "Y" (FSP-WR[y]).
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters.
- 3) Set MR16 OP [6] = 0<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> to select CBT mode (CBT[y]).
- 4) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
- 5) Drive DQ [11] HIGH, and then change CK frequency to the high frequency operating point.
- 6) Update the VREF (CA) setting if required. VREF (CA) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF (CA) setting from DQ [6:0] during CBT mode.
- 7) Issue CK Sync NOP command.
- 8) Issue reset by asserting DQ [9] pulse signal to reset the LFSR and Command bus output results. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK.
- 9) Perform Command Bus Training (VREF(CA), CS and CA).
  - a. Send the long burst of CA PRBS pattern.
  - b. DRAM has matching LFSR to compare each phase / bit and return the output results on DQ bus
  - c. SoC check the results
- 10) Repeat steps 6-9 as required to complete the Command bust training
- 11) Exit training by driving DQ [11] LOW, a change CK frequency to the low frequency operating point prior to driving DQ [11] Low.
- 12) Issue CK Sync NOP
- 13) and then issue MRW-1 and MRW-2 commands to exit Command Bus Training mode.  
When DQ [11] is driven LOW and SDRAM samples the LOW level of DQ [11] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 14) DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied. After time tMRD, the LPDDR6 SDRAM is ready for normal operation.
- 15) Write the trained values to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 16) Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] to turn on termination and change CK frequency to the high frequency operation point. At this point the Command Bus is trained, and other training or normal operation can be executed.

#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems

Note that an example shown here is assuming an initial low-frequency, un-termination operating point, training a high-frequency or a mid-frequency, termination operating point. The blue text is low-frequency, the red text is high-frequency. Any operating point may be trained from any known good operating point. This example is assuming on the following condition. Frequency Set Point "X" for low frequency operation and Frequency Set Point "Y" for high frequency operation. FSP-WR[x] and FSP-OP[x] are initial state for both terminated rank and non-terminated rank. DQ ODT and NT-ODT for both terminated rank and non-terminated rank are required to be disabled with both FSP-OP[x] and FSP-OP[y] prior to start the command bus training.

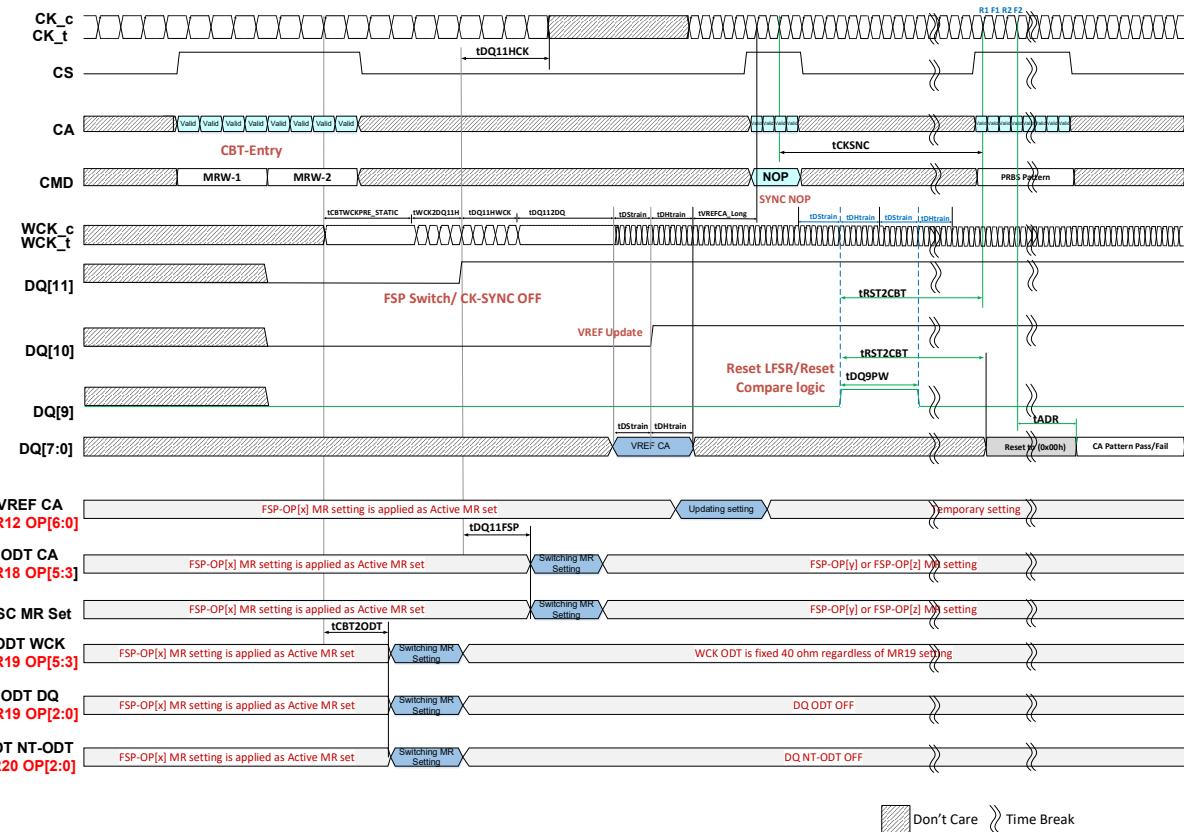
- 1) Set MR13 OP [5:4]to enable writing to Frequency Set Point "Y" (FSP-WR[y]) for both ranks.
- 2) Write FSP-WR[y] registers for all channels to set up high frequency operating parameters for both ranks.
- 3) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on the terminating rank: Set MR16 OP [6] = 0<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> to select CBT mode (CBT[y]).
- 4) Drive DQ [11] HIGH on the terminating rank (or all ranks), and then change CK frequency to the high frequency operating point.
- 5) Update the VREF (CA) setting if required. VREF (CA) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF (CA) setting from DQ [6:0] during CBT.
- 6) Issue CK Sync NOP command.
- 7) Issue reset by asserting DQ [9] pulse signal to reset the LFSR and Command bus output results. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK.
- 8) Perform Command Bus Training (VREF(CA), CS and CA) on terminating rank.
  - a. Send the long burst of CA PRBS pattern.
  - b. DRAM has matching LFSR to compare each phase / bit and return the output results on DQ bus
  - c. SoC check the results
- 9) Repeat steps 5-9 as required to complete the Command bust training on terminating rank
- 10) Change CK frequency to the low frequency operating point, and then drive DQ [11] LOW on the terminating rank (or all ranks). When DQ [11] is driven LOW and SDRAM samples the LOW level of DQ [11] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 11) Issue MRW-1 and MRW-2 commands to exit Command Bus Training mode (Normal Operation) on the terminating rank: Set MR16 OP [5:4] to select Normal Operation.
- 12) Write the trained values to FSP-WR[y] of the terminating rank by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 13) Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode (CBT[y]) on non-terminating rank: Set MR16 OP [6] = 0<sub>B</sub> and MR16 OP [5:4] = 01<sub>B</sub>, 10<sub>B</sub>, or 11<sub>B</sub> to select CBT mode (CBT[y]). But keep DQ [11] LOW.
- 14) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination. and then change CK frequency to the high frequency operating point.
- 15) Drive DQ [11] HIGH on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y].
- 16) Update the VREF (CA) setting for non-terminating rank if required. VREF (CA) setting updated via DQ [6:0]. DQ [10] is a dedicated pin for capturing the VREF (CA) setting from DQ [6:0] during CBT.
- 17) Issue CK Sync NOP command.

#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems (cont'd)

- 18) Issue reset by asserting DQ [9] pulse signal to reset the LFSR and Command bus output results. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK.
- 19) Perform Command Bus Training (VREF(CA), CS and CA) on non-terminating rank.
  - a. Send the long burst of CA PRBS pattern.
  - b. DRAM has matching LFSR to compare each phase / bit and return the output results on DQ bus
  - c. SoC check the results
- 20) Repeat steps 5-9 as required to complete the Command bust training on non-terminating rank
- 21) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] to turn off termination.
- 22) Exit training by driving DQ [11] LOW on the non-terminating rank, change CK frequency to the low frequency operating point, and issue MRW-1 and MRW-2 commands to exit Command Bus Training mode. When DQ [11] is driven LOW and SDRAM samples the LOW level of DQ [11] by WCK, the SDRAM will automatically switch back to the FSP-OP registers that were in use prior to training (i.e., trained values are not retained by the SDRAM).
- 23) Write the trained values of the non-terminating rank to FSP-WR[y] by issuing MRW-1 and MRW-2 commands to the SDRAM and setting all applicable mode register parameters.
- 24) Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] to turn on termination, and change CK frequency to the high frequency operation point. At this point the
- 25) Command Bus is trained for both ranks and other training or normal operation can be executed.

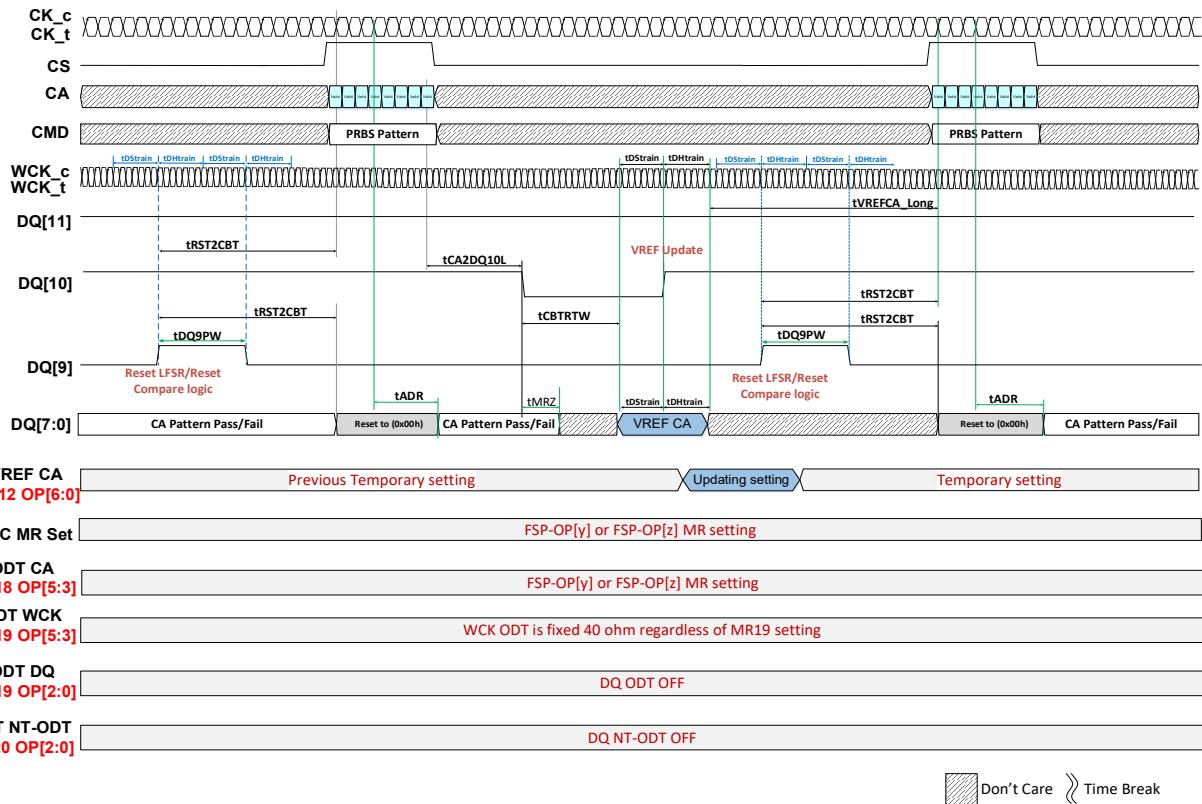
The basic timing diagrams of Command Bus Training are shown in following figures.

#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems (cont'd)



- NOTE 1 CS-CK training is done before CBT training.
- NOTE 2 FSP switch and CK sync off when DQ [11] is asserted or de-asserted.
- NOTE 3 After DQ [11] is driven HIGH and the SDRAM samples the HIGH level of DQ [11] by WCK toggle in CBT mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set.
- NOTE 4 CK sync NOP is required after entering CBT training mode.
- NOTE 5 CBT pattern starts at CK even edge with CS=High.
- NOTE 6 After tDQ11HCK, clock (CK) can be stopped, or frequency changed any time.
- NOTE 7 WCK\_t and WCK\_c are input pins for capturing DQ [11], DQ [10] and DQ [9] levels by toggling, and DQ [10] is a dedicated pin for capturing the VREF(CA) setting from DQ [6:0] during CBT training mode.
- NOTE 8 The value of the DQ [6:0] signal level is sampled by the DQ [10] rising edge. The DRAM updates its VREFCA setting of MR12 temporarily, after time tVREFCA\_long.
- NOTE 9 tVREFCA\_long may be reduced to tVREFCA\_short.
- NOTE 10 WCK ODT state is set to a fixed value 40 ohm regardless of MR19 setting and DQ ODT/NT-ODT are turned off during CBT training.
- NOTE 11 Differential WCK input is needed during CBT training mode.
- NOTE 12 DQ [9] is used to reset the LFSR and output compare logic. The LPDDR6 SDRAM samples the high and low level of DQ [9] using WCK. The WCK toggle timing tDStrain + tDHtrain must be satisfied to capture the high-to-low and low-to-high transition of DQ [9].
- NOTE 13 WCK frequency is don't care during CBT training as far as the frequency is within the allowed range of each frequency mode (MR11 OP [6]). WCK toggle may be stopped during tDQ11DQ and after tDHtrain, but WCK pair should be driven at static levels as WCK\_t = Low and WCK\_c = High. WCK should toggle to satisfy tWCK2DQ11H and tDStrain before either DQ [11] or DQ [10] changes again.

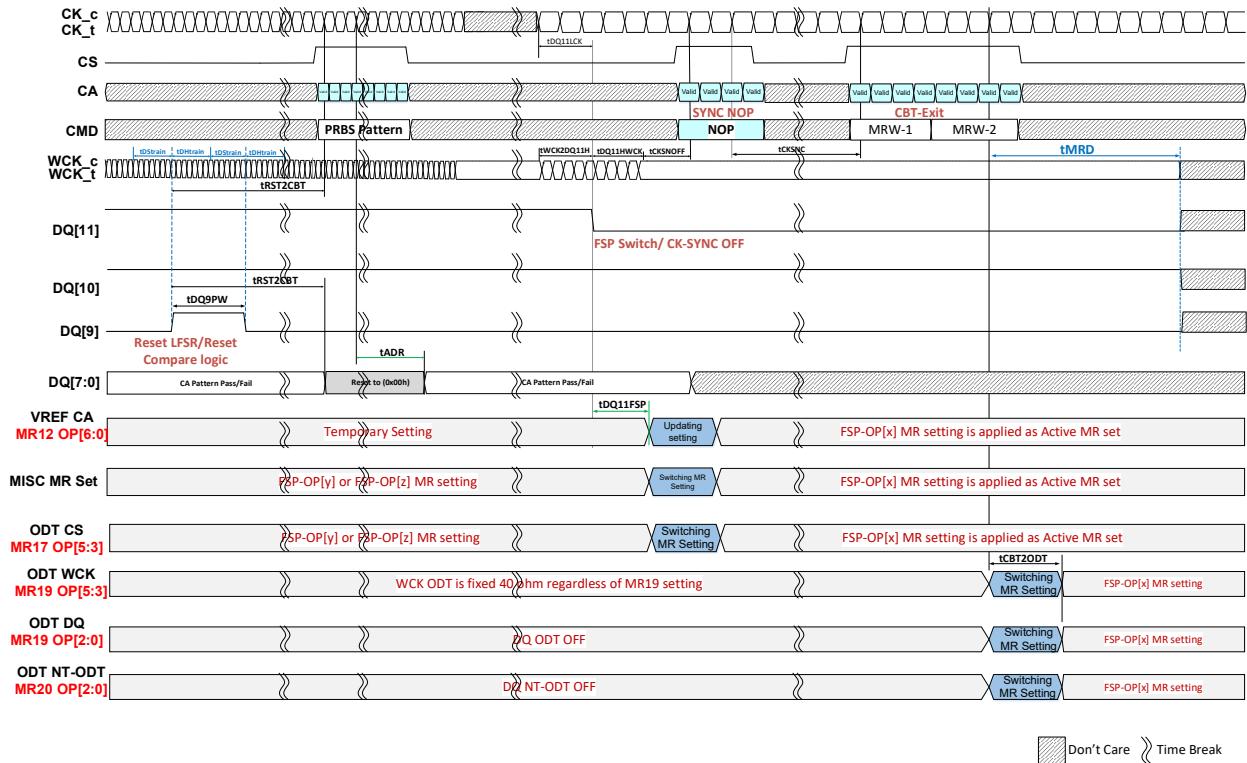
#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems (cont'd)



- NOTE 1 To change read mode to write mode for DQ pins, DQ [10] has to be driven LOW.  
 NOTE 2 The value of the DQ [6:0] signal level is sampled by DQ [10] rising edge. The DRAM updates its VREFCA setting of MR12 temporarily, after time tVREFCA\_long.  
 NOTE 3 tVREFCA\_long may be reduced to tVREFCA\_short.  
 NOTE 4 DQ [9] is used to reset the LFSR and Compare logic output.  
 NOTE 5 The host stops driving VREF on DQ [6:0] after satisfying the tDHtrain minimum and before resetting the DRAM LFSR/compare logic via DQ [9].

Figure 24 – CBT Sequence VREF Change

#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems (cont'd)



- NOTE 1 CK is required to satisfy tDQ11LCK before DQ [11] is driven low.
- NOTE 2 FSP switch and CK sync off performed when DQ [11] is asserted or de-asserted.
- NOTE 3 After DQ [11] is driven Low and the SDRAM samples the Low level of DQ [11] by WCK toggle in CBT mode, the SDRAM will switch its FSP-OP registers to use the alternate (i.e., non-active) set.
- NOTE 4 DQ [9] is used to reset the LFSR and Compare logic output.
- NOTE 5 WCK doesn't need to synchronize with clock signal during CBT mode.
- NOTE 6 DQ [11], DQ [10], DQ [9] and WCK signal are required to be valid level until tMRD which is caused by MRW command to exit this mode is satisfied.
- NOTE 7 Training values are not retained by the SDRAM and must be written to the FSP-OP register set before returning to operation at the trained frequency. Example: VREF(CA) will return to the value programmed in the original set point.

**Figure 25 – CBT Exit Sequence**

#### 4.2.3.11 Training Sequence Steps Multi-Rank Systems (cont'd)

Item Description	Parameters	Min/ Max	Data Rate	Unit	Note
			Up to 10667 Mbps		
Set-up margin between DQ11 and WCK	tWCK2DQ11H	Min	max (5ns, 12nWCK)	ns	
Hold margin between DQ11 and WCK	tDQ11HWCK	Min	max (5ns, 12nWCK)	ns	
Clock and Command Valid after DQ11 High	tDQ11HCK	Min	max (5ns, 4nCK)	ns	
Static WCK period (CBT entry to WCK toggling start)	tCBTWCKPRE_static	Min	max (20ns, 2nCK)	ns	
DQ11 High to valid DQ [6:0] input for VREFCA setting	tDQ11DQ	Min	250	ns	
Asynchronous Data Read	tADR	Max	2nCK + 18ns	ns	
Data Setup margin between DQ and WCK	tDStrain	Min	max (5ns, 12nWCK)	ns	
Data Hold margin between DQ and WCK	tDHtrain	Min	max (5ns, 12nWCK)	ns	
Switching from DQ input to output margin	tDHtrain	Max	max (20ns, 24nWCK)	ns	3
Last PRBS CA beat to DQ10 low	tCA2DQ10L	Min	max (tADR, 4nCK)	ns	
VREF Step Time – Long	VREFCA_long	Min	250 + 0.5tCK	ns	1
VREF Step Time – short	VREFCA_short	Min	200 + 0.5tCK	ns	2
CK Sync Period	tCKSNC	Min	TBD	ns	
CK Sync Off	tCKSNOFF	Min	TBD	ns	
DQ read out mode disable	tCBTRTW	Min	max (20ns, 24nWCK)	ns	
LFSR reset (DQ9H) to CBT	tRST2CBT	Min	max (20ns, 24nWCK)	ns	
LFSR reset (DQ9H) pulse width	tDQ9PW	Min	max (10ns, 12nWCK)	ns	
DQ10 Low to DQ driver off	tMRZ	Min	TBD	ns	
FSP change latency after DQ11 High or Low	tDQ11FSP	Min	20ns	ns	
NOTE 1	VREFCA_Long is for at least 2 step-size increment/decrement change including up to VREFmin to VREFmax or VREFmax to VREFmin change in VREF voltage.				
NOTE 2	VREFCA_short is for a single step-size increment/decrement change in VREF voltage.				
NOTE 3	The host stops driving VREF on DQ [6:0] after satisfying the tDHtrain minimum and before resetting the DRAM LFSR/compare logic via DQ [9].				

#### 4.2.4 WCK2CK Leveling

##### 4.2.4.1 WCK2CK Leveling Mode

To ensure proper CK-to-WCK timing and enable WCK2CK-Sync. operation, the LPDDR6 SDRAM provides a WCK2CK Leveling feature. This feature compensates for CK-to-WCK timing skew that may affect WCK2CK-Sync. operation. The memory controller uses asynchronous feedback on the DQ bus to adjust the CK-to-WCK relationship for the WCK\_t/WCK\_c signal pair. This ensures that the signals align with the phase cycle corresponding to the Write Latency delay after the WRITE FIFO (WFF) command. Once WCK2CK Leveling is complete, tWCK2CK, which represents the CK-to-WCK relationship, is determined, and WCK2CK-Sync. operation can be performed with optimized margin.

During WCK2CK Leveling mode, the CK frequency can be any frequency supported by the DRAM, such as 2400 MHz for a 9600 Mbps data rate device.

The LPDDR6 SDRAM enters WCK2CK Leveling mode when the mode register MR16 OP[2] is set HIGH. When in this mode, the state of the DQ pins is undefined. During WCK2CK Leveling training, the WCK\_t/WCK\_c pattern includes the fully programmed WCK preamble and only the first toggle of the normal data burst sequence. The DRAM samples the Internal WLV Pulse relative to the first WCK\_t/WCK\_c toggle of the data burst sequence (last rising differential WCK edge sent by the controller) and provides asynchronous feedback on the DQ bus after satisfying tWLVO. All data bits carry the training feedback to the controller. If the DQ bus output is LOW after tWLVO, the WLV Pulse signal was sampled while it was deasserted (LOW). Conversely, if the DQ bus output is HIGH after tWLVO, the Internal WLV Pulse signal was sampled while it was asserted (HIGH). The sampled feedback state remains on the DQ bus until a subsequent WCK2CK Leveling sample changes the state or until WCK2CK Leveling training is exited.

The Internal WLV Pulse is generated by the DRAM internal CK in response to a WRITE FIFO (WFF) command and held statically LOW otherwise. To perform WCK2CK Leveling training, the controller repeatedly sends a WRITE FIFO (WFF) command, delays WCK, and monitors the DQ feedback after tWLVO until a transition from 0 to 1 is detected, indicating alignment with the Internal WLV Pulse.

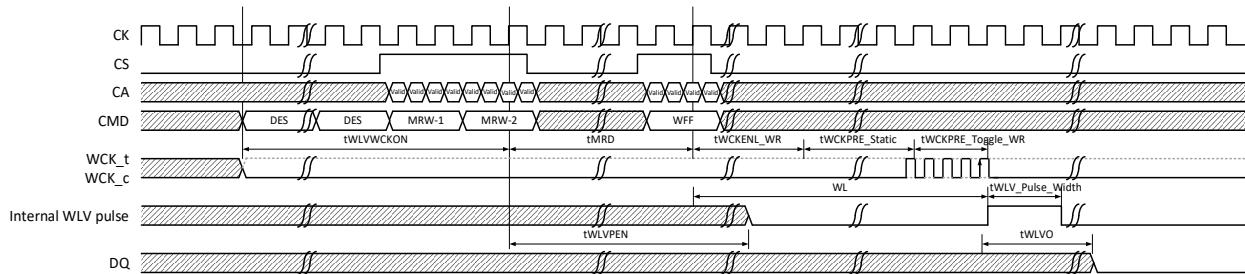
Upon completion of the WCK2CK Leveling, the SDRAM exits from WCK2CK Leveling mode when MR16 OP[2] is reset LOW.

WCK2CK Leveling should be performed before write training.

#### 4.2.4.2 WCK2CK Leveling Procedure and Related AC Parameters

Figure 26, Figure 27, and Figure 28 depict an example of WCK2CK Leveling procedure.

- 1) Start to drive WCK\_t LOW and WCK\_c HIGH.
- 2) Enter WCK2CK Leveling mode by setting MR16 OP[2]=1B. In WCK2CK Leveling mode, NT-ODT will be disabled even though NT-ODT is enabled by MR20 OP[2:0].
- 3) The controller issues a WRITE FIFO command with WS=1, followed by the WCK preamble (follow WCK pre-amble setting defined in the table "WCK2CK Sync AC Parameters for Write operation") and only the first toggle of the normal data burst sequence.
- 4) The LPDDR6 SDRAM generates an Internal WLV Pulse in response to a WRITE FIFO command.
- 5) The LPDDR6 SDRAM samples the Internal WLV Pulse relative to the first WCK\_t/WCK\_c toggle of the data burst sequence.
- 6) The LPDDR6 SDRAM provides asynchronous feedback of the sample result on all the DQ bits after time tWLVO. The feedback indicates whether the WLV Pulse signal was sampled while it was deasserted (LOW) or asserted (HIGH).
- 7) The controller references the feedback to increment or decrement the WCK\_t and WCK\_c delay setting. The controller can adjust the WCK delay setting only when it drives WCK\_t LOW and WCK\_c HIGH to prevent glitches in the WCK signal.
- 8) Repeat steps 3 through 7 until the proper WCK\_t/WCK\_c delay is established.
- 9) Exit from WCK2CK Leveling mode by setting MR16 OP[2]=0B. NT-ODT will come back to enable if NT-ODT is enabled by MR20 OP[2:0].



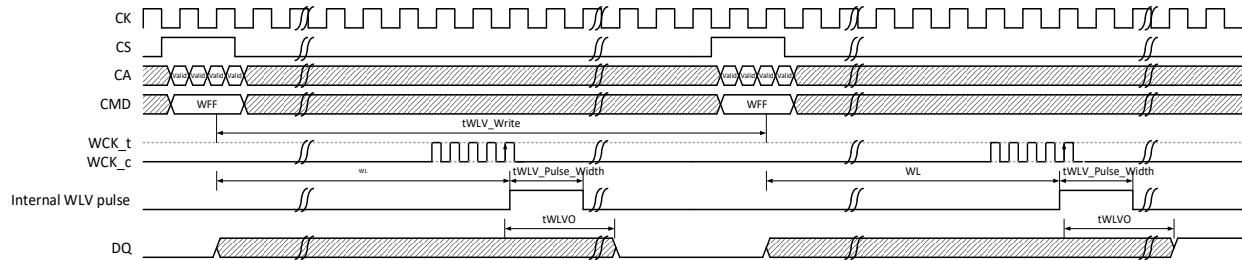
NOTE 1 WCK must be driven tWLWCKON earlier than WCK2CK Leveling entry.

NOTE 2 WCK2CK sample result on DQ bus is LOW since WCK phase is earlier than CK phase.

NOTE 3 tWCKPRE\_toggle\_WR = 2nCK in this example. Follow WCK pre-amble setting defined in the table "WCK2CK Sync AC Parameters for Write operation".

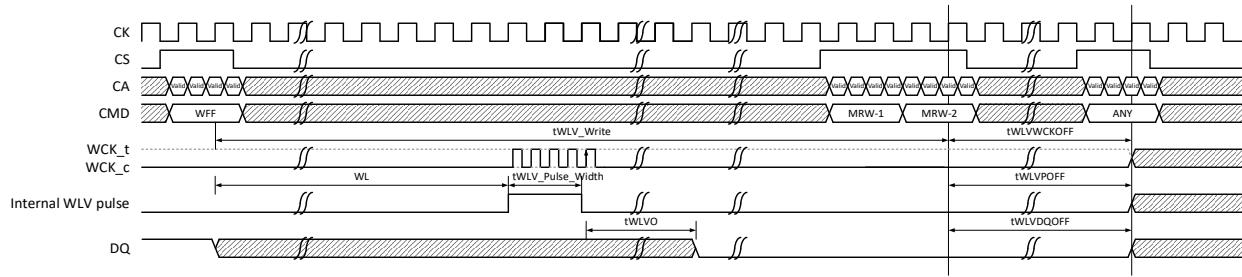
**Figure 26 – WCK2CK Leveling Entry and Leveling Result Output**

#### 4.2.4.2 WCK2CK Leveling Procedure and Related AC Parameters (cont'd)



- NOTE 1 DQ output transits from LOW to HIGH when WCK phase starts to be later than CK phase.
- NOTE 2 The controller is allowed to change WCK phase only when it is driving WCK\_t LOW and WCK\_c HIGH.
- NOTE 3 tWCKPRE\_toggle\_WR = 2nCK in this example. Follow WCK pre-amble setting defined in the table "WCK2CK Sync AC Parameters for Write operation".

**Figure 27 – Consecutive WCK2CK Leveling**



- NOTE 1 WCK2CK sample result on DQ bus is LOW since WCK is shifted more than 2\*nCK away from WL.
- NOTE 2 tWCKPRE\_toggle\_WR = 2nCK in this example. Follow WCK pre-amble setting defined in the table "WCK2CK Sync AC Parameters for Write operation".

**Figure 28 – WCK2CK Leveling Exit**

#### 4.2.4.2 WCK2CK Leveling Procedure and Related AC Parameters (cont'd)

Table 29 summarizes the timing parameters associated with the WCK2CK Leveling mode.

**Table 29 – WCK2CK Leveling Timing Parameters**

Parameter	Symbol	Min/ Max	Value	Units	Notes
WCK_t/WCK_c drive start to WCK2CK Leveling mode entry	tWLWCKON	Min	2	tCK	
WCK2CK Leveling training enable MRW to Internal WLV Pulse logic valid interval	tWLPEN	Max	15	ns	
Width of the Internal WLV Pulse	tWLV_Pulse_Width	Min/Max	2	tCK	
WCK2CK Leveling output delay	tWLVO	Min	0	ns	
		Max	Max(2tCK,20ns)	ns	
WCK off delay after WCK2CK Leveling mode exit	tWLWCKOFF	Min	Max(14ns,5tCK)	ns	
DQ off delay after WCK2CK Leveling mode exit	tWLVDQOFF	Max	Max(14ns,5tCK)	ns	
WRITE FIFO command to subsequent command interval during WCK2CK Leveling	tWLV_Write	Min	WL + tWLV_Pulse_Width + tWLVO(Max) + 2nCK		
WCK to CK phase offset	tWCK2CK	Min	Max(-0.5*tWCK,TBDps)	ps	
		Max	Min(0.5*tWCK,TBDps)	ps	

#### 4.2.5 Duty Cycle Adjuster (DCA)

LPDDR6 SDRAM supports a mode-register-adjustable WCK DCA to allow the memory controller to adjust the DRAM internal WCK clock tree duty cycle to compensate for systemic duty cycle error. WCK DCA is allowed only in WCK High Frequency mode (MR11 OP[6]=1<sub>B</sub>). WCK DCA is not guaranteed under WCK Low Frequency mode (MR11 OP[6]=0<sub>B</sub>) and DCA code, MR45 OP[3:0], should be set to 0000<sub>B</sub> in WCK Low Frequency mode.

The WCK DCA is located before the WCK divider or equivalent place. The WCK DCA will affect WCK duty cycle during the following operations:

- Read
- Write
- Mode Register Read
- Read FIFO
- Write FIFO
- Read DQ Calibration
- Duty Cycle Monitor

The controller can adjust the duty cycle through the MR45 OP[3:0] setting and can determine the optimal Mode Register setting for DCA in multiple different ways.

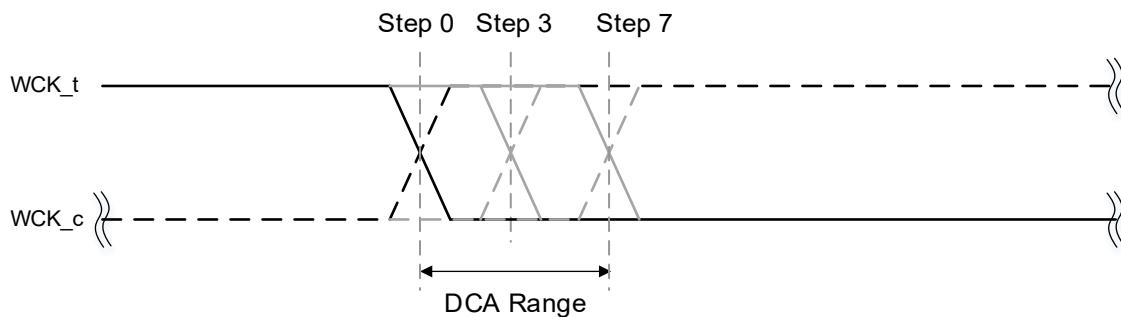
This function adjusts the SDRAM internal WCK duty cycle (Static).

##### 4.2.5.1 Duty Cycle Adjuster Range

The step range between the step 0 to 7(-7) is as follows. The difference of actual value between step N and step N+1 is defined to be within a spec range, since the variation of duty cycle by changing DCA code is not linear.

**Table 30 – Duty Cycle Adjuster Range**

Parameter	Min/Avg/Max	Value	Units	Note		
Duty Cycle Adjuster Total Range	Min	7.5	ps	1,2		
	Max	28				
Duty Cycle Adjuster 1-step Range	Min	1	ps	1,3		
	Max	4				
NOTE 1 These values are guaranteed by design.						
NOTE 2 Total range means the range from step 0 to step +7(-7).						
NOTE 3 1-step range includes non-linearity of each step.						

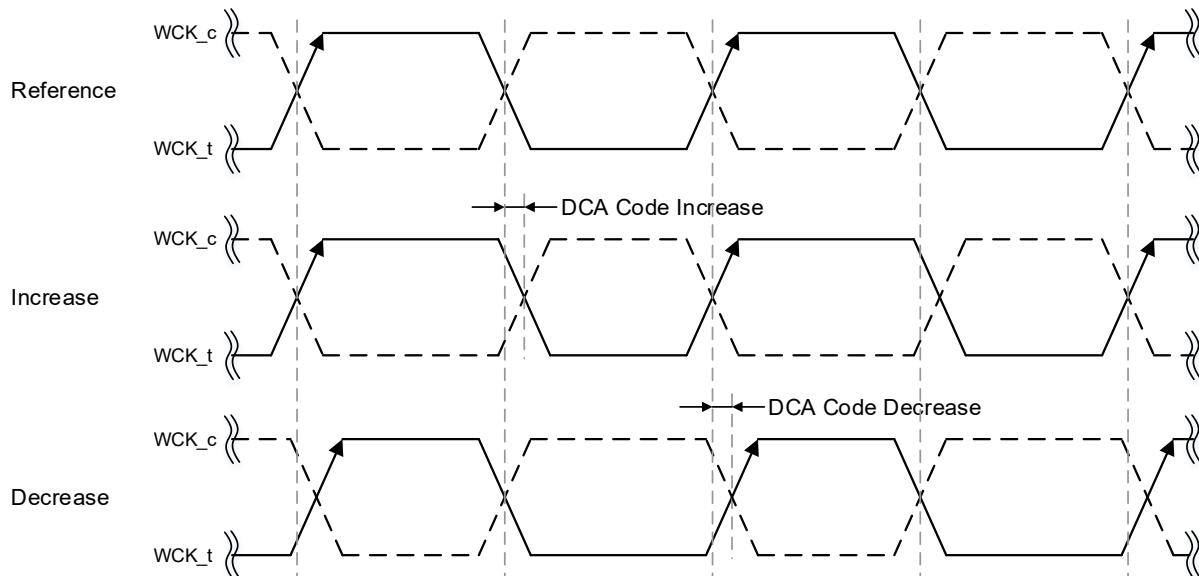


**Figure 29 – Duty Cycle Adjuster Range**

#### 4.2.5.2 Relationship between WCK Waveform and DCA Code Change

The basic operation of the DAC code change is as follows.

After DCA code change, it is recommended to re-execute WCK2CK leveling.



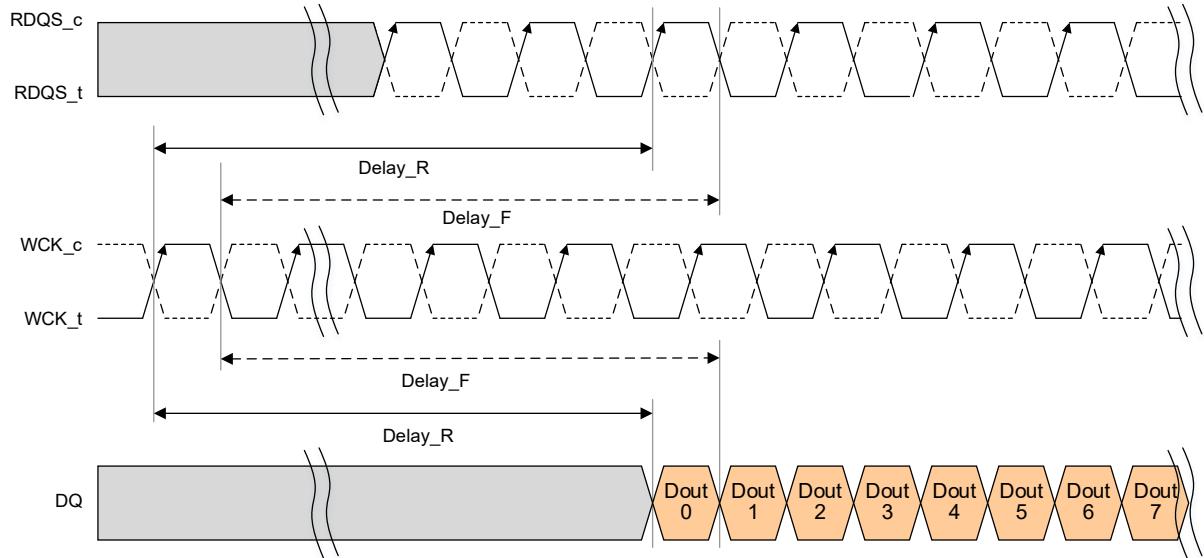
NOTE 1 Refer to clause 15.2: Write Clock Specification for the definition of tWCKH(avg) and tWCK(avg)

**Figure 30 – Relationship between WCK Waveform and DCA Code Change (Example)**

#### 4.2.5.3 Relationship between DCA Code Change and DQ Output/RDQS Timing

The WCK DCA code change effect to DQ Output and RDQS are as follows. The rising edge of WCK\_t affects to the rising edge of RDQS\_t and the even data output. The falling edge of WCK\_t affects to the falling edge of RDQS\_t and the odd data output. The complimentary signal (WCK\_c and RDQS\_c) is the same as the true signal.

The relationship between the DCA code change and delay time variation (Delay\_R/F) only can define in a qualitative manner.



**Figure 31 – Relationship between WCK Waveform, DQS\_t/c, and DQ Output (Example)**

#### 4.2.6 Read DCA (Duty Cycle Adjuster)

LPDDR6 SDRAM has read DCA function. Read DCA is also a mode-register-adjustable DCA to allow the memory controller to adjust DRAM read data duty to compensate duty distortion dedicated to read DQ.

Read DCA is located on adjusted WCK clock tree to provide dedicated read duty adjustment.

The read DCA will affect read data during following operations.

Read

Mode Register Read

Read FIFO

Read DQ Calibration

The controller can adjust the read duty cycle through the MR46 OP[6:3] setting and can determine the optimal Mode Register setting for DCA in multiple different ways. Since Read DCA has influence from WCK DCA, read DCA training should be after WCK DCA training. DRAM read data duty is to be monitored by the controller. To get proper duty distortion adjustment, LPDDR6 SDRAM WCK adjustment and sync should be performed in proper way.

##### 4.2.6.1 Read Duty Cycle Adjuster Range

The step range between the step 0 to 7 (-7) is as follows. The difference of actual value between step N and step N+1 cannot be defined, since the variation of duty cycle by changing Read DCA code is not linear.

For detail Read DCA code and timing relation, please refer to “Duty Cycle Adjuster Range” section.

**Table 31 – Read DCA Range**

Parameter	Min/Avg./Max	Value	Unit	Notes		
Read Duty Cycle Adjuster Total Range	Min	7.5	ps	1,2		
	Max	28				
Read Duty Cycle Adjuster 1-step Range	Min	1	ps	1,3		
	Max	4				
NOTE 1 These values are guaranteed by design.						
NOTE 2 Total range means the range from step 0 to step +7 (-7).						
NOTE 3 1-step range includes non-linearity of each step.						

##### 4.2.6.2 Relationship between Read DCA Code Change and DQ Output/RDQS Timing

The Read DCA code change effect to DQ Output and RDQS are as follows. The rising edge of WCK\_t affects the rising edge of RDQS\_t and the even data output. The falling edge of WCK\_t affects the falling edge of RDQS\_t and the odd data output. The complimentary signal (WCK\_c and RDQS\_c) is the same as the true signal.

The relationship between the Read DCA code change and delay time variation (Delay\_R/F) only can define in a qualitative manner.

For reference information please refer to Figure 31 (Relationship between WCK waveform and DQS\_t/c and DQ output).

## 4.2.7 Duty Cycle Monitor (DCM)

### 4.2.7.1 DCM Functional Description

LPDDR6 SDRAM devices feature a duty cycle monitor (DCM) to allow the memory controller to monitor WCK duty cycle distortion in the SDRAM internal WCK clock tree.

DCM operation is started by writing MR26 OP[0] (DCM Start/Stop) = 1<sub>B</sub>. Setting MR26 OP[0] = 0<sub>B</sub> terminates DCM operation. Prior to starting DCM operation, WCK2CK SYNC operation shall be performed with a CAS command in accordance with clause 7.3.1 WCK2CK Synchronization Operation. Continuous toggling of WCK input is required while DCM operation is enabled until TBD after DCM operation is halted by writing MR26 OP[0] = 0<sub>B</sub>.

DCM results may be inaccurate if DCM circuit hysteresis is present. To increase the accuracy of this function, the DCM supports flipping the input by setting MR26 OP[1] (DCM Flip) to the opposite state and then repeating the measurement.

DCM results will be continuously output to DQ after DCM starts and updated upon every DCM Flip switching activity. A separate DQ is assigned for the results of each DCM Flip state: DQ[2] reports DCM results of when DCM Flip bit is set to a logic low (MR26 OP[1] = 0<sub>B</sub>), and DQ[3] reports DCM results of when DCM Flip bit is set to a logic high (MR26 OP[1] = 1<sub>B</sub>). DCM results on each DQ will be updated when DCM Flip is switched away from its corresponding state. For example, DQ[2] will be updated when DCM Flip bit is switched from a logic low to a logic high.

The DCM circuit monitors both read/write WCK clock path. DCM operation requires WCK frequency higher than 1600 MHz.

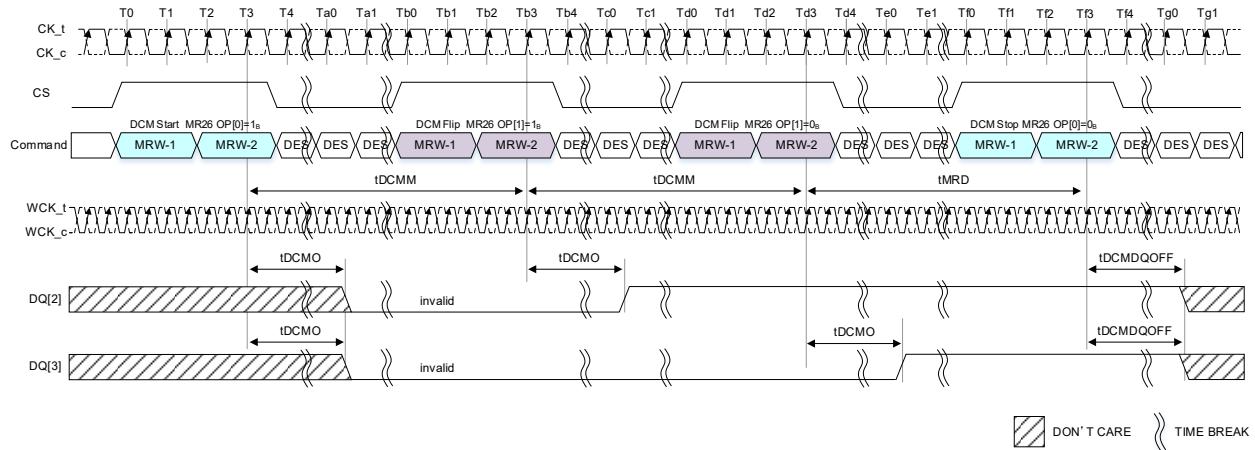
### 4.2.7.2 DCM Sequence

DCM training is expected to be done after CST and CBT to ensure that MRW operation can be reliably performed. Below is a DCM sequence that examines the duty cycle of the WCK path:

1. Update the FSP settings.
2. Issue a CAS command with WS=1 to toggle WCK at full rate before DCM starts.
3. Issue MRW-1 and MRW-2 to start DCM.
  - 3.1. Invalid data will be reported on DQ[2] and DQ[3] after tDCMO.
4. Wait tDCMM for the DCM to complete duty cycle measurement.
5. Issue MRW-1 and MRW-2 to switch MR26 OP[1] to flip the inputs of DCM.
  - 5.1. Switching the flip bit from a logic low to a logic high will:
    - 5.1.1. Capture the current DCM results of low DCM Flip state and output to DQ[2] after tDCMO
    - 5.1.2. Reset and start the DCM of high DCM Flip state
  - 5.2. Switching the flip bit from a logic high to a logic low will:
    - 5.2.1. Capture the current DCM results of high DCM Flip state and output to DQ[3] after tDCMO
    - 5.2.2. Reset and start the DCM of low DCM Flip state
6. Wait tDCMM for the DCM to complete duty cycle measurement with the flipped inputs
7. Exit DCM by issuing MRW-1 and MRW-2 to the LPDDR6 SDRAM device.

Changing DCA code (MR45 OP[3:0]) via MRW is prohibited during DCM operation (MR26 OP[0]=1<sub>B</sub>). Additionally, WRITE, WFF, READ, RDC, MRR and RFF commands are also prohibited during MR26 OP[0]=1<sub>B</sub>, and tMRD must be expired after setting MR26 OP[0]=0<sub>B</sub> by MRW command before they can be issued.

#### 4.2.7.2 DCM Sequence (cont'd)



**Figure 32 – DCM Timing Example**

The following table describes the relationship between DCM Flip state (MR26 OP[1]) and DCM results.

**Table 32 – DCM Output Example**

Comp. Output 0: < 50% 1: >= 50%	DCA Code	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7
	DCM Flip 'L'	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
	DCM Flip 'H'	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

**Table 33 – Duty Cycle Monitor Timing**

Parameter	Symbol	Min/Max	Value	Unit	Note
Duty Cycle Monitor Measurement Time	tDCMM	Min	2	μs	
Duty Cycle Monitor DQ Output Delay	tDCMO	Max	Max(35ns,4nCK)	ns	
DQ Off Delay After DCM Stop	tDCMDQOFF	Max	Max(35ns,4nCK)	ns	

#### 4.2.8 READ DQ Calibration

The LPDDR6 SDRAM devices feature a READ DQ Calibration training function that outputs a 24-bit user-defined pattern on the DQ pins. READ DQ Calibration is initiated by issuing a READ DQ CALIBRATION (RDC) command, which causes the LPDDR6 SDRAM to drive the contents of MR30 OP[3:0] followed by the contents of MR31 OP[7:0] on each of DQ[11:0]. The pattern can be either inverted or low-fixed on selected DQ pins according to user-defined invert masks or output data fix0 written to MR32, MR33 and MR34. The selection of either inverted or low-fixed is decided based on MR16 OP[3].

##### 4.2.8.1 READ DQ Calibration Training Procedure

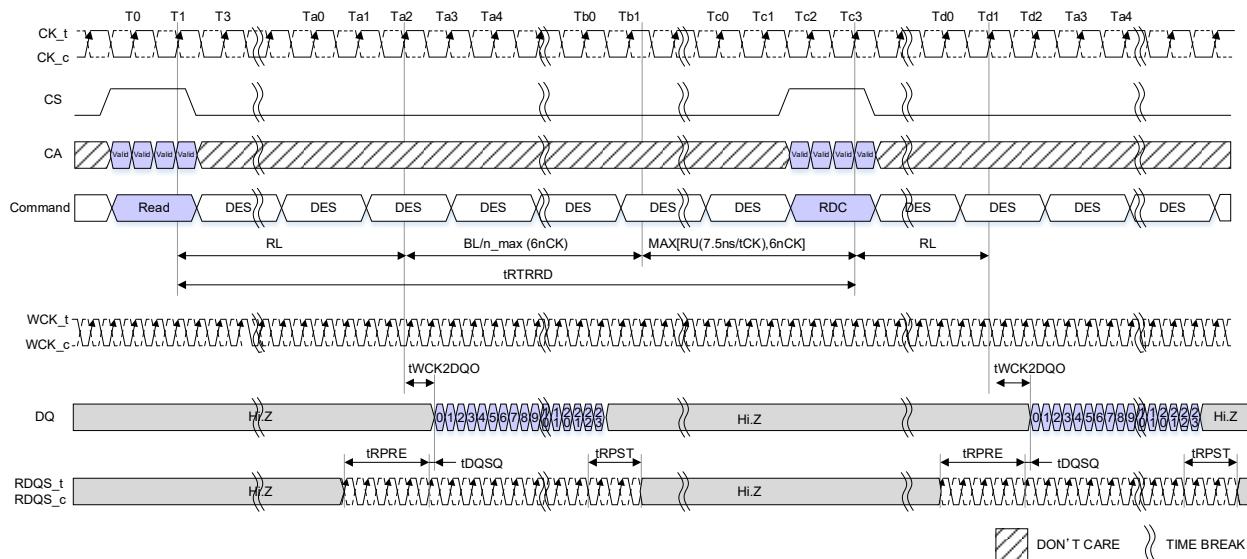
The procedure for executing READ DQ Calibration is:

- Issue MRW commands to write MR30 OP[3:0] (DQ[11:8]), MR31 (DQ[7:0]), MR32/33/34 (eight-bit invert mask or output data fix0 for byte0/1).
  - Optionally this step could be skipped to use the default patterns.
    - MR32 default = 5A<sub>H</sub>
    - MR33 default = 3C<sub>H</sub>
    - MR34 default = 50<sub>H</sub>
- RD DQ Calibration is initiated by issuing Read DQ Calibration (RDC) command while in a WCK2CK SYNC state.
- Each time an RDC command is received, the LPDDR6 SDRAM will drive a 24-bit data burst, after the currently set RL, by driving the eight bits programmed in MR32 followed by the eight bits programmed in MR33 and the eight bits in MR34 on all I/O pins. CAS command (WS = 1) is not required as long as WCK2CK-sync state is kept.
- When MR16 OP[3] = 0<sub>B</sub>, the data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
- When MR16 OP[3] = 1<sub>B</sub>, the data pattern will be low fixed for IO pins with a '1' programmed in the corresponding output data fix0 mode register bit (see Table 34).
- The RDC command can be issued seamlessly, and tRTRRD delay is required between Array Read command and the RDC command as well the delay required between the RDC command and an array read.
- The operands received with the CAS command must be driven LOW except WS\_RD.
- The function set by previous CAS operands is ignored. (DC0~3 and B3 are ignored.)
- DQ Read Training can be performed with any or no banks active, during Refresh, or during SREF without Power Down.

#### 4.2.8.1 READ DQ Calibration Training Procedure (cont'd)

Table 34 – Invert Mask or Output Data fix0 Assignments

DQ Pin	Pattern selects MR16 OP[3]	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
MR30	0	DQ8 invert	DQ9 invert	DQ10 invert	DQ11 invert	V	V	V	V
	1	DQ8 Fix0	DQ9 Fix0	DQ10 Fix0	DQ11 Fix0	V	V	V	V
MR31	0	DQ0 invert	DQ1 invert	DQ2 invert	DQ3 invert	DQ4 invert	DQ5 invert	DQ6 invert	DQ7 invert
	1	DQ0 Fix0	DQ1 Fix0	DQ2 Fix0	DQ3 Fix0	DQ4 Fix0	DQ5 Fix0	DQ6 Fix0	DQ7 Fix0



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK Always on mode.

NOTE 3 Read to Read DQ Calibration operation is shown as an example of command to command timing.  
Timing from Read to Read DQ Calibration is tRTRRD.

NOTE 4 Read DQ Calibration uses the same command to data timing relationship as Read command.

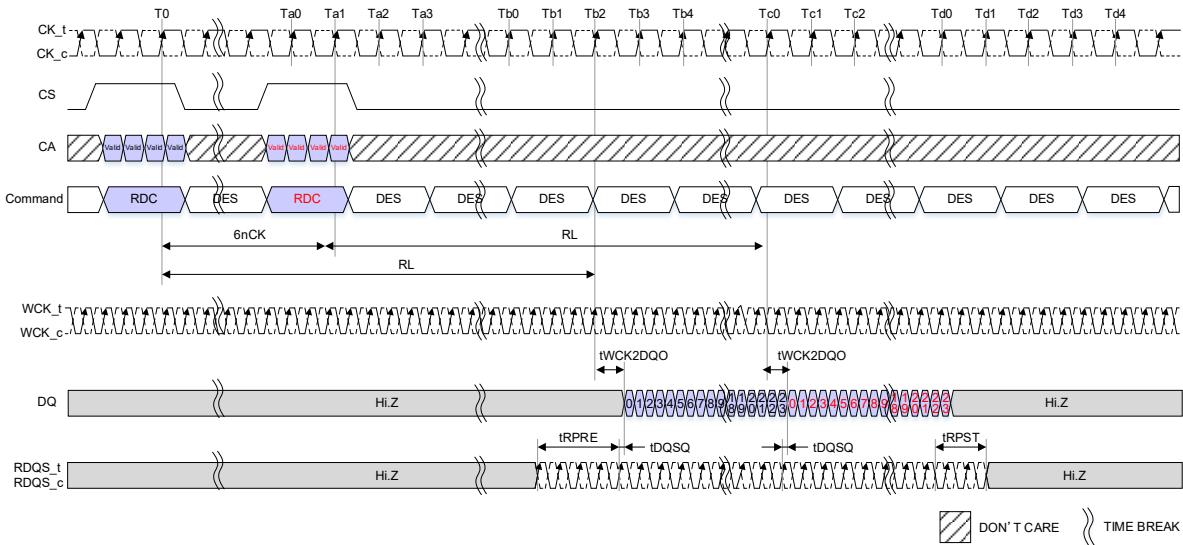
NOTE 5 If WCK2CK Sync off state, issuing CAS(WS) command is required prior to issuing Read DQ Calibration command. It means that WCK2CK Sync operation must be executed before issuing Read DQ Calibration command.

Read DQ Calibration uses the same timing relationship with the WCK2CK Sync operation as READ command.

NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 33 – Read to Read DQ Calibration Timing

#### 4.2.8.1 READ DQ Calibration Training Procedure (cont'd)



- NOTE 1 tWCK2CK is 0 ps in this instance.  
 NOTE 2 WCK Always on mode.  
 NOTE 3 Read DQ Calibration to Read DQ Calibration operation is shown as an example of command to command timing. Seamless Read DQ Calibration commands may be executed by repeating the command every period defined Training-Related Timing Constraints table.  
 NOTE 4 Read DQ Calibration uses the same command to data timing relationship as Read command.  
 NOTE 5 If WCK2CK Sync off state, issuing CAS(WS\_RD) or CAS(WS) command is required prior to issuing Read DQ Calibration command. It means that WCK2CK Sync operation must be executed before issuing Read DQ Calibration command. Read DQ Calibration uses the same timing relationship with the WCK2CK Sync operation as READ command.  
 NOTE 6 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 34 – Read DQ Calibration to Read DQ Calibration Timing

#### 4.2.8.2 READ DQ Calibration Example

An example of READ DQ Calibration Training output is shown in Table 35. This shows the 24-bit data pattern that will be driven on each DQ when one READ DQ CALIBRATION command is executed. This output assumes the following mode register values are used.

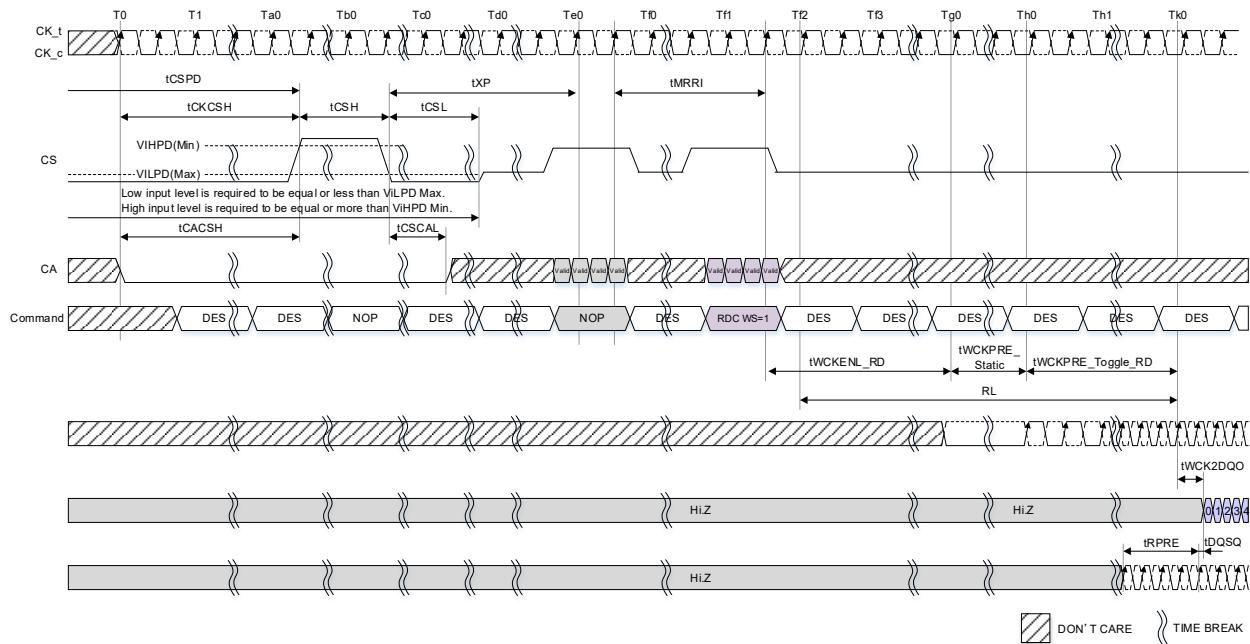
- MR32 default = 5A<sub>H</sub>
- MR33 default = 3C<sub>H</sub>
- MR34 default = 50<sub>H</sub>

Table 35 – Read DQ Calibration Bit Ordering, Inversion, Output Data fix0 Example for DQ

PIN	MR16 OP[3]	DQ	DQ output Data fix0	Bit Sequence																							
				23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQx	0	Yes	-	1	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
		No	-	0	1	0	1	1	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	1	1	0	0
	1	-	Yes	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		-	No	0	1	0	1	1	0	0	1	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

#### 4.2.8.3 READ DQ Calibration after Power Down Exit

Following the power down state, an additional time, tMRRI, is required prior to issuing the READ DQ CALIBRATION command. This additional time is required in order to be able to maximize power down current savings by allowing more power-up time for the Read DQ data in MR32, MR33 and MR34 data path after exit from standby, power down mode.



NOTE 1 tWCK2CK is 0 ps in this instance.

**Figure 35 – READ DQ CALIBRATION following Power Down State**

#### 4.2.9 WCK-DQ Training

The LPDDR6 SDRAM uses an un-matched WCK-DQ path to enable high speed performance and save power in the SDRAM. As a result, WCK is required to be trained to arrive at the DQ latch center-aligned with the data eye. The SDRAM DQ receiver is located at the DQ pad and has a shorter internal delay in the SDRAM than does the WCK signal. The SDRAM DQ receiver will latch the data present on the DQ bus when WCK reaches the latch, and training is accomplished by delaying the DQ signals relative to WCK such that the data eye arrives at the receiver latch centered on the WCK transition.

The LPDDR6 SDRAM provides a Command-based FIFO Write/Read training operation using user-specific patterns.

##### 4.2.9.1 Training Procedure

To perform Write Training, the controller is required to Write FIFO command to write data into the FIFO. Timing for the Write FIFO command is identical to the Write command. Up to 8 consecutive Write FIFO commands with user-defined patterns may be issued to the SDRAM to store up to 192 values (BL24 x 8) per pin that can be read back via the Read FIFO command.

The burst length of the Write FIFO and the Read FIFO command is limited to BL24.

The Write/Read FIFO Pointer operation is described later in this section.

After writing data to the SDRAM with the Write FIFO command, the data can be read back with the Read FIFO command and results compared with "expected" data to see if further training is needed. To read back the data, the controller is required to issue Read FIFO command to read back data from FIFO. Timing for the Read FIFO command is identical to the Read command.

The Read FIFO operation is non-destructive to the data captured in the FIFO, so data may be read continuously until it is overwritten by the Write FIFO command. For example: If 8 Write FIFO commands are executed sequentially, then a series of Read FIFO commands will read valid data from FIFO[0], FIFO[1]....FIFO[7], and will then wrap back to FIFO[0] on the next Read FIFO. If fewer than 8 Write FIFO commands were executed, then unwritten registers will have undefined (but valid) data when read back. For instance, if fewer than 8 Write FIFO commands are executed sequentially (example=3), then a series of Read FIFO commands will return valid data for FIFO[0], FIFO[1], and FIFO[2], however the next (8-3) Read FIFO commands will return undefined data for FIFO[3] through FIFO[7] before wrapping back to the valid data in FIFO[0].

During WCK-DQ Training, only the following commands are allowed to prevent overwriting of the Write and Read FIFO and to simplify this training procedure.

CAS(WS=1)  
CAS(WS\_OFF=1)  
Read FIFO  
Write FIFO  
DES  
NOP  
Refresh (All-bank and Dual-bank)  
Mode Register Write for FSP-WR: MR13 OP[5:4], FSP-OP: MR13 OP[7:6] VRCG: MR13 OP[3], and VREF(DQ[11:0]): MR14 OP[6:0].

WCK-DQ Training can be started at Idle, Bank active, during Refresh or Self Refresh of the SDRAM. WCK-DQ Training can be terminated when the FIFO pointer is the same value between Write and Read FIFO.

#### 4.2.9.1.1 WCK to DQ Training Requirement

WCK to DQ timing depends on the combination of Data Rate, ODT/NT-ODT setting, DVFSQ, and DVFSH/L state in use by a given system, and systems need to train under all combinations used. For example, a system that uses the following five conditions, would need to train WCK to DQ at all five conditions.

**Table 36 – System Operating Condition: Example**

Condition	Data Rate	ODT	NT-ODT	DVFSQ	DVFSH	DVFSL	DVFSB
1	1067Mbps	Disable	Disable	Disable	Disable	Disable	Disable
2				Enable	Disable	Enable	Disable
3	3200Mbps	Disable	Disable	Enable	Disable	Enable	Disable
4				Enable	Disable	Disable	Disable
5	10667Mbps	Enable	Enable	Disable	Enable	Disable	Enable

#### 4.2.9.1.2 Packet Format for WCK to DQ Training

WFF/RFF packet format is shown in Table 37.

32 metadata fields have been replaced by D256 (Extra) ~ D287 (Extra).

D256 (Extra) ~ D287 (Extra) data bits are stored into the FIFO the same as D0 ~ D255. It means that the data of D256 (Extra) ~ D287 (Extra) written by WFF command is read out by RFF command exactly as it is, and D256 (Extra) ~ D287 (Extra) never use with Meta, DBI and Link protection data.

**Table 37 – Burst Sequence (BL24) for WFF/RFF**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	D256 (Extra)	D257 (Extra)	D258 (Extra)	D259 (Extra)	D144	D145	D146	D147	D192	D193	D194	D195	D272 (Extra)	D273 (Extra)	D274 (Extra)	D275 (Extra)
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	D260 (Extra)	D261 (Extra)	D262 (Extra)	D263 (Extra)	D148	D149	D150	D151	D196	D197	D198	D199	D276 (Extra)	D277 (Extra)	D278 (Extra)	D279 (Extra)
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	D264 (Extra)	D265 (Extra)	D266 (Extra)	D267 (Extra)	D168	D169	D170	D171	D216	D217	D218	D219	D280 (Extra)	D281 (Extra)	D282 (Extra)	D283 (Extra)
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	D268 (Extra)	D269 (Extra)	D270 (Extra)	D271 (Extra)	D172	D173	D174	D175	D220	D221	D222	D223	D284 (Extra)	D285 (Extra)	D286 (Extra)	D287 (Extra)

#### 4.2.9.1.3 Relationship between MR Setting and FIFO Training Behavior

Write FIFO and Read FIFO command can be issued regardless of following MR setting. It means that these functions do not affect Write/Read data by WFF/RFF command even though each function is enabled.

- MR3 OP[0]: Read DBI
- MR3 OP[1]: Enhanced Write DBI
- MR23 OP[0]: Write Link ECC Mode
- MR23 OP[1]: Write Link EDC Mode
- MR23 OP[2]: Read Link ECC/EDC Mode

However, Read DBI and Read Link ECC/EDC Mode setting affect Read latencies, and Efficiency mode setting also affect Read latencies at RFF command. Refer to clause 7.4.2.2 Read and Read-to-Precharge Latencies for detail.

#### 4.2.9.2 FIFO Pointer Reset and Synchronism

The Read and Write FIFO pointers are reset under the following conditions:

Power-up initialization

RESET\_n asserted

Power-down entry

Self-Refresh Power-Down entry

The Write FIFO command advances the Write-FIFO pointer, and the Read FIFO command advances the Read-FIFO pointer. To keep the pointers aligned, the SoC memory controller must adhere to the following restriction at the end of WCK-DQ Training period:

- $b = a + (n \times c)$

Where:

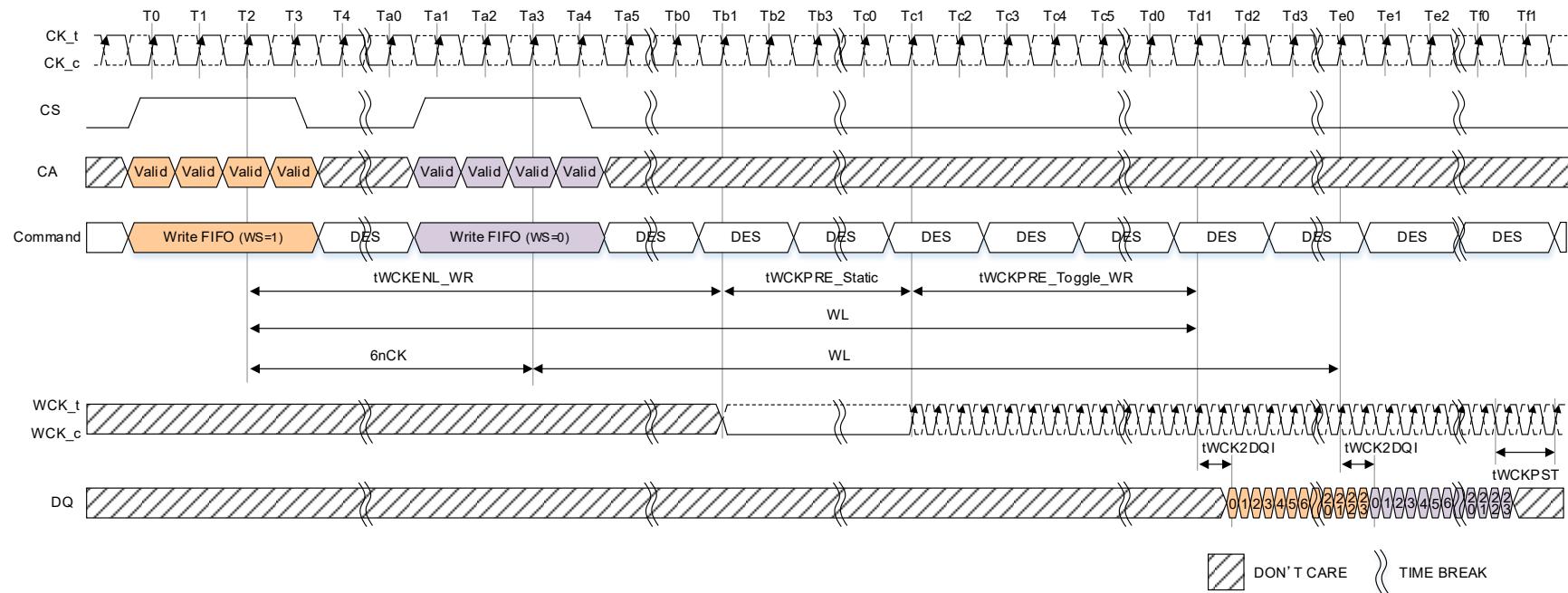
'a' is the number of Write FIFO commands

'b' is the number of Read FIFO commands

'c' is the FIFO depth (=8)

'n' is a positive integer,  $\geq 0$

#### 4.2.9.3 Timing Diagrams



NOTE 1 tWCK2CK is 0 ps in this instance.

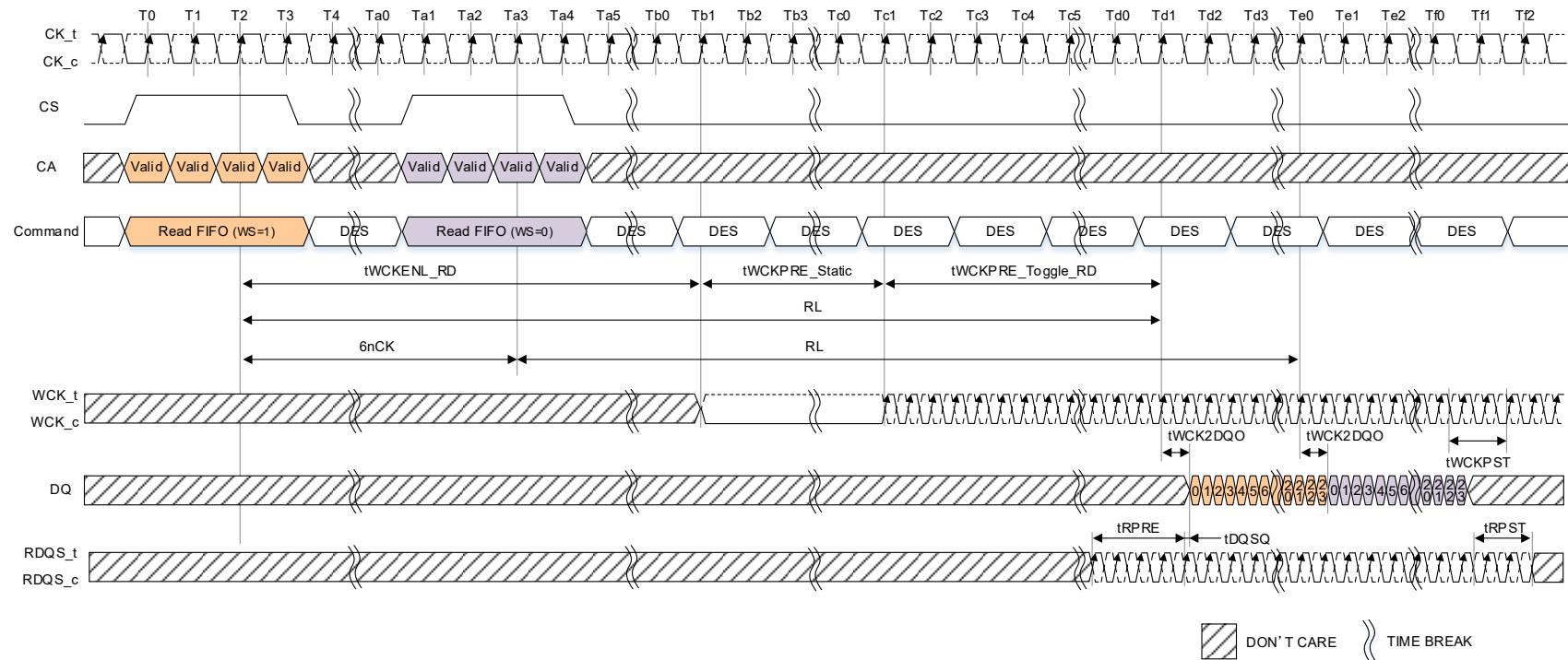
NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance.

NOTE 3 The (8 + 1) Write FIFO command will overwrite the FIFO data from the first command. If fewer than 8 Write FIFO commands are executed, then the remaining FIFO locations will contain undefined data.

NOTE 4 WS\_ON operand of Write FIFO command must be set accordingly depending on the WCK synchronization state.

Figure 36 – Consecutive Write FIFO Operation Timing

#### 4.2.9.3 Timing Diagrams (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 The end of both RL and tWCKPRE\_Toggle\_RD are the same timing in this instance.

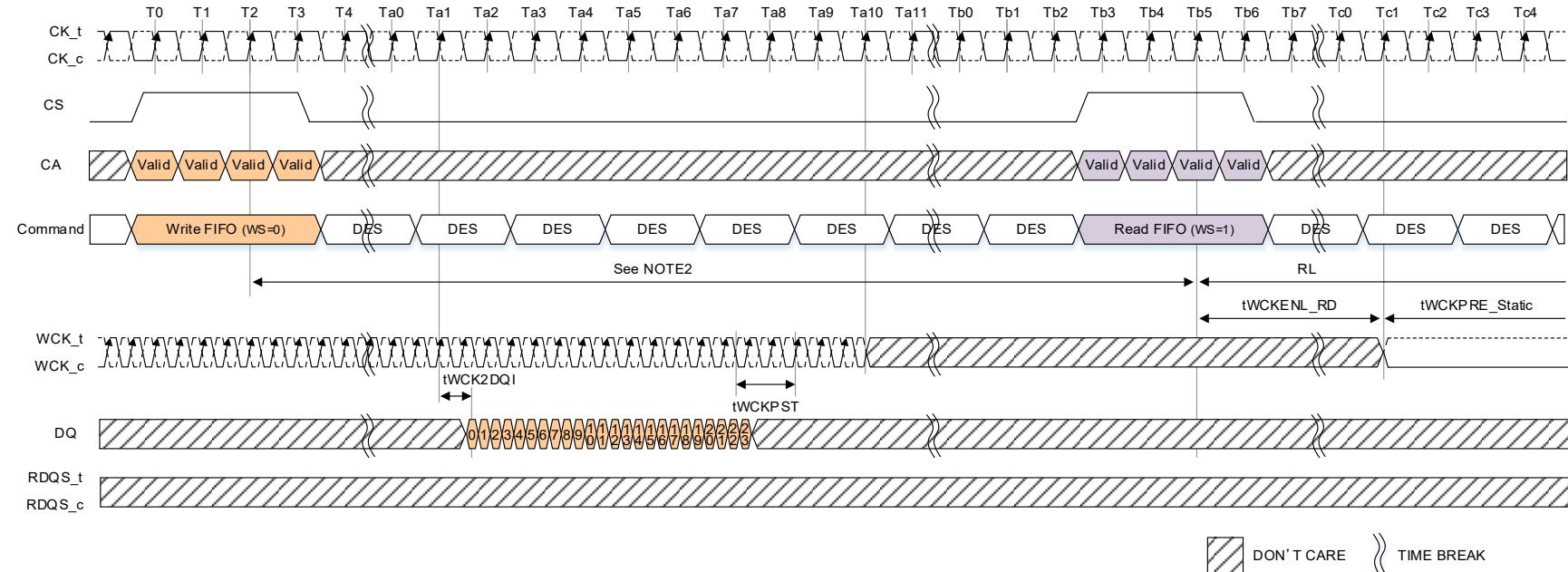
NOTE 3 Data may be continuously read from the FIFO without any data corruption. After 8 Read-FIFO commands the FIFO pointer will wrap back to the 1st FIFO and continue advancing.

NOTE 4 WS\_ON operand of Read FIFO command must be set accordingly depending on the WCK synchronization state.

Figure 37 – Consecutive Read FIFO Operation Timing

#### 4.2.9.4 Command Constraints for Write/Read FIFO Command

The command constraints related to Write FIFO and Read FIFO commands are described in clause 8.7 Training-related Timing Constraints.

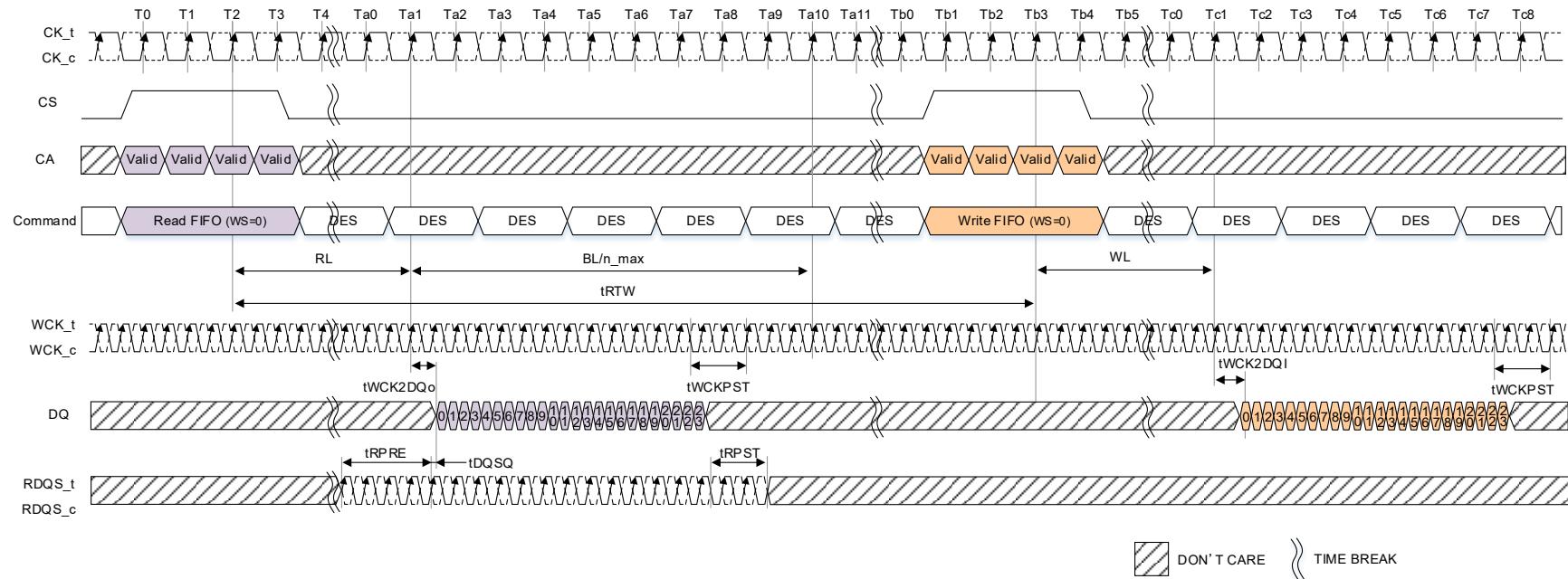


NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 Max(4nCK, WL+BL/n\_max-RL +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT disabled (MR20 OP[2:0] = 0B)  
 Max(4nCK, WL+BL/n\_max-RL+RU[tODToff(max)/tCK] +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT enabled (MR20 OP[2:0] ≠ 0B)  
 See Table 398 - Training-Related Timing Constraints for more detail.

Figure 38 – Write FIFO to Read FIFO Timing

#### 4.2.9.4 Command Constraints for Write/Read FIFO Command (cont'd)



NOTE 1  $t_{WCK2CK}$  is 0 ps in this instance.

Figure 39 – Read FIFO to Write FIFO Timing

#### 4.2.10 Enhanced RDQS Training

LPDDR6 SDRAM will enter Enhanced RDQS training mode by setting MR46 OP[0]=1<sub>B</sub>. Before entering Enhanced RDQS training mode, WCK2CK Sync should start by CAS (WS=1) command.

After WCKENL\_FS+tWCKPRE static period satisfied, MRW commands can be issued to enable Enhanced RDQS training mode. tERQE is passed after MRW command issued, the LPDDR6 will start driving RDQS\_t = low and RDQS\_c =high state.

To keep RDQS low impedance, during enhanced RDQS training mode WCK must continue toggling. When the LPDDR6 receives a Read, MRR or RDC Command, the LPDDR6 SDRAM will output RDQS and data. The RDQS preamble and post amble are followed MR Settings that includes RDQS Pre-shift and Half rate setting. LPDDR6 SDRAM will both keep up RDQS low-Z and WCK2CK sync state while in this mode even if Read, MRR and RDC were executed.

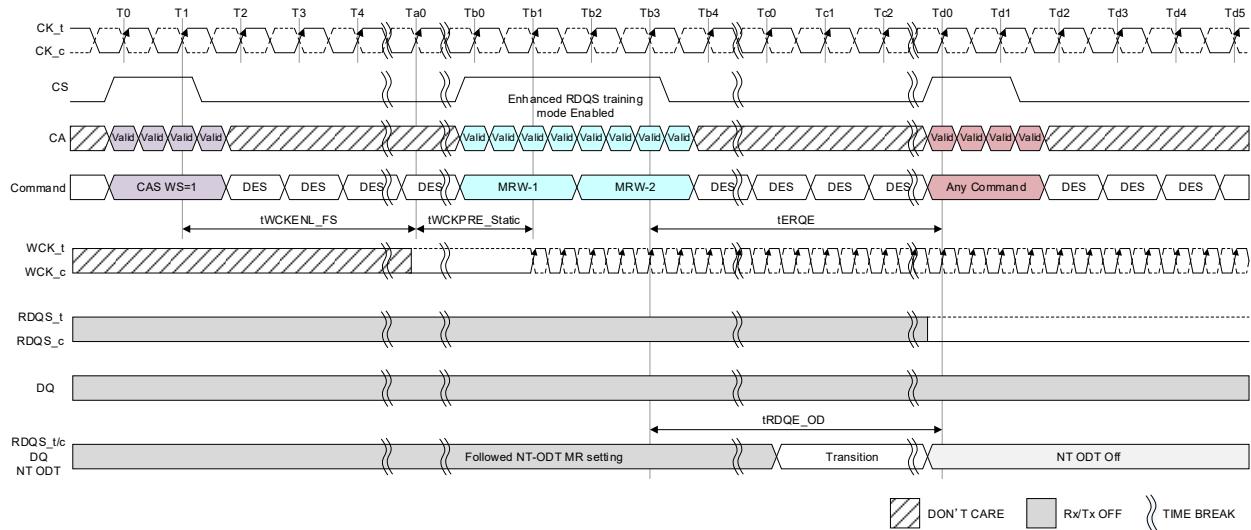
LPDDR6 SDRAM exits Enhanced RDQS training mode by setting MR46 OP[0]=0<sub>B</sub>. After tERQX has passed from MRW command, LPDDR6 SDRAM RDQS will transit to a Hi-impedance state. During tERQX period, WCK must continue toggling.

In tERQE and tERQX period, only the DES command is allowed and during Enhanced RDQS mode, ACT-1, ACT-2, PREpb, PREab, REFdb, REFab, READ (BL24), READ (BL48), MRR, MPC, and RDC can be issued but other commands are not allowed. Regarding MRW-1, MRW-2 command, only allowed exits from Enhanced RDQS training mode, other MRW command is prohibited.

RDQS and DQ ODT is disabled after tRDQE\_OD following Enhanced RDQS training entry via MRW command.

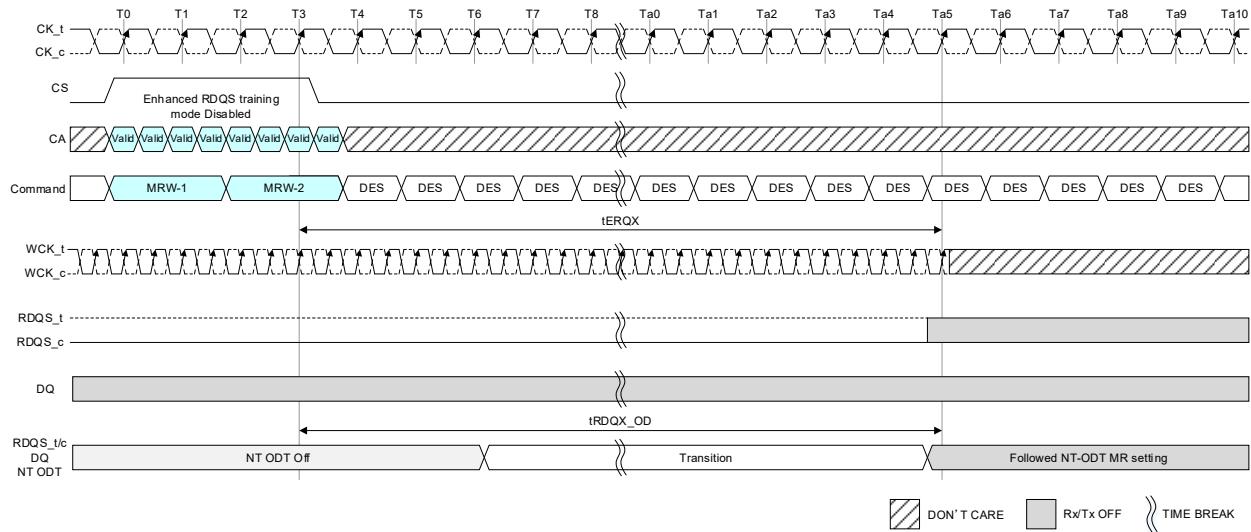
RDQS and DQ ODT are enabled with setting of NT-ODT MR after tRDQX\_OD following Enhanced RDQS training mode exit via MRW command.

#### 4.2.10 Enhanced RDQS Training (cont'd)



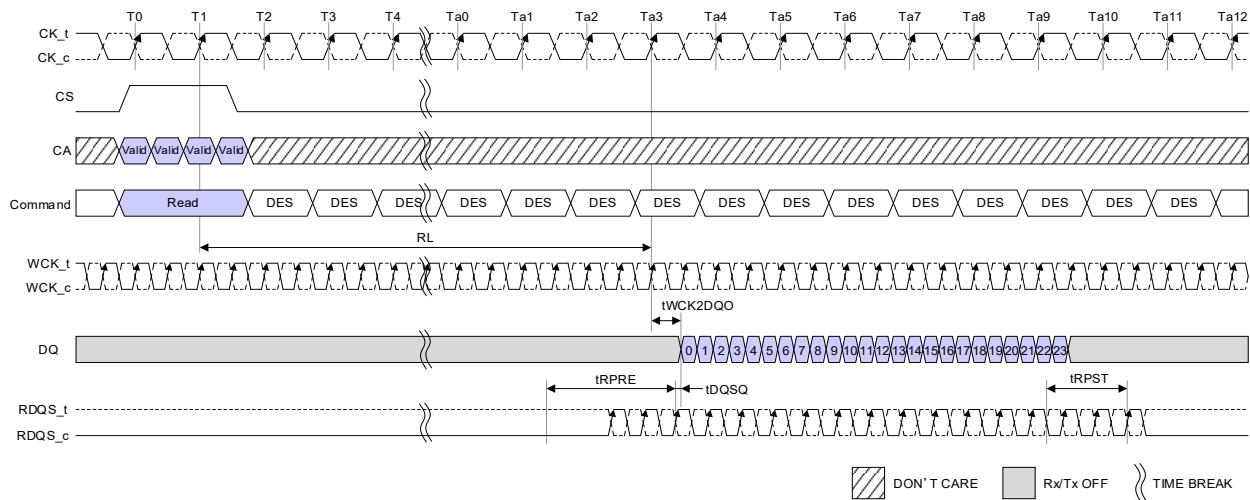
NOTE 1 In this case, "Any command" means a command that is allowed in the Enhanced DQS training mode.

**Figure 40 – Enhanced RDQS Training Mode Entry**



**Figure 41 – Enhanced RDQS Training Mode Exit**

#### 4.2.10 Enhanced RDQS Training (cont'd)



NOTE 1 WCK2CK Sync state.

NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 BL=24, tRPRE=2tWCK (Static) + 2tWCK (Toggle), tRPST=2.5tWCK(Toggle)

Figure 42 – Read Operation during Enhanced RDQS Training Mode

Table 38 – MR# and Operand Allowed to Change during Enhanced RDQS Training Mode

Function	MR# and Operand	Note
Enhanced RDQS (Enhanced RDQS training mode)	MR46 OP[0]	
TBD		
TBD		
TBD		

Table 39 – Enhanced Training Mode Entry and Exit Timing

Parameter	Symbol	Min/ Max	Value	Unit	Notes
Enhanced RDQS toggle mode entry	tERQE	Max	Max (35ns, 4nCK)	ns	
Enhanced RDQS toggle mode exit	tERQX	Max	Max (35ns, 4nCK)	ns	
ODT disable from Enhanced RDQS toggle mode entry	tRDQE_OD	Max	Max (35ns, 4nCK)	ns	
ODT enable from Enhanced RDQS toggle mode exit	tRDQX_OD	Max	Max (35ns, 4nCK)	ns	

#### 4.2.11 RDQS Toggle Mode

LPDDR6 SDRAM features an RDQS toggle mode that outputs continuous-toggle pattern on the RDQS pins. To enter RDQS toggle mode to set MR46 OP[1]=1<sub>B</sub>.

Before entering RDQS toggle mode, WCK2CK Sync should start by CAS (WS=1) command.

After WCKENL\_FS+tWCKPRE static period satisfied, MRW commands can be issued to enable RDQS toggle mode: MR46 OP[1]=1<sub>B</sub>. After "tERQE" passed after MRW command is issued, LPDDR6 SDRAM will start driving RDQS\_t and RDQS\_c. During RDQS toggle mode WCK must continue toggling.

LPDDR6 SDRAM exits the RDQS toggle mode by issuing a MRW MR46 OP[1]=0<sub>B</sub>. After "tERQX" has passed from MRW MR46 OP[1]=0<sub>B</sub>, RDQS\_t/c will transit to a Hi-impedance state. During tERQX period, WCK must continue toggling.

Refer to 4.2.10 for information on LPDDR6 enhanced RDQS training mode for tERQE, tERQX and ODT related timing.

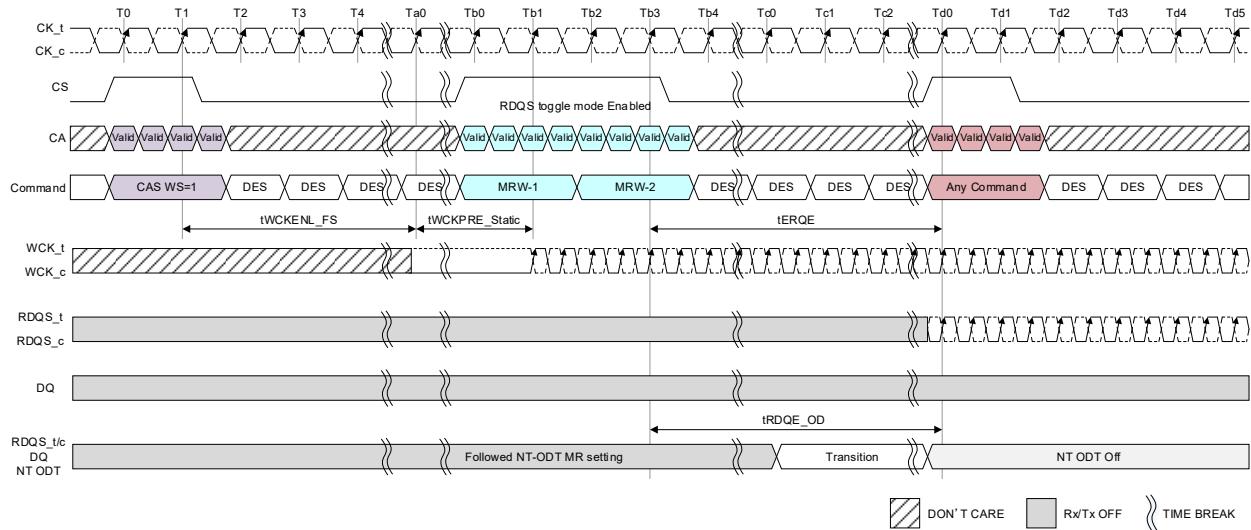
RDQS\_t/c output behavior follows RDQS: MR22 OP[1:0] setting. Therefore, enabling RDQS toggle mode is meaningless if MR22 OP[1:0] is 00<sub>B</sub>: RDQS\_t and RDQS\_c disabled.

In tERQE and tERQX period, only the DES command is allowed and during RDQS toggle mode, ACT-1, ACT-2, PREpb, PREab, REFdb, REFab and MPC can be issued but other commands are not allowed. Regarding MRW-1, MRW-2 command, only allowed exits from RDQS toggle mode, other MRW command is prohibited.

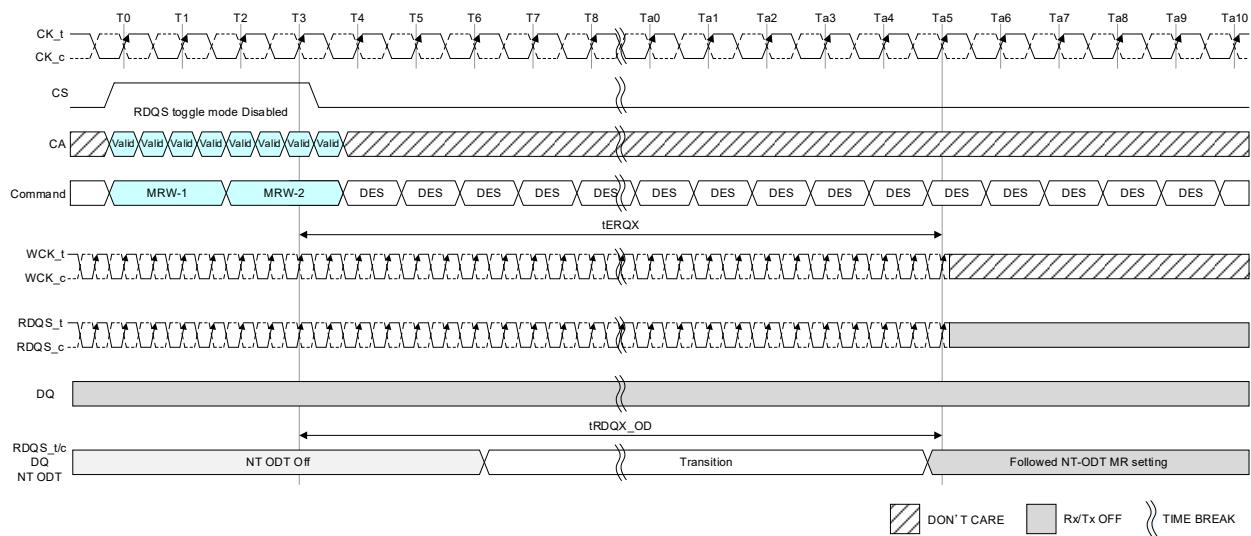
RDQS and DQ ODT is disabled after tRDQE\_OD following RDQS toggle entry via MRW command.

RDQS and DQ ODT are enabled with setting of NT-ODT MR after tRDQX\_OD following RDQS toggle mode exit via MRW command.

#### 4.2.11 RDQS Toggle Mode (cont'd)



**Figure 43 – RDQS Toggle Mode Entry**



**Figure 44 – RDQS Toggle Mode Exit**

**Table 40 – MR# and Operand Allowed to Change during RDQ Toggle Mode**

Function	MR# and Operand	Note
RDQS toggle (RDQS toggle mode)	MR46 OP[1]	
TBD		
TBD		
TBD		

## 4.2.12 Rx Offset Calibration Training

### 4.2.12.1 Offset Calibration Training Description

LPDDR6 SDRAM provides Offset Calibration Training for adjusting DQ Rx offset. It is recommended to operate the training every power-up and initialization training sequence to cope with the SDRAM operating condition change. Offset calibration is enabled by MR15 OP[7]. When the SDRAM starts the training, DQ channel can be floated. DQ ODTs shall be automatically enabled after MRW-1 and MRW-2 are issued for starting an Offset calibration training.

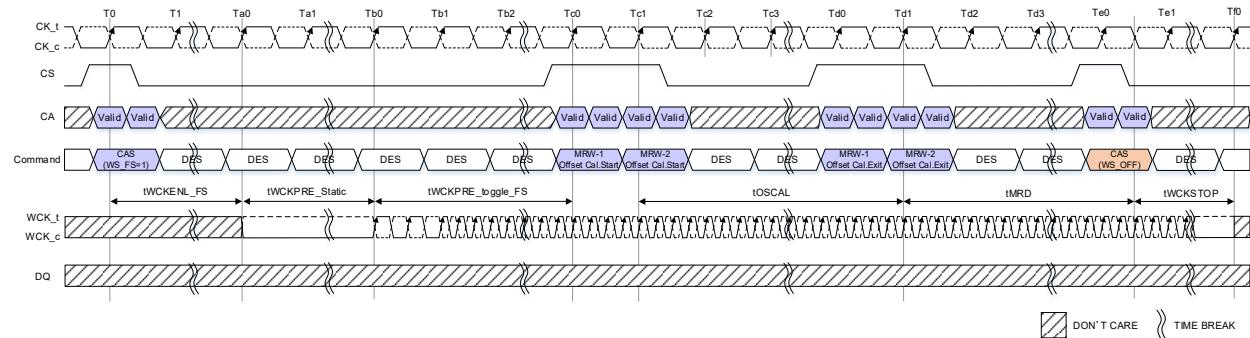
During the training, the SDRAM is required to be in WCK2CK sync state and WCK shall be toggled at full rate. It is recommended to synchronize WCK to CK by using CAS(WS) before the training. It is required to issue a CAS(WS\_OFF) command after the training exit for guaranteeing a safe WCK buffer Off.

In the case of WCK Always On mode (MR22 OP[5]=1B), the SDRAM sustains previous WCK2CK sync state after the training but a new WCK2CK sync operations is recommended for updating the training result. Please refer to “7.3.4 Write Clock Always On Mode (WCK Always On Mode)” for WCK buffer off and new WCK2CK sync.

### 4.2.12.2 Offset Calibration Training Sequence

Below is an Offset Calibration Training sequence.

1. Issue a CAS(WS) command and operate WCK2CK synchronization refer to “7.3.3.3 CAS with WCK2CK Synchronization” and keep toggling WCK at full rate.
2. Issue MRW-1 and MRW-2 for starting an Offset Calibration Training
3. Wait tOSCAL until the LPDDR6 SDRAM completes the Offset Calibration.
4. Issue MRW-1 and MRW-2 for exiting the Offset Calibration Training.
5. Issue CAS(WS\_OFF) command for WCK buffer off and keep toggling or stable WCK until tWCKSTOP.



**Figure 45 – Rx Offset Calibration Training Timing**

**Table 41 – Rx Offset Calibration Training Time Parameter**

Item	Symbol	Min/Max	Value	Unit	Note
Rx Offset Calibration Training time	tOSCAL	Max	TBD	μs	1
NOTE 1 This is the maximum time for SDRAM offset calibration operation.					

**Table 42 – Rx Offset Calibration Training Command Timing Constraint**

From	To	Min/Max	Timing constraint	Unit	Note
MRW-2 Offset Cal. Start	MRW-2 Offset Cal. Exit	Min	RU(tOSCAL/tCK)	nCK	-

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## 5 Simplified LPDDR6 State Diagram

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LPDDR6 SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

For the command definition, see section 4 Initialization and Training, and section 7 Command and Operation.

## 5 Simplified LPDDR6 State Diagram (cont'd)

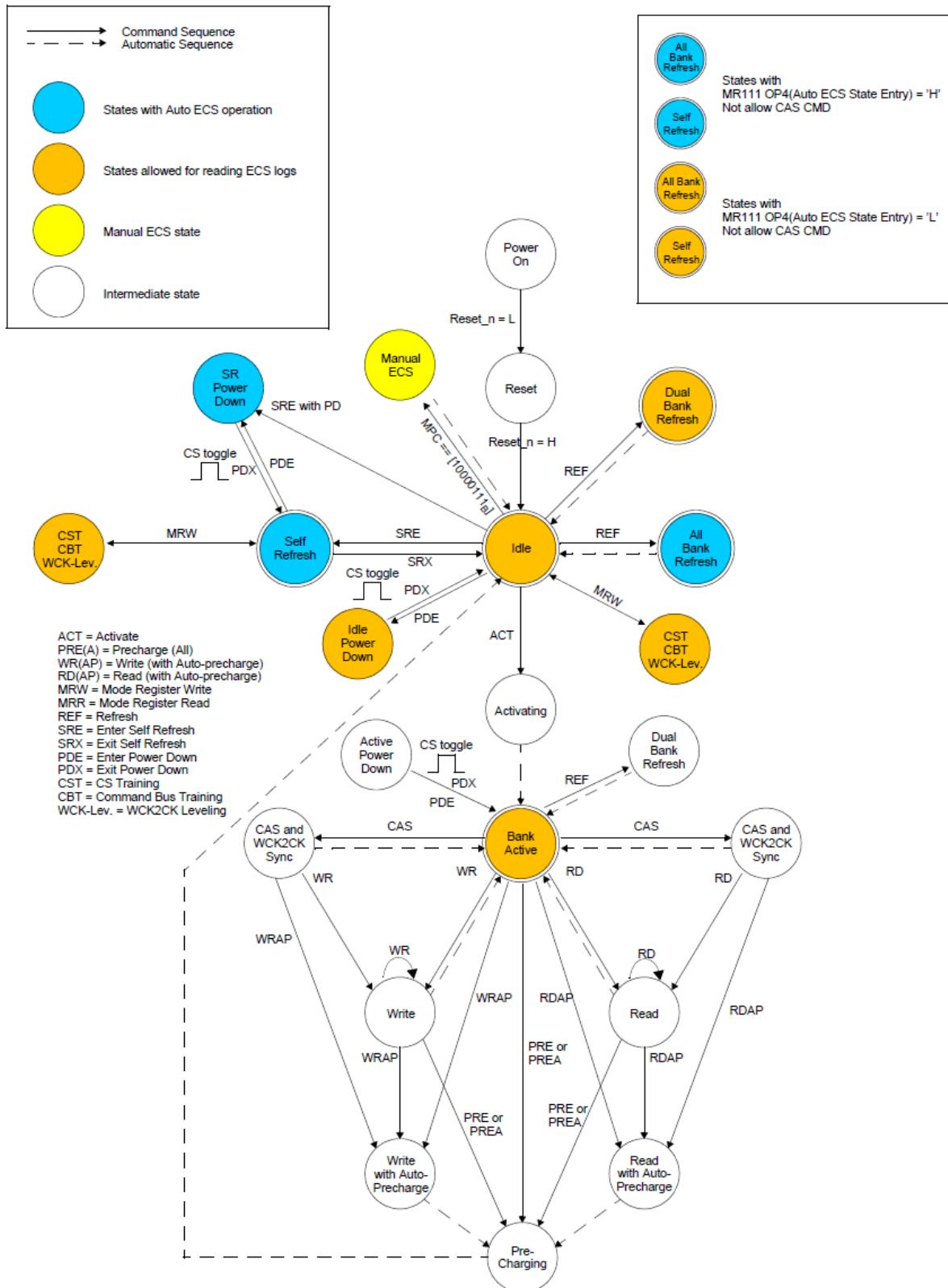


Figure 46 – LPDDR6: Simplified Bus Interface State Diagram

## 5 Simplified LPDDR6 State Diagram (cont'd)

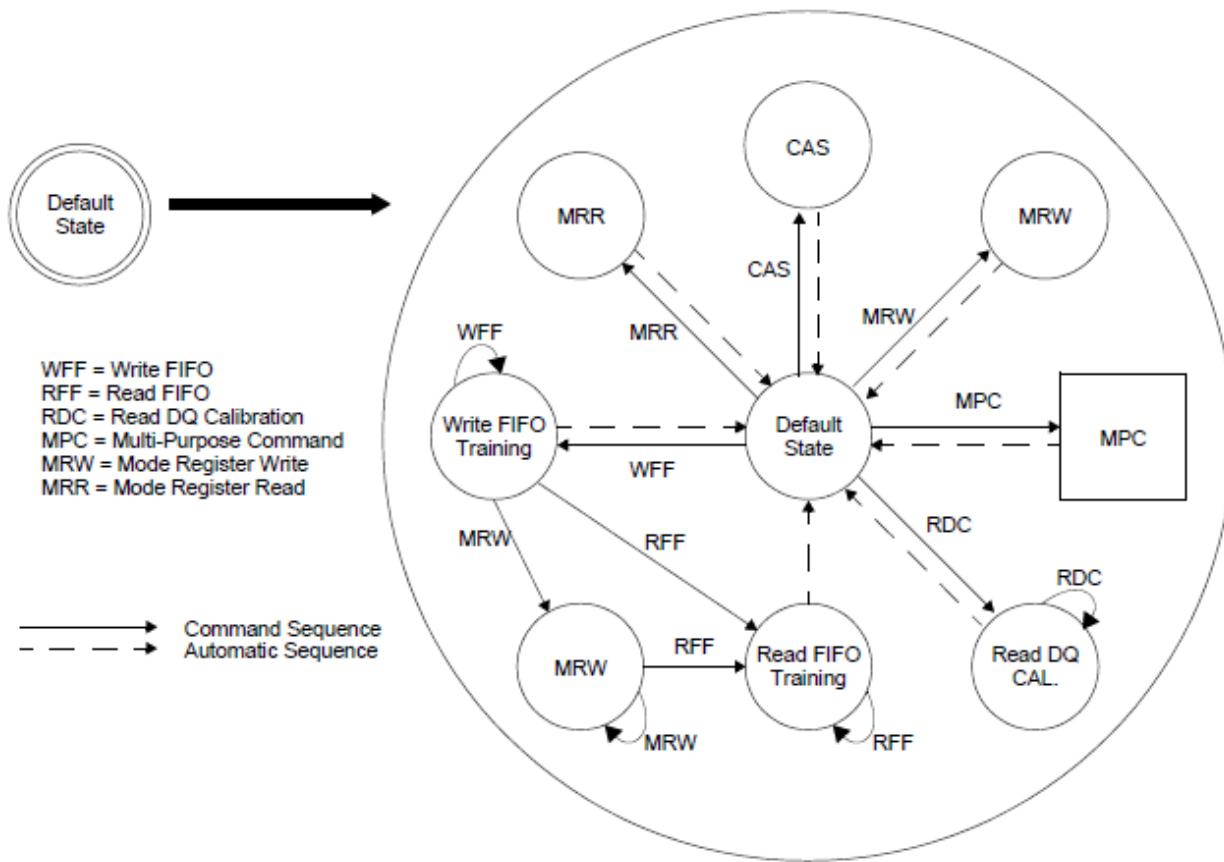
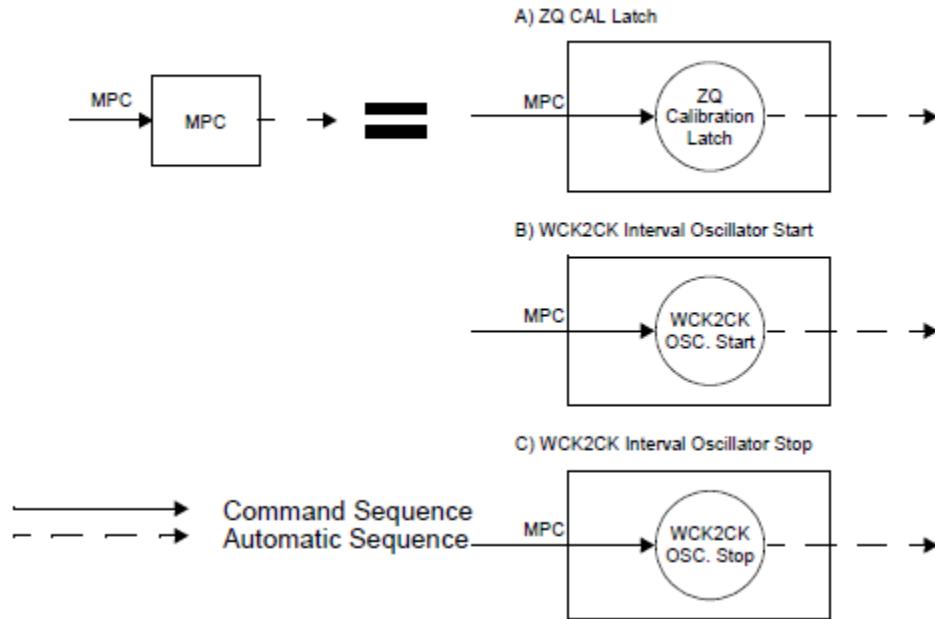


Figure 47 – Sub-State Diagram-1 Related with MRR, MRW, CAS, WFF, RFF, RDC, and MPC Commands

## 5 Simplified LPDDR6 State Diagram (cont'd)



**Figure 48 – Sub-State Diagram-2: Related with MPC State**

- NOTE 1 From the Self-Refresh state the device can enter Power-Down, MRR, MRW and MPC states. See TBD, on Self-Refresh, for more information.
- NOTE 2 In IDLE state, all banks are pre-charged.
- NOTE 3 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See TBD, on Mode Register Write (MRW), for more information.
- NOTE 4 In the case of an MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See TBD, on Multi-Purpose Command (MPC), for more information.
- NOTE 5 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
- NOTE 6 States that have an "automatic return" and can be accessed from more than one prior state (e.g., MRW from either idle or Active states) will return to the state from when they were initiated (e.g., MRW from Idle will return to Idle).
- NOTE 7 The RESET\_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET state applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET\_n.
- NOTE 8 Bank Active state can enter "CAS and WCK2CK Sync" State for WCK-to-CK Synchronization, Non-Target ODT setting or Burst Length setting if it is needed.
- NOTE 9 "Bank Active" to "Per-2-Bank Refresh" transition only refers to different banks not the same bank.
- NOTE 10 Only MRW commands for MR13 OP[5:4]: FSP-WR, OP[7:6]: FSP-OP, OP[3]: VRCG and MR14 OP[6:0]:VREF(DQ[11:0]) are allowed from WRITE FIFO command to READ FIFO command.
- NOTE 11 LPDDR6 supports dedicated CAS command and Read/Write with WS=1 for WCK2CK sync operation. WCK2CK sync status should be required for "Read"/"Write" state from "Bank Active".

## 6 Mode Register

LPDDR6 SDRAM has an independent Mode Register set for each sub channel. DVFS related mode registers such as DVFSH, DVFSB, DVFSL, and DVFSQ should be aligned to same condition before supply voltage change.

Additionally, the two sub-channels that constitute one channel must operate at the same operating frequency. Hence, any mode registers that prescribes a different setting for each speed grade, such as RL/WL/nWTP/nRTP/nACU, should be aligned to the same condition.

## 6.1 Mode Register Assignment and Definition in LPDDR6 SDRAM

Table 43 shows the mode registers for LPDDR6 SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register. LPDDR6 device provides additional MRR capability to some write-only Mode Registers containing important memory system configuration and status info.

**Table 43 – Mode Register Assignment in LPDDR6 SDRAM**

**Table 43 — Mode Register Assignment in LPDDR6 SDRAM (cont'd)**

**Table 43 — Mode Register Assignment in LPDDR6 SDRAM (cont'd)**

MR#	MA[6:0]	Access	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]			
32	20 <sub>H</sub>	W		DQ Calibration Pattern "A"									
33	21 <sub>H</sub>	W		DQ Calibration Pattern "B"									
34	22 <sub>H</sub>	W		DQ Calibration Pattern "C"									
35	23 <sub>H</sub>	R		WCK2DQI Oscillator Count – LSB									
36	24 <sub>H</sub>	R		WCK2DQI Oscillator Count – MSB									
37	25 <sub>H</sub>	R/W		WCK2DQI interval timer run time setting									
38	26 <sub>H</sub>	R		WCK2DQO Oscillator Count – LSB									
39	27 <sub>H</sub>	R		WCK2DQO Oscillator Count - MSB									
40	28 <sub>H</sub>	R/W		WCK2DQO interval timer run time setting									
41	29 <sub>H</sub>	R/W	RFU	MBIST Status	PPRE	MBIST Selection	MBIST Availability	PDFEC	PDFEC	PDFEC			
42	2A <sub>H</sub>	W		PPR KEY Protection									
43	2B <sub>H</sub>	R	PPR Resource BG1/Bank3	PPR Resource BG1/Bank2	PPR Resource BG1/Bank1	PPR Resource BG1/Bank0	PPR Resource BG0/Bank3	PPR Resource BG0/Bank2	PPR Resource BG0/Bank1	PPR Resource BG0/Bank0			
44	2C <sub>H</sub>	R	PPR Resource BG3/Bank3	PPR Resource BG3/Bank2	PPR Resource BG3/Bank1	PPR Resource BG3/Bank0	PPR Resource BG2/Bank3	PPR Resource BG2/Bank2	PPR Resource BG2/Bank1	PPR Resource BG2/Bank0			
45	2D <sub>H</sub>	W	RFU	RFU	RFU	RFU	DCA						
46	2E <sub>H</sub>	W	RFU	Read DCA				RFU	RDQS Toggle	Enhanced RDQS			
47	2F <sub>H</sub>	R		Serial ID-1									
48	30 <sub>H</sub>	R		Serial ID-2									
49	31 <sub>H</sub>	R		Serial ID-3									
50	32 <sub>H</sub>	R		Serial ID-4									
51	33 <sub>H</sub>	R		Serial ID-5									
52	34 <sub>H</sub>	R		Serial ID-6									
53	35 <sub>H</sub>	R		Serial ID-7									
54	36 <sub>H</sub>	R		Serial ID-8									
55	37 <sub>H</sub>	N/A		DNU (Do Not Use)									
56	38 <sub>H</sub>	W		Valid 0 or 1									
57	39 <sub>H</sub>	N/A		RFU									
58	3A <sub>H</sub>	N/A		RFU									
59	3B <sub>H</sub>	N/A		DNU (Do Not Use)									
60	3C <sub>H</sub>	W		Valid 0 or 1									
61	3D <sub>H</sub> - 63 - 3F <sub>H</sub>	N/A		DNU (Do Not Use)									
64	40 <sub>H</sub> - 68 - 44 <sub>H</sub>	N/A		RFU									
69	45 <sub>H</sub>	W	RFU				RFU						
70	46 <sub>H</sub>	W	RFU	DFEDQ1			RFU	DFEDQ0					
				DFEDQ1				DFEDQ0					
				DFEDQ1				DFEDQ0					

**Table 43 — Mode Register Assignment in LPDDR6 SDRAM (cont'd)**

**Table 43 — Mode Register Assignment in LPDDR6 SDRAM (cont'd)**

MR#	MA[6:0]	Access	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]						
91	5B <sub>H</sub>	W					DNU (Do Not Use)									
92	5C <sub>H</sub>	W	System Meta Mode Enable	RFU	Loopback Phase Select					Loopback Mode and Target DQ						
93	5D <sub>H</sub>	W					Enhanced Write DBI Set 0									
94	5E <sub>H</sub>	W					Enhanced Write DBI Set 1									
95	5F <sub>H</sub>	W					PAMM Segment									
96	60 <sub>H</sub>	N/A					RFU									
97	61 <sub>H</sub>	R	Sum of FMR2	MR4 Refresh rate change	CA Parity Fault Mode	RFU	OD-ECC MBE Fault	Write Link ECC SBE CA	Link ECC/EDC Fault	PRAC Limit Exceeded						
98	62 <sub>H</sub>	N/A					RFU									
99	63 <sub>H</sub>	W	Sum of FMR2	MR4 Refresh rate change	Alert State on CA parity Fault	RFU	OD-ECC MBE Fault	Write Link ECC SBE CA	Link ECC/EDC Fault	PRAC Limit Exceeded						
100	64 <sub>H</sub>	N/A					RFU									
101 -108	65 <sub>H</sub> 6C <sub>H</sub>	N/A					DNU (Do Not Use)									
109	6D <sub>H</sub>	R					TSRO									
110	6E <sub>H</sub>	R/W					RFU									
111	6F <sub>H</sub>	W	RFU	RFU	ECS support	Manual ECS On	Auto ECS State Entry	ECS Flag Reset	ECS Reset	Auto ECS On						
112	70 <sub>H</sub>	R	ECS CE Flag	ECS UE Flag	RFU	RFU	RFU	UE Address RA[16]	RFU	Max CE Per Row Address RA[16]						
113	71 <sub>H</sub>	R		Max CE Per Row Address BA[3:0]			UE Address BA[3:0]									
114	72 <sub>H</sub>	R					Max CE Per Row Address RA[15:8]									
115	73 <sub>H</sub>	R					Max CE Per Row Address RA[7:0]									
116	74 <sub>H</sub>	R					UE Address RA[15:8]									
117	75 <sub>H</sub>	R					UE Address RA[7:0]									
118	76 <sub>H</sub>	W	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU						
119	77 <sub>H</sub>	N/A	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU						
120 -123	78 <sub>H</sub> -7B <sub>H</sub>	N/A					DNU (Do Not Use)									
124	7C <sub>H</sub>	N/A					RFU									
125	7D <sub>H</sub>	R	CA3(F1)	CA2(F1)	CA1(F1)	CA0(F1)	CA3(R1)	CA2(R1)	CA1(R1)	CA0(R1)						
126	7E <sub>H</sub>	R	CA3(F2)	CA2(F2)	CA1(F2)	CA0(F2)	CA3(R2)	CA2(R2)	CA1(R2)	CA0(R2)						
127	7F <sub>H</sub>	N/A					RFU									
<table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td style="background-color: #d9e1f2;"></td><td>Applied when FSP=0</td></tr> <tr><td style="background-color: #f2e1e1;"></td><td>Applied when FSP=1</td></tr> <tr><td style="background-color: #c2e1c1;"></td><td>Applied when FSP=2</td></tr> </table>												Applied when FSP=0		Applied when FSP=1		Applied when FSP=2
	Applied when FSP=0															
	Applied when FSP=1															
	Applied when FSP=2															

NOTE 1 RFU bits shall be set to '0' during writes.

NOTE 2 All mode registers that are specified as RFU or write-only shall return undefined data when read.

NOTE 3 All mode registers that are specified as RFU should not be written.

NOTE 4 Writes to read-only registers shall have no impact on the functionality of the device.

NOTE 5 In order to guarantee proper operation, all mode registers that can be written shall be set to specified data, except "Reserved" and "RFU".

## 6.2 Mode Register Definition

**Table 44 – MR0 Register Information (MA [7:0] = 00<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Density per die			Sub-Ch	Eff status	Type		

**Table 45 – MR0 Definition**

Function	Register Type	Operand	Data	Notes
Type (Support Data Rate)	Read only	OP[1:0]	00 <sub>B</sub> : Up to 10667Mbps 01 <sub>B</sub> : RFU 10 <sub>B</sub> : RFU 11 <sub>B</sub> : RFU	
Eff status (Efficiency mode Status)		OP[2]	0 <sub>B</sub> : Device is switchable both normal and dynamic efficiency mode 1 <sub>B</sub> : Device supports efficiency mode only (Static Efficiency Mode)	
Sub-Ch (Sub-Channel Indicator)		OP[3]	0 <sub>B</sub> : Sub-Channel 0 (Primary) 1 <sub>B</sub> : Sub-Channel 1 (Secondary)	1
Density per die		OP[7:4]	0000 <sub>B</sub> : 4Gb 0001 <sub>B</sub> : 6Gb 0010 <sub>B</sub> : 8Gb 0011 <sub>B</sub> : 12Gb 0100 <sub>B</sub> : 16Gb 0101 <sub>B</sub> : 24Gb 0110 <sub>B</sub> : 32Gb 0111 <sub>B</sub> : 48Gb 1000 <sub>B</sub> : 64Gb All Others: Reserved	

NOTE 1 Regarding Primary/Secondary Sub-Channel, refer to clause 7.8.29 Efficiency Mode.

## 6.2 Mode Register Definition (cont'd)

**Table 46 – MR1 Register Information (MA [7:0] = 01<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Eff Latency	Eff CNTL	WLS			RL/WL/nWTP/nRTP/nACU		

**Table 47 – MR1 Definition**

Function	Register Type	Operand	Data	Notes															
RL/WL/nWTP/nRTP/nACU (Read/Write Latencies and Write w/ AP to PRECHARGE delay/nRTP (Read w/ AP to PRECHARGE delay)/Activation Counter Update time)	Read /Write	OP[4:0]	See Table 48	1,2,3,4,5,6															
WLS (Write Latency Set)		OP[5]	0 <sub>B</sub> : Write Latency Set A (default) 1 <sub>B</sub> : Write Latency Set B	1,2															
Eff CNTL (Efficiency mode Control)		OP[6]	0 <sub>B</sub> : Normal (default) 1 <sub>B</sub> : Dynamic efficiency mode	7,9															
Eff Latency (Efficiency Mode Latency)	Read-Only	OP[7]	0 <sub>B</sub> : Normal Latency 1 <sub>B</sub> : Efficiency Mode Latency	8															
NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.																			
NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.																			
NOTE 3 Some Operating features can affect Read Latency: Usage of Set 0/1/2 is below.																			
			<table border="1"> <thead> <tr> <th>Read DBI</th> <th>Efficiency mode</th> <th>Apply</th> </tr> </thead> <tbody> <tr> <td>Disable</td> <td>Disable</td> <td>Set 0</td> </tr> <tr> <td>Enable</td> <td>Disable</td> <td>Set 1</td> </tr> <tr> <td>Disable</td> <td>Enable</td> <td>Set 1</td> </tr> <tr> <td>Enable</td> <td>Enable</td> <td>Set 2</td> </tr> </tbody> </table>	Read DBI	Efficiency mode	Apply	Disable	Disable	Set 0	Enable	Disable	Set 1	Disable	Enable	Set 1	Enable	Enable	Set 2	
Read DBI	Efficiency mode	Apply																	
Disable	Disable	Set 0																	
Enable	Disable	Set 1																	
Disable	Enable	Set 1																	
Enable	Enable	Set 2																	
NOTE 4 The Write Latency applies regardless of the following function setting: (Disable/Enable) Efficiency Mode (Including Static Efficiency mode) Write DBI, Link Protection and DVFSL.																			
NOTE 5 Write Latency Set "A" and Set "B" is determined by MR1 OP[5]. When MR1 OP[5]=0 <sub>B</sub> , then Write Latency Set "A" should be used. When MR1 OP[5]=1 <sub>B</sub> , then Write Latency Set "B" should be used.																			
NOTE 6 The programmed value of nWTP is the number of clock cycles the LPDDR6-SDRAM device uses to determine the starting point of an internal Pre-charge operation after a Write with AP (auto-pre-charge) command executed.																			
NOTE 7 MR1 OP[6] setting is ignored if the LPDDR6 SDRAM only supports Static Efficiency mode (MR0 OP[2]=1 <sub>B</sub> ). Read out value by MRR command is meaningless too.																			
NOTE 8 MR1 OP[7] should be automatically updated by MR1 OP[6] based on package configuration.																			
NOTE 9 MR1 OP[6] should be same between multi-rank system.																			

## 6.2 Mode Register Definition (cont'd)

**Table 48 – RL/WL/nWTP/nRTP/nACU Setting Summary**

Table #	Raed DBI	Efficiency Mode	DVFSL		Write Link Protection	Read Link Protection
Table 49	Disable	Disable	Disable		Disable	Disable
Table 50	Enable	Disable	Disable		Disable	Disable
Table 51	Disable	Enable	Disable		Disable	Disable
Table 52	Enable	Enable	Disable		Disable	Disable
Table 53	Disable	Disable	Enable		Disable	Disable
Table 54	Enable	Disable	Enable		Disable	Disable
Table 55	Disable	Enable	Enable		Disable	Disable
Table 56	Enable	Enable	Enable		Disable	Disable
Table 57	Disable	Disable	Disable		Enable	Disable
Table 58	Enable	Disable	Disable		Enable	Disable
Table 59	Disable	Enable	Disable		Enable	Disable
Table 60	Enable	Enable	Disable		Enable	Disable
Table 61	Disable	Disable	Enable		Enable	Disable
Table 62	Enable	Disable	Enable		Enable	Disable
Table 63	Disable	Enable	Enable		Enable	Disable
Table 64	Enable	Enable	Enable		Enable	Disable
Table 65	-	Disable	Disable		Disable	Enable
Table 66	-	Enable	Disable		Disable	Enable
Table 67	-	Disable	Enable		Disable	Enable
Table 68	-	Enable	Enable		Disable	Enable
Table 69	-	Disable	Disable		Enable	Enable
Table 70	-	Enable	Disable		Enable	Enable
Table 71	-	Disable	Enable		Enable	Enable
Table 72	-	Enable	Enable		Enable	Enable



## 6.2 Mode Register Definition (cont'd)

**Table 51 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 1	Set A	Set B				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	6
00001 <sub>B</sub>	10	6	7	6	7	13	9
00010 <sub>B</sub>	13	8	10	8	7	13	12
00011 <sub>B</sub>	17	8	13	10	7	13	16
00100 <sub>B</sub>	19	10	15	12	7	13	18
00101 <sub>B</sub>	22	12	18	14	8	14	21
00110 <sub>B</sub>	25	12	21	15	8	14	24
00111 <sub>B</sub>	28	14	24	17	8	14	27
01000 <sub>B</sub>	32	16	28	20	8	14	31
01001 <sub>B</sub>	37	18	32	23	8	14	36
01010 <sub>B</sub>	44	20	38	27	11	23	42
01011 <sub>B</sub>	50	22	44	30	11	23	47
01100 <sub>B</sub>	56	24	50	34	13	25	53
01101 <sub>B</sub>	62	26	54	38	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 52 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 2	Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	6	7	13	9
00010 <sub>B</sub>	14	8	10	8	7	13	12
00011 <sub>B</sub>	18	8	13	10	7	13	16
00100 <sub>B</sub>	21	10	15	12	7	13	18
00101 <sub>B</sub>	24	12	18	14	8	14	21
00110 <sub>B</sub>	28	12	21	15	8	14	24
00111 <sub>B</sub>	31	14	24	17	8	14	27
01000 <sub>B</sub>	35	16	28	20	8	14	31
01001 <sub>B</sub>	41	18	32	23	8	14	36
01010 <sub>B</sub>	48	20	38	27	11	23	42
01011 <sub>B</sub>	54	22	44	30	11	23	47
01100 <sub>B</sub>	62	24	50	34	13	25	53
01101 <sub>B</sub>	68	26	54	38	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## 6.2 Mode Register Definition (cont'd)

**Table 53 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 0	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	7	
00001 <sub>B</sub>	10	6	7	6	7	13	11	
00010 <sub>B</sub>	14	8	10	8	7	13	14	
00011 <sub>B</sub>	17	8	13	10	8	14	18	
00100 <sub>B</sub>	20	10	15	12	8	14	21	

**Table 54 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 1	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7	
00001 <sub>B</sub>	11	6	7	6	7	13	11	
00010 <sub>B</sub>	15	8	10	8	7	13	14	
00011 <sub>B</sub>	19	8	13	10	8	14	18	
00100 <sub>B</sub>	22	10	15	12	8	14	21	

**Table 55 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 1	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7	
00001 <sub>B</sub>	11	6	7	7	7	13	11	
00010 <sub>B</sub>	15	8	10	9	7	13	14	
00011 <sub>B</sub>	19	8	13	12	8	14	18	
00100 <sub>B</sub>	22	10	15	13	8	14	21	

**Table 56 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 2	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	9	4	5	6	7	13	7	
00001 <sub>B</sub>	12	6	7	7	7	13	11	
00010 <sub>B</sub>	16	8	10	9	7	13	14	
00011 <sub>B</sub>	21	8	13	12	8	14	18	
00100 <sub>B</sub>	24	10	15	13	8	14	21	



## 6.2 Mode Register Definition (cont'd)

**Table 59 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set A	Set B				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	6
00001 <sub>B</sub>	10	6	7	8	7	13	9
00010 <sub>B</sub>	13	8	10	10	7	13	12
00011 <sub>B</sub>	17	8	13	13	7	13	16
00100 <sub>B</sub>	19	10	15	15	7	13	18
00101 <sub>B</sub>	22	12	18	17	8	14	21
00110 <sub>B</sub>	25	12	21	20	8	14	24
00111 <sub>B</sub>	28	14	24	22	8	14	27
01000 <sub>B</sub>	32	16	28	25	8	14	31
01001 <sub>B</sub>	37	18	32	29	8	14	36
01010 <sub>B</sub>	44	20	38	34	11	23	42
01011 <sub>B</sub>	50	22	44	39	11	23	47
01100 <sub>B</sub>	56	24	50	44	13	25	53
01101 <sub>B</sub>	62	26	54	48	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 60 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	8	7	13	9
00010 <sub>B</sub>	14	8	10	10	7	13	12
00011 <sub>B</sub>	18	8	13	13	7	13	16
00100 <sub>B</sub>	21	10	15	15	7	13	18
00101 <sub>B</sub>	24	12	18	17	8	14	21
00110 <sub>B</sub>	28	12	21	20	8	14	24
00111 <sub>B</sub>	31	14	24	22	8	14	27
01000 <sub>B</sub>	35	16	28	25	8	14	31
01001 <sub>B</sub>	41	18	32	29	8	14	36
01010 <sub>B</sub>	48	20	38	34	11	23	42
01011 <sub>B</sub>	54	22	44	39	11	23	47
01100 <sub>B</sub>	62	24	50	44	13	25	53
01101 <sub>B</sub>	68	26	54	48	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## 6.2 Mode Register Definition (cont'd)

**Table 61 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 0	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	7	
00001 <sub>B</sub>	10	6	7	8	7	13	11	
00010 <sub>B</sub>	14	8	10	10	7	13	14	
00011 <sub>B</sub>	17	8	13	13	8	14	18	
00100 <sub>B</sub>	20	10	15	15	8	14	21	

**Table 62 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 1	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7	
00001 <sub>B</sub>	11	6	7	8	7	13	11	
00010 <sub>B</sub>	15	8	10	10	7	13	14	
00011 <sub>B</sub>	19	8	13	13	8	14	18	
00100 <sub>B</sub>	22	10	15	15	8	14	21	

**Table 63 – RL/WL/nWTP/nRTP/nACU for Read DBI is Disabled, Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 1	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7	
00001 <sub>B</sub>	11	6	7	9	7	13	11	
00010 <sub>B</sub>	15	8	10	12	7	13	14	
00011 <sub>B</sub>	19	8	13	15	8	14	18	
00100 <sub>B</sub>	22	10	15	17	8	14	21	

**Table 64 – RL/WL/nWTP/nRTP/nACU for Read DBI is Enabled, Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Disabled**

MR1 OP[4:0]	Read Latency [nCK]		Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
	Set 2	Set A	Set A	Set B				
00000 <sub>B</sub> (default)	9	4	5	6	7	13	7	
00001 <sub>B</sub>	12	6	7	9	7	13	11	
00010 <sub>B</sub>	16	8	10	12	7	13	14	
00011 <sub>B</sub>	21	8	13	15	8	14	18	
00100 <sub>B</sub>	24	10	15	17	8	14	21	

## 6.2 Mode Register Definition (cont'd)

**Table 65 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Disabled, DVFSL is Disabled, Write Link Protection is Disabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 0	Set A				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	6	7	13	9
00010 <sub>B</sub>	14	8	10	7	7	13	12
00011 <sub>B</sub>	17	8	13	9	7	13	16
00100 <sub>B</sub>	20	10	15	10	7	13	18
00101 <sub>B</sub>	23	12	18	12	8	14	21
00110 <sub>B</sub>	26	12	21	13	8	14	24
00111 <sub>B</sub>	29	14	24	15	8	14	27
01000 <sub>B</sub>	33	16	28	17	8	14	31
01001 <sub>B</sub>	39	18	32	20	8	14	36
01010 <sub>B</sub>	46	20	38	23	11	23	42
01011 <sub>B</sub>	52	22	44	26	11	23	47
01100 <sub>B</sub>	58	24	50	29	13	25	53
01101 <sub>B</sub>	64	26	54	32	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 66 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Disabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 1	Set A				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	6	7	13	9
00010 <sub>B</sub>	15	8	10	8	7	13	12
00011 <sub>B</sub>	19	8	13	10	7	13	16
00100 <sub>B</sub>	22	10	15	12	7	13	18
00101 <sub>B</sub>	25	12	18	14	8	14	21
00110 <sub>B</sub>	28	12	21	15	8	14	24
00111 <sub>B</sub>	32	14	24	17	8	14	27
01000 <sub>B</sub>	36	16	28	20	8	14	31
01001 <sub>B</sub>	42	18	32	23	8	14	36
01010 <sub>B</sub>	50	20	38	27	11	23	42
01011 <sub>B</sub>	56	22	44	30	11	23	47
01100 <sub>B</sub>	64	24	50	34	13	25	53
01101 <sub>B</sub>	70	26	54	38	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## 6.2 Mode Register Definition (cont'd)

**Table 67 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7
00001 <sub>B</sub>	12	6	7	6	7	13	11
00010 <sub>B</sub>	15	8	10	8	7	13	14
00011 <sub>B</sub>	19	8	13	10	8	14	18
00100 <sub>B</sub>	22	10	15	12	8	14	21

**Table 68 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Disabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 1	Set A				
00000 <sub>B</sub> (default)	9	4	5	6	7	13	7
00001 <sub>B</sub>	13	6	7	7	7	13	11
00010 <sub>B</sub>	17	8	10	9	7	13	14
00011 <sub>B</sub>	21	8	13	12	8	14	18
00100 <sub>B</sub>	24	10	15	13	8	14	21

**Table 69 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Disabled, DVFSL is Disabled, Write Link Protection is Enabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 0	Set A				
00000 <sub>B</sub> (default)	7	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	7	7	13	9
00010 <sub>B</sub>	14	8	10	9	7	13	12
00011 <sub>B</sub>	17	8	13	12	7	13	16
00100 <sub>B</sub>	20	10	15	13	7	13	18
00101 <sub>B</sub>	23	12	18	15	8	14	21
00110 <sub>B</sub>	26	12	21	18	8	14	24
00111 <sub>B</sub>	29	14	24	20	8	14	27
01000 <sub>B</sub>	33	16	28	23	8	14	31
01001 <sub>B</sub>	39	18	32	26	8	14	36
01010 <sub>B</sub>	46	20	38	31	11	23	42
01011 <sub>B</sub>	52	22	44	35	11	23	47
01100 <sub>B</sub>	58	24	50	39	13	25	53
01101 <sub>B</sub>	64	26	54	43	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

## 6.2 Mode Register Definition (cont'd)

**Table 70 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Enabled, DVFSL is Disabled, Write Link Protection is Enabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set A	Set B				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	6
00001 <sub>B</sub>	11	6	7	8	7	13	9
00010 <sub>B</sub>	15	8	10	10	7	13	12
00011 <sub>B</sub>	19	8	13	13	7	13	16
00100 <sub>B</sub>	22	10	15	15	7	13	18
00101 <sub>B</sub>	25	12	18	17	8	14	21
00110 <sub>B</sub>	28	12	21	20	8	14	24
00111 <sub>B</sub>	32	14	24	22	8	14	27
01000 <sub>B</sub>	36	16	28	25	8	14	31
01001 <sub>B</sub>	42	18	32	29	8	14	36
01010 <sub>B</sub>	50	20	38	34	11	23	42
01011 <sub>B</sub>	56	22	44	39	11	23	47
01100 <sub>B</sub>	64	24	50	44	13	25	53
01101 <sub>B</sub>	70	26	54	48	14	26	59
01110 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 71 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Disabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 0	Set A				
00000 <sub>B</sub> (default)	8	4	5	6	7	13	7
00001 <sub>B</sub>	12	6	7	8	7	13	11
00010 <sub>B</sub>	15	8	10	10	7	13	14
00011 <sub>B</sub>	19	8	13	13	8	14	18
00100 <sub>B</sub>	22	10	15	15	8	14	21

**Table 72 – RL/WL/nWTP/nRTP/nACU for Efficiency Mode is Enabled, DVFSL is Enabled, Write Link Protection is Enabled, Read Link Protection is Enabled**

MR1 OP[4:0]	Read Latency [nCK]	Write Latency [nCK]		nWTP [nCK]	nRTP (BL24) [nCK]	nRTP (BL48) [nCK]	nACU [nCK]
		Set 1	Set A				
00000 <sub>B</sub> (default)	9	4	5	6	7	13	7
00001 <sub>B</sub>	13	6	7	9	7	13	11
00010 <sub>B</sub>	17	8	10	12	7	13	14
00011 <sub>B</sub>	21	8	13	15	8	14	18
00100 <sub>B</sub>	24	10	15	17	8	14	21

## 6.2 Mode Register Definition (cont'd)

**Table 73 – MR2 Register Information (MA [7:0] = 02<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	RFU	sPPR Support	System Meta Mode Support	CA Parity Support

**Table 74 – MR2 Definition**

Function	Register Type	Operand	Data	Notes
CA Parity Support (CA parity check support)	Read-Only	OP[0]	0 <sub>B</sub> : CA parity check supported 1 <sub>B</sub> : CA parity check not supported	
System Meta Mode Support		OP[1]	0 <sub>B</sub> : System Meta Mode not supported 1 <sub>B</sub> : System Meta Mode supported	
sPPR Support (Soft Post Package Repair support)		OP[2]	0 <sub>B</sub> : sPPR supported 1 <sub>B</sub> : sPPR not supported	

**Table 75 – MR3 Register Information (MA [7:0] = 03<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
	PDDS		RFU	RFU	RFU	EDBI-WR	DBI-RD

**Table 76 — MR3 Definition**

Function	Register Type	Operand	Data	Notes
DBI-RD (DBI-Read Select)	Read-Only	OP[0]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Read DBI-DC Enabled	1,2
EDBI-WR (Enhanced DBI-Write select)		OP[1]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Enhanced Write DBI-DC Enabled	1,2
PDDS (Pull-Down Drive Strength)	Read/Write	OP[7:5]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.				
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.			

## 6.2 Mode Register Definition (cont'd)

**Table 77 — MR4 Register Information (MA[6:0] = 04<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	ZQ Initiator	ZQUF			RM		

**Table 78 – MR4 Definition**

Function	Register Type	Operand	Data	Notes		
Refresh Multiplier (RM)	Read-only	OP[4:0]	00000 <sub>B</sub> : SDRAM Low temperature operating limit exceeded 00001 <sub>B</sub> : 8x 00010 <sub>B</sub> : 6x 00011 <sub>B</sub> : 4x 00100 <sub>B</sub> : 3.3x 00101 <sub>B</sub> : 2.5x 00110 <sub>B</sub> : 2.0x 00111 <sub>B</sub> : 1.7x 01000 <sub>B</sub> : 1.3x 01001 <sub>B</sub> : 1x 01010 <sub>B</sub> : 0.7x 01011 <sub>B</sub> : 0.5x 01100 <sub>B</sub> : 0.25x, no de-rating 01101 <sub>B</sub> : 0.25x, with de-rating 01110 <sub>B</sub> : 0.125x, no de-rating 01111 <sub>B</sub> : 0.125x, with de-rating 11111 <sub>B</sub> : SDRAM High temperature operating limit exceeded All others are reserved.	1,2,3,4,5,6,7		
			OP[5]	0 <sub>B</sub> : No change in calibration code since previous ZQ Latch command 1 <sub>B</sub> : Calibration code has changed since previous ZQ Latch command		
			OP[6]	0 <sub>B</sub> : Not an Initiator die 1 <sub>B</sub> : Initiator die for ZQ Calibration purposes		
			OP[7]	0 <sub>B</sub> : No change in OP[4:0] since last MR4 read 1 <sub>B</sub> : Change in OP[4:0] since last MR4 read (default)		
NOTE 1 The refresh rate for each MR4-OP[4:0] setting applies to tREFI, tREFIdb, and tREFW. OP[4:0]=01001 <sub>B</sub> corresponds to a device temperature of 85 °C. Other values require either a longer (1.3x, 8x) refresh interval at lower temperatures, or a shorter (0.7x, 0.125x) refresh interval at higher temperatures. If OP[4:0] is from 01010 <sub>B</sub> to 11111 <sub>B</sub> , the device temperature is greater than 85 °C.						
NOTE 2 At higher temperatures (>85°C), AC timing derating may be required. If derating is required, the LPDDR6-SDRAM will set OP[4:0]=01101 <sub>B</sub> or 01111 <sub>B</sub> . See derating timing requirements in Table 424.						
NOTE 3 DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.						
NOTE 4 The device may not operate properly when OP[4:0]=00000 <sub>B</sub> or 11111 <sub>B</sub> .						
NOTE 5 When OP[7] = 1 <sub>B</sub> , the refresh rate reported in OP[4:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0 <sub>B</sub> '.						
NOTE 6 OP[4:0] bits indicate the latest Refresh Rate whenever OP[7] = 1 <sub>B</sub> .						
NOTE 7 See Temperature Sensor (7.8.12) for information on the recommended frequency of reading MR4.						
NOTE 8 After Power up initialization and reset sequence have been completed, ZQUF MR4 OP[5] indicates 0 <sub>B</sub> .						
NOTE 9 LPDDR6 packages with more than one ZQ pin may include more than one ZQ Initiator die.						

## 6.2 Mode Register Definition (cont'd)

**Table 79 – MR5 Register Information (MA[7:0] = 05<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR6 Manufacturer ID							

**Table 80 – MR5 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Manufacturer ID	Read-only	OP[7:0]	See JEPxxx, LPDDR6 Manufacturer ID Codes	

**Table 81 — MR6 Register Information (MA[7:0] = 06<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

**Table 82 – MR6 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Revision ID-1	Read-only	OP[7:0]	00000000 <sub>B</sub> : A-version 00000001 <sub>B</sub> : B-version	1
NOTE 1 MR6 is vendor specific.				

**Table 83 – MR7 Register Information (MA[7:0] = 07<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

**Table 84 – MR7 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Revision ID-2	Read-only	OP[7:0]	00000000 <sub>B</sub> : A-version 00000001 <sub>B</sub> : B-version	1
NOTE 1 MR7 is vendor specific.				

## 6.2 Mode Register Definition (cont'd)

**Table 85 – MR8 Register Information (MA[7:0] = 08<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-3							

**Table 86 – MR8 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Revision ID-3	Read-only	OP[7:0]	00000000 <sub>B</sub> : A-version 00000001 <sub>B</sub> : B-version	1
NOTE 1 MR8 is vendor specific.				

**Table 87 – MR9 Register Information (MA[7:0] = 09<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

**Table 88 – MR9 Definition**

Function	Register Type	Operand	Data	Notes
Vendor Specific Test Register	Write only	OP[7:0]	Vendor Specific	1
NOTE 1 Only 00H should be written to this register				

## 6.2 Mode Register Definition (cont'd)

**Table 89 – MR10 Register Information (MA [7:0] = 0A<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RDQS PST Length		RDQS PST Mode		RDQS PRE		RDQS RT	RDQS PS

**Table 90 – MR10 Definition**

Function	Register Type	Operand	Data	Notes			
RDQS PS (RDQS Pre-Shift)	Write-Only	OP[0]	0 <sub>B</sub> : 0*tWCK (default) 1 <sub>B</sub> : 2*tWCK	1,2,3,4,5			
RDQS RT (RDQS to WCK Ratio)		OP[1]	0 <sub>B</sub> : WCK:RDQS ratio = 1:1 ratio (default) 1 <sub>B</sub> : WCK:RDQS ratio = 2:1 ratio	1,2,3			
RDQS PRE (RD Pre-amble Length)		OP[4:2]	When MR10 OP[1]=0 <sub>B</sub> 000 <sub>B</sub> : 4*tWCK static, 0*tWCK toggle (default) 001 <sub>B</sub> : 2*tWCK static, 2*tWCK toggle 010 <sub>B</sub> : 4*tWCK static, 4*tWCK toggle 011 <sub>B</sub> : 2*tWCK static, 6*tWCK toggle All others are RFU When MR10 OP[1]=1 <sub>B</sub> 000 <sub>B</sub> : 2*Unit static, 0*Unit toggle (default) 001 <sub>B</sub> : 1*Unit static, 1*Unit toggle 010 <sub>B</sub> : 2*Unit static, 2*Unit toggle 011 <sub>B</sub> : 1*Unit static, 3*Unit toggle All others are RFU	1,2,3,6,7			
RDQS PST Mode (RDQS Post-amble Mode)		OP[5]	0 <sub>B</sub> : Toggle Mode (default) 1 <sub>B</sub> : Static Mode	1,2,3			
RDQS PST Length (RDQD Post-amble Length)		OP[7:6]	When MR10 OP[1]=0 <sub>B</sub> 00 <sub>B</sub> : 0.5*tWCK (default) 01 <sub>B</sub> : 2.5*tWCK 10 <sub>B</sub> : 4.5*tWCK 11 <sub>B</sub> : Reserved When MR10 OP[1]=1 <sub>B</sub> 00 <sub>B</sub> : 0.5*Unit toggle (default) 01 <sub>B</sub> : 2.5*Unit toggle 10 <sub>B</sub> : 4.5*Unit toggle 11 <sub>B</sub> : Reserved	1,2,3			
NOTE 1		There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.					
NOTE 2		There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.					
NOTE 3		Refer to RDQS Mode (7.5.1.3) for detail.					
NOTE 4	MR10 OP[0]=0 <sub>B</sub> supported over all frequency ranges.						
NOTE 5	MR10 OP[0]=1 <sub>B</sub> setting is allowed for greater than 8533 Mbps operation.						
NOTE 6	MR10 OP[4:2] = 000 <sub>B</sub> /001 <sub>B</sub> supported over all frequency ranges.						
NOTE 7	MR10 OP[4:2] = 010 <sub>B</sub> /011 <sub>B</sub> setting is allowed for greater than 8533 Mbps operation.						

## 6.2 Mode Register Definition (cont'd)

**Table 91 – MR11 Register Information (MA [6:0] = 0B<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQ OSC FM	WCK FM	DVFSQ	DVFSL	DVFSB	DVFSH	RFU	RFU

**Table 92 – MR11 Definition**

Function	Register Type	Operand	Data	Notes
DVFSH (VDD2C Dynamic Voltage and Frequency for High Data Rate)	Write-only	OP[2]	0 <sub>B</sub> : VDD2C = 1.00 V (default) 1 <sub>B</sub> : VDD2C = 1.025 V	1,2,3
DVFSB (VDD2D Dynamic Voltage and Frequency for High Data Rate)		OP[3]	0 <sub>B</sub> : VDD2D = 0.875 V (default) 1 <sub>B</sub> : VDD2D = 0.90 V	1,2,4
DVFSL (VDD2D Dynamic Voltage and Frequency for Low Data Rate)		OP[4]	0 <sub>B</sub> : VDD2D = 0.875 V (default) 1 <sub>B</sub> : VDD2D = 0.85 V	1,2,5
DVFSQ (VDDQ Dynamic Voltage and Frequency Scaling VDDQ)		OP[5]	0 <sub>B</sub> : VDDQ = 0.5 V (default) 1 <sub>B</sub> : VDDQ = 0.3 V	1,2,6
WCK FM (WCK Frequency Mode)		OP[6]	0 <sub>B</sub> : Low frequency mode (default) 1 <sub>B</sub> : High frequency mode	1,2,7
WCK2DQ OSC FM		OP[7]	0 <sub>B</sub> : WCK2DQ oscillator for WCK low frequency mode (default) 1 <sub>B</sub> : WCK2DQ oscillator for WCK high frequency mode	1,2,8
NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.				
NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.				
NOTE 3 MR11 OP[2] is required to be set to 1 <sub>B</sub> at high data rates as indicated by MR21 OP[1:0] (DVFSH Requirement) when MR21 OP[1:0] = 01 <sub>B</sub> or 10 <sub>B</sub> . Otherwise, it should be set to 0 <sub>B</sub> .				
NOTE 4 MR11 OP[3] is required to be set to 1 <sub>B</sub> at high data rates as indicated by MR21 OP[3:2] (DVFSB Requirement) when MR21 OP[3:2] = 01 <sub>B</sub> or 10 <sub>B</sub> . Otherwise, it should be set to 0 <sub>B</sub> .				
NOTE 5 MR11 OP[4] is allowed to be set to 1 <sub>B</sub> at low data rates as indicated by MR21 OP[5:4] (DVFSL Support) when MR21 OP[5:4] = 01 <sub>B</sub> or 10 <sub>B</sub> .				
NOTE 6 When MR11 OP[5] is set to 1 <sub>B</sub> , SDRAM will turn off all ODT – DQ, CS, CA, CK, WCK, DQ NT-ODT, and DQ Write NT-ODT – regardless of the relevant ODT and NT-ODT MR settings.				
NOTE 7 tWCK2DQ AC parameters can be changed by MR11 OP[6]. Refer to tWCK2DQ AC parameter table. WCK single-ended mode (MR22 OP[3:2]) can be allowed during Low frequency mode only.				
NOTE 8 When operating in WCK low frequency mode (MR11 OP[6]=0 <sub>B</sub> ), WCK2DQ oscillator for WCK high frequency mode (MR11 OP[7]=1 <sub>B</sub> ) can be enabled, and vice versa.				

## 6.2 Mode Register Definition (cont'd)

**Table 93 – MR12 Register Information (MA[7:0] = 0C<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	V <sub>REF</sub> (CA)						

**Table 94 – MR12 Definition**

Function	Register Type	Operand	Data	Notes
V <sub>REF</sub> (CA) (V <sub>REF</sub> (CA) Setting)	Read/ Write	OP[6:0]	0000000 <sub>B</sub> : -- Thru -- 1111111 <sub>B</sub> : See Table 95	1,2,3,4, 5
NOTE 1 This register controls the VREF(CA) levels for Frequency-Set-Point[2:0].				
NOTE 2 A read (MRR) to this register places the contents of OP[6:0] on DQ[6:0]. DQ[11:7] will read 00000B. See 7.8.1 for more information on MRR Operation.				
NOTE 3 A write to MR12 OP[6:0] sets the internal VREF(CA) level for FSP[0] when MR16 OP[1:0]=00B, sets FSP[1] when MR16 OP[1:0]=01B or sets FSP[2] when MR16 OP[1:0]=10B. The time required for VREF(CA) to reach the set level depends on the step size from the current level to the new level. See TBD for more information on VREF(CA) training.				
NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.				
NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.				

## 6.2 Mode Register Definition (cont'd)

**Table 95 – MR12 VREF(CA) Settings**

## 6.2 Mode Register Definition (cont'd)

**Table 96 – MR13 Register Information (MA[7:0] = 0D<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP		FSP-WR		VRCG	VRO		Thermal Offset

**Table 97 – MR13 Definition**

Function	Register Type	Operand	Data	Notes
Thermal Offset	Read/Write	OP[1:0]	00 <sub>B</sub> : No offset, 0~5 °C gradient (default) 01 <sub>B</sub> : 5°C offset, 5~10 °C gradient 10 <sub>B</sub> : 10°C offset, 10~15 °C gradient 11 <sub>B</sub> : Reserved	5
VRO (VREF Output)		OP[2]	0 <sub>B</sub> : Normal operation (default) 1 <sub>B</sub> : Output the VREF(CS), VREF(CA) and VREF(DQ) values on DQ bits	1
VRCG (VREF Current Generator)	Read/Write	OP[3]	0 <sub>B</sub> : Normal operation (default) 1 <sub>B</sub> : VREF Fast Response (high current) Mode	4
FSP-WR (Frequency Set Point Write Enable)	Read/Write	OP[5:4]	00 <sub>B</sub> : Frequency-Set-Point [0] (default) 01 <sub>B</sub> : Frequency-Set-Point [1] 10 <sub>B</sub> : Frequency-Set-Point [2] 11 <sub>B</sub> : Reserved	2
FSP-OP (Frequency Set Point Operation Mode)		OP[7:6]	00 <sub>B</sub> : Frequency-Set-Point [0] (default) 01 <sub>B</sub> : Frequency-Set-Point [1] 10 <sub>B</sub> : Frequency-Set-Point [2] 11 <sub>B</sub> : Reserved	3
NOTE 1	When set, the LPDDR6-SDRAM will output the VREF(CS), VREF(CA) and VREF(DQ) voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7:6], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels and its accuracy is guaranteed at or less than 25 °C. The DQ pins used for VREF output are vendor specific.			
NOTE 2	FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V <sub>REF</sub> (CA) Setting, V <sub>REF</sub> (DQ) Setting. For more information, refer to 7.8.3.			
NOTE 3	FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V <sub>REF</sub> (CA) Setting, V <sub>REF</sub> (DQ) Setting. For more information, refer to 7.8.3.			
NOTE 4	When OP[3]=1 <sub>B</sub> , the VREF circuit uses a high-current mode to improve VREF settling time.			
NOTE 5	Thermal offset (MR13 OP[1:0]) should be set same value between SC0 and SC1.			

## 6.2 Mode Register Definition (cont'd)

**Table 98 — MR14 Register Information (MA[7:0] = 0E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VREF(DQ[11:0])						

**Table 99 — MR14 Definition**

Function	Register Type	Operand	Data	Notes
V <sub>REF</sub> (DQ[11:0]) (V <sub>REF</sub> (DQ[11:0]) Setting)	Read/ Write	OP[6:0]	0000000 <sub>B</sub> : -- Thru -- 1111111 <sub>B</sub> : See Table 100	1,2,3,4,5
NOTE 1 This register controls the VREF(DQ[11:0]) levels for Frequency-Set-Point[2:0].				
NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.				
NOTE 3 A write to OP[6:0] sets the internal VREF(DQ[11:0]) level for FSP[0] when MR16 OP[1:0]=00 <sub>B</sub> , sets FSP[1] when MR16 OP[1:0]=01 <sub>B</sub> or sets FSP[2] when MR16 OP[1:0]=10 <sub>B</sub> . The time required for VREF(DQ[11:0]) to reach the set level depends on the step size from the current level to the new level. See the section on VREF(DQ[11:0]) training for more information.				
NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.				
NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				

## 6.2 Mode Register Definition (cont'd)

**Table 100 — MR14 VREF(DQ[11:0]) Settings**

Function	Operand	V <sub>REF</sub> Values (% of VDDQ)							Notes
VREF Settings for MR14	OP [6:0]	0000000 <sub>B</sub> :	10.0 <sup>*5</sup>	0100000 <sub>B</sub> :	26.0	1000000 <sub>B</sub> :	42.0	1100000 <sub>B</sub> :	58.0
		0000001 <sub>B</sub> :	10.5 <sup>*5</sup>	0100001 <sub>B</sub> :	26.5	1000001 <sub>B</sub> :	42.5	1100001 <sub>B</sub> :	58.5
		0000010 <sub>B</sub> :	11.0 <sup>*5</sup>	0100010 <sub>B</sub> :	27.0	1000010 <sub>B</sub> :	43.0	1100010 <sub>B</sub> :	59.0
		0000011 <sub>B</sub> :	11.5 <sup>*5</sup>	0100011 <sub>B</sub> :	27.5	1000011 <sub>B</sub> :	43.5	1100011 <sub>B</sub> :	59.5
		0000100 <sub>B</sub> :	12.0 <sup>*5</sup>	0100100 <sub>B</sub> :	28.0	1000100 <sub>B</sub> :	44.0	1100100 <sub>B</sub> :	60.0
		0000101 <sub>B</sub> :	12.5 <sup>*5</sup>	0100101 <sub>B</sub> :	28.5	1000101 <sub>B</sub> :	44.5	1100101 <sub>B</sub> :	60.5
		0000110 <sub>B</sub> :	13.0 <sup>*5</sup>	0100110 <sub>B</sub> :	29.0	1000110 <sub>B</sub> :	45.0	1100110 <sub>B</sub> :	61.0
		0000111 <sub>B</sub> :	13.5 <sup>*5</sup>	0100111 <sub>B</sub> :	29.5	1000111 <sub>B</sub> :	45.5	1100111 <sub>B</sub> :	61.5
		0001000 <sub>B</sub> :	14.0 <sup>*5</sup>	0101000 <sub>B</sub> :	30.0	1001000 <sub>B</sub> :	46.0	1101000 <sub>B</sub> :	62.0
		0001001 <sub>B</sub> :	14.5 <sup>*5</sup>	0101001 <sub>B</sub> :	30.5	1001001 <sub>B</sub> :	46.5	1101001 <sub>B</sub> :	62.5
		0001010 <sub>B</sub> :	15.0	0101010 <sub>B</sub> :	31.0	1001010 <sub>B</sub> :	47.0	1101010 <sub>B</sub> :	63.0
		0001011 <sub>B</sub> :	15.5	0101011 <sub>B</sub> :	31.5	1001011 <sub>B</sub> :	47.5	1101011 <sub>B</sub> :	63.5
		0001100 <sub>B</sub> :	16.0	0101100 <sub>B</sub> :	32.0	1001100 <sub>B</sub> :	48.0	1101100 <sub>B</sub> :	64.0
		0001101 <sub>B</sub> :	16.5	0101101 <sub>B</sub> :	32.5	1001101 <sub>B</sub> :	48.5	1101101 <sub>B</sub> :	64.5
		0001110 <sub>B</sub> :	17.0	0101110 <sub>B</sub> :	33.0	1001110 <sub>B</sub> :	49.0	1101110 <sub>B</sub> :	65.0
		0001111 <sub>B</sub> :	17.5	0101111 <sub>B</sub> :	33.5	1001111 <sub>B</sub> :	49.5	1101111 <sub>B</sub> :	65.5
		0010000 <sub>B</sub> :	18.0	0110000 <sub>B</sub> :	34.0	1010000 <sub>B</sub> : (default)	50.0	1110000 <sub>B</sub> :	66.0
		0010001 <sub>B</sub> :	18.5	0110001 <sub>B</sub> :	34.5	1010001 <sub>B</sub> :	50.5	1110001 <sub>B</sub> :	66.5
		0010010 <sub>B</sub> :	19.0	0110010 <sub>B</sub> :	35.0	1010010 <sub>B</sub> :	51.0	1110010 <sub>B</sub> :	67.0
		0010011 <sub>B</sub> :	19.5	0110011 <sub>B</sub> :	35.5	1010011 <sub>B</sub> :	51.5	1110011 <sub>B</sub> :	67.5
		0010100 <sub>B</sub> :	20.0	0110100 <sub>B</sub> :	36.0	1010100 <sub>B</sub> :	52.0	1110100 <sub>B</sub> :	68.0
		0010101 <sub>B</sub> :	20.5	0110101 <sub>B</sub> :	36.5	1010101 <sub>B</sub> :	52.5	1110101 <sub>B</sub> :	68.5
		0010110 <sub>B</sub> :	21.0	0110110 <sub>B</sub> :	37.0	1010110 <sub>B</sub> :	53.0	1110110 <sub>B</sub> :	69.0
		0010111 <sub>B</sub> :	21.5	0110111 <sub>B</sub> :	37.5	1010111 <sub>B</sub> :	53.5	1110111 <sub>B</sub> :	69.5
		0011000 <sub>B</sub> :	22.0	0111000 <sub>B</sub> :	38.0	1011000 <sub>B</sub> :	54.0	1111000 <sub>B</sub> :	70.0
		0011001 <sub>B</sub> :	22.5	0111001 <sub>B</sub> :	38.5	1011001 <sub>B</sub> :	54.5	1111001 <sub>B</sub> :	70.5
		0011010 <sub>B</sub> :	23.0	0111010 <sub>B</sub> :	39.0	1011010 <sub>B</sub> :	55.0	1111010 <sub>B</sub> :	71.0
		0011011 <sub>B</sub> :	23.5	0111011 <sub>B</sub> :	39.5	1011011 <sub>B</sub> :	55.5	1111011 <sub>B</sub> :	71.5
		0011100 <sub>B</sub> :	24.0	0111100 <sub>B</sub> :	40.0	1011100 <sub>B</sub> :	56.0	1111100 <sub>B</sub> :	72.0
		0011101 <sub>B</sub> :	24.5	0111101 <sub>B</sub> :	40.5	1011101 <sub>B</sub> :	56.5	1111101 <sub>B</sub> :	72.5
		0011110 <sub>B</sub> :	25.0	0111110 <sub>B</sub> :	41.0	1011110 <sub>B</sub> :	57.0	1111110 <sub>B</sub> :	73.0
		0011111 <sub>B</sub> :	25.5	0111111 <sub>B</sub> :	41.5	1011111 <sub>B</sub> :	57.5	1111111 <sub>B</sub> :	73.5

**NOTE 1** These values may be used for MR14 OP[6:0] to set the VREF(DQ[11:0]) levels in the LPDDR6-SDRAM.

**NOTE 2** The MR14 registers represents either FSP[0], FSP[1] or FSP[2]. Three frequency-set-points each for DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

**NOTE 3** Absolute DQ[11:0] Vref low level (%code \* VDDQ) must be higher than or equal to TBD mV for normal operation. Vref error is not included in this calculation.

**NOTE 4** Absolute DQ[11:0] Vref high level (%code \* VDDQ) must be lower than or equal to TBD mV when WCK is less than or equal to TBD MHz. Absolute DQ[11:0] Vref high level (%code \* VDDQ) must be lower than or equal to TBD mV when WCK is higher than TBD MHz. VREF error is not included in this calculation.

## 6.2 Mode Register Definition (cont'd)

**Table 101 – MR15 Register Information (MA[7:0] = 0F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
OCC	VREF(CS)						

**Table 102 – MR15 Definition**

Function	Register Type	Operand	Data	Notes
VREF(CS) (V <sub>REF</sub> (CS) Setting)	Read/ Write	OP[6:0]	0000000 <sub>B</sub> : -- Thru -- 1111111 <sub>B</sub> : See Table 103	1,2,3,4,5
OCC (Offset Calibration Control)	Write	OP[7]	0 <sub>B</sub> : Offset calibration disable(default) 1 <sub>B</sub> : Offset calibration enable	

NOTE 1 This register controls the VREFCS levels for Frequency-Set-Point[2:0].

NOTE 2 A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.

NOTE 3 A write to OP[6:0] sets the internal VREFCS level for FSP[0] when MR13 OP[5:4]=00B, sets FSP[1] when MR13 OP[5:4]=01B or sets FSP[2] when MR13 OP[5:4]=10B. The time required for VREFCS to reach the set level depends on the step size from the current level to the new level. See the section on VREFCS training for more information.

NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 5 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

## 6.2 Mode Register Definition (cont'd)

**Table 103 – MR15 VREF CS Settings**

## 6.2 Mode Register Definition (cont'd)

**Table 104 – MR16 Register Information (MA[6:0] = 10<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CBT/CST Select	CBT/CST		RDC DQ Mode	WCK2CK Leveling		RFU

**Table 105 – MR16 Definition**

Function	Register Type	Operand	Data	Notes
WCK2CK Leveling	Write-only	OP[2]	0 <sub>B</sub> : WCK2CK Leveling Mode disabled (default) 1 <sub>B</sub> : WCK2CK Leveling Mode enabled	
RDC DQ mode		OP[3]	In Read DQ Calibration, DQ output pattern is controlled by MR32/33/34 (pattern) and MR30/31 (per-bit control), where MR30/31 function is defined as: 0 <sub>B</sub> : MR30/31 decides whether to “invert” or not (default) 1 <sub>B</sub> : MR30/31 decides whether to “fix to low” or not	
CBT/CST (Command Bus Training/ CS Training Enable)		OP[5:4]	00 <sub>B</sub> : Normal operation (default) 01 <sub>B</sub> : CBT/CST enabled for FSP0 10 <sub>B</sub> : CBT/CST enabled for FSP1 11 <sub>B</sub> : CBT/CST enabled for FSP2	1
CBT/CST Select (Command Bus Training/ CS Training Select)		OP[6]	0 <sub>B</sub> : Command Bus Training Mode (default) 1 <sub>B</sub> : CS Training Mode	
NOTE 1 A write to set OP[5:4]= 01 <sub>B</sub> , 10 <sub>B</sub> or 11 <sub>B</sub> causes the SDRAM to enter the Command Bus Training mode or the CS Training mode depending on OP[6] configuration (CBT entered when OP[6]=0 <sub>B</sub> and CST when OP[6]=1 <sub>B</sub> ).				

## 6.2 Mode Register Definition (cont'd)

**Table 106 – MR17 Register Information (MA[6:0] = 11<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU		CS ODT			SoC ODT	

**Table 107 – MR17 Definition**

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Read/ Write	OP[2:0]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	1,3,4,5
CS ODT (CS termination)		OP[5:3]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	2,3,4,6

NOTE 1 All values are "typical".  
 NOTE 2 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.  
 NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.  
 NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.  
 NOTE 5 DRAM Pull-up driver strength is controlled by OP[2:0] SOC ODT setting when DQ termination is disabled.  
 NOTE 6 To ensure proper operation in a multi-rank configuration, when CS is enabled, the rank providing ODT will continue to terminate in all DRAM states except Idle Power-down, Active Power-down, and Self-refresh Power-down. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.

## 6.2 Mode Register Definition (cont'd)

**Table 108 – MR18 Register Information (MA[6:0] = 12<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU		CA ODT			CK ODT	

**Table 109 – MR18 Definition**

Function	Register Type	Operand	Data	Notes
CK ODT (CK Receiver On-Die-Termination)	Read/ Write	OP[2:0]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	1,2,3,4
CA ODT (CA Bus Receiver On-Die-Termination)			000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	
NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary. NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address. NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation. NOTE 4 To ensure proper operation in a multi-rank configuration, when CA and CK ODT are enabled, the rank providing ODT will continue to terminate the command bus in all DRAM states including Self-refresh Power-down, Active Power-down and Idle Power-down.				

## 6.2 Mode Register Definition (cont'd)

**Table 110 – MR19 Register Information (MA[6:0] = 13<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU			WCK ODT			DQ ODT	

**Table 111 – MR19 Definition**

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Read/ Write	OP[2:0]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	1,2,3
			000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	
WCK ODT		OP[5:3]		1,2,3,4

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.

NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.

NOTE 4 The SDRAM will continue to terminate WCK in all states, if termination is enabled by MR19 OP[5:3].

## 6.2 Mode Register Definition (cont'd)

**Table 112 – MR20 Register Information (MA[6:0] = 14<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU		DQ WR NT-ODT			DQ NT-ODT	

**Table 113 – MR20 Definition**

Function	Register Type	Operand	Data	Notes
DQ NT-ODT (DQ Bus Receiver On-die Termination at Non-target Die)	Read/ Write	OP[2:0]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	1,2,3
DQ WR NT-ODT (DQ Bus Receiver On-die Termination at Non-target die for Write)		OP[5:3]	000 <sub>B</sub> : Disabled (default) 001 <sub>B</sub> : RZQ/1 010 <sub>B</sub> : RZQ/2 011 <sub>B</sub> : RZQ/3 100 <sub>B</sub> : RZQ/4 101 <sub>B</sub> : RZQ/5 110 <sub>B</sub> : RZQ/6 111 <sub>B</sub> : RFU	1,2,3
NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary. NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address. NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1 and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.				

## 6.2 Mode Register Definition (cont'd)

**Table 114 – MR21 Register Information (MA[7:0] = 15<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	DVFSL (VDD2D Step-down range) support	DVFSB (VDD2D Step-up range) requirement	DVFSH (VDD2C Step-up range) requirement				

**Table 115 – MR21 Definition**

Function	Register Type	Operand	Data	Notes
DVFSH (VDD2C Dynamic Voltage and Frequency for High data rate) requirement	Read-only	OP[1:0]	00 <sub>B</sub> : VDD2C Step-up range is not required 01 <sub>B</sub> : VDD2C Step-up range is required at more than 8533 Mbps 10 <sub>B</sub> : VDD2C Step-up range is required at more than 9600 Mbps 11 <sub>B</sub> : RFU	
DVFSB (VDD2D Dynamic Voltage and Frequency for high data rate) requirement	Read-only	OP[3:2]	00 <sub>B</sub> : VDD2D Step-up range is not required 01 <sub>B</sub> : VDD2D Step-up range is required at more than 8533 Mbps 10 <sub>B</sub> : VDD2D Step-up range is required at more than 9600 Mbps 11 <sub>B</sub> : RFU	
DVFSL (VDD2D Dynamic Voltage and frequency for low-data rate indicator	Read-only	OP[5:4]	00 <sub>B</sub> : VDD2D Step-down range is not supported. 01 <sub>B</sub> : VDD2D Step-down range is supported at equal or less than 1600 Mbps 10 <sub>B</sub> : VDD2D Step-down range is supported at equal or less than 3200 Mbps 11 <sub>B</sub> : RFU	

## 6.2 Mode Register Definition (cont'd)

**Table 116 – MR22 Register Information (MA[6:0] = 16<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK PST	WCK ON	CK Mode		WCK Mode		RDQS	

**Table 117 – MR22 Definition**

Function	Register Type	Operand	Data	Notes
RDQS (Read DQS)	Write-only	OP[1:0]	00 <sub>B</sub> : RDQS_t and RDQS_c disabled 01 <sub>B</sub> : RDQS_t enabled and RDQS_c disabled (default) 10 <sub>B</sub> : RDQS_t and RDQS_c enabled 11 <sub>B</sub> : RDQS_t disabled and RDQS_c enabled	1,2,3, 6,7,9
WCK Mode		OP[3:2]	00 <sub>B</sub> : differential (default) 01 <sub>B</sub> : single-ended from WCK_t 10 <sub>B</sub> : single-ended from WCK_c 11 <sub>B</sub> : reserved	1,2,4, 5,8
CK Mode		OP[4]	0 <sub>B</sub> : differential (default) 1 <sub>B</sub> : single-ended	1,2,10
WCK ON (WCK Always On mode)		OP[5]	0 <sub>B</sub> : WCK Always On Mode disabled (default) 1 <sub>B</sub> : WCK Always On Mode enabled	1,2
WCK PST (WCK Post-amble Length)		OP[7:6]	00 <sub>B</sub> : 2.5*tWCK (default) 01 <sub>B</sub> : 4.5*tWCK 10 <sub>B</sub> : 6.5*tWCK 11 <sub>B</sub> : reserved	1,2,11, 12
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	WCK clocking generates RDQS_t and RDQS_c.			
NOTE 4	When MR22 OP[3:2]= 01 <sub>B</sub> , WCK_t is used as WCK timing, and WCK_c should be maintained at a valid logic level.			
NOTE 5	When MR22 OP[3:2]= 10 <sub>B</sub> , WCK_c is used as WCK timing, and WCK_t should be maintained at a valid logic level			
NOTE 6	When MR22 OP[1:0]= 01 <sub>B</sub> , RDQS_t is used as RDQS timing, and RDQS_c should be Hi-Z state.			
NOTE 7	When MR22 OP[1:0]= 11 <sub>B</sub> , RDQS_c is used as RDQS timing, and RDQS_t should be Hi-Z state.			
NOTE 8	When MR22 OP[3:2]= 01 <sub>B</sub> , WCK_t polarity is the same as WCK_t when MR22 OP[3:2]=00 <sub>B</sub> , and when MR22 OP[3:2]= 10 <sub>B</sub> , WCK_c polarity is the same as WCK_c when MR22 OP[3:2]=00 <sub>B</sub> .			
NOTE 9	When MR22 OP[1:0]= 01 <sub>B</sub> , RDQS_t polarity is the same as RDQS_t when MR22 OP[1:0]=10 <sub>B</sub> , and when MR22 OP[1:0]= 11 <sub>B</sub> , RDQS_c polarity is the same as RDQS_c when MR22 OP[1:0]=10 <sub>B</sub> .			
NOTE 10	When MR22 OP[4]= 1 <sub>B</sub> , CK_t is used as CK timing and CK_c is set to a valid logic state.			
NOTE 11	tWCKPST length should be larger than tRPST length.			
NOTE 12	WCK PST MR22 OP[7:6] applies to both read and write operation timing as the same setting.			

## 6.2 Mode Register Definition (cont'd)

**Table 118 — MR23 Register Information (MA [7:0] = 17<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	CS ODT PD	RFU	RECC/REDC	WEDC	WECC

**Table 119 — MR23 Definition**

Function	Register Type	Operand	Data	Notes
Write Link ECC Mode	Write-only	OP[0]	0 <sub>B</sub> : Not Enabled (default) 1 <sub>B</sub> : Enabled	1,2,3
Write Link EDC Mode		OP[1]	0 <sub>B</sub> : Not Enabled (default) 1 <sub>B</sub> : Enabled	1,2,3
RECC/REDC (Read Link ECC/EDC Mode)		OP[2]	0 <sub>B</sub> : Not Enabled (default) 1 <sub>B</sub> : Enabled	1,2
CS ODT PD (CS ODT behavior option on Power Down)		OP[4]	0 <sub>B</sub> : CS ODT is disabled on Power Down (default) 1 <sub>B</sub> : CS ODT follows MR setting (MR17 OP[5:3]) on Power Down	4
NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.				
NOTE 2 Refer to 7.8.21 for LPDDR6 Selectable Link ECC/EDC Mode description.				
NOTE 3 Write Link ECC and EDC modes are mutually exclusive functions, and hence, enabling both features at the same time (MR23 OP[0] = 1 <sub>B</sub> and MR23 OP[1] = 1 <sub>B</sub> ) is prohibited.				
NOTE 4 CS ODT follows MR setting (MR17 OP[5:3]) in Power Down regardless of OP[4] if Dynamic Write NT-ODT is enabled: MR20 OP[5:3] ≠ 000B.				

## 6.2 Mode Register Definition (cont'd)

**Table 120 – MR25 Register Information (MA[6:0] = 19<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Optimized Refresh mode	PARC	CA Inputs TERM	CK Pair TERM				RFU

**Table 121 – MR25 Definition**

Function	Register Type	Operand	Data	Notes
CK Pair TERM (Other Shared dies' CK ODT Info)	Write-only	OP[4]	0 <sub>B</sub> : All ranks sharing CK Pair are un-terminated (default) 1 <sub>B</sub> : One of the ranks sharing CK Pair is terminated	1,2
CA Inputs TERM (Other Shared dies' CA ODT Info)		OP[5]	0 <sub>B</sub> : All ranks sharing CA Inputs are un-terminated (default) 1 <sub>B</sub> : One of the ranks sharing CA Inputs is terminated	1,2
PARC (Partial Array Refresh Control)		OP[6]	0 <sub>B</sub> : PARC disable (default) 1 <sub>B</sub> : PARC enable	3,4
Optimized Refresh mode (Optimized Refresh mode Enable)		OP[7]	0 <sub>B</sub> : Optimized Refresh mode disabled 1 <sub>B</sub> : Optimized Refresh mode enabled (default)	5,6
NOTE 1 MR25 OP[5] and [4] are set to notify CA/CK ODT status of other shared dies. NOTE 2 When CK and CA ODT status is different from each other (ex. CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer uses the fixed level reference voltage (TBD). NOTE 3 MR27 PASR Segment Mask is applied to PARC (Partial Array Refresh Control) operation if PARC is enabled. NOTE 4 Refer to 7.6.6 for LPDDR6 PASR descriptions. NOTE 5 In case of MR25 OP[7]=0 <sub>B</sub> , Refresh operation needs to follow the refresh requirement which is defined in 7.6.3 Refresh Requirement. NOTE 6 SoC which does not support the optimized refresh mode can use SDRAM without changing MR OP[7] to 0 <sub>B</sub> , if the SoC follows the requirements specified in 7.6.3 Refresh Requirement.				

## 6.2 Mode Register Definition (cont'd)

**Table 122 – MR26 Register Information (MA[7:0] = 1A<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	sPPR		WSOE	CA Parity	DCM Flip	DCM Start/Stop

**Table 123 – MR26 Definition**

Function	Register Type	Operand	Data	Notes
DCM Start/Stop	Write-only	OP[0]	0 <sub>B</sub> : Stop (default) 1 <sub>B</sub> : Start	
DCM Flip (Flip inputs to cancel offset)		OP[1]	0 <sub>B</sub> : No flip (default) 1 <sub>B</sub> : Flip	
CA Parity (CA parity check control)		OP[2]	0 <sub>B</sub> : CA parity check disable (default) 1 <sub>B</sub> : CA parity check enable	1,2
WSOE (WCK Sync-Off Extension Control)		OP[3]	0 <sub>B</sub> : WCK Sync-Off Extension Control disable (default) 1 <sub>B</sub> : WCK Sync-Off Extension Control enable	
sPPR (Soft Post Package Repair control)		OP[5:4]	00 <sub>B</sub> : Disabled (Normal Operation) 01 <sub>B</sub> : sPPR Enabled 10 <sub>B</sub> : sPPR Undo Enabled 11 <sub>B</sub> : sPPR Lock Enabled	

NOTE 1 Enabling WCK Always On mode: MR22 OP[5]=1<sub>B</sub> is required before setting MR26 OP[2]=1<sub>B</sub>.  
 NOTE 2 The combination of MR22 OP[5]=0<sub>B</sub> and MR26 OP[2]=1<sub>B</sub> is prohibited.

## 6.2 Mode Register Definition (cont'd)

**Table 124 – MR27 Register Information (MA[6:0] = 1B<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

**Table 125 – MR27 Definition**

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write Only	[7:0]	0 <sub>B</sub> : Segment Refresh Enable (default) 1 <sub>B</sub> : Segment Refresh Disable	1,2

**Table 126 – Row Address of Masked Segment**

Segment	OP[n]	Segment Mask	Density per 1 Sub-channel								
			2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
			R12:R10	R13:R11	R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14
0	0	xxxxxx1									000 <sub>B</sub>
1	1	xxxxx1x									001 <sub>B</sub>
2	2	xxxx1xx									010 <sub>B</sub>
3	3	xxx1xxx									011 <sub>B</sub>
4	4	xx1xxxx									100 <sub>B</sub>
5	5	xx1xxxxx									101 <sub>B</sub>
6	6	x1xxxxx	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>
7	7	1xxxxxx	111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>

NOTE 1 This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.  
 NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00<sub>B</sub>).

## 6.2 Mode Register Definition (cont'd)

**Table 127 – MR28 Register Information (MA [7:0] = 1C<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
	RFU			ZQ Interval		ZQ Stop	ZQ Reset

**Table 128 – MR28 Definition**

Function	Register Type	Operand	Data	Notes
ZQ Reset	Write-only	OP[0]	0 <sub>B</sub> : Normal Operation (default) 1 <sub>B</sub> : ZQ Reset	1,2,5
ZQ Stop		OP[1]	0 <sub>B</sub> : Normal Operation (default) 1 <sub>B</sub> : Background ZQ Calibration is halted after tZQSTOP	3,5
ZQ Interval		OP[3:2]	00 <sub>B</sub> : Background Cal Interval ≤ 32ms 01 <sub>B</sub> : Background Cal Interval ≤ 64ms (default) 10 <sub>B</sub> : Background Cal Interval ≤ 128ms 11 <sub>B</sub> : Background Cal Interval ≤ 256ms	4
NOTE 1 See Table 24 for calibration latency and timing. NOTE 2 Asserting ZQ Reset will set the calibration values to their default setting. NOTE 3 When ZQ Stop is enabled, the ZQ resource is available for use by other devices. See 4.2.2.2 NOTE 4 ZQ Interval is only applicable to ZQ Initiator die. This setting will be ignored by ZQ Target die. NOTE 5 It is prohibited to simultaneously enable ZQ Reset and ZQ Stop as they are mutually exclusive functions.				

## 6.2 Mode Register Definition (cont'd)

**Table 129 – MR30 Register Information (MA [7:0] = 1E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	RFU	DQ[11:8] for per-bit control Register for Read DQ Calibration			

**Table 130 – MR30 Definition**

Function	Register Type	Operand	Data	Notes
DQ[11:8] for per-bit control Register for Read DQ Calibration	Write-Only	OP[3:0]	<p>The following values may be written for any operand OP[3:0], and will be applied to the corresponding DQ locations DQ[11:8]:</p> <p>In RDC DQ mode (MR16 OP[3] = 0<sub>B</sub>),            0<sub>B</sub>: Do not invert            1<sub>B</sub>: Invert the DQ Calibration patterns in MR32, MR33 and MR34</p> <p>In RDC DQ mode (MR16 OP[3] = 1<sub>B</sub>),            0<sub>B</sub>: Do not apply low-fix            1<sub>B</sub>: Data pattern is low-fixed</p> <p>Default value for OP[3:0]= 5<sub>H</sub></p>	1,2
NOTE 1 This register will invert or apply low-fix for the Read DQ Calibration pattern found in MR32, MR33 and MR34 for any single DQ, or any combination of DQ's. Example: In case of DQ inversion mode, If MR30 OP[3:0]=0101 <sub>B</sub> , then the DQ Calibration patterns transmitted on DQ[11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[10,8] will be inverted. In case of DQ output fix0 mode, If MR30 OP[3:0]=0101 <sub>B</sub> , then the DQ Calibration patterns transmitted on DQ[11,9] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[10,8] will be low-fixed.				
NOTE 2 In case of High Capacity mode or Efficiency mode, (Reserved)				

**Table 131 – MR30 Invert Register Pin Mapping**

PIN	DQ8	DQ9	DQ10	DQ11
MR30	OP0	OP1	OP2	OP3

## 6.2 Mode Register Definition (cont'd)

**Table 132 – MR31 Register Information (MA [7:0] = 1F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ[7:0] for per-bit control Register for Read DQ Calibration							

**Table 133 – MR31 Definition**

Function	Register Type	Operand	Data	Notes
DQ[7:0] for per-bit control Register for Read DQ Calibration	Write-Only	OP[7:0]	<p>The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0]:</p> <p>In RDC DQ mode (MR16 OP[3] = 0<sub>B</sub>),            0<sub>B</sub>: Do not invert            1<sub>B</sub>: Invert the DQ Calibration patterns in MR32, MR33 and MR34</p> <p>In RDC DQ mode (MR16 OP[3] = 1<sub>B</sub>),            0<sub>B</sub>: Do not apply low-fix            1<sub>B</sub>: Data pattern is low-fixed</p> <p>Default value for OP[7:0]=55<sub>H</sub></p>	1,2
NOTE 1 This register will invert or apply low-fix for the Read DQ Calibration pattern found in MR32, MR33 and MR34 for any single DQ, or any combination of DQ's. Example: In case of DQ inversion mode, If MR31 OP[3:0]= 00010101 <sub>B</sub> , then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted. In case of DQ output fix0 mode, If MR31 OP[7:0]= 00010101 <sub>B</sub> , then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be low-fixed, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be low-fixed.				
NOTE 2 In case of High Capacity mode or Efficiency mode, (Reserved)				

**Table 134 – MR31 Invert Register Pin Mapping**

PIN	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
MR31	OP[0]	OP[1]	OP[2]	OP[3]	OP[4]	OP[5]	OP[6]	OP[7]

## 6.2 Mode Register Definition (cont'd)

**Table 135 – MR32 Register Information (MA [7:0] = 20<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "A"							

**Table 136 – MR32 Definition**

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR33 + MR34	Write-Only	OP[7:0]	X <sub>B</sub> : DQ Calibration Pattern A "5A <sub>H</sub> " (default)	1,2,3
NOTE 1	Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in this register followed by the contents of MR33 and MR34. The pattern contained in MR32 is transmitted on each bit of DQ[11:0] when DQ Read Calibration is issued. The pattern is transmitted serially on each data lane, and is organized as "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR32 is 27 <sub>H</sub> , then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 11100100 <sub>B</sub> . A default pattern "5A <sub>H</sub> " is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. The contents of MR30 and MR31 may invert the data pattern for a given DQ. See MR30 and MR31 definitions for more information.			
NOTE 2	MR30 and MR31 may be used to invert the MR32/MR33/MR34 data patterns on the DQ pins. See MR30 (Table 129, Table 130, and Table 131) and MR31 (Table 132, Table 133, and Table 134) definitions for more information.			
NOTE 3	No Data Bus Inversion (DBI) function is enacted during Read DQ Calibration, even if DBI is enabled in MR2 OP[7:5].			

**Table 137 – MR33 Register Information (MA [7:0] = 21<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B"							

**Table 138 – MR33 Definition**

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR33 + MR34	Write-Only	OP[7:0]	X <sub>B</sub> : DQ Calibration Pattern B "3C <sub>H</sub> " (default)	1,2,3
NOTE 1	Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in MR32 followed by the contents of this register, and then MR34 followed. The pattern contained in MR33 is concatenated to the end of MR32 and transmitted on each bit of DQ[11:0] when DQ Read Calibration is issued. The pattern is transmitted serially on each data lane, organized "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR33 is 27 <sub>H</sub> , then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 111100100 <sub>B</sub> . A default pattern "3C <sub>H</sub> " is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. See MR32 (Table 136) for more information.			
NOTE 2	MR30 and MR31 may be used to invert the MR32/MR33/MR34 data patterns on the DQ pins. See MR30 (Table 129, Table 130, Table 131) and MR31 (Table 132, Table 133, Table 134) definitions for more information.			
NOTE 3	No Data Bus Inversion (DBI) function is enacted during Read DQ Calibration, even if DBI is enabled in MR2 OP[7:5].			

## 6.2 Mode Register Definition (cont'd)

**Table 139 – MR34 Register Information (MA [7:0] = 22<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "C"							

**Table 140 – MR34 Definition**

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR33 + MR34	Write-Only	OP[7:0]	X <sub>B</sub> : DQ Calibration Pattern C "A0 <sub>H</sub> " (default)	1,2,3
NOTE 1	Read DQ Calibration command (RDC) causes the device to return the DQ Calibration Pattern contained in MR32 and MR33 followed by the contents of this register. The pattern contained in MR34 is concatenated to the end of MR33 and transmitted on each bit of DQ[11:0] when DQ Read Calibration is issued. The pattern is transmitted serially on each data lane, organized "big endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR34 is 27 <sub>H</sub> , then the first bit transmitted will be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 111100100 <sub>B</sub> . A default pattern "A0 <sub>H</sub> " is loaded at power-up or RESET, or the pattern may be overwritten with an MRW to this register. See MR32 (Table 136) for more information.			
NOTE 2	MR30 and MR31 may be used to invert the MR32/MR33/MR34 data patterns on the DQ pins. See MR30 (Table 129, Table 130, Table 131) and MR31 (Table 132, Table 133, Table 134) definitions for more information.			
NOTE 3	No Data Bus Inversion (DBI) function is enacted during Read DQ Calibration, even if DBI is enabled in MR2 OP[7:5].			

## 6.2 Mode Register Definition (cont'd)

**Table 141 — MR35 Register Information (MA[7:0] = 23<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI Oscillator Count - LSB							

**Table 142 – MR35 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQI Oscillator (DQ input Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM WCK2DQI Oscillator Count	1,2,3,4
NOTE 1 MR35 reports the LSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.				
NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.				
NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.				
NOTE 4 WCKDQI & WCKDQO cannot be operated simultaneously.				

**Table 143 – MR36 Register Information (MA[7:0] = 24<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI Oscillator Count - MSB							

**Table 144 – MR36 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQI Oscillator (DQ input Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM WCK2DQI Oscillator Count	1,2,3,4
NOTE 1 MR36 reports the MSB bits of the DRAM WCK2DQI Oscillator count. The DRAM WCK2DQI Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of WCK relative to DQ.				
NOTE 2 Both MR35 and MR36 must be read (MRR) and combined to get the value of the WCK2DQI Oscillator count.				
NOTE 3 A new MPC [Start WCK2DQI Oscillator] could be issued to reset the contents of MR35/MR36.				
NOTE 4 WCKDQI & WCKDQO cannot be operated simultaneously.				

## 6.2 Mode Register Definition (cont'd)

**Table 145 – MR37 Register Information (MA[7:0] = 25<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQI interval timer run time setting							

**Table 146 – MR37 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQI interval timer run time	Write/Read	OP[7:0]	00000000 <sub>B</sub> : WCK2DQI interval timer stop via MPC Command (Default) 00000001 <sub>B</sub> : WCK2DQI timer stops automatically at 16th clock after timer start 00000010 <sub>B</sub> : WCK2DQI timer stops automatically at 32nd clock after timer start 00000011 <sub>B</sub> : WCK2DQI timer stops automatically at 48th clock after timer start 00000100 <sub>B</sub> : WCK2DQI timer stops automatically at 64th clock after timer start ----- Thru ----- 00111111 <sub>B</sub> : WCK2DQI timer stops automatically at (63X16)th clock after timer start 01XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 2048th clock after timer start 10XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 4096th clock after timer start 11XXXXXX <sub>B</sub> : WCK2DQI timer stops automatically at 8192nd clock after timer start	1,2
NOTE 1 MPC command with OP[6:0]= 10000010 <sub>B</sub> (Stop WCK2DQI Interval Oscillator) stops WCK2DQI interval timer in case of MR37 OP[7:0] = 00000000 <sub>B</sub> .				
NOTE 2 MPC command with OP[6:0]= 10000010 <sub>B</sub> (Stop WCK2DQI Interval Oscillator) is illegal with non-zero values in MR37 OP[7:0].				

## 6.2 Mode Register Definition (cont'd)

**Table 147 – MR38 Register Information (MA[7:0] = 26<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO Oscillator Count - LSB							

**Table 148 – MR38 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQO Oscillator (DQ output Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM WCK2DQO Oscillator Count	1,2,3
NOTE 1 MR38 reports the LSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.				
NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.				
NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.				

**Table 149 – MR39 Register Information (MA[7:0] = 27<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO Oscillator Count - MSB							

**Table 150 – MR39 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQO Oscillator (DQ output Training WCK Oscillator)	Read-only	OP[7:0]	0 - 255 MSB DRAM WCK2DQO Oscillator Count	1,2,3
NOTE 1 MR39 reports the MSB bits of the DRAM WCK2DQO Oscillator count. The DRAM WCK2DQO Oscillator count value is used to train WCK to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQ output relative to WCK.				
NOTE 2 Both MR38 and MR39 must be read (MRR) and combined to get the value of the WCK2DQO Oscillator count.				
NOTE 3 A new MPC [Start WCK2DQO Oscillator] can be issued at any time before sending MPC [Stop WCK2DQO Oscillator]. A new MPC [Start WCK2DQO Oscillator] resets the contents of MR38/MR39.				

## 6.2 Mode Register Definition (cont'd)

**Table 151 – MR40 Register Information (MA[7:0] = 28<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WCK2DQO interval timer run time setting							

**Table 152 – MR40 Definition**

Function	Register Type	Operand	Data	Notes
WCK2DQO interval timer run time	Write/Read	OP[7:0]	00000000 <sub>B</sub> : WCK2DQO interval timer stop via MPC Command (Default) 00000001 <sub>B</sub> : WCK2DQO timer stops automatically at 16th clock after timer start 00000010 <sub>B</sub> : WCK2DQO timer stops automatically at 32nd clock after timer start 00000011 <sub>B</sub> : WCK2DQO timer stops automatically at 48th clock after timer start 00000100 <sub>B</sub> : WCK2DQO timer stops automatically at 64th clock after timer start ----- Thru ----- 00111111 <sub>B</sub> : WCK2DQO timer stops automatically at (63X16)th clock after timer start 01XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 2048th clock after timer start 10XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 4096th clock after timer start 11XXXXXX <sub>B</sub> : WCK2DQO timer stops automatically at 8192nd clock after timer start	1, 2
NOTE 1 MPC command with OP[7:0]=10000100 <sub>B</sub> (Stop WCK2DQO Interval Oscillator) stops WCK2DQO interval timer in case of MR40 OP[7:0] = 00000000 <sub>B</sub> .				
NOTE 2 MPC command with OP[7:0]=10000100 <sub>B</sub> (Stop WCK2DQO Interval Oscillator) is illegal with non-zero values in MR40 OP[7:0].				

## 6.2 Mode Register Definition (cont'd)

**Table 153 – MR41 Register Information (MA[7:0] = 29<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	MBIST Status	PPRE		MBIST Selection		MBIST Availability	PDFEC

**Table 154 – MR41 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Control (PDFEC)	Write Only	OP[0]	0 <sub>B</sub> : Per-pin DFE disable & Broadcast DFEDQ0 to all DQs (default) 1 <sub>B</sub> : Per-pin DFE enable	1,2
MBIST Availability	Read Only	OP[1]	0 <sub>B</sub> : No MBIST 1 <sub>B</sub> : Supports MBIST (optional)	
MBIST Selection	Write Only	OP[3:2]	00 <sub>B</sub> : Disable 01 <sub>B</sub> : RFU 10 <sub>B</sub> : MBIST-Test enabled 11 <sub>B</sub> : MBIST-mPPR enabled	3,4
PPRE	Write Only	OP[4]	0 <sub>B</sub> : PPR Disable (default) 1 <sub>B</sub> : PPR Enable	3
MBIST Status	Read Only	OP[6:5]	00 <sub>B</sub> : No error detected 01 <sub>B</sub> : Error detected; repair resources available 10 <sub>B</sub> : Error detected; repair resources expired 11 <sub>B</sub> : Unresolved operation, abort required	5,6
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address or read from with an MRR command to this address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	MBIST requires MBIST-Test to be performed prior to MBIST-mPPR and only MBIST-Test, MBIST-mPPR, or PPR maybe enabled at any given time.			
NOTE 4	The array data is undefined upon completion of MBIST testing.			
NOTE 5	The MBIST status after power-up and initialization is MR41 OP[6:5] = 00 <sub>B</sub> . The host must initiate at least one MBIST-Test sequence for valid MR41 OP[6:5] = 00 <sub>B</sub> reading.			
NOTE 6	MBIST Status = 11 <sub>B</sub> indicates that the MBIST Test circuitry detected an inability to complete the test. It signals to the host that the test is broken.			

## 6.2 Mode Register Definition (cont'd)

**Table 155 – MR42 Register Information (MA[7:0] = 2A<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Key Protection							

**Table 156 – MR42 Definition**

Function	Register Type	Operand	Data	Notes
PPR Key Protection	Write-only	OP[7:0]	PPR Key Protection code	1
NOTE 1 PPR entry and exit sequence details are described in 7.8.16				

**Table 157 – MR43 Register Information (MA[7:0] = 2B<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Resource Bank Group 1 / Bank 3	PPR Resource Bank Group 1 / Bank 2	PPR Resource Bank Group 1 / Bank 1	PPR Resource Bank Group 1 / Bank 0	PPR Resource Bank Group 0 / Bank 3	PPR Resource Bank Group 0 / Bank 2	PPR Resource Bank Group 0 / Bank 1	PPR Resource Bank Group 0 / Bank 0

**Table 158 – MR43 Definition**

Function	Register Type	Operand	Data	Notes
PPR Resource Bank Group 1 / Bank 3	Read-only	OP[7]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 1 / Bank 2		OP[6]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 1 / Bank 1		OP[5]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 1 / Bank 0		OP[4]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 0 / Bank 3		OP[3]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 0 / Bank 2		OP[2]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 0 / Bank 1		OP[1]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 0 / Bank 0		OP[0]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	

## 6.2 Mode Register Definition (cont'd)

**Table 159 – MR44 Register Information ( $MA[7:0] = 2C_H$ )**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PPR Resource Bank Group 3 / Bank 3	PPR Resource Bank Group 3 / Bank 2	PPR Resource Bank Group 3 / Bank 1	PPR Resource Bank Group 3 / Bank 0	PPR Resource Bank Group 2 / Bank 3	PPR Resource Bank Group 2 / Bank 2	PPR Resource Bank Group 2 / Bank 1	PPR Resource Bank Group 2 / Bank 0

**Table 160 – MR44 Definition**

Function	Register Type	Operand	Data	Notes
PPR Resource Bank Group 3 / Bank 3	Read-only	OP[7]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 3 / Bank 2		OP[6]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 3 / Bank 1		OP[5]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 3 / Bank 0		OP[4]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 2 / Bank 3		OP[3]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 2 / Bank 2		OP[2]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 2 / Bank 1		OP[1]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	
PPR Resource Bank Group 2 / Bank 0		OP[0]	0 <sub>B</sub> : PPR Resource is not available 1 <sub>B</sub> : PPR Resource is available	

## 6.2 Mode Register Definition (cont'd)

**Table 161 — MR45 Register Information (MA[7:0] = 2D<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	RFU	Reserved <sup>1</sup>		Duty Cycle adjuster		
NOTE 1 OP[4] is reserved to make extensibility for DCA in the future.							

**Table 162 – MR45 Definition**

Function	Register Type	Operand	Data	Notes
Duty Cycle adjuster (DCA)	Write-only	OP[3:0]	0000 <sub>B</sub> : 0 Steps (default no adjustment) 0001 <sub>B</sub> : -1 Steps 0010 <sub>B</sub> : -2 Steps 0011 <sub>B</sub> : -3 Steps 0100 <sub>B</sub> : -4 Steps 0101 <sub>B</sub> : -5 Steps 0110 <sub>B</sub> : -6 Steps 0111 <sub>B</sub> : -7 Step 1000 <sub>B</sub> : RFU 1001 <sub>B</sub> : +1 Step 1010 <sub>B</sub> : +2 Steps 1011 <sub>B</sub> : +3 Steps 1100 <sub>B</sub> : +4 Steps 1101 <sub>B</sub> : +5 Steps 1110 <sub>B</sub> : +6 Steps 1111 <sub>B</sub> : +7 Steps	1,2,3,4
NOTE 1 0001 <sub>B</sub> to 0111 <sub>B</sub> of bit sets will decrease the internal WCK duty cycle.				
NOTE 2 1001 <sub>B</sub> to 1111 <sub>B</sub> of bit sets will increase the internal WCK duty cycle.				
NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.				
NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the SDRAM and may be changed without affecting SDRAM operation.				

## 6.2 Mode Register Definition (cont'd)

**Table 163 — MR46 Register Information (MA [7:0] = 2E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved <sup>1</sup>				Read DCA	RFU	RDQS Toggle	Enhanced RDQS
NOTE 1 OP[7] is reserved to make extensibility for DCA in the future.							

**Table 164 — MR46 Definition**

Function	Register Type	Operand	Data	Notes
Enhanced RDQS (Enhanced RDQS training mode)	Write-Only	OP[0]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Enhanced RDQS training mode Enabled	
RDQS Toggle (RDQS toggle mode)		OP[1]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : RDQS toggle mode Enabled	
Read DCA (Read Duty Cycle adjuster)		OP[6:3]	0000 <sub>B</sub> : 0 Steps (default no adjustment) 0001 <sub>B</sub> : -1 Steps 0010 <sub>B</sub> : -2 Steps 0011 <sub>B</sub> : -3 Steps 0100 <sub>B</sub> : -4 Steps 0101 <sub>B</sub> : -5 Steps 0110 <sub>B</sub> : -6 Steps 0111 <sub>B</sub> : -7 Step 1000 <sub>B</sub> : RFU 1001 <sub>B</sub> : +1 Step 1010 <sub>B</sub> : +2 Steps 1011 <sub>B</sub> : +3 Steps 1100 <sub>B</sub> : +4 Steps 1101 <sub>B</sub> : +5 Steps 1110 <sub>B</sub> : +6 Steps 1111 <sub>B</sub> : +7 Steps	1,2,3,4
NOTE 1 0001B to 0111B of bit sets will decrease the internal WCK duty cycle. NOTE 2 1001B to 1111B of bit sets will increase the internal WCK duty cycle. NOTE 3 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address. NOTE 4 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The SDRAM will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the SDRAM and may be changed without affecting SDRAM operation.				

## 6.2 Mode Register Definition (cont'd)

**Table 165 – MR47 Register Information (MA[7:0] = 2F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-1							

**Table 166 – MR47 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-1	Read-only	OP[7:0]	Serial ID-1	1
NOTE 1 MR47 is vendor specific.				

**Table 167 – MR48 Register Information (MA[7:0] = 30<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-2							

**Table 168 – MR48 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-2	Read-only	OP[7:0]	Serial ID-2	1
NOTE 1 MR48 is vendor specific.				

**Table 169 – MR49 Register Information (MA[7:0] = 31<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-3							

**Table 170 – MR49 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-3	Read-only	OP[7:0]	Serial ID-3	1
NOTE 1 MR49 is vendor specific.				

**Table 171 – MR50 Register Information (MA[7:0] = 32<sub>H</sub>)**

OP[7]	OP[6]	OP[5]		OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-4								

**Table 172 – MR50 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-4	Read-only	OP[7:0]	Serial ID-4	1
NOTE 1 MR50 is vendor specific.				

## 6.2 Mode Register Definition (cont'd)

**Table 173 – MR51 Register Information (MA[7:0] = 33<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-5							

**Table 174 – MR51 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-5	Read-only	OP[7:0]	Serial ID-5	1
NOTE 1 MR51 is vendor specific.				

**Table 175 – MR52 Register Information (MA[7:0] = 34<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-6							

**Table 176 – MR52 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-6	Read-only	OP[7:0]	Serial ID-6	1
NOTE 1 MR52 is vendor specific.				

**Table 177 – MR53 Register Information (MA[7:0] = 35<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-7							

**Table 178 – MR53 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-7	Read-only	OP[7:0]	Serial ID-7	1
NOTE 1 MR53 is vendor specific.				

**Table 179 – MR54 Register Information (MA[7:0] = 36<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Serial ID-8							

**Table 180 – MR54 Definition**

Function	Register Type	Operand	Data	Notes
LPDDR6 Serial ID-8	Read-only	OP[7:0]	Serial ID-8	1
NOTE 1 MR54 is vendor specific.				

## 6.2 Mode Register Definition (cont'd)

**Table 181 – MR70 Register Information (MA[7:0] = 46<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ1 (DFEDQ1)		RFU	Per-pin DFE Quantity for DQ0 (DFEDQ0)			

**Table 182 – MR70 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ0 (DFEDQ0)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ1 (DFEDQ1)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 183 – MR71 Register Information (MA[7:0] = 47<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ3 (DFEDQ3)		RFU	Per-pin DFE Quantity for DQ2 (DFEDQ2)			

**Table 184 – MR71 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ2 (DFEDQ2)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ3 (DFEDQ3)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 185 – MR72 Register Information (MA[7:0] = 48<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ5 (DFEDQ5)			RFU	Per-pin DFE Quantity for DQ4 (DFED4)		

**Table 186 – MR72 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ4 (DFEDQ4)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ5 (DFEDQ5)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 187 – MR73 Register Information (MA[7:0] = 49<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ7 (DFEDQ7)			RFU	Per-pin DFE Quantity for DQ6 (DFEDQ6)		

**Table 188 – MR73 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ6 (DFEDQ6)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ7 (DFEDQ7)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 189 – MR74 Register Information ( $MA[7:0] = 4A_H$ )**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ9 (DFEDQ9)			RFU	Per-pin DFE Quantity for DQ8 (DFEDQ8)		

**Table 190 – MR74 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ8 (DFEDQ8)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ9 (DFEDQ9)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 191 – MR75 Register Information ( $MA[7:0] = 4B_H$ )**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	Per-pin DFE Quantity for DQ11 (DFEDQ11)				RFU	Per-pin DFE Quantity for DQ10 (DFEDQ10)	

**Table 192 – MR75 Definition**

Function	Register Type	Operand	Data	Notes
Per-pin DFE Quantity for DQ10 (DFEDQ10)	Write	OP[2:0]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[3]	RFU	
Per-pin DFE Quantity for DQ11 (DFEDQ11)	Write	OP[6:4]	000 <sub>B</sub> : DFE disabled (Default) 001 <sub>B</sub> : Minimum negative feedback quantity : : 111 <sub>B</sub> : Maximum negative feedback quantity	1,2,3
RFU	N/A	OP[7]	RFU	
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR16 OP[1:0]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR16 OP[3:2]). The values in the registers for the inactive set point will be ignored by the device and may be changed without affecting device operation.			
NOTE 3	If PDFEC disabled and broadcast DFEDQ0 to all DQs(MR41 OP[0]=0b), MR71 OP[7:4], MR72~MR75 are ignored			

## 6.2 Mode Register Definition (cont'd)

**Table 193 – MR78 Register Information (MA[7:0] = 4E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PUDS for DQ3	Pre-PUDS for DQ2	Pre-PUDS for DQ1	Pre-PUDS for DQ0				

**Table 194 – MR78 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ0	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ1		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ2		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ3		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 195 – MR79 Register Information (MA[7:0] = 4F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PUDS for DQ7		Pre-PUDS for DQ6		Pre-PUDS for DQ5		Pre-PUDS for DQ4	

**Table 196 – MR79 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ4	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ5		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ6		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ7		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 197 – MR80 Register Information (MA[7:0] = 50<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PUDS for DQ11		Pre-PUDS for DQ10		Pre-PUDS for DQ9		Pre-PUDS for DQ8	

**Table 198 – MR80 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ8	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ9		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ10		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for DQ11		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 199 – MR81 Register Information (MA[7:0] = 51<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PDDS for DQ3	Pre-PDDS for DQ2	Pre-PDDS for DQ1	Pre-PDDS for DQ0				

**Table 200 – MR81 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ0	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ1		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ2		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ3		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 201 – MR82 Register Information (MA[7:0] = 52<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PDDS for DQ7		Pre-PDDS for DQ6		Pre-PDDS for DQ5		Pre-PDDS for DQ4	

**Table 202 – MR82 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ4	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ5		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ6		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ7		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 203 – MR83 Register Information (MA[7:0] = 53<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PDDS for DQ11		Pre-PDDS for DQ10		Pre-PDDS for DQ9		Pre-PDDS for DQ8	

**Table 204 – MR83 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ8	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ9		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ10		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for DQ11		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.			
NOTE 2	There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.			
NOTE 3	Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.			
NOTE 4	Each MR bit can be enabled only by FSP procedure.			
NOTE 5	The pre-emphasis applies above 6400 Mbps.			

## 6.2 Mode Register Definition (cont'd)

**Table 205 – MR84 Register Information (MA[7:0] = 54<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Pre-PDDS for RDQS_c	Pre-PDDS for RDQS_t	Pre-PUDS for RDQS_c	Pre-PUDS for RDQS_t				

**Table 206 – MR84 Definition**

Function	Register Type	Operand	Data	Notes
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for RDQS_t	Write-only	OP[1:0]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PUDS (Pre-Emphasis Pull-up Drive Strength) for RDQS_c		OP[3:2]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for RDQS_t		OP[5:4]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for RDQS_c		OP[7:6]	00 <sub>B</sub> : Disabled (Default) 01 <sub>B</sub> : Weak strength: TBD 10 <sub>B</sub> : Middle strength: TBD 11 <sub>B</sub> : Strong strength: TBD	1,2,3, 4,5
NOTE 1 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[5:4]) will be written to with an MRW command to this MR address.				
NOTE 2 There are three physical registers assigned to each bit of this MR parameter, designated set point 0, set point 1, and set point 2. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7:6]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.				
NOTE 3 Active MR bit which is selected by FSP-OP: MR13 OP[7:6] cannot be changed directly by MRW command except Reset and Initialization procedure.				
NOTE 4 Each MR bit can be enabled only by FSP procedure.				
NOTE 5 The pre-emphasis applies above 6400 Mbps.				

## 6.2 Mode Register Definition (cont'd)

**Table 207 – MR85 Register Information (MA [7:0] = 55<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Alert Verification Enable	Alert Verification Support (Optional)	Alert Back-Off Flag	RFU	Activation Counter Initialization Complete	Activation Counter Initialization	Counter Address Report Flag	Counter Error Flag

**Table 208 – MR85 Definition**

Function	Register Type	Operand	Data	Notes
Counter Error Flag	Read/Write	OP[0]	0 <sub>B</sub> : Clear (default) 1 <sub>B</sub> : Counter error detected	
Counter Address Report Flag	Read/Write	OP[1]	0 <sub>B</sub> : Clear (default) 1 <sub>B</sub> : Failing row address available in MR87, MR88, and MR89	
Activation Counter Initialization	Read/Write	OP[2]	0 <sub>B</sub> : Normal operating mode (default) 1 <sub>B</sub> : Initialization mode	
Activation Counter Initialization Complete	Read-Only	OP[3]	0 <sub>B</sub> : Initialization not completed 1 <sub>B</sub> : Initialization completed	
Alert Back-Off Flag	Read-Only	OP[5]	0 <sub>B</sub> : Clear 1 <sub>B</sub> : Source of Alert_n	
Alert Verification Support (Optional)	Read-Only	OP[6]	0 <sub>B</sub> : Alert Verification not supported 1 <sub>B</sub> : Alert Verification supported	
Alert Verification Enable	Read/Write	OP[7]	0 <sub>B</sub> : Alert Verification Disabled (default) 1 <sub>B</sub> : Alert Verification Trigger	

## 6.2 Mode Register Definition (cont'd)

**Table 209 – MR86 Register Information ( $MA[7:0] = 56_{H}$ )**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	PRAC Testing Initialization Enable	PRAC Testing Enable	PRAC Testing Support		Adaptive PRAC		MRFMaACT

**Table 210 – MR86 Definition**

Function	Register Type	Operand	Data	Notes
MRFMaACT	Read/Write	OP[1:0]	Min RFMab Commands during ABO_RFMs(Recovery Period) and min ACT Commands during ABO_delay(Alert Back-Off Delay) 00 <sub>B</sub> : 4 (default) 01 <sub>B</sub> : 2 10 <sub>B</sub> : 1 11 <sub>B</sub> : RFU	
Adaptive PRAC	Read/Write	OP[3:2]	00 <sub>B</sub> : Default Mitigation Threshold 01 <sub>B</sub> : Mitigation Level A 10 <sub>B</sub> : Mitigation Level B 11 <sub>B</sub> : Mitigation Level C	
PRAC Testing Support	Read-only	OP[4]	0 <sub>B</sub> : PRAC Testing not supported 1 <sub>B</sub> : PRAC Testing supported	
PRAC Testing Enable	Read/Write	OP[5]	0 <sub>B</sub> : PRAC Testing disabled (default) 1 <sub>B</sub> : PRAC Testing enabled	
PRAC Testing Initialization Enable	Read/Write	OP[6]	0 <sub>B</sub> : PRAC Testing Initialization disable (default) 1 <sub>B</sub> : PRAC Testing Initialization Enable	

## 6.2 Mode Register Definition (cont'd)

**Table 211 – MR87 Register Information (MA[7:0] = 57H)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
8bits of the Row Address for PRAC							

**Table 212 – MR87 Definition**

Function	Register Type	Operand	Data	Notes
8 bits of the Row Address for PRAC	Read-Only	OP[7:0]	Activation Counter RAS Row Error Address[7:0]	

**Table 213 – MR88 Register Information (MA[7:0] = 58H)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
8bits of the Row Address for PRAC							

**Table 214 – MR88 Definition**

Function	Register Type	Operand	Data	Notes
8 bits of the Row Address for PRAC	Read-Only	OP[7:0]	Activation Counter RAS Row Error Address[15:8]	

**Table 215 – MR89 Register Information (MA[7:0] = 59H)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	2 bits of the Bank Group for PRAC	2 bits of the Bank Address for PRAC	RFU	1 bit of the Row Address for PRAC		

**Table 216 – MR89 Definition**

Function	Register Type	Operand	Data	Notes
1 bit of the Row Address for PRAC	Read-Only	OP[0]	Activation Counter RAS Row Error Address[16]	
2 bits of the Bank Address for PRAC	Read-Only	OP[3:2]	Activation Counter RAS Row Error Bank Address BA[1:0]	
2 bits of the Bank Group for PRAC	Read-Only	OP[5:4]	Activation Counter RAS Row Error Bank Group BG[1:0]	

## 6.2 Mode Register Definition (cont'd)

**Table 217 – MR92 Register Information (MA[7:0] = 5C<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]	
System Meta mode enable	RFU	Loopback Phase selection			Loopback Mode and Target DQ			

**Table 218 – MR92 Definition**

Function	Register Type	Operand	Data	Notes	
Loopback Mode and Target DQ (Loopback mode Enable/Disable and Target DQ pin selection)	Write-only	OP[3:0]	0000 <sub>B</sub> : Disable (Default) 0001 <sub>B</sub> : DQ0 is loopback target input & LBDO is DQ5 0010 <sub>B</sub> : DQ1 is loopback target input & LBDO is DQ5 0011 <sub>B</sub> : DQ2 is loopback target input & LBDO is DQ5 0100 <sub>B</sub> : DQ3 is loopback target input & LBDO is DQ5 0101 <sub>B</sub> : DQ4 is loopback target input & LBDO is DQ5 0110 <sub>B</sub> : RFU 0111 <sub>B</sub> : RFU 1000 <sub>B</sub> : RFU 1001 <sub>B</sub> : DQ5 is loopback target input & LBDO is DQ4 1010 <sub>B</sub> : DQ6 is loopback target input & LBDO is DQ4 1011 <sub>B</sub> : DQ7 is loopback target input & LBDO is DQ4 1100 <sub>B</sub> : DQ8 is loopback target input & LBDO is DQ4 1101 <sub>B</sub> : DQ9 is loopback target input & LBDO is DQ4 1110 <sub>B</sub> : DQ10 is loopback target input & LBDO is DQ4 1111 <sub>B</sub> : DQ11 is loopback target input & LBDO is DQ4	1	
Loopback Phase selection			00 <sub>B</sub> : PhaseA (Default) 01 <sub>B</sub> : PhaseB 10 <sub>B</sub> : PhaseC 11 <sub>B</sub> : PhaseD		
System Meta mode enable		OP[7]	0 <sub>B</sub> : System Meta Mode Disable (Default) 1 <sub>B</sub> : System Meta Mode Enable		
NOTE 1 Selection of an unsupported DQ for the device configuration will result in undefined LBDO output					
NOTE 2 Loopback Phase selection is applied to any DQ selected by Loopback DQ selected by MR92 OP[3:0]					

## 6.2 Mode Register Definition (cont'd)

**Table 219 – MR93 Register Information (MA[6:0] = 5D<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enhanced Write DBI Set 0							

**Table 220 – MR93 Definition**

Function	Register Type	Operand	Data	Notes
Enhanced Write DBI Set 0	Write Only	[7:0]	X <sub>B</sub> : Write DBI Pattern “0000 0000 <sub>B</sub> ”(default)	1
NOTE 1 When Enhanced Write DBI-DC function is enabled (MR3 OP[1]= 1 <sub>B</sub> ), each DBI bit selects one of two mode registers (0 <sub>B</sub> for MR93 OP[7:0] and 1 <sub>B</sub> for MR94 OP[7:0]) for enhanced Write DBI operation. The selected mode register's 8-bit operands are applied to bit-wise XOR operation with corresponding Write data bits. Refer to 7.5.5.2 Write Data Bus Inversion Function for more detailed information.				

**Table 221 – MR94 Register Information (MA[6:0] = 5E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Enhanced Write DBI Set 1							

**Table 222 – MR94 Definition**

Function	Register Type	Operand	Data	Notes
Enhanced Write DBI Set 1	Write Only	[7:0]	X <sub>B</sub> : Write DBI Pattern “1111 1111 <sub>B</sub> ”(default)	1
NOTE 1 When Enhanced Write DBI-DC function is enabled (MR3 OP[1]= 1 <sub>B</sub> ), each DBI bit selects one of two mode registers (0 <sub>B</sub> for MR93 OP[7:0] and 1 <sub>B</sub> for MR94 OP[7:0]) for enhanced Write DBI operation. The selected mode register's 8-bit operands are applied to bit-wise XOR operation with corresponding Write data bits. Refer to 7.5.5.2 Write Data Bus Inversion Function for more detailed information.				

## 6.2 Mode Register Definition (cont'd)

**Table 223 – MR95 Register Information (MA[6:0] = 5F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PAMM Segment							

**Table 224 – MR95 Definition**

Function	Register Type	Operand	Data	Notes
PAMM Segment (Partial Array Meta Mode Segment)	Write Only	[7:0]	0 <sub>B</sub> : Segment disabled (default) 1 <sub>B</sub> : Segment enabled	

**Table 225 – Row Address of Enabled Segment**

Segment	OP[n]	Density per 1 Sub-channel								
		2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
		R12:R10	R13:R11	R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14
0	0									000 <sub>B</sub>
1	1									001 <sub>B</sub>
2	2									010 <sub>B</sub>
3	3									011 <sub>B</sub>
4	4									100 <sub>B</sub>
5	5									101 <sub>B</sub>
6	6	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>	Not Allowed	110 <sub>B</sub>
7	7	111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>		111 <sub>B</sub>

NOTE 1 This table indicates the range of row addresses in each enabled segment.  
 NOTE 2 For 3Gb, 6Gb, 12Gb, and 24Gb densities, OP[7:6] must always be LOW (=00<sub>B</sub>).

## 6.2 Mode Register Definition (cont'd)

**Table 226 – MR97 {FMR1} Register Information (MA[6:0] = 61<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Sum of MR98 OP[7:0]	TBD	CA/ADDR Parity Check Mode	TBD	On-die ECC MBE Fault	Write Link ECC SBE Correction Attempted	Write Link ECC MBE Fault/Write Link EDC SBE/MBE Fault	PRAC limit exceeded

**Table 227 – MR97 Definition**

Function	Register Type	Operand	Data	Notes
PRAC limit exceeded	Read	OP[0]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Write Link ECC MBE Fault / Write Link EDC SBE/MBE Fault	Read	OP[1]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Write Link ECC SBE Correction Attempted	Read	OP[2]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
On-die ECC MBE Fault	Read	OP[3]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
TBD	Read	OP[4]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
CA/ADDR Parity Check Mode	Read	OP[5]	0 <sub>B</sub> : No Error occurred 1 <sub>B</sub> : CA Parity Error occurred	
TBD	Read	OP[6]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Sum of MR98 OP[7:0]	Read	OP[7]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	1
NOTE 1 FMR1 OP[7] is sum of FMR2 OP[7:0]				

## 6.2 Mode Register Definition (cont'd)

**Table 228 – MR98 {FMR2} Register Information (MA[6:0] = 62<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

**Table 229 – MR98 Definition**

Function	Register Type	Operand	Data	Notes
RFU	Read	OP[0]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[1]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[2]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[3]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[4]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[5]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[6]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[7]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	

## 6.2 Mode Register Definition (cont'd)

**Table 230 – MR99 {FMR3} Register Information (MA[6:0] = 63<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Sum of FMR2 OP[7:0]	TBD	Alert State on CA Parity Fault	TBD	On-die ECC MBE Fault	Write Link ECC SBE Correction Attempted	Write Link ECC MBE Fault/ Write Link EDC SBE/MBE Fault	PRAC limit exceeded

**Table 231 – MR99 Definition**

Function	Register Type	Operand	Data	Notes
PRAC limit exceeded	Write	OP[0]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
Write Link ECC MBE Fault/ Write Link EDC SBE/MBE Fault	Write	OP[1]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
Write Link ECC SBE Correction Attempted	Write	OP[2]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
On-die ECC MBE Fault	Write	OP[3]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
TBD	Write	OP[4]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
Alert State on CA Parity Fault	Write	OP[5]	0 <sub>B</sub> : Alert not active 1 <sub>B</sub> : Alert active	
TBD	Write	OP[6]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
Sum of FMR2 OP[7:0]	Write	OP[7]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
NOTE 1 MR99 OP[0] Controls if PRAC ABO Protocol drives ALERT active.				

## 6.2 Mode Register Definition (cont'd)

**Table 232 – MR100 {FMR4} Register Information (MA[6:0] = 64<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							

**Table 233 – MR100 Definition**

Function	Register Type	Operand	Data	Notes
RFU	Write	OP[0]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[1]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[2]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[3]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[4]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[5]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[6]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[7]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1

NOTE 1 MR99 OP[7] set to 0<sub>B</sub> overrides MR100 OP[7:0] and prevents MR100 OP[7:0] from affecting Alert Output.

## 6.2 Mode Register Definition (cont'd)

**Table 234 – MR109 Register Information (MA[7:0] = 6D<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TSRO							

**Table 235 – MR109 Definition**

Function	Register Type	Operand	Data	Notes
TSRO (Temperature sensor read out)	Read	OP[7:0]	00000000 <sub>B</sub> : Lower than low temperature sensor limit 00000001 <sub>B</sub> : -40 °C 00000010 <sub>B</sub> : -39 °C 00000011 <sub>B</sub> : -38 °C   01000000 <sub>B</sub> : 23 °C 01000001 <sub>B</sub> : 24 °C   01000010 <sub>B</sub> : 25 °C 01000011 <sub>B</sub> : 26 °C   10010001 <sub>B</sub> : 104 °C 10010010 <sub>B</sub> : 105 °C   10010011 <sub>B</sub> : 106 °C 10010100 <sub>B</sub> : 107 °C   10100101 <sub>B</sub> : 124 °C 10100110 <sub>B</sub> : 125 °C   10100111 <sub>B</sub> : RFU 10101000 <sub>B</sub> : RFU   11111101 <sub>B</sub> : RFU 11111110 <sub>B</sub> : RFU   11111111 <sub>B</sub> : Higher than high temperature sensor limit	1 1, 2 1 1, 2 1

NOTE 1 LPDDR temperature sensor cannot provide accurate enough temperature due to circuits and placement. SOC can use this information as temperature gradient information. Temperature accuracy is not guaranteed by design values.

NOTE 2 These temperature ranges are optional. Please consult with vendor.

## 6.2 Mode Register Definition (cont'd)

**Table 236 – MR111 Register Information (MA[7:0] = 6F<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	RFU	ECS Support	Manual ECS On	Auto ECS State Entry	ECS Flag Reset	ECS Reset	Auto ECS On

**Table 237 – MR111 Definition**

Function	Register Type	Operand	Data	Notes
Auto ECS On	Write-only	OP[0]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Enabled	1
ECS Reset		OP[1]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Reset (bit is self-clearing)	2
ECS Flag Reset		OP[2]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Reset (bit is self-clearing)	2
Auto ECS State Entry		OP[3]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Enabled	
Manual ECS On		OP[4]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Enabled	3
ECS Support	Read-only	OP[5]	0 <sub>B</sub> : Not support ECS 1 <sub>B</sub> : Support ECS	1
NOTE 1 Auto ECS On (MR111 OP[0]) and Manual ECS On(MR111 OP[4]) are mutually exclusive.				
NOTE 2 The bit is self-clearing. The value returns to 0 <sub>B</sub> after the reset has been issued.				
NOTE 3 When Auto ECS On (MR111 OP[0]= 'H') is enabled, the host needs to use Auto ECS State Entry (MR111 OP[4]= 'H') for Auto ECS operation. If Auto ECS State Entry is not enabled ('L'), the host can issue CAS CMD in LPDDR6 state diagram.				

**Table 238 – MR112 Register Information (MA[7:0] = 70<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
ECS CE Flag	ECS UE Flag	RFU	RFU	RFU	UE Address RA[16]	RFU	Max CE Per Row Address RA[16]

**Table 239 – MR112 Definition**

Function	Register Type	Operand	Data	Notes
Max CE Per Row Address RA[16]	Read-only	OP[0]	Max CE Per Row Address RA[16]	
UE Address RA[16]	Read-only	OP[2]	UE Address RA[16]	
ECS UE Flag	Read-only	OP[6]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Enabled	
ECS CE Flag		OP[7]	0 <sub>B</sub> : Disabled (Default) 1 <sub>B</sub> : Enabled	

**Table 240 – MR113 Register Information (MA[7:0] = 71<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Max CE Per Row Address BA[3:0]				UE Address BA [3:0]			

**Table 241 – MR113 Definition**

Function	Register Type	Operand	Data	Notes
UE Address BA [3:0]	Read-only	OP[3:0]	UE Address BA [3:0]	
Max CE Per Row Address BA[3:0]		OP[7:4]	Max CE Per Row Address BA[3:0]	

## 6.2 Mode Register Definition (cont'd)

**Table 242 – MR114 Register Information (MA[7:0] = 72<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Max CE Per Row Address RA[15:8]							

**Table 243 – MR114 Definition**

Function	Register Type	Operand	Data	Notes
Max CE Per Row Address RA[15:8]	Read-only	OP[7:0]	Max CE Per Row Address RA[15:8]	

**Table 244 – MR115 Register Information (MA[7:0] = 73<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Max CE Per Row Address RA[7:0]							

**Table 245 – MR115 Definition**

Function	Register Type	Operand	Data	Notes
Max CE Per Row Address RA[7:0]	Read-only	OP[7:0]	Max CE Per Row Address RA[7:0]	

**Table 246 – MR116 Register Information (MA[7:0] = 74<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
UE Row Address RA[15:8]							

**Table 247 – MR116 Definition**

Function	Register Type	Operand	Data	Notes
UE Row Address RA[15:8]	Read-only	OP[7:0]	UE Row Address RA[15:8]	

**Table 248 – MR117 Register Information (MA[7:0] = 75<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
UE Row Address RA[7:0]							

**Table 249 – MR117 Definition**

Function	Register Type	Operand	Data	Notes
UE Row Address RA[7:0]	Read-only	OP[7:0]	UE Row Address RA[7:0]	

## 6.2 Mode Register Definition (cont'd)

**Table 250 – MR125 Register Information (MA[7:0] = 7D<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CA3 (F1)	CA2 (F1)	CA1 (F1)	CA0 (F1)	CA3 (R1)	CA2 (R1)	CA1 (R1)	CA0 (R1)

**Table 251 – MR125 Definition**

Function	Register Type	Operand	Data	Notes
Command input data at parity error (First half)	Read-only	OP[7:0]	CA0(R1) is input data to CA0 at first rising edge and CA0(F1) is input data to CA0 at first falling edge. The same shall thought of hereinafter for CA1(R1), CA2(R1), CA3(R1), CA1(F1), CA2(F1) and CA3(F1).	
NOTE 1 0000 0000B is default (Reset Value)				
NOTE 2 These bits are reset on power-up, SDRAM Reset, MR26 OP[2] sets to 1 <sub>B</sub> from 0 <sub>B</sub> and on each read of this Mode Register.				

**Table 252 – MR126 Register Information (MA[7:0] = 7E<sub>H</sub>)**

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CA3 (F2)	CA2 (F2)	CA1 (F2)	CA0 (F2)	CA3 (R2)	CA2 (R2)	CA1 (R2)	CA0 (R2)

**Table 253 — MR126 Definition**

Function	Register Type	Operand	Data	Notes
Command input data at parity error (Second half)	Read-only	OP[7:0]	CA0(R2) is input data to CA0 at second rising edge and CA0(F2) is input data to CA0 at second falling edge. The same shall thought of hereinafter for CA1(R2), CA2(R2), CA3(R2), CA1(F2), CA2(F2) and CA3(F2).	
NOTE 1 0000 0000B is default (Reset Value)				
NOTE 2 These bits are reset on power-up, SDRAM Reset, MR26 OP[2] sets to 1 <sub>B</sub> from 0 <sub>B</sub> and on each read of this Mode Register.				

## 7 Command and Operation

### 7.1 Command Truth Table

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR6 device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.

**Table 254 – Command Truth Table**

SDRAM COMMAND	CS	DDR COMMAND PIN				CK_t Edge	Notes
		CA0	CA1	CA2	CA3		
DESELECT (DES)	L	X	X	X	X	R1	2
	X	X	X	X	X	F1	
NO OPERATION (NOP)	H	L	L	L	V/PAR	R1	1, 2, 17
	X	L	L	L	V	F1	
	H	X	X	X	X	R2	
	X	X	X	X	X	F2	
POWER DOWN ENTRY (PDE)	H	L	L	L	V/PAR	R1	1, 2, 9, 17
	X	L	H	L	V	F1	
	H	X	X	X	X	R2	
	X	X	X	X	X	F2	
POWER DOWN EXIT (PDX-NT)	H	V	X	X	X	R1	1, 2, 9, 15
	X	V	X	X	X	F1	
	H	V	X	X	X	R2	
	X	V	X	X	X	F2	
SELF REFRESH ENTRY (SRE)	H	L	L	L	V/PAR	R1	1, 2, 8, 17
	X	L	L	H	PD	F1	
	H	X	X	X	X	R2	
	X	X	X	X	X	F2	
SELF REFRESH EXIT (SRX)	H	L	L	L	V/PAR	R1	1, 2, 17
	X	L	H	H	V	F1	
	H	X	X	X	X	R2	
	X	X	X	X	X	F2	
PRECHARGE (PRE) (Per Bank, All Banks)	H	L	L	L	V/PAR	R1	1, 2, 3, 5, 12, 17
	X	H	H	V	SC	F1	
	H	V	V	V	AB	R2	
	X	BA0	BA1	BG0	BG1	F2	
REFRESH (REF) (Dual Bank, All Banks)	H	L	L	L	V/PAR	R1	1, 2, 3, 5, 11, 12, 17
	X	H	L	RFM	SC	F1	
	H	dBG0	dBG1	V	AB	R2	
	X	BA0	BA1	BG0	BG1	F2	
ACTIVATE-1 (ACT-1)	H	H	H	H	V/PAR	R1	1, 2, 3, 4, 12, 17
	X	H	R15	R16	SC	F1	
	H	R11	R12	R13	R14	R2	
	X	BA0	BA1	BG0	BG1	F2	
ACTIVATE-2 (ACT-2)	H	H	H	H	V/PAR	R1	1, 2, 4, 17
	X	L	R8	R9	R10	F1	
	H	R4	R5	R6	R7	R2	
	X	R0	R1	R2	R3	F2	
WRITE (BL24) (WR-S)	H	H	L	H	WS/PAR	R1	1, 2, 3, 6, 10, 12, 13, 16, 17, 18
	X	C0	C1	AP	SC	F1	
	H/L	C2	C3	C4	C5	R2	
	X	BA0	BA1	BG0	BG1	F2	
WRITE (BL48) (WR-L)	H	L	L	H	WS/PAR	R1	1, 2, 3, 6, 10, 12, 13, 17, 18
	X	L	C1	AP	SC	F1	
	H/L	C2	C3	C4	C5	R2	
	X	BA0	BA1	BG0	BG1	F2	

Table 254 - Command Truth Table (cont'd)

SDRAM COMMAND	CS	DDR COMMAND PIN				CK_t edge	Notes
		CA0	CA1	CA2	CA3		
READ (BL24) (RD-S)	H	H	H	L	WS/PAR	R1	1, 2, 3, 6, 10, 12, 16, 17, 18
	X	C0	C1	AP	SC	F1	
	H	C2	C3	C4	C5	R2	
	X	BA0	BA1	BG0	BG1	F2	
READ (BL48) (RD-L)	H	L	H	L	WS/PAR	R1	1, 2, 3, 6, 10, 12, 17, 18
	X	C0	C1	AP	SC	F1	
	H	C2	C3	C4	C5	R2	
	X	BA0	BA1	BG0	BG1	F2	
CAS	H	H	L	L	WS	R1	1, 2, 7, 17, 18
	X	H	H	H	WS_OFF	F1	
	H	V	V	V	V/PAR	R2	
	X	V	V	V	V	F2	
MODE REGISTER READ (MRR)	H	H	L	L	WS/PAR	R1	1, 2, 10, 12, 14, 17
	X	L	H	H	SC	F1	
	H	MA4	MA5	MA6	MA7	R2	
	X	MA0	MA1	MA2	MA3	F2	
MULTI PURPOSE COMMAND (MPC)	H	H	L	L	V/PAR	R1	1, 2, 17
	X	H	L	H	V	F1	
	H	OP4	OP5	OP6	OP7	R2	
	X	OP0	OP1	OP2	OP3	F2	
MODE REGISTER WRITE-1 (MRW-1)	H	H	L	L	V/PAR	R1	1, 2, 17, 19
	X	L	L	H	BC	F1	
	H	MA4	MA5	MA6	MA7	R2	
	X	MA0	MA1	MA2	MA3	F2	
MODE REGISTER WRITE-2 (MRW-2)	H	H	L	L	V/PAR	R1	1, 2, 17
	X	H	H	L	V	F1	
	H	OP4	OP5	OP6	OP7	R2	
	X	OP0	OP1	OP2	OP3	F2	
WRITE FIFO (WFF)	H	H	L	L	WS/PAR	R1	1, 2, 10, 13, 17
	X	L	H	L	V	F1	
	H/L	V	V	V	V	R2	
	X	V	V	V	V	F2	
READ FIFO (RFF)	H	H	L	L	WS/PAR	R1	1, 2, 10, 17
	X	H	L	L	V	F1	
	H	V	V	V	V	R2	
	X	V	V	V	V	F2	
READ DQ CALIBRATION (RDC)	H	H	L	L	WS/PAR	R1	1, 2, 10, 17
	X	L	L	L	V	F1	
	H	V	V	V	V	R2	
	X	V	V	V	V	F2	
RFU	H	L	H	H	V/PAR	R1	1, 2, 17
	X	V	V	V	V	F1	
	H	V	V	V	V	R2	
	X	V	V	V	V	F2	

**Table 254 - Command Truth Table (cont'd)**

NOTE 1	LPDDR6 commands are two clock cycles long and defined by the states of CS at the 1st and 2nd rising edge (R1, R2) of clock and CA[3:0] at the 1st rising edge (R1), the 1st falling edge (F1), the 2nd rising edge (R2) and the 2nd falling edge (F2) of clock. Note that some operations such as ACTIVATE and MODE REGISTER WRITE require two commands to initiate.
NOTE 2	"V" means "H" or "L" (a defined logic level). "X" means don't care in which case CK_t, CK_c and CA[3:0] can be floated.
NOTE 3	Bank Group Address BG[0:1] and Bank Address BA[0:1] determine which bank is to be operated upon.
NOTE 4	An ACTIVATE-1 command must be followed by an ACTIVATE-2 command. Only CAS, WRITE, READ, PRECHARGE (to a different bank), REFRESH (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. The maximum timing gap (tAAD) between ACTIVATE-1 and ACTIVATE-2 commands are TBD clock cycles. An ACTIVATE-1 command must be issued first before issuing an ACTIVATE-2 command. Once an ACTIVATE-1 command is issued, an ACTIVATE-2 command must be issued before issuing another ACTIVATE-1 command.
NOTE 5	AB "HIGH" during PRECHARGE or REFRESH command indicates that command must be applied to all banks and bank address is a don't care.
NOTE 6	AP "HIGH" during WRITE or READ commands indicates that an auto-precharge will occur to the bank associated with the WRITE or READ command.
NOTE 7	CAS command is a standalone command which is required if WCK2CK SYNC ALWAYS ON (WS) or OFF (WS_OFF) or WCK2CK SYNC extension is applied to a target device. Refer to CAS command description for WS and WS_OFF operand's decoding.
NOTE 8	PD "HIGH" during SELF REFRESH ENTRY command indicates that both Self Refresh Entry and Power Down Entry will occur together.
NOTE 9	CS shall be compliant to Power Down Entry/Exit timing requirements. Refer to Power Down Function and Timing Description.
NOTE 10	WRITE (WR-S, WR-L), READ (RD-S, RD-L), MODE REGSITER READ (MRR), WRITE FIFO (WFF), READ FIFO (RFF) and READ DQ CALIBRATION (RDC) commands include a WCK2CK SYNC ON operand (WS) to initiate new WCK2CK SYNC operation.
NOTE 11	Bank Group Address dBG[0:1] and Bank Address BA[0:1] determine the 2nd target bank of Dual Bank Refresh operation.
NOTE 12	SC is an operand to select either Sub-Channel 0 (SC0) or Sub-Channel 1 (SC1) in case Efficiency Mode is enabled (MR0 OP[2]=1 <sub>B</sub> or MR1 OP[6]=1 <sub>B</sub> ). The following commands support a "SC" operand when the Efficiency Mode is enabled - Bank Active (ACT-1), Precharge (PRE), Refresh (RFM), Write (WR-S, WR-L), Read (RD-S, RD-L), and Mode Register Read (MRR).
NOTE 13	When Write command (WR-S, WR-L, WFF) is issued, CS for the non-target rank should be asserted "H" at R1 of command clock and de-asserted "L" at R2 to control NT-ODT setting. Write command (WR-S, WR-L, WFF) to the target rank is defined such that CS is asserted "H" during R1 and R2 to distinguish target and non-target ranks.
NOTE 14	Some Mode Registers in the secondary sub-channel can be read out from the primary sub-channel in case of Efficiency Mode enabled. Refer to Mode Register Read function description.
NOTE 15	Power Down Exit (PDX-NT) command to a Non-Target device is valid only when dynamic Write NT-ODT is enabled.
NOTE 16	When LPDDR6 System Meta Mode is enabled (MR92 OP[7]=1 <sub>B</sub> ), Meta-Write/Meta-Read commands can be distinguished from normal Write/Read commands by PAMM segment hit or miss in a target bank and associated column address (C[5:2]). Refer to 7.5.6 System Meeta Function Mode.
NOTE 17	In case CA Parity Check Mode is supported and enabled (MR2 OP[0]=1 <sub>B</sub> AND MR26 OP[2]=1 <sub>B</sub> ), a host generates a parity operand (PAR) based on the 1st and 2nd rising and falling edges of CA[3:0] signals, excluding the CA Parity bit. When CA Parity Mode is enabled, "X" (don't care) defined in the command truth table shall be replaced by "V" (a defined logic level) except for DES command since the defined logic level ("H" or "L") is required in the command input to compute the parity state.
NOTE 18	When the WCK SYNC Off extension feature is enabled (MR26 OP[3]=1 <sub>B</sub> ), if a CAS command (with "WSOE"=1 <sub>B</sub> ) is issued immediately after a Write (WR-S, WR-L) or Read (RD-S, RD-L) command without any nCK gap, the WCK sync-off timing is extended. This means that the WCK sync state is maintained until the next WR-S/L or RD-S/L command is issued. Refer to 7.3.6 WCK SYNC Off extension.
NOTE 19	BC "HIGH" during an MRW-1 command indicates a MRW operation can be broadcasted to both SC0 and SC1 sub-channels.

## 7.2 Every other Cycle Command Input

LPDDR6 command input must be started only on even edges of the CK\_t rising edges to optimize power consumption. Controller should label LPDDR6 CK\_t/CK\_c even and odd cycles by CK synchronization at CK toggle start period before issuing a valid command.

### 7.2.1 Command Input

LPDDR6 shall start command input at CK\_t rising edge and CS level is detected at only even CK\_t as command input start.

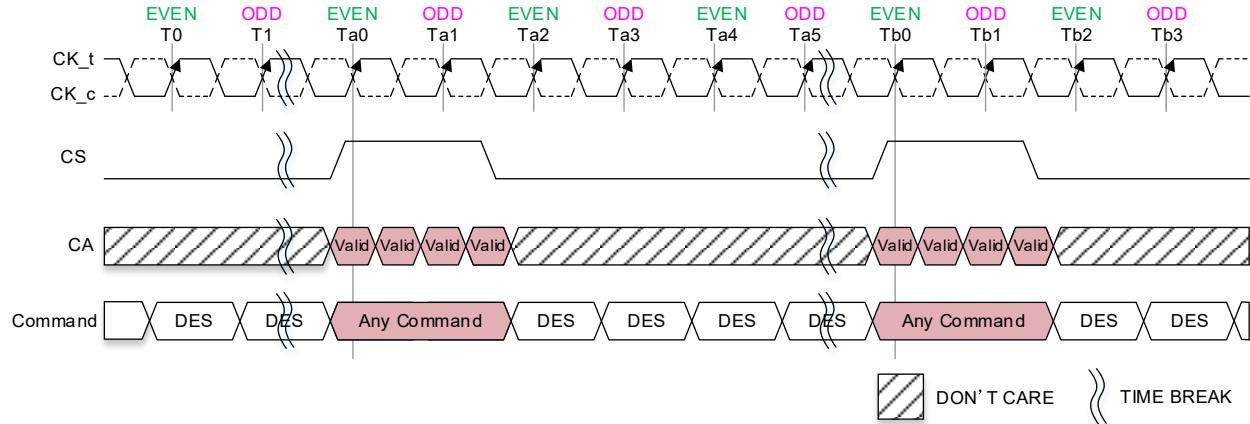


Figure 49 – Example of Every other Command Input

### 7.2.2 CK Sync and Sync Off Operation

#### 7.2.2.1 CK Sync Off Operation

LPDDR6 sync state is stopped by following conditions.

- Power down entry with dynamic Write NT-ODT disabled
- Reset
- FSP-OP switching including FSP-OP switching during CS Training and Command bus Training (CBT) too.
- MPC CK sync off

### 7.2.2.2 CK Sync Operation

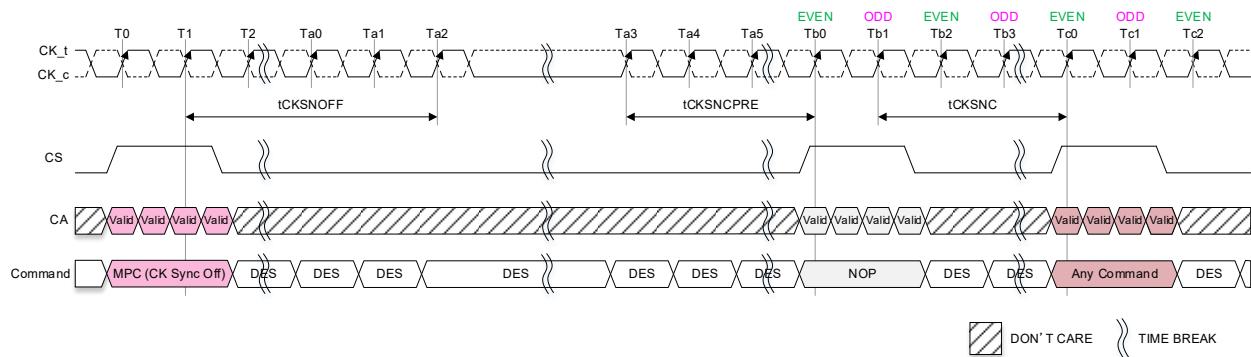
CK sync operation is started by issuing a NOP command when CK is in non-sync state. It is prohibited to issue any command except DES prior to issuing the NOP command for CK sync when CK is not in a sync state.

Timing for Clock Sync stop by MPC command and Clock sync start by NOP command is shown in NOTE 1 Before clock stop, MPC CK off has to be issued.

NOTE 2 MPC (CK Sync Off) command is included Any Command.

NOTE 3 In tCKSNC period, the DES command is only allowed.

Figure 50 and Figure 51.



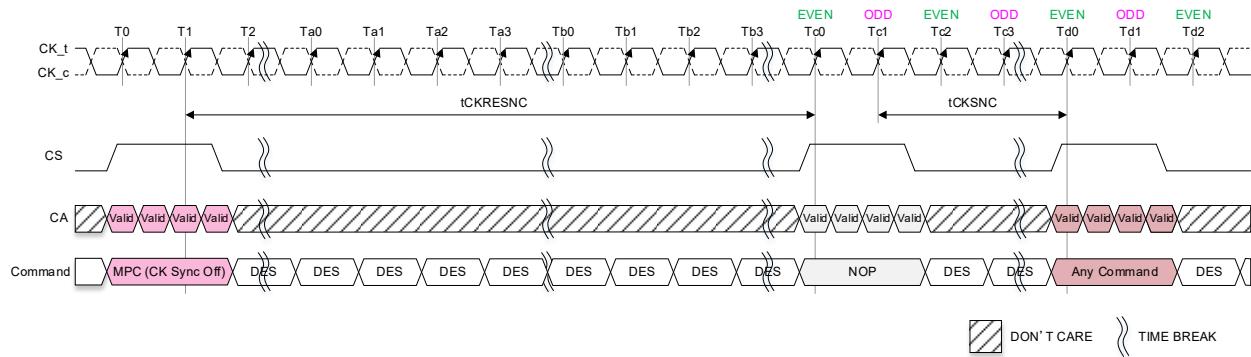
NOTE 1 Before clock stop, MPC CK off has to be issued.

NOTE 2 MPC (CK Sync Off) command is included Any Command.

NOTE 3 In tCKSNC period, the DES command is only allowed.

**Figure 50 – Clock Sync Stop/Start Timing**

### 7.2.2.2 CK Sync Operation (cont'd)



NOTE 1 The clock never stops or changes from T1 to Td0.

NOTE 2 MPC (CK Sync Off) command is included Any Command.

NOTE 3 In tCKSNC period, the DES command is only allowed.

**Figure 51 – Clock Sync Stop/Start Timing without Clock Stop/Frequency Change**

**Table 255 – Clock Sync Stop/Start AC Parameters**

Parameter	Symbol	Min/Max	Value	Unit	Note
CK sync pre toggle	tCKSNCPRE	Min	Max(7ns, 4nCK)	ns	
CK sync period	tCKSNC	Min	1 + EVEN(3ns/tCK)	nCK	1
CK sync off	tCKSNOFF	Min	4nCK	ns	
CK Re-sync	tCKRESNC	Min	Max(8ns, 8nCK)	ns	
NOTE 1 The EVEN function rounds numbers up to the next even integer. For example, EVEN(3ns/1.25ns)=EVEN(2.4)=4.					

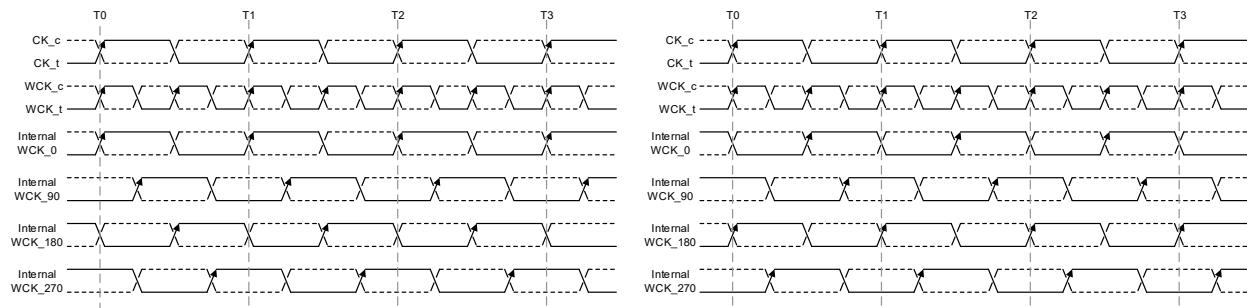
Refer to Power-up, Reset, Power Down, Frequency Set Point (FSP), CS Training and CBT Training section for Clock Sync procedure after Power-up, Reset, Power Down, Frequency Set Point (FSP), CS Training, and CBT Training.

## 7.3 WCK Operation

### 7.3.1 WCK2CK Synchronization Operation

#### 7.3.1.1 WCK2CK Synchronization

An LPDDR6 SDRAM utilizes two types of clocks with different frequencies. The frequency of the Write Clock (WCK) is twice the Command Clock (CK), which requires LPDDR6 SDRAM to have clock divider in the WCK clock tree. However, the WCK divider's initial state is unpredictable and results in two different states in an LPDDR6 SDRAM: aligned with CK state and misaligned with CK state. Figure 52 illustrates these two cases.



**Figure 52 — Aligned WCK to CK (Left) and Misaligned WCK to CK (Right)**

LPDDR6 SDRAM is required to be in the “aligned WCK to CK state” prior to data output/input from/to DQs, such as Read, Write operation.

The aligned WCK to CK state which called "WCK2CK sync" is realized by operation that is defined as WCK2CK Synchronization.

Issuing WCK2CK synchronization command which operand: WS=1 is prohibited during WCK2CK sync state.

#### 7.3.1.2 WCK2CK Synchronization Mode

LPDDR6 SDRAM has two WCK2CK Synchronization Modes.

One is Auto-sync off mode and the other is Write Clock Always on mode (WCK Always on mode).

When Auto-sync off mode, WCK2CK sync is expired at Sync off timing which is defined WCK2CK SYNC Off Timing Definition.

On the other hand, LPDDR6 SDRAM is maintaining on WCK2CK sync until SDRAM receives CAS(WS\_OFF), Power Down, Self-Refresh Power-Down mode commands or reset, when WCK Always on mode.

These modes can be selected by MR22 OP[5] and WCK2CK sync off state is required to be when changing WCK2CK Synchronization Mode from Auto Sync off mode to WCK Always On Mode and vice versa by MR22 OP[5].

#### 7.3.2 WCK2CK Training

WCK2CK Training is required to be performed prior to WCK2CK Synchronization. Refer to WCK2CK leveling section for detail.

### 7.3.3 Auto-Sync Off Mode

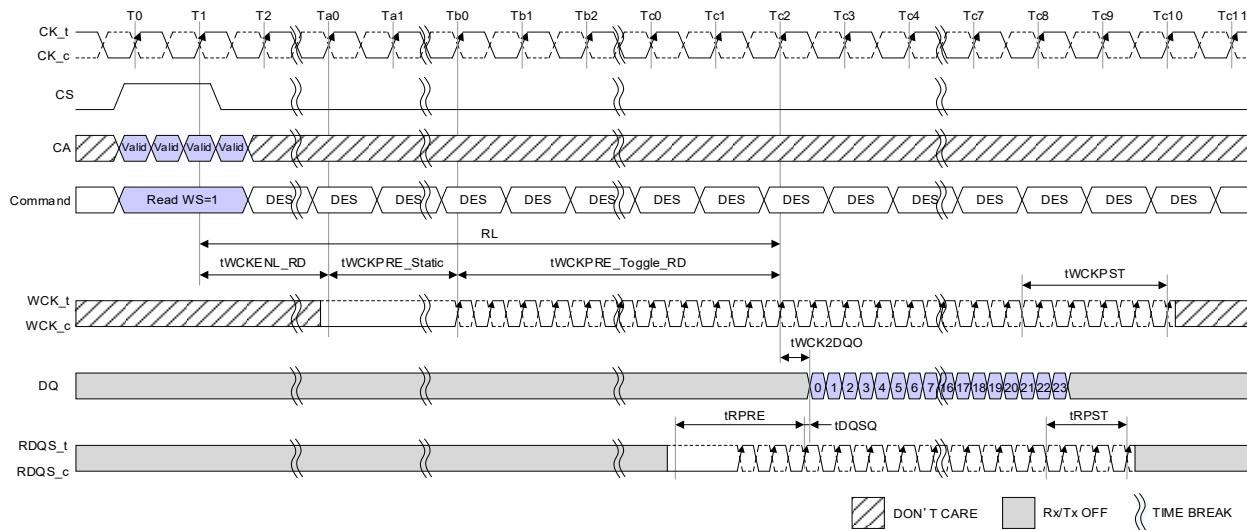
The LPDDR6 WCK2CK Synchronization process is initiated by the command, which is Read, Write, Mode Register Read (MRR), Write FIFO (WFF), Read FIFO (RFF), or Read DQ Calibration (RDC) command by doing their WS bit is enabled. Refer to Command Truth Table: Table 254 for detail for Read, Write, MRR, WFF, RFF, and RDC commands with WCK2CK Synchronization operand (WS). These command with "1" at WCK2CK Synchronization flag operand (WS) will be started SDRAM WCK2CK Synchronization procedure.

#### 7.3.3.1 Read with WCK2CK Synchronization

Following figures show the LPDDR6 WCK2CK Sync operation by Read command with WCK2CK Sync operand is enabled: Read (WS=1).

SDRAM controller is required to start to drive WCK as  $WCK_t/WCK_c=L/H$  before  $tWCKENL\_RD$  is satisfied. The WCK2CK Sync operation occurs after  $tWCKENL\_RD + tWCKPRE\_static$ . The SDRAM requires the proper WCK toggle pattern prior to insure WCK2CK sync properly. After the WCK2CK Sync is completed, the WCK is required to continue to toggle until  $tWCKPST$  is satisfied.

This WCK2CK synchronization timing applies MRR, RFF, and RDC commands too.

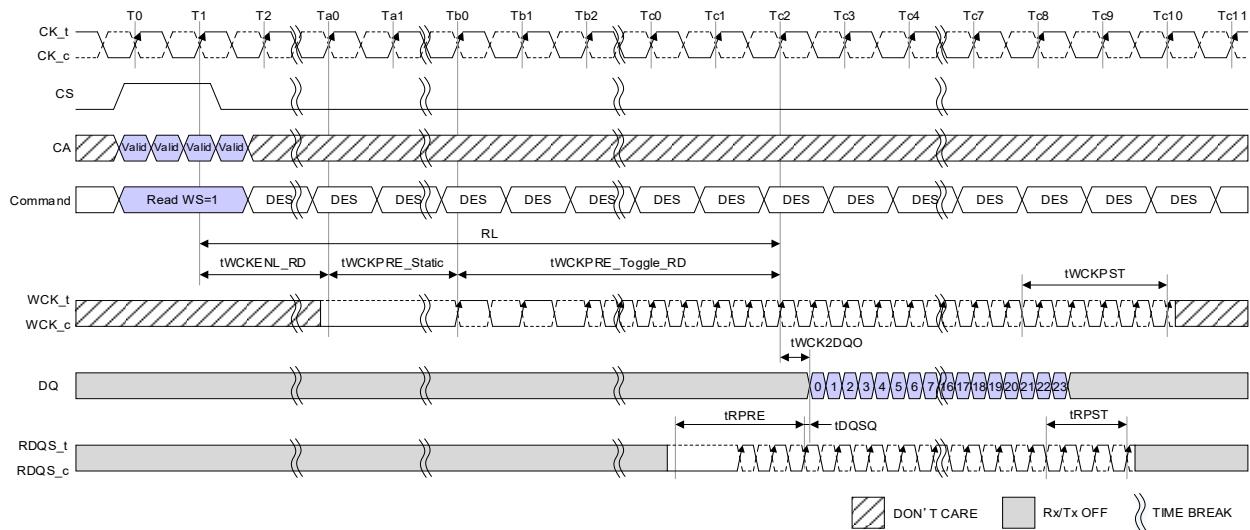


NOTE 1  $tWCK2CK$  is 0 ps in this instance.

NOTE 2  $BL=24$ ,  $tRPRE=4tWCK$  (Static=2tWCK, Toggle=2tWCK),  $tRPST=2.5tWCK$ (Toggle),  $tWCKPST=4.5tWCK$

**Figure 53 — WCK2CK Sync Operation by Read Command with WS Operand is Enabled: without Half Toggle for tWCKPRE \_toggle\_RD**

### 7.3.3.1 Read with WCK2CK Synchronization (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

**Figure 54 – WCK2CK Sync Operation by Read Command with WS Operand is Enabled:  
with Half Toggle for tWCKPRE \_toggle\_RD**

**Table 256 – WCK2CK Sync AC Parameters for Read, MRR, RFF, and RDC Operation**  
**Read Link Protection is Disabled and DVFSL is Disabled**

### 7.3.3.1 Read with WCK2CK Synchronization (cont'd)

**Table 257 – WCK2CK Sync AC Parameters for Read, MRR, RFF and RDC Operation  
Read Link Protection is Enabled and DVFSL is Disabled**

Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]								
Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	READ Latency		tWCKENL_RD			tWCKPRE_static	tWCKPRE_toggle_RD		tWCKPRE_total_RD
				Set 0	Set 1	Set 0	Set 1	Set 1		Half	Full	
80	1067	20	267	7	8	0	1	2	2	0	5	7
1067	1600	267	400	11	11	4	4	2	0	5	7	
1600	2133	400	533	14	15	6	7	2	0	6	8	
2133	2750	533	688	17	19	7	9	3	0	7	10	
2750	3200	688	800	20	22	10	12	3	0	7	10	
3200	3750	800	938	23	25	12	14	4	0	7	11	
3750	4267	938	1067	26	28	13	15	4	0	9	13	
4267	4800	1067	1200	29	32	15	18	5	0	9	14	
4800	5500	1200	1375	33	36	18	21	6	0	9	15	
5500	6400	1375	1600	39	42	22	25	6	2	9	17	
6400	7500	1600	1875	46	50	27	31	7	2	10	19	
7500	8533	1875	2133	52	56	32	36	8	2	10	20	
8533	9600	2133	2400	58	64	35	41	9	2	12	23	
9600	10667	2400	2667	64	70	40	46	10	2	12	24	
10667	11733	2667	2933	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
11733	12800	2933	3200	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
12800	14400	3200	3600	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

**Table 258 – WCK2CK Sync AC Parameters for Read, MRR, RFF, and RDC Operation  
Read Link Protection is Disabled and DVFSL is Enabled**

Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]									
Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	READ Latency			tWCKENL_RD			tWCKPRE_static	tWCKPRE_toggle_RD		tWCKPRE_total_RD
				Set 0	Set 1	Set 2	Set 0	Set 1	Set 2		Half	Full	
80	1067	20	267	7	8	9	0	1	2	2	0	5	7
1067	1600	267	400	10	11	12	3	4	5	2	0	5	7
1600	2133	400	533	14	15	16	6	7	8	2	0	6	8
2133	2750	533	688	17	19	21	7	9	11	3	0	7	10
2750	3200	688	800	20	22	24	10	12	14	3	0	7	10

**Table 259 – WCK2CK Sync AC Parameters for Read, MRR, RFF, and RDC Operation  
Read Link Protection is Enabled and DVFSL is Enabled**

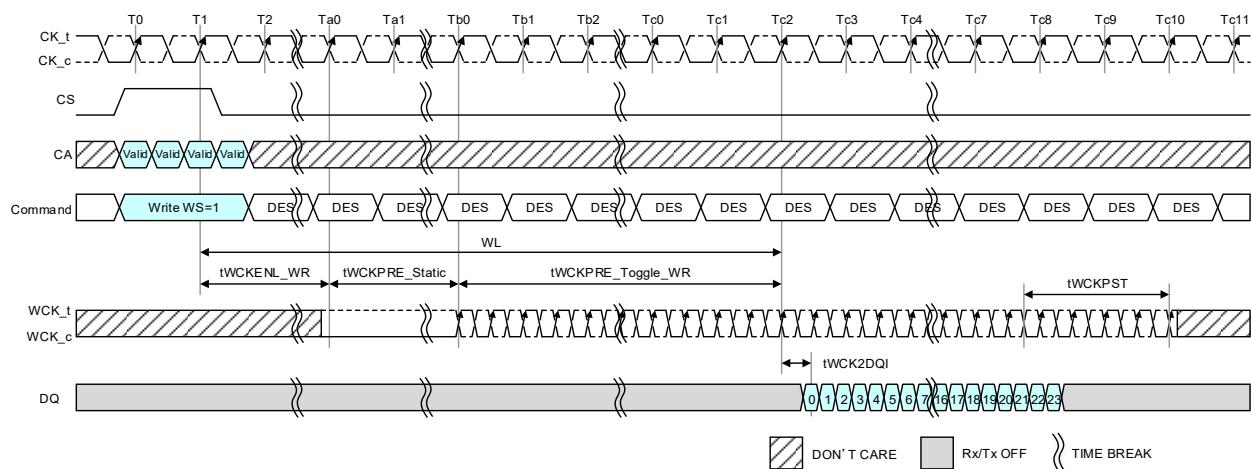
Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync READ AC Parameters [nCK]								
Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	READ Latency		tWCKENL_RD			tWCKPRE_static	tWCKPRE_toggle_RD		tWCKPRE_total_RD
				Set 0	Set 1	Set 0	Set 1	Set 1		Half	Full	
80	1067	20	267	8	9	1	2	2	2	0	5	7
1067	1600	267	400	12	13	5	6	2	0	5	7	
1600	2133	400	533	15	17	7	9	2	0	6	8	
2133	2750	533	688	19	21	9	11	3	0	7	10	
2750	3200	688	800	22	24	12	14	3	0	7	10	

### 7.3.3.2 Write with WCK2CK Synchronization

Following figures show the LPDDR6 WCK2CK Sync operation by Write command with WCK2CK Sync operand is enabled: Write (WS=1).

SDRAM controller is required to start to drive WCK as WCK\_t/WCK\_c=L/H before tWCKENL\_WR is satisfied. The WCK2CK Sync operation occurs after WCKENL\_WR + tWCKPRE\_Static. The SDRAM requires the proper WCK toggle pattern prior to insure WCK2CK sync properly. After the WCK2CK Sync is completed, the WCK is required to continue to toggle until satisfying tWCKPST is satisfied.

This WCK2CK synchronization timing applies to WFF command too.

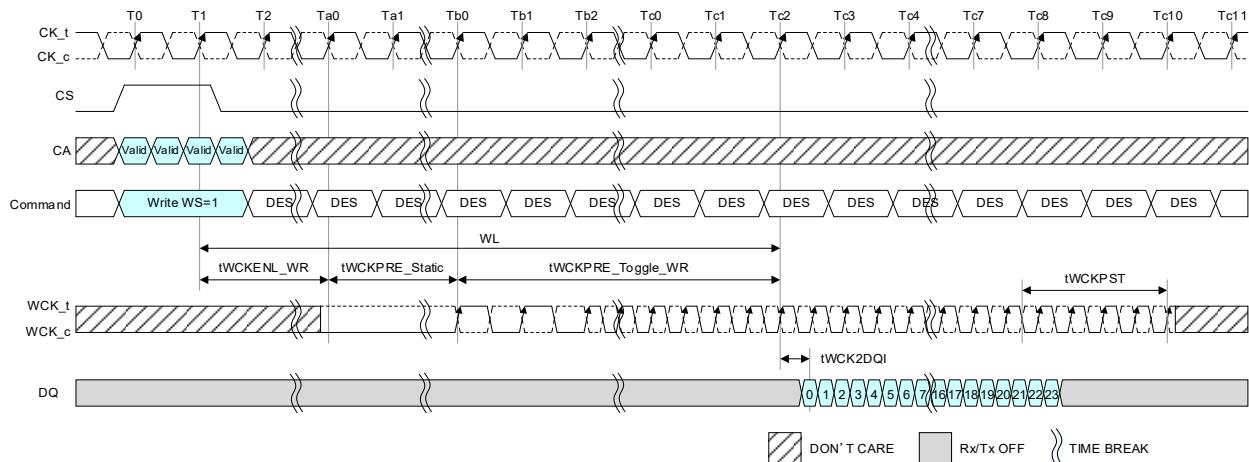


NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tWCKPST=4.5tWCK

**Figure 55 – WCK2CK Sync Operation by Write Command with WS Operand is Enabled: without Half Toggle for tWCKPRE\_toggle\_WR**

### 7.3.3.2 Write with WCK2CK Synchronization (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tWCKPST=4.5tWCK

**Figure 56 – WCK2CK Sync Operation by Write Command with WS Operand is Enabled:  
with Half Toggle for tWCKPRE toggle WR**

**Table 260 – WCK2CK Sync AC Parameters for Write and WFF Operation**

### 7.3.3.3 CAS with WCK2CK Synchronization

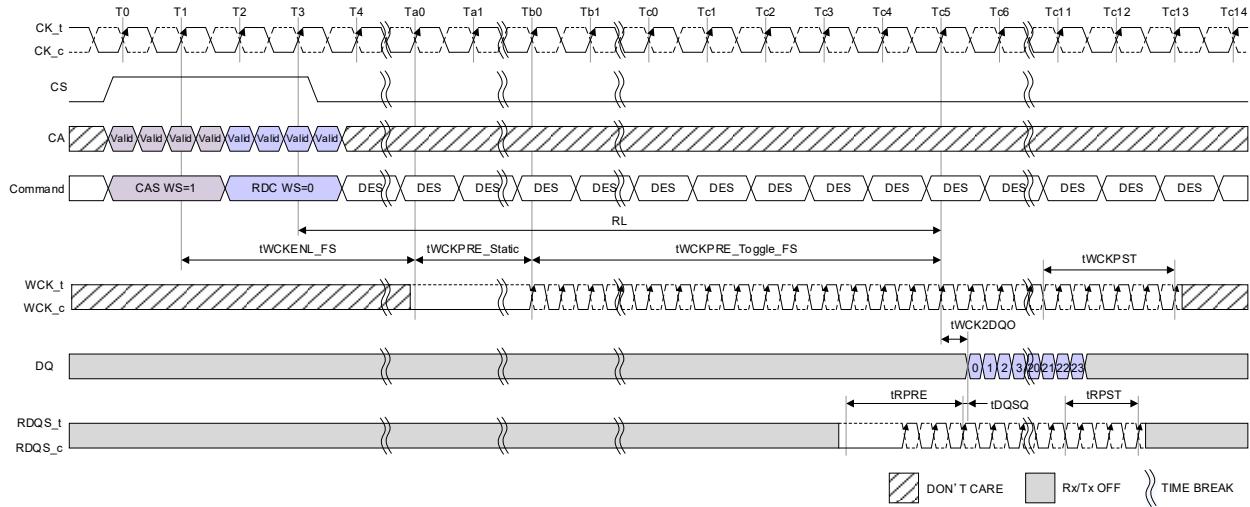
Following figures show the LPDDR6 WCK2CK Sync operation by CAS command with WCK2CK Sync operand (WS) is enabled.

SDRAM controller is required to start to drive WCK as WCK\_t/WCK\_c=L/H before tWCKENL\_FS is satisfied. The WCK2CK Sync operation occurs after WCKENL\_FS + tWCKPRE\_static. The SDRAM requires the proper WCK toggle pattern prior to insure WCK2CK sync properly. After the WCK2CK Sync is completed, the WCK is required to continue to toggle until satisfying tWCKPST is satisfied.

The WCK2CK Sync operation is performed with minimum latency, tWCKENL\_FS, when a CAS command with WS=1 is issued to an LPDDR6 SDRAM. By this way, the LPDDR6 SDRAM controller can put LPDDR6 SDRAM into WCK2CK Synchronized state as early as possible. CAS(WS=1) is used as a standalone command unlike Write (WS=1), Read (WS=1), MRR(WS=1), RDC(WS=1), WFF(WS=1), RFF(WS=1) and can be issued to not only one rank but also multi-ranks simultaneously. tWCKPRE\_toggle\_FS is varied by what is issued the command after issuing CAS(WS=1) command.

After CAS (WS =1) command is issued, not only Read, Write, RDC, WFF, RFF and MRR commands but also other commands like Active and Refresh can be issued. Refer to clause 8.5 CAS Command Timing Constraints.

### 7.3.3.3 CAS with WCK2CK Synchronization (cont'd)

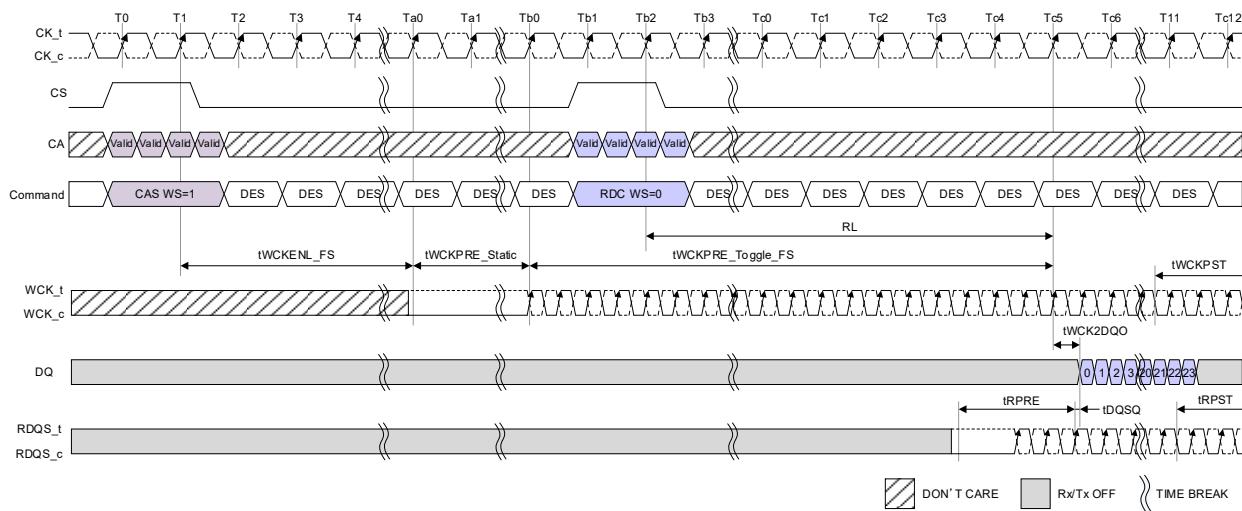


NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle),  
tWCKPST=4.5tWCK

NOTE 3 RDC can be replaced to Read (WS=0), Write (WS=0), WFF(WS=0), RFF(WS=0) and MRR(WS=0).

**Figure 57 – WCK2CK Sync Operation by CAS Command with WS Operand is Enabled without Command Gap**



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle),  
tWCKPST=4.5tWCK

NOTE 3 RDC can be replaced to Read (WS=0), Write (WS=0), WFF(WS=0), RFF(WS=0) and MRR(WS=0).

**Figure 58 – WCK2CK Sync Operation by CAS Command with WS Operand is Enabled with Command Gap**

### 7.3.3.3 CAS with WCK2CK Synchronization (cont'd)

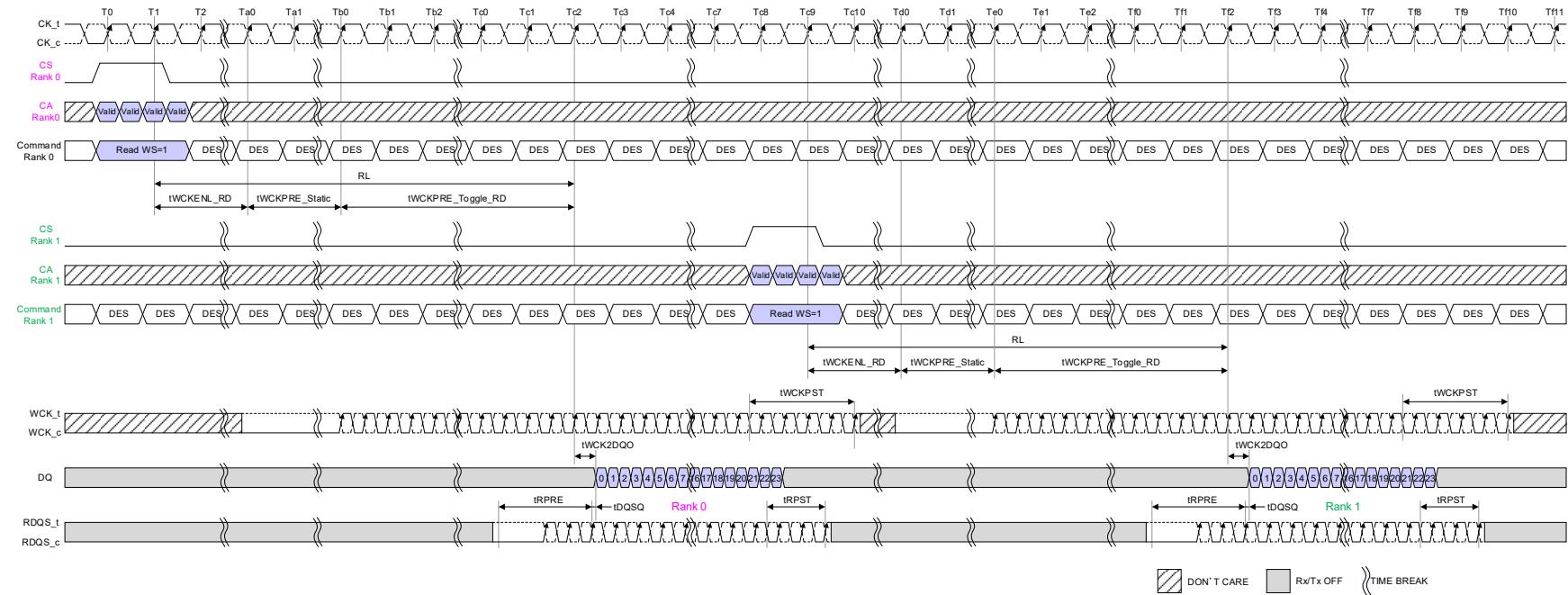
**Table 261 – WCK2CK Sync AC Parameters for CAS Operation**

Data Rate Range [Mbps]		CK Frequency Range [MHz]		WCK2CK Sync CAS WS AC Parameters		
Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	Read Latency: MR1 OP[4:0] Setting	tWCKENL_FS [nCK]	tWCKPRE _Static [nCK]
80	1067	20	267	00000 <sub>B</sub>	0	2
1067	1600	267	400	00001 <sub>B</sub>	2	2
1600	2133	400	533	00010 <sub>B</sub>	2	2
2133	2750	533	688	00011 <sub>B</sub>	4	3
2750	3200	688	800	00100 <sub>B</sub>	6	3
3200	3750	800	938	00101 <sub>B</sub>	7	4
3750	4267	938	1067	00110 <sub>B</sub>	7	4
4267	4800	1067	1200	00111 <sub>B</sub>	8	5
4800	5500	1200	1375	01000 <sub>B</sub>	9	6
5500	6400	1375	1600	01001 <sub>B</sub>	9	6
6400	7500	1600	1875	01010 <sub>B</sub>	9	7
7500	8533	1875	2133	01011 <sub>B</sub>	10	8
8533	9600	2133	2400	01100 <sub>B</sub>	11	9
9600	10667	2400	2667	01101 <sub>B</sub>	12	10
10667	11733	2667	2933	01110 <sub>B</sub>	TBD	TBD
11733	12800	2933	3200	01111 <sub>B</sub>	TBD	TBD
12800	14400	3200	3600	10000 <sub>B</sub>	TBD	TBD

NOTE 1 The need for half toggle for tWCKPRE\_toggle\_FS, refer to Table 256 or Table 260.

### 7.3.3.4 Rank to rank WCK2CK Sync Operation

There are two different methods to control WCK2CK Sync state of two rank LPDDR6 SDRAM. The first method is to start WCK2CK Sync process of rank 1 after completing DQ data burst of rank 0 as shown in Figure 59. In this case, tWCKPST of rank 0 and tWCKPRE of rank 1 should be guaranteed for right RDQS post-amble of read operation of rank 0 and for right WCK2CK Synchronization operation of rank 1, respectively.



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

**Figure 59 – Minimum Gap Rank to Rank Read Operation with WCK2CK Sync after Completing DQ Burst in One Rank**

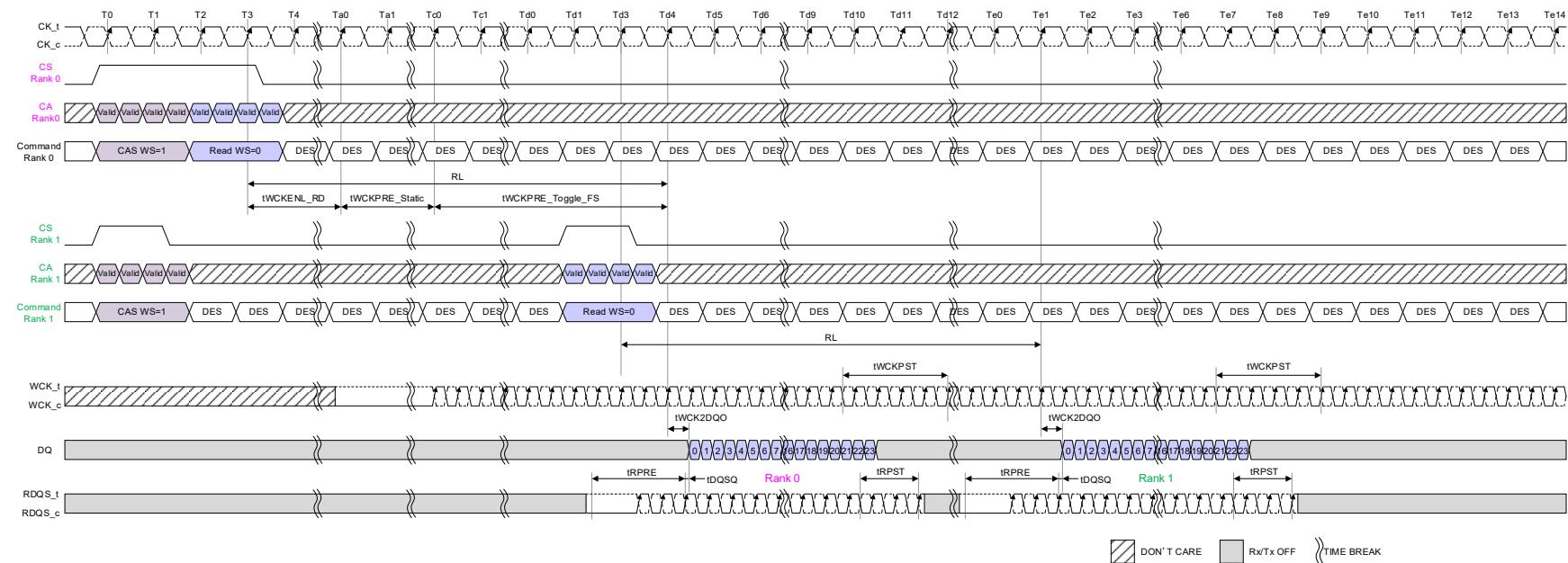
The second method is to start WCK2CK Sync process of both ranks simultaneously as shown in Figure 60. When both ranks are not in WCK2CK synchronized state and DQ bursts between two ranks are closed, a simultaneous CAS command with WS=1 is the recommended way, considering efficient DQ bus utilization.

If using this method, WCK always ON mode is enabled is recommended: MR22 OP[5]=1<sub>B</sub>. If not, WCK2CK synchronization is expired according to WCK2CK SYNC Off Timing Definition.

#### 7.3.3.4 Rank to rank WCK2CK Sync Operation (cont'd)

The WCK2CK synchronization can be stopped by CAS(WS\_OFF=1) command regardless of WCK always ON mode setting: MR22 OP[5].

If the following DQ bursts of one rank are far from the preceding ones of the other rank, extra power consumption due to WCK toggle should be considered. After synchronizing both ranks, if rank 0 is not used, CAS(WS\_OFF) command can be issued to rank 0 to save power.



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

**Figure 60 – Simultaneous WCK2CK Sync Process for Multi-ranks (especially Two Ranks): WCK always Run Mode is Enabled**

### 7.3.3.5 WCK2CK SYNC Off Timing Definition

WCK2CK Sync off timing is as follows.

Issuing CAS(WS\_OFF=1) command is not allowed during this Read/Write sync off timing period.

Operation	Sync Off Timing	Notes
Read	RL + BL/n_min + RD(tWCKPST/tCK)	1
Write	WL + BL/n_min + RD(tWCKPST/tCK)	2
NOTE 1 This Sync off timing also applies MRR, RDC and RFF operation.		
NOTE 2 This Sync off timing also applies WFF operation.		

### 7.3.4 Write Clock Always On Mode (WCK Always On Mode)

LPDDR6 SDRAM can choose WCK Always on mode (MR22 OP[5]=1<sub>B</sub>).

The LPDDR6 WCK2CK Synchronization process in WCK Always on mode may only be initiated by CAS(WS=1) command. In other words, in WCK Always on mode, using Write(WS=1), Read(WS=1), MRR(WS=1), RDC(WS=1), WFF(WS=1), or RFF(WS=1) is prohibited.

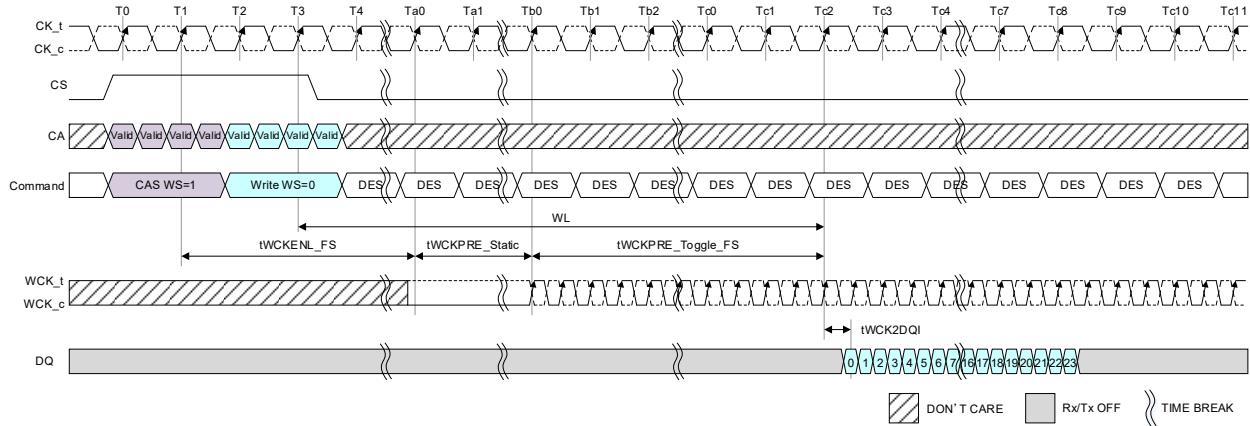
If WCK Always on mode is enabled by setting MR22 OP[5]=1<sub>B</sub>. The WCK buffer in an LPDDR6 SDRAM is turned on with WCK2CK synchronization and keeps being turned on until SDRAM receives CAS(WS\_OFF), Power Down, Self-Refresh Power-Down commands or reset.

Therefore, the SDRAM controller is required to keep WCK toggling at its full rate after WCK2CK synchronization regardless of DQ operation. As the WCK2CK synchronization information is lost with power down entry, the SDRAM controller is required to perform a WCK2CK synchronization sequence after power down exit before DQ operation. Note that WCK2CK sync conditions are the same as entering Self-Refresh PowerDown mode.

Figure 61 illustrates WCK Always on mode with WCK2CK synchronization followed by a write command. In this timing diagram, At T0, SDRAM is in Bank Active and WCK2CK Sync off state. Therefore, the WCK buffer in SDRAM is off state and has lost the WCK2CK synchronization information. Although, the WCK Always on mode: MR22 OP[5]=1<sub>B</sub>, the WCK buffer is not turned on until receiving a CAS (WS=1) command. At T0, a CAS (WS=1) command initiates WCK2CK synchronization process and turns on the WCK buffer in SDRAM.

The timing diagram of WCK Always on mode starting with WCK2CK synchronization followed by a Read (WS=0) command is shown in Figure 63.

### 7.3.4 Write Clock Always On Mode (WCK Always On Mode) (cont'd)

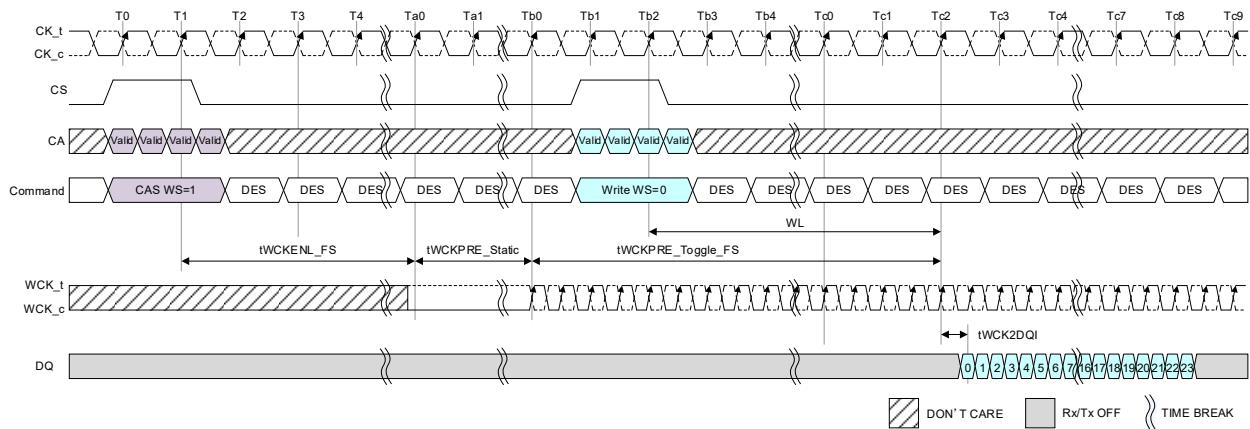


NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24

NOTE 3 Write (WS=0) can be replaced to WFF.

**Figure 61 – WCK Always On Mode Starting with WCK2CK-Sync Operation followed by a Write (WS=0) Command without Command Gap**



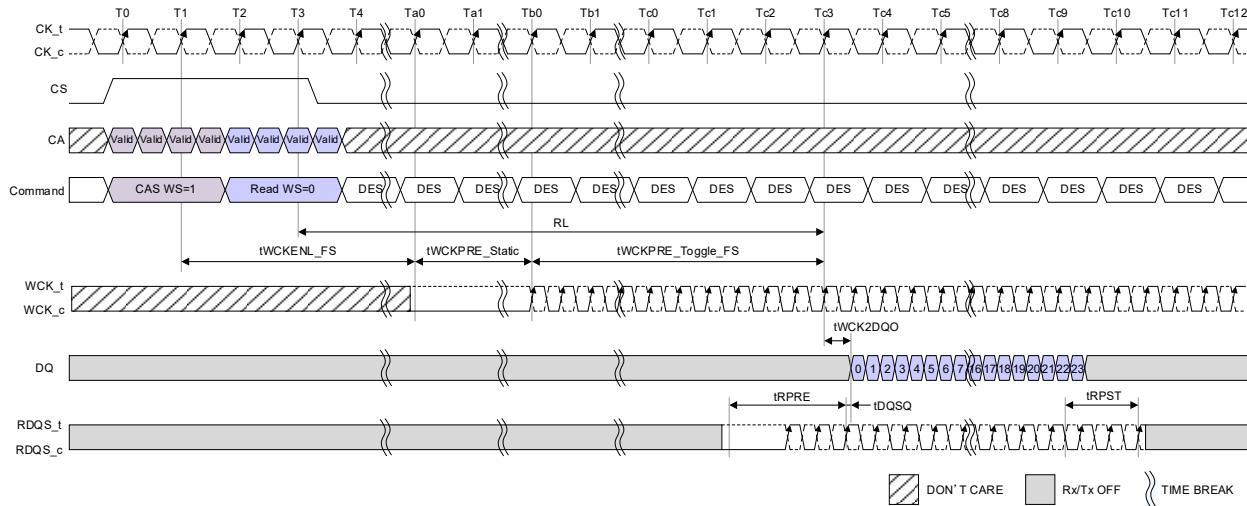
NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24

NOTE 3 Write (WS=0) can be replaced to WFF.

**Figure 62 – WCK Always On Mode Starting with WCK2CK-Sync Operation followed by a Write (WS=0) Command with Command Gap**

### 7.3.4 Write Clock Always On Mode (WCK Always On Mode) (cont'd)

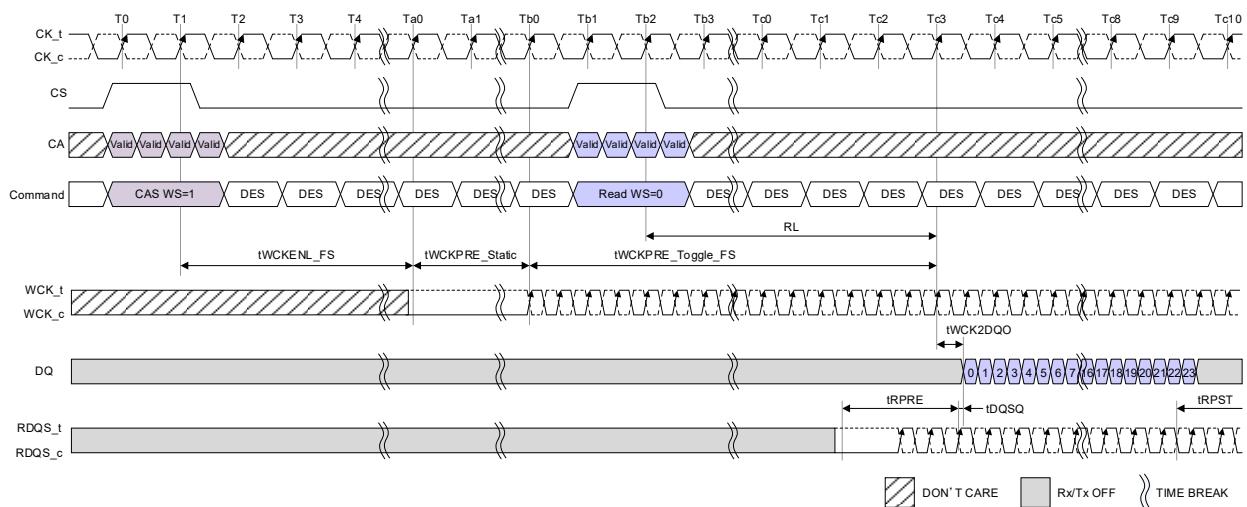


NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

NOTE 3 Read (WS=0) can be replaced to RDC, RFF and MRR.

**Figure 63 – WCK Always On Mode Starting with WCK2CK-Sync Operation followed by a Read (WS=0) Command without Command Gap**



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 BL=24, tRPRE=4tWCK (Static=2tWCK, Toggle=2tWCK), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

NOTE 3 Read (WS=0) can be replaced with RDC, RFF and MRR.

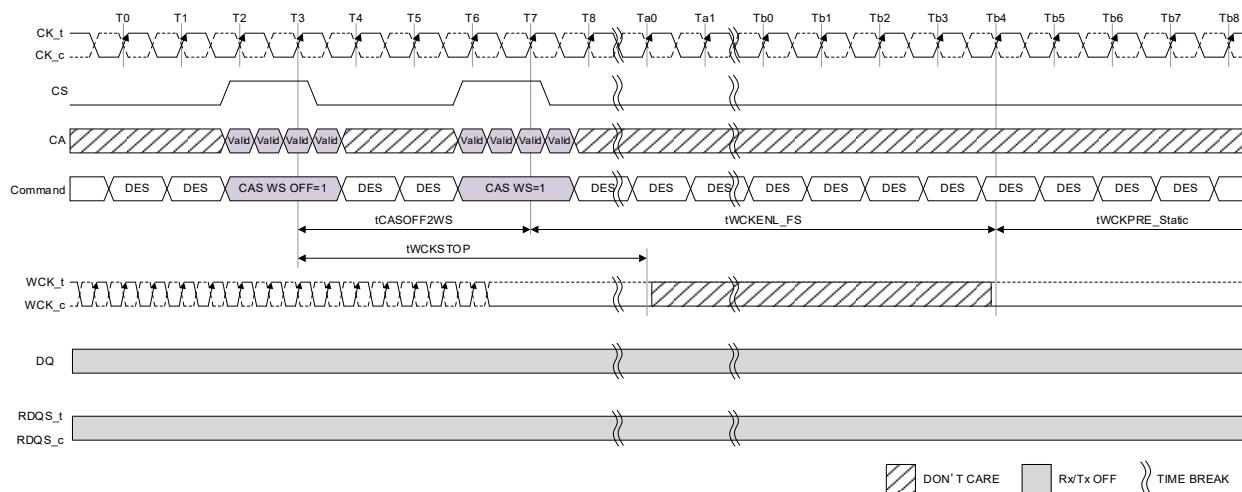
**Figure 64 – WCK Always On Mode Starting with WCK2CK-Sync Operation followed by a Read (WS=0) Command with Command Gap**

### 7.3.4.1 Sync-off Command: CAS(WS\_OFF=1)

In WCK2CK sync state, SDRAM controller can turn off WCK buffer in SDRAM by sending a CAS(WS\_OFF) command which operand: WS\_OFF=1 to save memory system power. SDRAM turns off WCK buffer asynchronously after receiving CAS(WS\_OFF) command. After WCK buffer off, a new WCK2CK synchronization sequence is required prior to DQ operation.

CAS(WS\_OFF) command is allowed only when there is no on-going write, read or other DQ operation in the SDRAM. Specifically, CAS(WS\_OFF) command is not allowed to issue during Read/Write sync off timing period. See section 7.3.3.5 WCK2CK SYNC Off Timing Definition for detail.

The delay time from commands required WCK2CK Sync to CAS(WS\_OFF) is defined CAS Command Timing Constraints table.



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK\_t/c can be a static level after 2nCK from CAS(WS\_OFF) command.

**Figure 65 – CAS(WS\_OFF) Timing: in case of tWCKSTOP and tWCKENL\_FS Overlap**

**Table 262 – WCK Stop AC Timing**

Parameter	Symbol	Min/ Max	Value	Unit	Notes
Valid Write Clock Requirement after CAS(WS_OFF) Command	tWCKSTOP	Min	Max(2nCK, 6ns)	-	
Delay time from CAS OFF command to CAS WS command	tCASOFF2WS	Min	4	nCK	

### 7.3.5 WCK2CK SYNC Off Timing Definition

The next commands which require WCK2CK SYNC can be issued up to the maximum timing defined as the following tables. Once the maximum timing is exceeded, Write/Read/MRR command with a WCK2CK SYNC operand (WS="H") is required. Continuous WCK input should maintain at least to meet the following minimum WCK toggling cycles in a WCK domain.

- WL + BL/n\_min + RD(tWCKPST/tCK)
- RL + BL/n\_min + RD(tWCKPST/tCK)

**Table 263 – WCK2CK SYNC Off Timing Definition for WR, RD, and MRR**

Current Command	Next Command	Bank Relationship	Command Timing Constraints w/o a new WCK2CK SYNC Start		Command Timing Constraints with a new WCK2CK SYNC Start (WS="H")	Note
			Min	Max		
WRITE (WR-S, WR-L)	WRITE (WR-S, WR-L)	Any Banks	BL/n	WL + BL/n_min + RD(tWCKPST/tCK)	WL + BL/n_min + RD(tWCKPST/tCK) +1	1
	META WRITE(WR-M)	Any Banks	BL/n	-		1, 6, 7
	READ (RD-S, RD-L)	Same or Different Banks in Same BG	Not Allowed	Not Allowed	WL + BL/n_max+ RU(tWTR_L/tCK)	1
		Different Banks in Different BG	Not Allowed	Not Allowed	WL + BL/n_min + RU(tWTR_S/tCK)	1
	META READ (RD-M)	Same or Different Banks in Same BG	WL + BL/n_max+ RU(tWTR_L/tCK)	-	WL + BL/n_max+ RU(tWTR_L/tCK)	1, 6, 7
		Different Banks in Different BG	WL + BL/n_min + RU(tWTR_S/tCK)	-	WL + BL/n_min + RU(tWTR_S/tCK)	1, 6, 7
	MRR	-	Not Allowed	Not Allowed	WL + BL/n_max+ RU(tWTR_L/tCK)	1
META WRITE (WR-M)	WRITE (WR-S, WR-L)	Any Banks	BL/n	WL + BL/n_min + RD(tWCKPST/tCK)	WL + BL/n_min + RD(tWCKPST/tCK) +1	1
	META WRITE(WR-M)	Any Banks	BL/n	-		1, 6, 7
	READ (RD-S, RD-L)	Same or Different Banks in Same BG	Not Allowed	Not Allowed	WL + BL/n_max+ RU(tWTR_L/tCK)	1
		Different Banks in Different BG	Not Allowed	Not Allowed	WL + BL/n_min + RU(tWTR_S/tCK)	1
	META READ (RD-M)	Same or Different Banks in Same BG	WL + BL/n_max+ RU(tWTR_L/tCK)	-	WL + BL/n_max+ RU(tWTR_L/tCK)	6, 7
		Different Banks in Different BG	WL + BL/n_min + RU(tWTR_S/tCK)	-	WL + BL/n_min + RU(tWTR_S/tCK)	6, 7
	MRR	-	Not Allowed	Not Allowed	WL + BL/n_max+ RU(tWTR_L/tCK)	1

**Table 263 - WCK2CK SYNC Off Timing Definition for WR, RD, and MRR (cont'd)**

Current Command	Next Command	Bank Relationship	Command Timing Constraints w/o a new WCK2CK SYNC Start		Command Timing Constraints with a new WCK2CK SYNC Start (WS="H")	Note	
			Min	Max			
READ (RD-S, RD-L)	WRITE (WR-S, WR-L)	Same or Different Banks in Same BG	tRTW	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1, 2	
		Different Banks in Different BG	tRTW			1, 2	
	META WRITE(WR-M)	Same or Different Banks in Same BG	RL + BL/n_max - WL	-		1, 6, 7	
		Different Banks in Different BG	RL + BL/n_min - WL	-		1, 6, 7	
	READ (RD-S, RD-L)	Any Banks	BL/n	RL + BL/n_min + RD(tWCKPST/tCK)		1	
	META READ (RD-M)	Any Banks	BL/n			1, 6, 7	
META READ (RD-M)	MRR	-	Not Allowed	Not Allowed	RL + BL/n_max + RD(tWCKPST/tCK) +1	1	
	WRITE (WR-S, WR-L)	Same or Different Banks in Same BG	RL + BL/n_max - WL	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1	
		Different Banks in Different BG	RL + BL/n_min - WL			1	
	META WRITE(WR-M)	Same or Different Banks in Same BG	RL + BL/n_max - WL	-		1, 6, 7	
		Different Banks in Different BG	RL + BL/n_min - WL	-		1, 6, 7	
	READ (RD-S, RD-L)	Any Banks	BL/n	RL + BL/n_min + RD(tWCKPST/tCK)		1	
MRR	META READ (RD-M)	Any Banks	BL/n			1, 6, 7	
	MRR	-	Not Allowed	Not Allowed	RL + BL/n_max + RD(tWCKPST/tCK) +1	1	
MRR	WRITE (WR-S, WR-L)	-	tRTW +2	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1, 3	
	META WRITE(WR-M)	-	tRTW +2	-		1, 6, 7	
	READ (RD-S, RD-L)	-	Not Allowed	Not Allowed	RL + BL/n_max + RD(tWCKPST/tCK) +1	1	
	META READ (RD-M)	-	Not Allowed	Not Allowed		1, 6, 7	
	MRR	-	tMRR	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1	

**Table 263 - WCK2CK SYNC Off Timing Definition for WR, RD, and MRR (cont'd)**

- |        |   |
|--------|---|
| NOTE 1 | Even nCK round-up is required for any command-to-command timing constraints.  |
| NOTE 2 | Another WCK2CK SYNC start (WS="H") command cannot be executed while the WCK2CK SYNC status is ON.   |
| NOTE 3 | WCK2CK SYNC shall be initiated before or when issuing the current command.  |
| NOTE 4 | In case the min timing exceeds the max timing with given RL, WL and tWCKDQO, the next command shall be issued with a new WCK2CK SYNC start (WS="H").  |
| NOTE 5 | In case of DQ ODT enabled, MRR-WRITE (min) should be "RL + BL/n_max + RU(tWCKDQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) +2".  |
| NOTE 6 | META WRITE (WR-M) or META READ (RD-M) command is issued with or without a new WCK2CK SYNC start (WS="H"). It is allowed to issue a META WRITE/READ command with WS="L" when WCK2CK SYNC state is off.                 |
| NOTE 7 | META WRITE/READ with WS ("L" or "H") operation is the same as normal WRITE/READ with WS ("L" or "H"). WCK2CK SYNC Off timing is extended by META WRITE/READ with WS=0, similar to how WRITE/READ with WS=0 operates." |

### 7.3.5 WCK2CK SYNC Off Timing Definition (cont'd)

**Table 264 – WCK2CK SYNC Off Timing Definition for Training Commands**

Current Command	Next Command	Command Timing Constraints w/o a new WCK2CK SYNC start		Command Timing Constraints with a new WCK2CK SYNC start (WS="H")	Note
		Min	Max		
WRITE FIFO (WFF)	WRITE FIFO (WFF)	6nCK	WL + BL/n_min + RD(tWCKPST/tCK)	WL + BL/n_min + RD(tWCKPST/tCK) +1	1, 2
	READ FIFO (RFF)	See Note 4	WL + BL/n_min + RD(tWCKPST/tCK)	WL + BL/n_min + RD(tWCKPST/tCK) +1	1, 2
	WRITE (WR-S, WR-L with or w/o AP), META WRITE	Not Allowed			2
	READ (RD-S, RD-L with or w/o AP), MRR, META READ (with or w/o AP)	Not Allowed			2
	READ DQ Calibration (RDC)	Not Allowed			2
READ FIFO (RFF)	WRITE FIFO (WFF)	tRTW	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1, 2
	READ FIFO (RFF)	6nCK	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	1, 2
	WRITE (WR-S, WR-L with or w/o AP), META WRITE	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ (RD-S, RD-L with or w/o AP), MRR, META READ (with or w/o AP)	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ DQ Calibration (RDC)	Not Allowed	Not Allowed	tRTRRD	1, 2
READ DQ Calibration (RDC)	WRITE FIFO (WFF)	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ FIFO (RFF)	Not Allowed			2
	WRITE (WR-S, WR-L with or w/o AP), META WRITE	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ (RD-S, RD-L with or w/o AP), MRR, META READ (with or w/o AP)	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ DQ Calibration (RDC)	6nCK	RL + BL/n_min + RD(tWCKPST/tCK)	RL + BL/n_min + RD(tWCKPST/tCK) +1	2
WRITE (WR-S, WR-L with or w/o AP). META WRITE (with or w/o AP)	WRITE FIFO (WFF)	Not Allowed	Not Allowed	tWRWTR	1, 2
	READ FIFO (RFF)	Not Allowed			2
	READ DQ Calibration (RDC)	Not Allowed	Not Allowed	WL + BL/n_max + RU(tWTR_L/tCK)	1, 2
READ (RD-S, RD-L with or w/o AP), MRR, META READ (with or w/o AP)	WRITE FIFO (WFF)	Not Allowed	Not Allowed	tRTRRD	1, 2
	READ FIFO (RFF)	Not Allowed			2
	READ DQ Calibration (RDC)	Not Allowed	Not Allowed	tRTRRD	1, 2
NOTE 1 Even nCK round-up is required for any command-to-command timing constraints.					
NOTE 2 Another WCK2CK SYNC start (WS=H) command cannot be executed while the WCK2CK SYNC status is ON.					
NOTE 3 WCK2CK SYNC shall be initiated before or when issuing the current command.					
NOTE 4 NT-ODT disabled : Max(6nCK, WL+BL/n_max-RL +Max[RU(10ns/tCK), 4nCK]), NT-ODT enabled : Max(6nCK, WL+BL/n_max-RL+RU[tODT off(max)/tCK] +Max[RU(10ns/tCK), 4nCK]).					

### 7.3.6 WCK Sync-Off Extension Overview

WCK Sync-Off Extension (WSOE) feature is enabled by setting MR26 OP[3]=1<sub>B</sub>. Because of its functionality, WCK Always on mode is a mutual exclusive function. Therefore, WCK Always on mode must be disabled before enabling WSOE feature. Once the feature is enabled, the "WS" and "WS\_OFF" operands in the CAS command are decoded to initiate WCK-Sync-Off Extension On-the-fly as show in Table 265.

#### 7.3.6.1 WCK Sync-Off Extension Functionality

When a CAS command is issued with WS=0<sub>B</sub> and WS\_OFF=0<sub>B</sub> after WCK sync. state has been established, WCK sync-off timing is extended, and WCK sync state is kept until the next command with WS=0<sub>B</sub>. The commands that can initiate WCK sync. state are the ones that have the WS operand and include Write, Read, Mode Register Read, Write FIFO, Read FIFO, and Read DQ Calibration. CAS with WS=0<sub>B</sub> and WS\_OFF=0<sub>B</sub> must be issued within an acceptable period as defined in Table 266. The extended WCK sync-off timing by CAS with WS=0<sub>B</sub> and WS\_OFF=0<sub>B</sub> is terminated by the next WS=0<sub>B</sub> command (Write, Read, Mode Register Read, Write FIFO, Read FIFO, and Read DQ Calibration with WS=0<sub>B</sub>). WSOE feature controls only WCK sync-off timing and does not change post-amble behavior.

**Table 265 – CAS Command Decoding Table**

	CAS Command Operand		Function
	WS	WS_OFF	
WCK Sync-Off Extension feature enabled MR26 OP[3]=1 <sub>B</sub>	0	0	WCK Sync-Off Extension

**Table 266 – Acceptable Period of WCK Sync-Off Extension from Previous Write or Read Command**

The previous command	Acceptable Period of CAS Command with WS=0 <sub>B</sub> and WS_OFF=0 <sub>B</sub> from the Previous Command		Note
	Min.	Max.	
Write (WR-S/WR-L),	>= 2nCK	< WL	
Write FIFO	>= 2nCK	< WL	
Read (RD-S/RD-L)	>= 2nCK	< RL	
Read FIFO	>= 2nCK	< RL	
Read DQ Cal.	>= 2nCK	< RL	
Mode Register Read	>= 2nCK	< RL	

### 7.3.6.1 WCK Sync-Off Extension Functionality (cont'd)

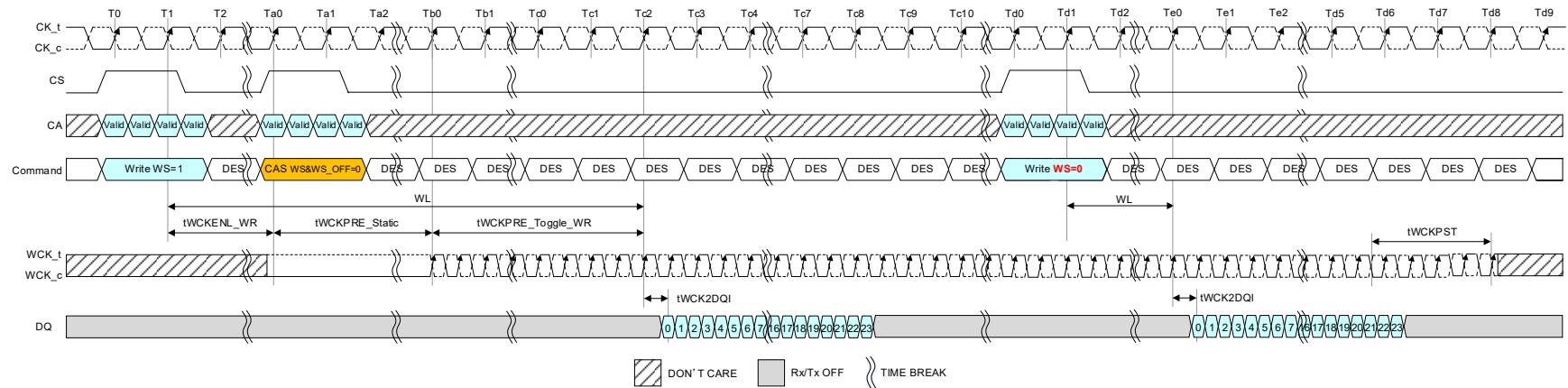


Figure 66 — Example of WCK Sync-Off Timing Extension by CAS with WS=0<sub>B</sub> and WS\_OFF=0<sub>B</sub> Command

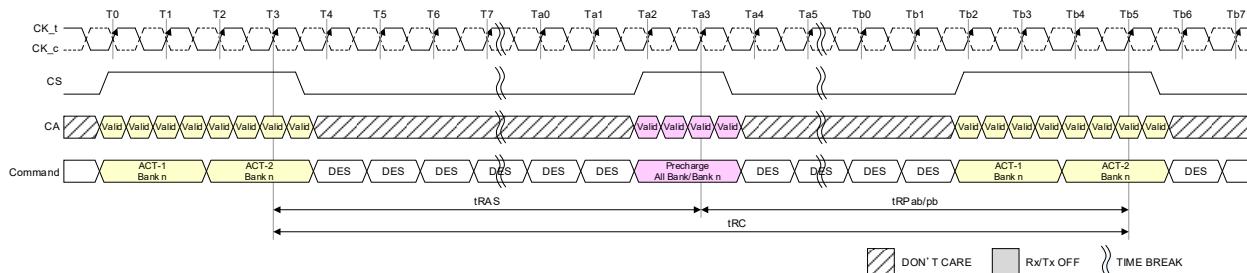
## 7.4 Row Operation

### 7.4.1 Activate Command

The ACTIVATE command is composed of two commands, Activate-1 command and Activate-2. Activate-2 command shall be issued within 8 clock cycles (tAAD) after Activate-1 command was issued. Within tAAD period Only CAS, WRITE, READ, MRR, PRECHARGE/Refresh (to a different bank) commands can be issued between ACTIVATE-1 and ACTIVATE-2 commands. It is an illegal operation if an Activate-2 command is not issued within tAAD of an Activate-1 command. Bank Group addresses are used to determine which Bank Group to activate, Bank addresses are used to determine which Bank to activate in the selected Bank Group. Row addresses are used to determine which row to activate in the selected Bank. The ACTIVATE command is required to be applied before any READ or WRITE operation can be executed. The SDRAM can accept a READ command at tRCDr after the ACTIVATE command is issued and the SDRAM can accept a WRITE command at tRCDw after the ACTIVATE command is issued. After a bank has been activated, precharge command is issued to precharge bank or banks.

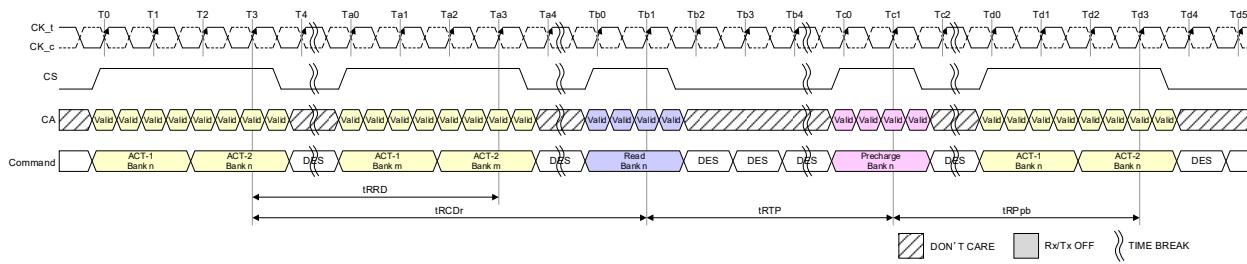
The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between ACTIVATE commands to the same bank is determined by the RAS cycle time of the SDRAM (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

The definition of tRAS has been changed from conventional Low Power SDRAM such as LPDDR5, LPDDR4, since LPDDR6 applies Per Row Activation Counting (PRAC) function. Refer to PRAC clause 7.8.27 Per Row Activation Counting (PRAC) for detail.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

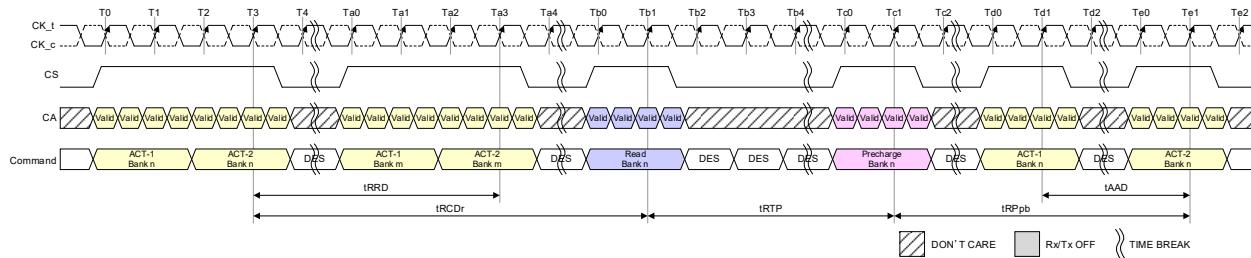
**Figure 67 — tRAS and tRC Timing**



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

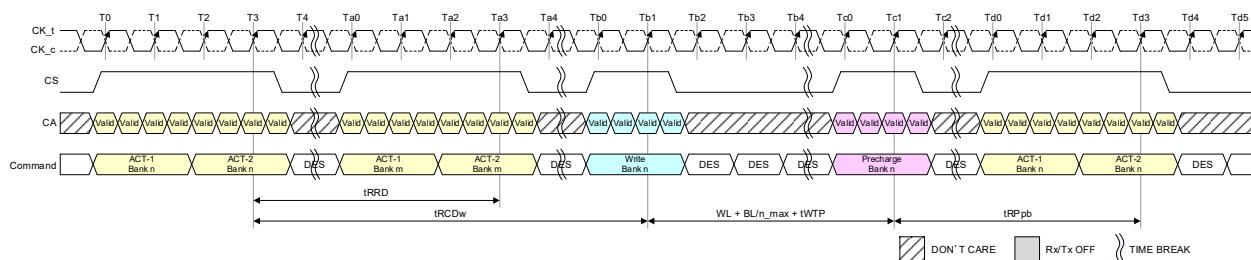
**Figure 68 — Activate Command followed Read Command**

### 7.4.1 Activate Command (cont'd)



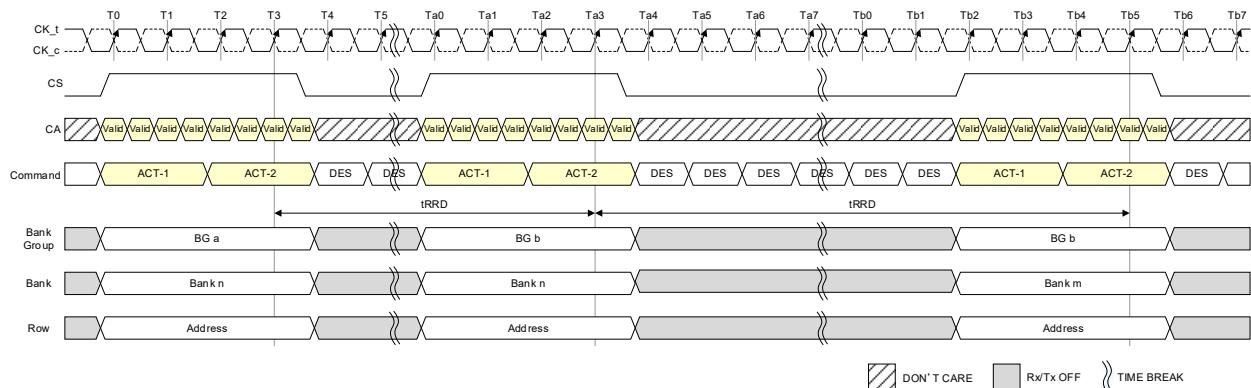
NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 69 — Activate Command with Activate1 and Activate-2 Spacing**



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 70 — Activate Command followed Write Command**



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 tRRD: ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to different Bank Group.

NOTE 3 tRRD: ACTIVATE to ACTIVATE Command period: Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group, too.

**Figure 71 — Activate to Activate Command Period: tRRD**

### 7.4.1.1 Sequential Bank Activation Restriction

Certain restrictions on operation of LPDDR6 SDRAM is required to be observed the regarding the number of sequential ACTIVATE commands that can be issued.

No more than 4 Banks may be activated (or refreshed, in the case of REFdb) in a rolling tFAW window. The number of clocks in a tFAW period is dependent upon the clock frequency, which may vary. If the clock frequency is not changed over this period, converting clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to the next integer value. As an example of the rolling window, if RU(tFAW /tCK) is 20 clocks, and an ACTIVATE command is issued in clock n, no more than three further ACTIVATE commands can be issued between clock n + 4 and n + 18. REFdb also counts as bank activation for purposes of tFAW. If the clock frequency is changed during the tFAW period, the rolling tFAW window may be calculated in clock cycles by adding up the time spent in each clock period. The tFAW requirement is met when the previous n clock cycles exceed the tFAW time.

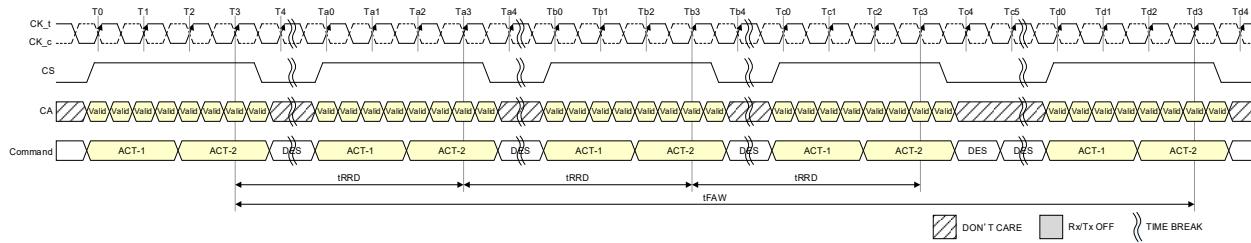


Figure 72 — tFAW Timing

#### 7.4.2 Pre-Charge Operation

The Precharge command is used to Precharge or close a bank that has been activated. The Precharge command is initiated with CS, and CA[3:0] in the proper state as defined by the Command Truth table (Table 254). The Precharge command can be used to precharge each bank independently or all banks simultaneously. The AB flag and the bank address bit are used to determine which bank(s) to Precharge. The Precharged bank(s) will be available for subsequent row access tRPab after an all-bank Precharge command is issued, or tRPpb after a single-bank Precharge command is issued.

To ensure that LPDDR6 devices can meet the instantaneous current demands, the row-Precharge time for an all-bank Precharge (tRPab) is longer than the per bank Precharge time (tRPpb).

Issuing Precharge command to Idle bank is allowed, classic case is some bank is being at idle state when Precharge all command is issued.

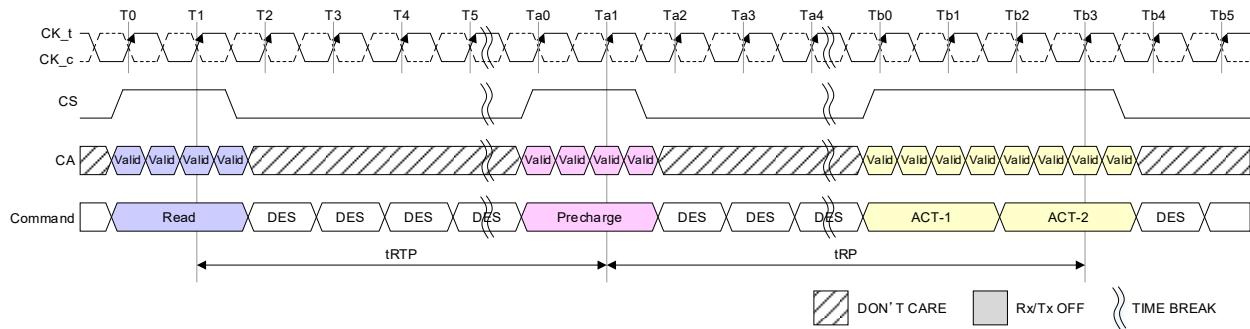
tRP period needs to be satisfied before issuing next commands such as Activate, Self-refresh Entry, and Refresh, even if the target bank of the Precharge command is in the idle state.

**Table 267 – Precharge Bank Selection 4 Bank / 4 Bank Group**

AB	BG1	BG0	BA1	BA0	Precharged Bank(s)
0	0	0	0	0	Bank Group 0, Bank 0 only
0	0	0	0	1	Bank Group 0, Bank 1 only
0	0	0	1	0	Bank Group 0, Bank 2 only
0	0	0	1	1	Bank Group 0, Bank 3 only
0	0	1	0	0	Bank Group 1, Bank 0 only
0	0	1	0	1	Bank Group 1, Bank 1 only
0	0	1	1	0	Bank Group 1, Bank 2 only
0	0	1	1	1	Bank Group 1, Bank 3 only
0	1	0	0	0	Bank Group 2, Bank 0 only
0	1	0	0	1	Bank Group 2, Bank 1 only
0	1	0	1	0	Bank Group 2, Bank 2 only
0	1	0	1	1	Bank Group 2, Bank 3 only
0	1	1	0	0	Bank Group 3, Bank 0 only
0	1	1	0	1	Bank Group 3, Bank 1 only
0	1	1	1	0	Bank Group 3, Bank 2 only
0	1	1	1	1	Bank Group 3, Bank 3 only
1	Valid	Valid	Valid	Valid	All Banks

#### 7.4.2 Pre-Charge Operation (cont'd)

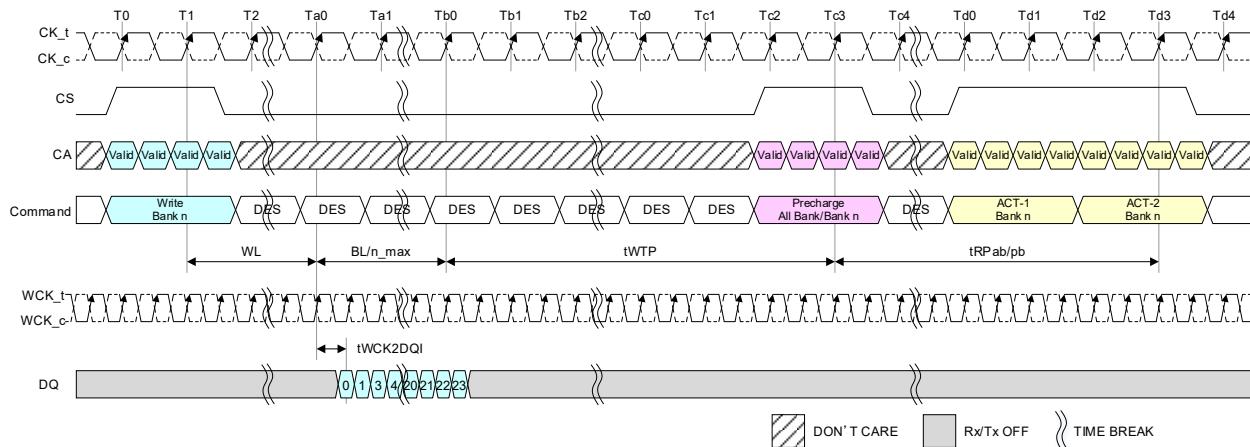
The Precharge command following Read Command can be issued after tRTP has been satisfied. Refer to clause 8.3 Command Timing Constraints for details. However, Precharge cannot be issued until after tRAS is satisfied. A new bank Activate command can be issued to the same bank after the row Precharge time (tRP) has elapsed. The minimum Read-to-Precharge time must also satisfy a minimum analog time from the second rising CK\_t edge the Read command. For LPDDR6 Read-to- Precharge timings, see Figure 73.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 73 — Burst Read followed by Precharge**

LPDDR6 SDRAM devices write data to the memory array in prefetch multiples. The minimum Write-to-Precharge time for commands to the same bank is WL + BL/n\_max + tWTP clock cycles when bank organization. Refer to clause 8.3 Command Timing Constraints for details .



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 74 — Burst Write followed by Precharge**

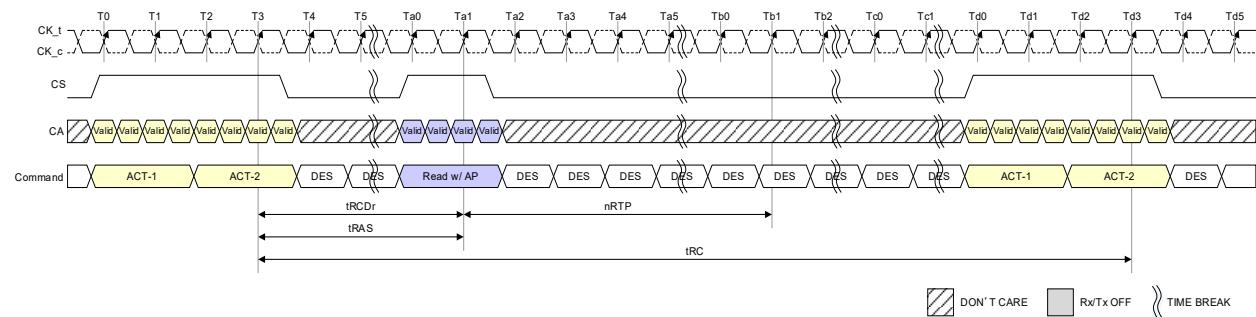
#### 7.4.2.1 Auto-Precharge Operation

When a Read or Write command is issued to the LPDDR6 SDRAM, the AP bit (CA2/F1) can be set to enable the activated bank to automatically begin Precharge at the earliest possible moment during the burst Read or Write cycle.

If AP is LOW when the Read and Write command is issued, then the normal Read or Write burst operation is executed and the bank remains activated at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, the Auto-Precharge function is engaged. This feature enables the Precharge operation to be partially or completely hidden during burst Read/Write cycles (dependent upon Read or Write latency), thus improving system performance for random data access. Read with Auto Precharge or Write with Auto Precharge commands may be issued after tRCDr/tRCDw has been satisfied. The LPDDR6 SDRAM RAS Lockout feature will schedule the internal Precharge to assure that tRAS is satisfied.

tRC needs to be satisfied prior to issuing subsequent Activate commands to the same bank. Figure 75 shows example of RAS lock function.

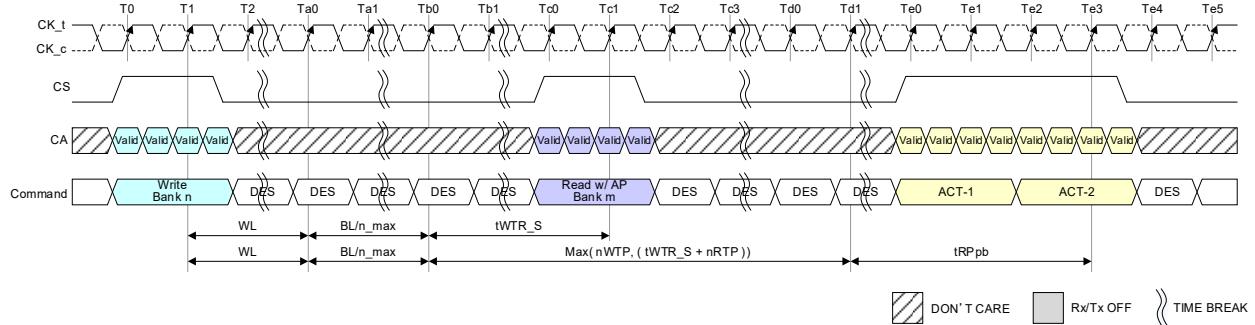


NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 75 — Command Input Timing with RAS Lock**

#### 7.4.2.1.1 Delay Time from Write to Read with Auto Precharge

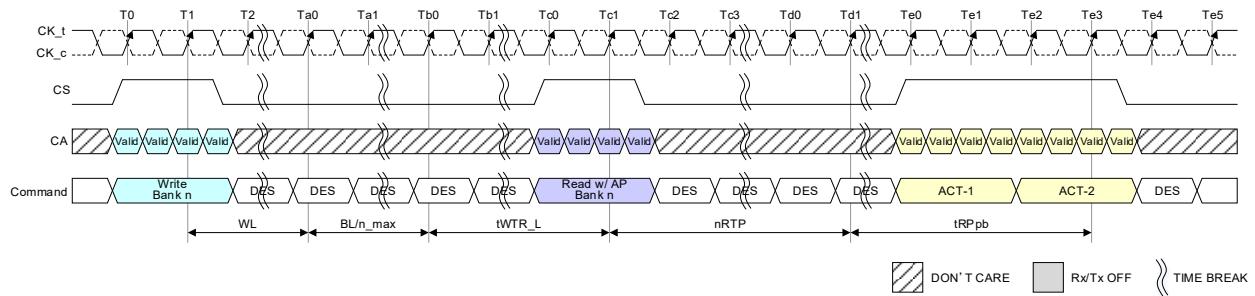
In the case of write command followed by Read with auto-Precharge, the delay time from Write/Read command to Activate command is required to satisfy following timings, refer to Figure 76 and Figure 77 for detail.



NOTE 1 tWTR\_S starts at the second rising edge of CK\_t after WL + BL/n\_max from Write command.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 76 — Delay Time from Write to Read with Auto Precharge (Different Bank Write followed Read)**



NOTE 1 tWTR\_L starts at the second rising edge of CK\_t after WL + BL/n\_max from Write command.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 77 — Delay Time from Write to Read with Auto Precharge (Same Bank Write followed Read)**

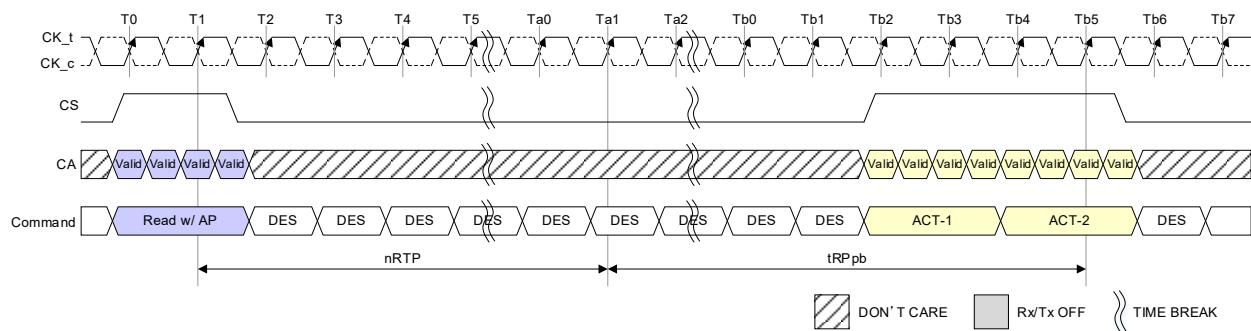
#### 7.4.2.1.2 Burst Read with Auto-Precharge

If AP is HIGH when a Read command is issued, the Read with Auto-Precharge function is engaged. An internal Precharge procedure starts the following delay time after the Read command.

Refer to clause 8.3 for the command constraints tables for actual delay time from Read with Auto-Precharge.

Auto-Precharge operation, an Activate command can be issued to the same bank if the following two conditions are both satisfied:

- The RAS Precharge time ( $t_{RP}$ ) has been satisfied from the clock at which the Auto-Precharge began.
- The RAS cycle time ( $t_{RC}$ ) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

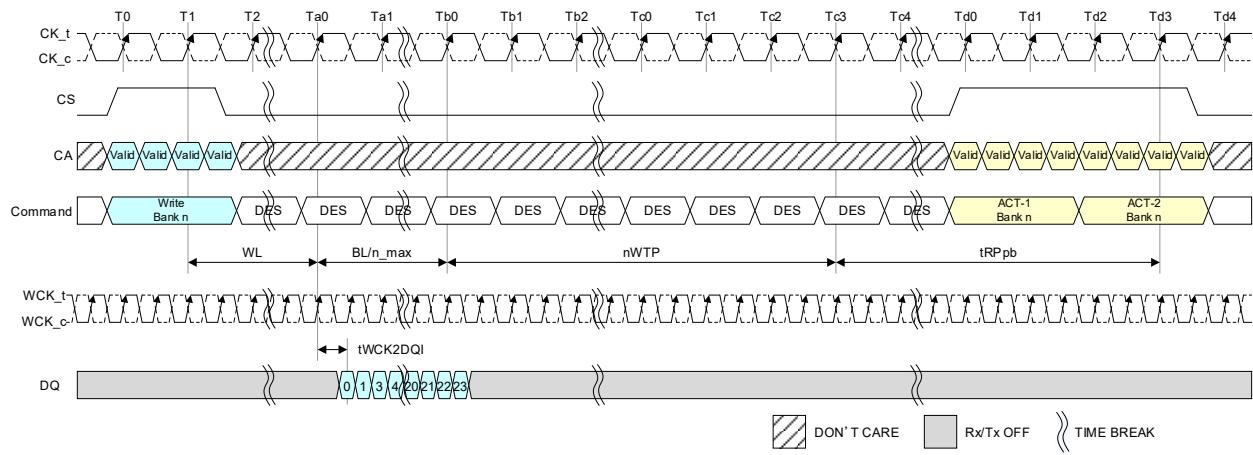
**Figure 78 — Burst Read with Auto-Precharge**

#### 7.4.2.1.3 Burst Write with Auto-Precharge

If AP is HIGH when a Write command is issued, the Write with Auto-Precharge function is engaged. The device starts an Auto-Precharge on the rising edge nWTP cycles after the completion of the Burst Write.

Write with Auto-Precharge, an Activate command can be issued to the same bank if the following conditions are met:

- The RAS Precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge began, and
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 79 — Burst Write with Auto- Precharge

#### 7.4.2.2 Read and Read-to-Precharge Latencies

Latencies related to Read timing are measured from the second rising edge of CK\_t of the Read command. The Read Latencies depend on the settings of DVFSL, Read Link protection, and Efficiency mode Disable/Enable.

For each MR1 OP[4:0] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

**Table 268 – Read Latencies Tables Summary**

Table	Link protection	DVFSL
Table 269	Disable	Disable
Table 270	Enable	Disable
Table 271	Disable	Enable
Table 272	Enable	Enable

### 7.4.2.2 Read and Read-to-Precharge Latencies (cont'd)

**Table 269 – Read Latencies for Link Protection is Disabled and DVFSL is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRTP [nCK]	
					Set 0	Set 1	Set 2	BL24	BL48
00000 <sub>B</sub>	80	1067	20	267	7	7	8	7	13
00001 <sub>B</sub>	1067	1600	267	400	9	10	11	7	13
00010 <sub>B</sub>	1600	2133	400	533	12	13	14	7	13
00011 <sub>B</sub>	2133	2750	533	688	15	17	18	7	13
00100 <sub>B</sub>	2750	3200	688	800	17	19	21	7	13
00101 <sub>B</sub>	3200	3750	800	938	20	22	24	8	14
00110 <sub>B</sub>	3750	4267	938	1067	23	25	28	8	14
00111 <sub>B</sub>	4267	4800	1067	1200	26	28	31	8	14
01000 <sub>B</sub>	4800	5500	1200	1375	30	32	35	8	14
01001 <sub>B</sub>	5500	6400	1375	1600	34	37	41	8	14
01010 <sub>B</sub>	6400	7500	1600	1875	40	44	48	11	23
01011 <sub>B</sub>	7500	8533	1875	2133	46	50	54	11	23
01100 <sub>B</sub>	8533	9600	2133	2400	52	56	62	13	25
01101 <sub>B</sub>	9600	10667	2400	2667	56	62	68	14	26
01110 <sub>B</sub>	10667	11733	2667	2933	TBD	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD	TBD	TBD	TBD	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Read DBI	Static/Dynamic Efficiency mode	Apply
Disable	Disable	Set 0
Enable	Disable	Set 1
Disable	Enable	Set 1

NOTE 3 The programmed value of nRTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read with AP(Auto Precharge) command. It is determined by “BL/n + RU(1.25/tCK)”.

#### 7.4.2.2 Read and Read-to-Precharge Latencies (cont'd)

**Table 270 – Read Latencies for Link Protection is Enabled and DVFSL is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRTP [nCK]	
					Set 0	Set 1	BL24	BL48
00000 <sub>B</sub>	80	1067	20	267	7	8	7	13
00001 <sub>B</sub>	1067	1600	267	400	11	11	7	13
00010 <sub>B</sub>	1600	2133	400	533	14	15	7	13
00011 <sub>B</sub>	2133	2750	533	688	17	19	7	13
00100 <sub>B</sub>	2750	3200	688	800	20	22	7	13
00101 <sub>B</sub>	3200	3750	800	938	23	25	8	14
00110 <sub>B</sub>	3750	4267	938	1067	26	28	8	14
00111 <sub>B</sub>	4267	4800	1067	1200	29	32	8	14
01000 <sub>B</sub>	4800	5500	1200	1375	33	36	8	14
01001 <sub>B</sub>	5500	6400	1375	1600	39	42	8	14
01010 <sub>B</sub>	6400	7500	1600	1875	46	50	11	23
01011 <sub>B</sub>	7500	8533	1875	2133	52	56	11	23
01100 <sub>B</sub>	8533	9600	2133	2400	58	64	13	25
01101 <sub>B</sub>	9600	10667	2400	2667	64	70	14	26
01110 <sub>B</sub>	10667	11733	2667	2933	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD	TBD	TBD	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Static/Dynamic Efficiency mode	Apply
Disable	Set 0
Enable	Set 1

NOTE 3 The programmed value of nRTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read with AP(Auto Precharge) command. It is determined by “BL/n + RU(1.25/tCK)”.

### 7.4.2.2 Read and Read-to-Precharge Latencies (cont'd)

**Table 271 – Read Latencies for Link Protection is Disabled and DVFSL is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRTP [nCK]	
					Set 0	Set 1	Set 2	BL24	BL48
00000 <sub>B</sub>	80	1067	20	267	7	8	9	7	13
00001 <sub>B</sub>	1067	1600	267	400	10	11	12	7	13
00010 <sub>B</sub>	1600	2133	400	533	14	15	16	7	13
00011 <sub>B</sub>	2133	2750	533	688	17	19	21	8	14
00100 <sub>B</sub>	2750	3200	688	800	20	22	24	8	14

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Read DBI	Static/Dynamic Efficiency mode	Apply
Disable	Disable	Set 0
Enable	Disable	Set 1
Disable	Enable	Set 1
Enable	Enable	Set 2

NOTE 3 The programmed value of nRTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read with AP(Auto Precharge) command. It is determined by “BL/n + RU(1.25/tCK)”.

#### 7.4.2.2 Read and Read-to-Precharge Latencies (cont'd)

**Table 272 – Read Latencies for Link Protection is Enabled and DVFSL is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRTP [nCK]	
					Set 0	Set 1	BL24	BL48
00000 <sub>B</sub>	80	1067	20	267	8	9	7	13
00001 <sub>B</sub>	1067	1600	267	400	12	13	7	13
00010 <sub>B</sub>	1600	2133	400	533	15	17	7	13
00011 <sub>B</sub>	2133	2750	533	688	19	21	8	14
00100 <sub>B</sub>	2750	3200	688	800	22	24	8	14

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Static/Dynamic Efficiency mode	Apply
Disable	Set 0
Enable	Set 1

NOTE 3 The programmed value of nRTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read with AP(Auto Precharge) command. It is determined by “BL/n + RU(1.25/tCK)”.

### 7.4.2.3 Write to Auto Precharge Time

nWTP starts at the rising edge of CK\_t after WL + BL/n\_max from second rising edge of CK\_t of Write AP (Auto Precharge) command.

The table's summary in this section is shown in Table 273.

**Table 273 – nWTP Timing Tables Summary**

#	DVFSL	Write Link-Protection	Static/Dynamic Efficiency mode
Table 274	Disabled	Disabled	Disabled
Table 275	Disabled	Disabled	Enabled
Table 276	Disabled	Enabled	Disabled
Table 277	Disabled	Enabled	Enabled
Table 278	Enabled	Disabled	Disabled
Table 279	Enabled	Disabled	Enabled
Table 280	Enabled	Enabled	Disabled
Table 281	Enabled	Enabled	Enabled

**Table 274 – nWTP: DVFSL is Disabled, Write Link Protection is Disabled and Static/Dynamic Efficiency Mode is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	6
00010 <sub>B</sub>	1600	2133	400	533	7
00011 <sub>B</sub>	2133	2750	533	688	9
00100 <sub>B</sub>	2750	3200	688	800	10
00101 <sub>B</sub>	3200	3750	800	938	12
00110 <sub>B</sub>	3750	4267	938	1067	13
00111 <sub>B</sub>	4267	4800	1067	1200	15
01000 <sub>B</sub>	4800	5500	1200	1375	17
01001 <sub>B</sub>	5500	6400	1375	1600	20
01010 <sub>B</sub>	6400	7500	1600	1875	23
01011 <sub>B</sub>	7500	8533	1875	2133	26
01100 <sub>B</sub>	8533	9600	2133	2400	29
01101 <sub>B</sub>	9600	10667	2400	2667	32
01110 <sub>B</sub>	10667	11733	2667	2933	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD
NOTE 1	The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.				
NOTE 2	The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(12ns, 6nCK)”.				

### 7.4.2.3 Write to Auto Precharge Time (cont'd)

**Table 275 – nWTP: DVFSL is Disabled, Write Link protection is Disabled and Static/Dynamic Efficiency Mode is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	6
00010 <sub>B</sub>	1600	2133	400	533	8
00011 <sub>B</sub>	2133	2750	533	688	10
00100 <sub>B</sub>	2750	3200	688	800	12
00101 <sub>B</sub>	3200	3750	800	938	14
00110 <sub>B</sub>	3750	4267	938	1067	15
00111 <sub>B</sub>	4267	4800	1067	1200	17
01000 <sub>B</sub>	4800	5500	1200	1375	20
01001 <sub>B</sub>	5500	6400	1375	1600	23
01010 <sub>B</sub>	6400	7500	1600	1875	27
01011 <sub>B</sub>	7500	8533	1875	2133	30
01100 <sub>B</sub>	8533	9600	2133	2400	34
01101 <sub>B</sub>	9600	10667	2400	2667	38
01110 <sub>B</sub>	10667	11733	2667	2933	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD
NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.					
NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by "Max(14ns, 6nCK)".					

**Table 276 – nWTP: DVFSL is Disabled, Write Link Protection is Enabled and Static/Dynamic Efficiency Mode is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	7
00010 <sub>B</sub>	1600	2133	400	533	9
00011 <sub>B</sub>	2133	2750	533	688	12
00100 <sub>B</sub>	2750	3200	688	800	13
00101 <sub>B</sub>	3200	3750	800	938	15
00110 <sub>B</sub>	3750	4267	938	1067	18
00111 <sub>B</sub>	4267	4800	1067	1200	20
01000 <sub>B</sub>	4800	5500	1200	1375	23
01001 <sub>B</sub>	5500	6400	1375	1600	26
01010 <sub>B</sub>	6400	7500	1600	1875	31
01011 <sub>B</sub>	7500	8533	1875	2133	35
01100 <sub>B</sub>	8533	9600	2133	2400	39
01101 <sub>B</sub>	9600	10667	2400	2667	43
01110 <sub>B</sub>	10667	11733	2667	2933	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD
NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.					
NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by "Max(16ns, 6nCK)".					

#### 7.4.2.3 Write to Auto Precharge Time (cont'd)

**Table 277 – nWTP: DVFSL is Disabled, Write Link Protection is Enabled and Static/Dynamic Efficiency Mode is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	8
00010 <sub>B</sub>	1600	2133	400	533	10
00011 <sub>B</sub>	2133	2750	533	688	13
00100 <sub>B</sub>	2750	3200	688	800	15
00101 <sub>B</sub>	3200	3750	800	938	17
00110 <sub>B</sub>	3750	4267	938	1067	20
00111 <sub>B</sub>	4267	4800	1067	1200	22
01000 <sub>B</sub>	4800	5500	1200	1375	25
01001 <sub>B</sub>	5500	6400	1375	1600	29
01010 <sub>B</sub>	6400	7500	1600	1875	34
01011 <sub>B</sub>	7500	8533	1875	2133	39
01100 <sub>B</sub>	8533	9600	2133	2400	44
01101 <sub>B</sub>	9600	10667	2400	2667	48
01110 <sub>B</sub>	10667	11733	2667	2933	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD
NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.					
NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(18ns, 6nCK)”.					

**Table 278 – nWTP: DVFSL is Enabled, Write Link Protection is Disabled and Static/Dynamic Efficiency Mode is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	6
00010 <sub>B</sub>	1600	2133	400	533	8
00011 <sub>B</sub>	2133	2750	533	688	10
00100 <sub>B</sub>	2750	3200	688	800	12
NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.					
NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(13.8ns, 6nCK)”.					

#### 7.4.2.3 Write to Auto Precharge Time (cont'd)

**Table 279 – nWTP: DVFSL is Enabled, Write Link Protection is Disabled and Static/Dynamic Efficiency Mode is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	7
00010 <sub>B</sub>	1600	2133	400	533	9
00011 <sub>B</sub>	2133	2750	533	688	12
00100 <sub>B</sub>	2750	3200	688	800	13

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.

NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(16.1ns, 6nCK)”.

**Table 280 – nWTP: DVFSL is Enabled, Write Link Protection is Enabled and Static/Dynamic Efficiency Mode is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	8
00010 <sub>B</sub>	1600	2133	400	533	10
00011 <sub>B</sub>	2133	2750	533	688	13
00100 <sub>B</sub>	2750	3200	688	800	15

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.

NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(18.4ns, 6nCK)”.

**Table 281 – nWTP: DVFSL is Enabled, Write Link Protection is Enabled and Static/Dynamic Efficiency Mode is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nWTP
00000 <sub>B</sub>	80	1067	20	267	6
00001 <sub>B</sub>	1067	1600	267	400	9
00010 <sub>B</sub>	1600	2133	400	533	12
00011 <sub>B</sub>	2133	2750	533	688	15
00100 <sub>B</sub>	2750	3200	688	800	17

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each nWTP value.

NOTE 2 The programmed value of nWTP is the number of clock cycles the LPDDR6 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write with AP(Auto Precharge) command. It is determined by “Max(20.7ns, 6nCK)”.

## 7.5 Read/Write Operations

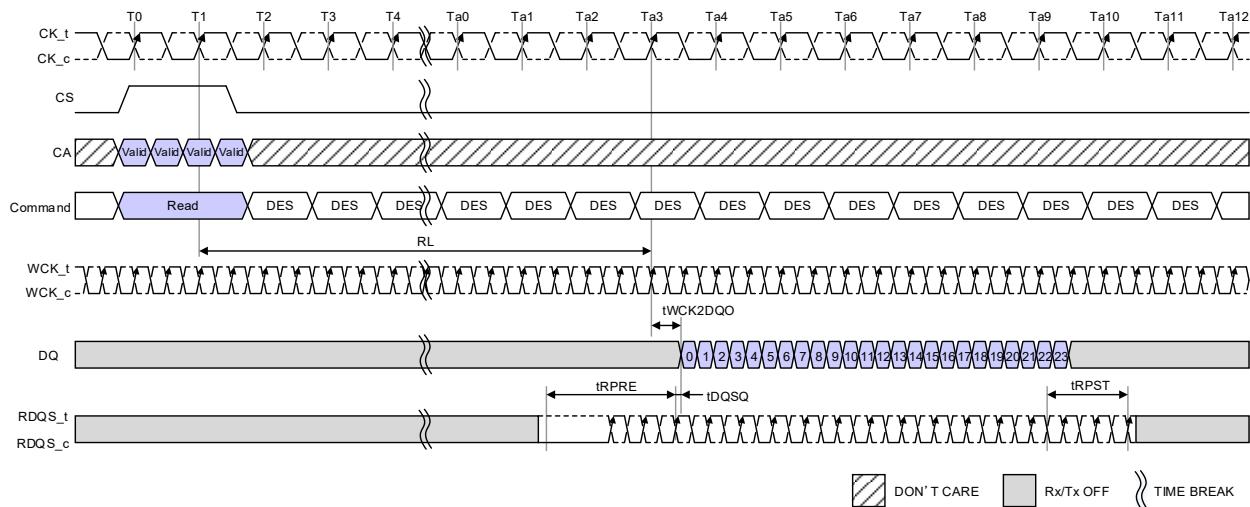
### 7.5.1 Read Operation

After a bank has been activated, the Read Operation causes LPDDR6 SDRAM to retrieve and output data stored in its array. The Read Operation is initiated by the Read Command during which the beginning column address and Bank/Bank group address for the data to be retrieved from the array is provided. The data is driven by the SDRAM on its DQ pins RL cycles after the Read Command along with the proper waveform on the Read DQS (RDQS) outputs. Read Latency is defined from the Read command to data and is not affected by the Read DQS offset timing.

#### 7.5.1.1 Read Preamble and Postamble

The RDQS strobe for the SDRAM requires a pre-amble prior to the first latching edge (the rising edge of RDQS\_t with data "valid"), and it requires a post-amble after the last latching edge. The pre-amble and post-amble lengths are set via mode register writes (MRW).

Preamble/postamble behavior such as static (no-toggle), toggling or combination of static and toggle, and its length can be set by mode register.



NOTE 1 WCK2CK Sync state (WCK Always On mode).

NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 BL=24, tRPRE=2tWCK (Static) + 2tWCK (Toggle), tRPST=2.5tWCK(Toggle)

Figure 80 – Read Operation: RDQS Read Preamble and Postamble

#### 7.5.1.2 Burst Read Operation

An LPDDR6 SDRAM requires to be in WCK2CK synchronization state before internal read operation starts and WCK post-amble is needed after all read DQ burst.

Refer to clause 7.3.1 WCK2CK Synchronization Operation for details on WCK2CK synchronization and WCK postamble.

### 7.5.1.2.1 Read Timing

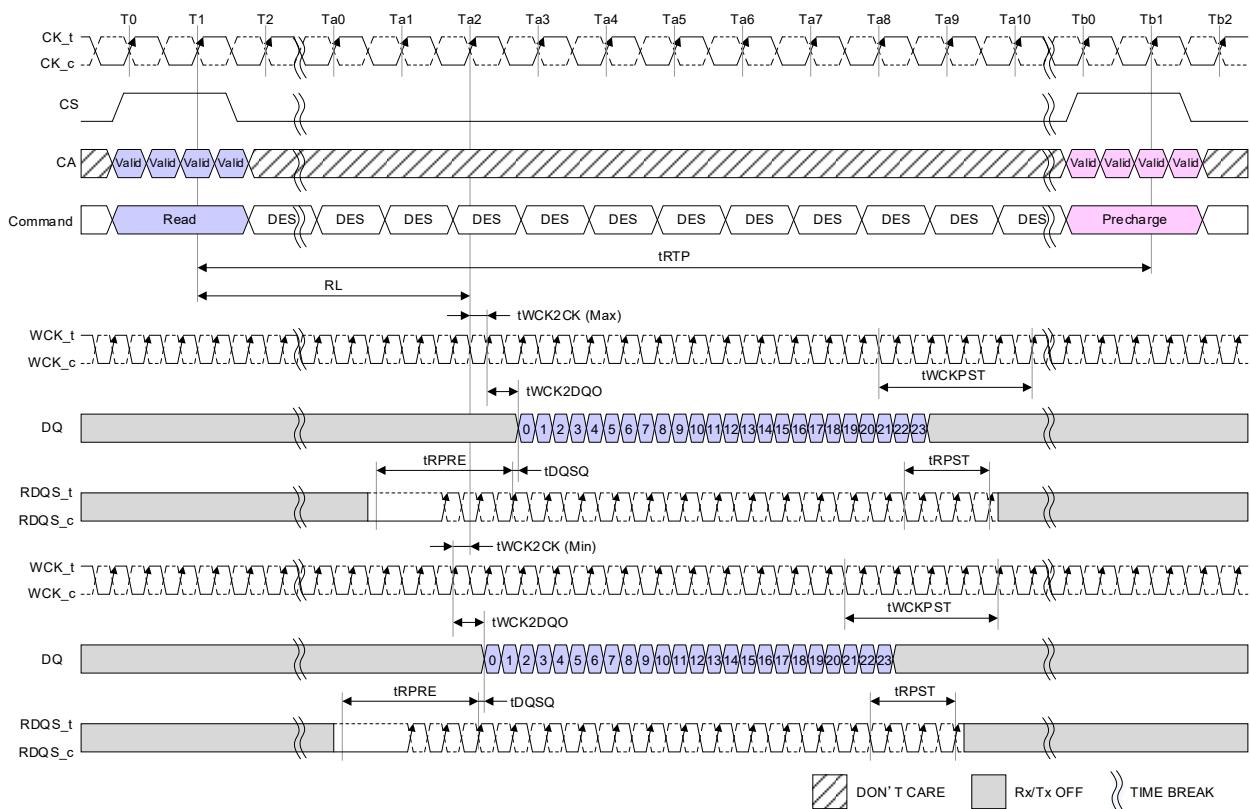
A read command is initiated with CS, and CA[3:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table, Table 254.

Read burst order is controlled by burst order bit, C0 only when BL48.

The read latency (RL) is defined from the rising edge of the CK\_t of 2nd command that starts a read command to the rising edge of the CK\_t from which ( $tWCK2CK + tWCK2DQO$ ) is measured.

The first valid data is available of  $RL * tCK + tWCK2CK + tWCK2DQO$  after the CK\_t rising edge of a read command.

The DQ-data is valid for tQW (DQ output window) and the controller is required to periodically train its internal capture clock to stay centered in the tQW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the controller on successive edges of WCK until the 24 or 48 bit data burst is complete. The WCK is required to remain active (toggling) for tWCKPST (WCK postamble) after the completion of the burst read. After a burst READ operation, tRTP is required to be satisfied before a PRECHARGE command to the same bank can be issued.



NOTE 1 WCK2CK Sync state (WCK Always On mode).

NOTE 2 BL=24, tRPRE=2tWCK (Static) + 2tWCK (Toggle), tRPST=2.5tWCK(Toggle), tWCKPST=4.5tWCK

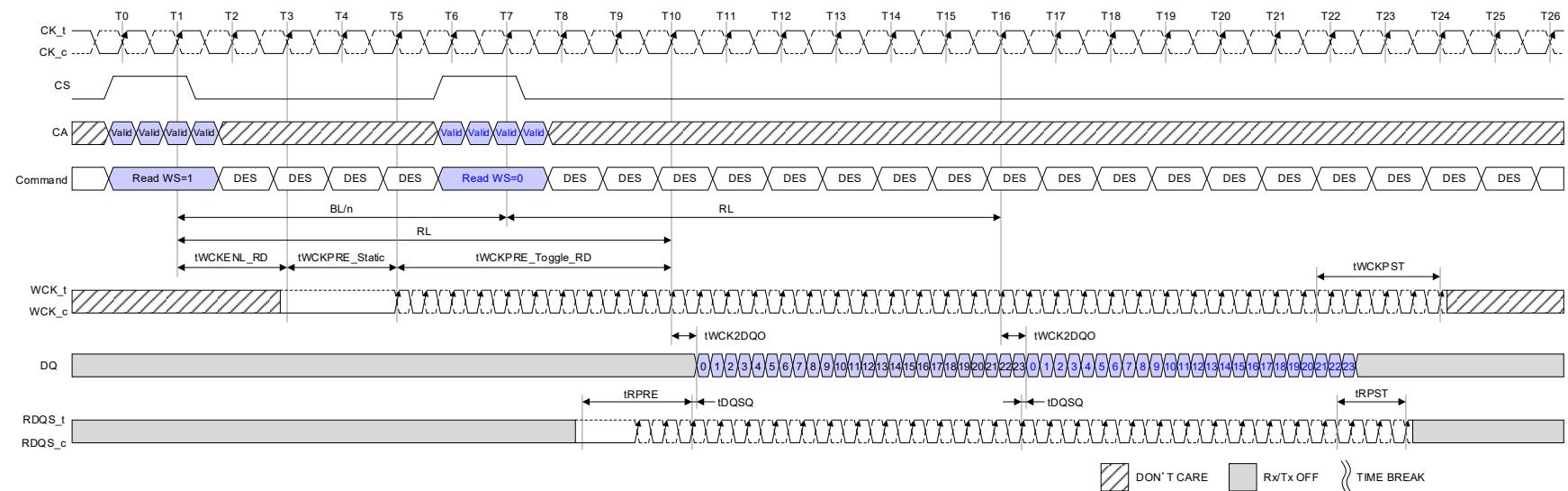
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 81 – Burst Read Operation

### 7.5.1.2.2 Read to Read Operation without Additional WCK2CK-sync

Figure 82 shows timing diagram of back to back Read operation with BL/n. First Read command should be with WS=1, making the SDRAM in WCK2CK-sync state. Second Read command is not required WS=1, because the WCK2CK-sync state continues until RL + BL/n\_min + RD(tWCKPST/tCK).

Additionally, issuing WCK2CK synchronization command which operand: WS=1 is prohibited during WCK2CK sync state. Therefore WS=1 at second Read command is illegal.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

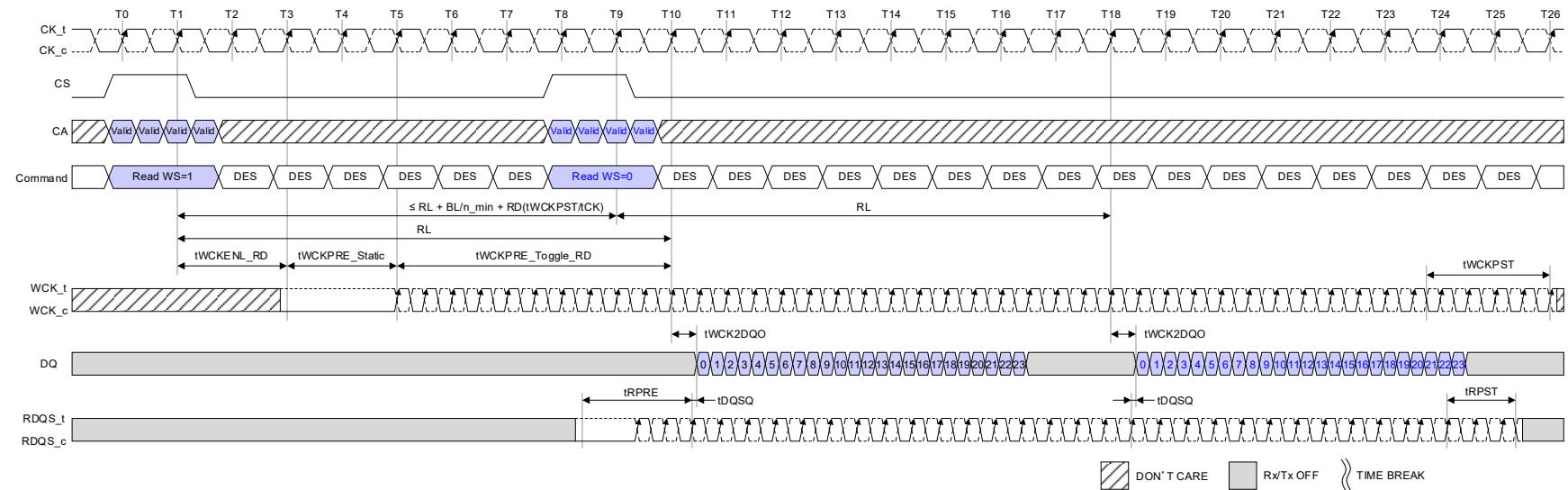
NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 tWCKENL\_RD=2, tWCKPRE\_Static=2, tWCKPRE\_toggle\_RD=5, RL=9, BL=24, tWCKPST=4.5tWCK

**Figure 82 – Back to Back Read Operation with BL/n**

### 7.5.1.2.2 Read to Read Operation without Additional WCK2CK-sync (cont'd)

When the command gap between two Read commands is larger than  $BL/n$  and equal or less than  $RL + BL/n_{min} + RD(tWCKPST/tCK)$ , a WS=1 in second Read command is not required and illegal, due to SDRAM is still in WCK2CK-sync state at second Read command issued.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2  $tWCK2CK$  is 0 ps in this instance.

NOTE 3  $tWCKENL\_RD=2$ ,  $tWCKPRE\_Static=2$ ,  $tWCKPRE\_toggle\_RD=5$ ,  $RL=9$ ,  $BL=24$ ,  $tWCKPST=4.5tWCK$

**Figure 83 – Back to Back Read Operation without Additional WCK2CK Sync Sequence**

### 7.5.1.2.3 Read to Read Operation with Additional WCK2CK-sync

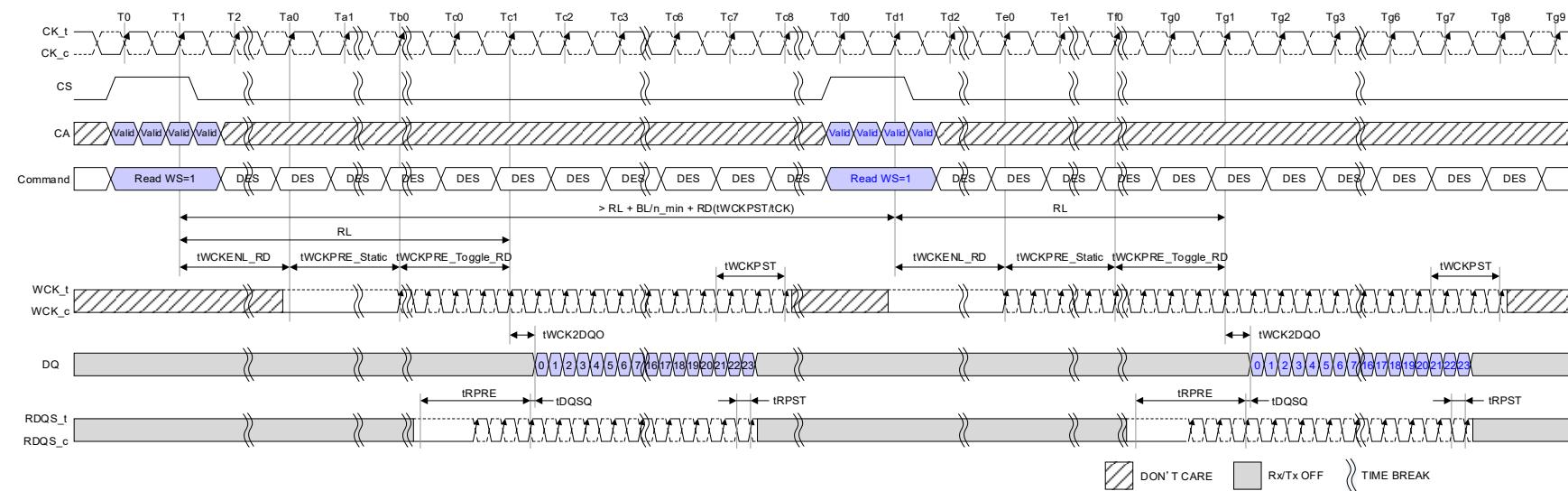
When the command gap between two Read commands is larger than  $RL + BL/n_{min} + RD(tWCKPST/tCK)$ , a new WCK2CK synchronization sequence is required.

NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2  $tWCK2CK$  is 0 ps in this instance.

NOTE 3  $BL=24$ ,  $tWCKPST=2.5tWCK$

Figure 84 shows the case when the command gap between two Read commands is larger than  $RL + BL/n_{min} + RD(tWCKPST/tCK)$ .



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

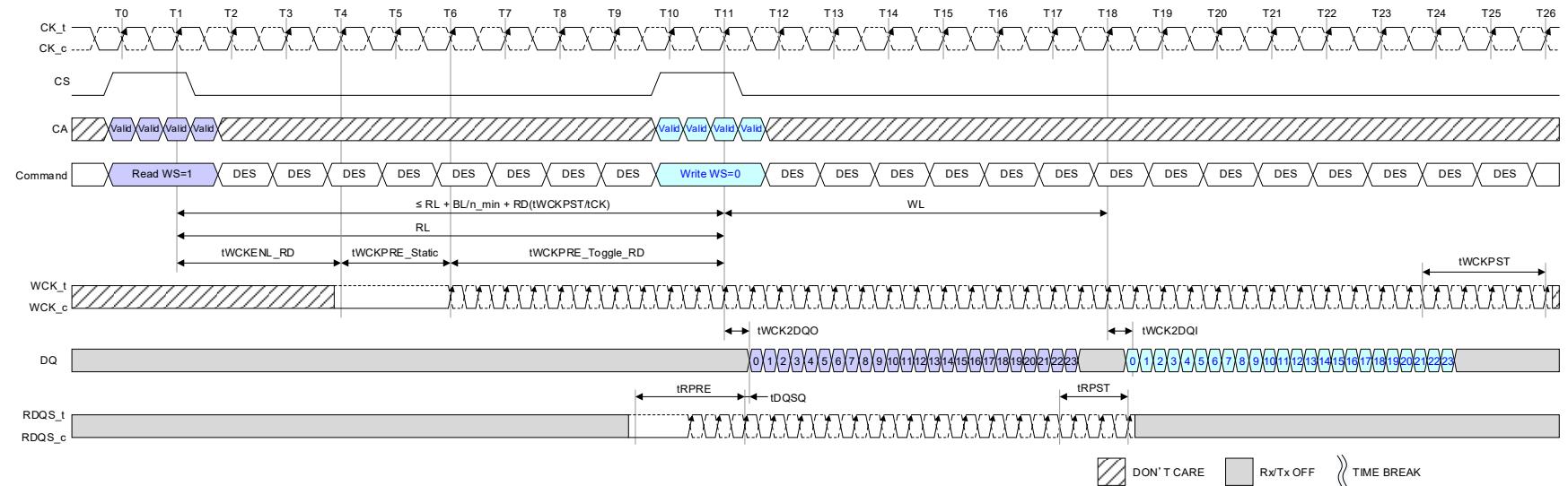
NOTE 2  $tWCK2CK$  is 0 ps in this instance.

NOTE 3  $BL=24$ ,  $tWCKPST=2.5tWCK$

**Figure 84 – Back to Back Read Operation with Additional WCK2CK Sync Sequence**

#### 7.5.1.2.4 Read Operation followed by Write Operation without Additional WCK2CK-sync

When the command gap between from Read command to Write command is larger than tRTW and equal or less than RL + BL/n\_min + RD(tWCKPST/tCK), a WS=1 in Write command is not required and illegal, due to SDRAM is still in WCK2CK-sync state at Write command issued.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

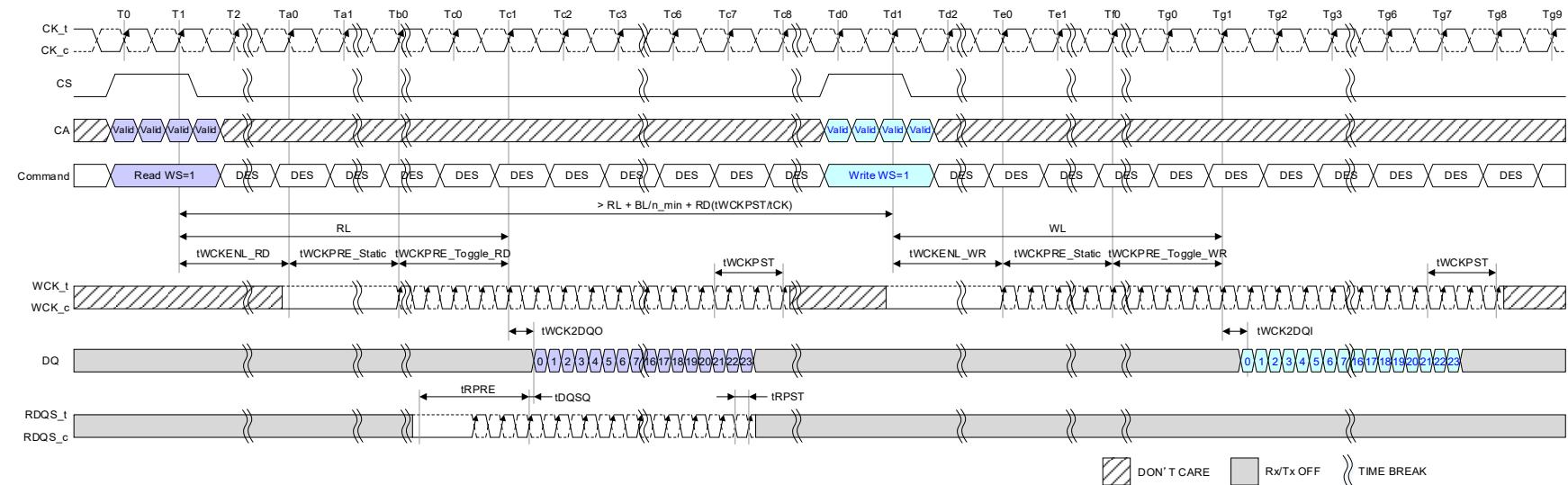
NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 tWCKENL\_RD=3, tWCKPRE\_Static=2, tWCKPRE\_toggle\_RD=5, RL=10, WL=7, BL=24, tWCKPST=4.5tWCK

Figure 85 – Read Operation followed by Write Operation without Additional WCK2CK-Sync Sequence

### 7.5.1.2.5 Read Operation followed by Write Operation with Additional WCK2CK-sync

When the command gap between from Read command to Write command is larger than  $RL + BL/n_{min} + RD(tWCKPST/tCK)$ , a new WCK2CK synchronization sequence is required. Figure 86 shows the case when the command gap between Read and Write is larger than  $RL + BL/n_{min} + RD(tWCKPST/tCK)$ .



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

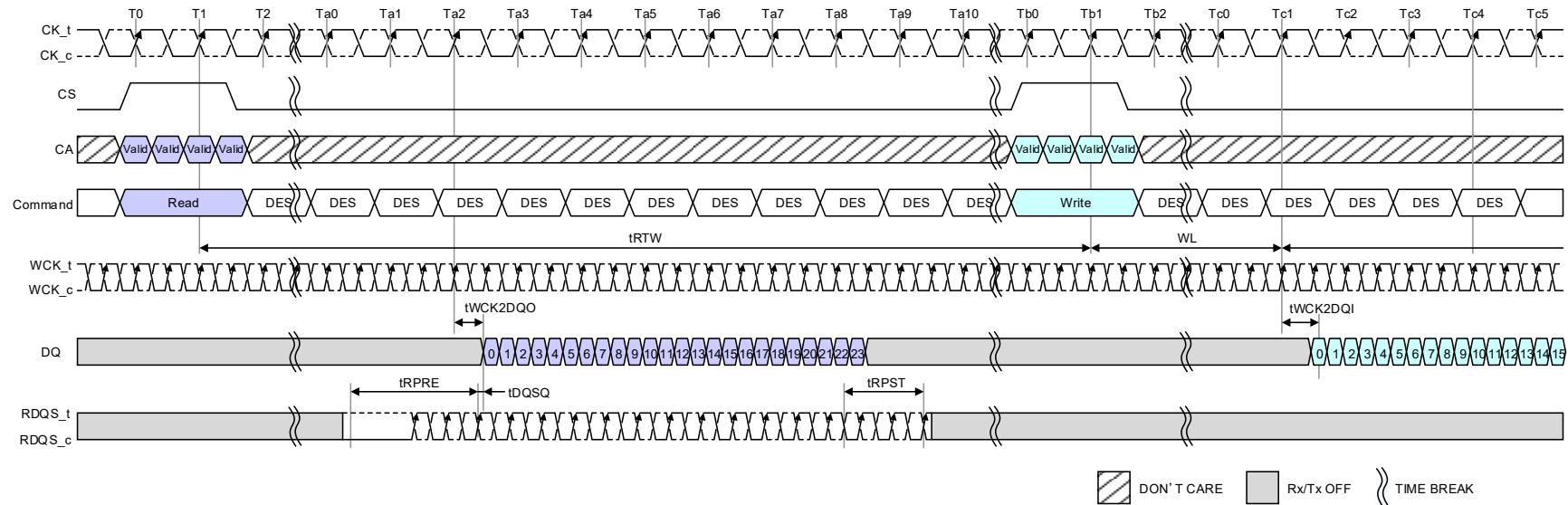
NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 BL=24, tWCKPST=2.5tWCK

**Figure 86 – Read Operation followed by Write Operation with Additional WCK2CK-sync Sequence**

### 7.5.1.2.6 Read Operation followed by Write Operation on WCK Always On Mode

The timing that a Write command following a Read command is issued on WCK Always on mode is below. Refer to clause 8.3.1: Read to Write Timing ( $t_{RTW}$ ) for detail on Read to Write timing.



NOTE 1 WCK2CK Sync state: WCK2CK Always on mode.

NOTE 2  $t_{WCK2CK}$  is 0 ps in this instance.

NOTE 3 BL=24,  $t_{RPRE}=2t_{WCK}$  (Static) +  $2t_{WCK}$  (Toggle),  $t_{RPST}=2.5t_{WCK}$  (Toggle)

NOTE 4 ODT/NT-ODT is disabled.

**Figure 87 – Burst Read followed by Burst Write**

### 7.5.1.3 RDQS Mode

For device operation at high clock frequencies, LPDDR6 SDRAM may be set into RDQS mode in which a READ DATA STROBE (or a pair of READ DATA STROBE) will be sent on RDQS\_t pin and RDQS\_c pin along with the READ data. SoC will use a single-ended RDQS or a differential RDQS to latch the READ data.

#### 7.5.1.3.1 RDQS Timing

Read timing with RDQS mode enabled is shown in Figure 88. Except the additional RDQS timing, all the timings are same as those of READ operation RDQS-related parameters, tDQSQ, tRPRE and tRPST are defined in Table 283.

RDQS is assumed as a differential pair, RDQS\_t and RDQS\_c in Figure 88.

The read latency (RL) is defined from the second rising edge of the CK\_t that starts a read command to the rising edge of the clock from which tWCK2DQO is measured. The first valid data is available for  $RL \cdot tCK + tWCK2CK + tWCK2DQO$  after the clock rising edge of a read command.

The first latching edge of RDQS will start later than the first valid data with "tDQSQ" delay.

RDQS requires a pre-amble prior at the first latching edge (the rising edge of RDQS with the first valid data), and it requires a post-amble after the last latching edge. The pre-amble (tRPRE) and post-amble (tRPST) time lengths are defined as parameters that can be set via mode register writes (MRW).

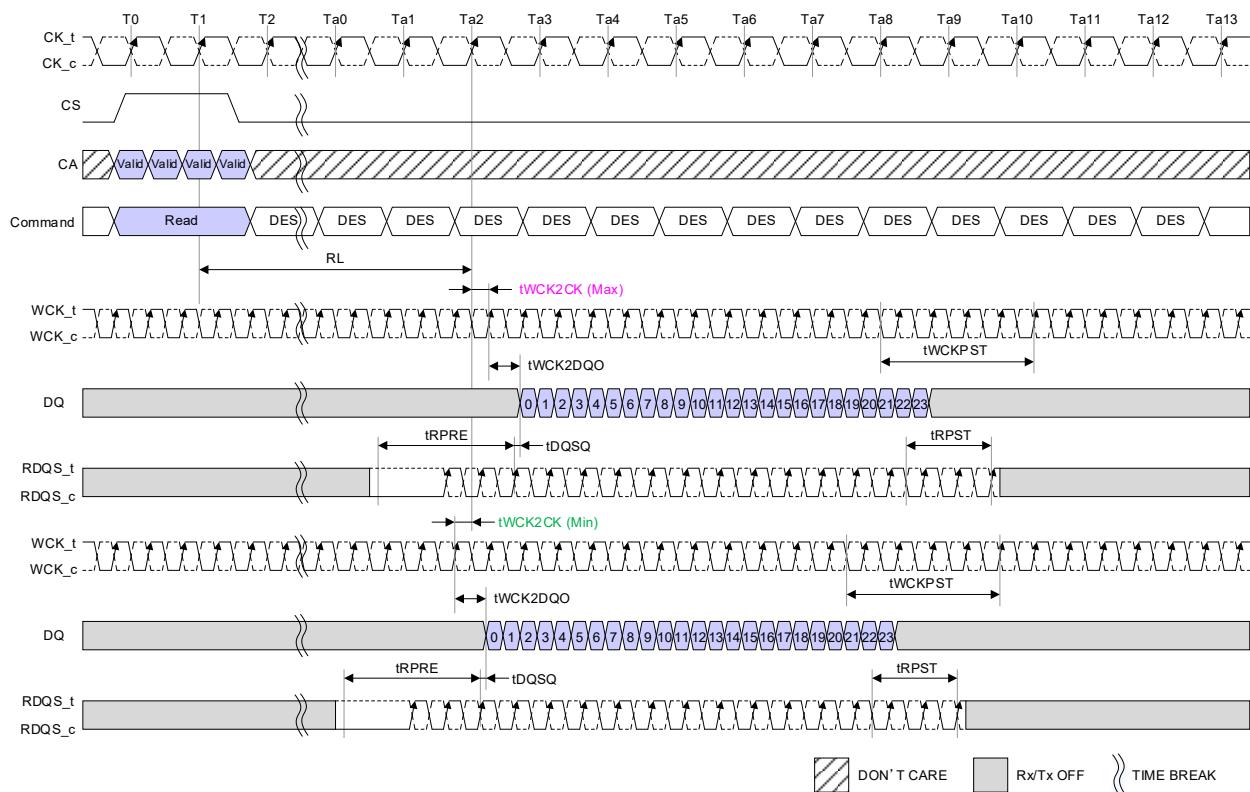
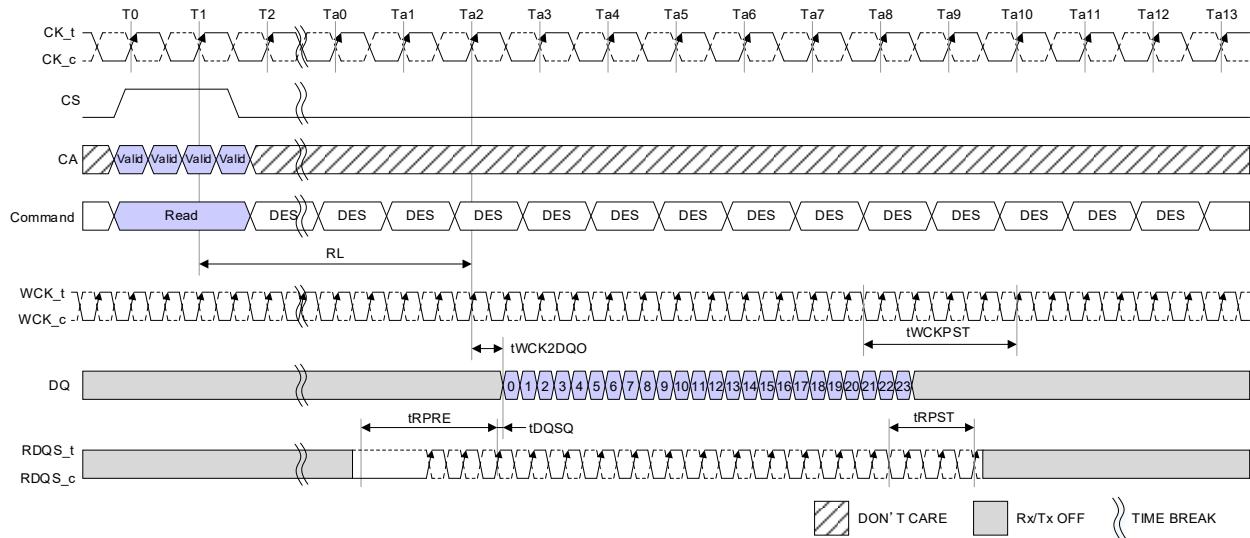


Figure 88 – Read Timing with RDQS and Related Timing Parameters

### 7.5.1.3.2 RDQS Related Functionalities

LPDDR6 SDRAM supports both a single-ended RDQS and a differential RDQS to help SoC to optimize power and performance. RDQS configuration is selected via mode register writes (MRW). RDQS\_t or RDQS\_c is used to send a read data strobe in a single-ended RDQS mode. RDQS\_c and RDQS\_t are used to send read data strobes in a differential RDQS mode. The examples of RDQS settings are shown in Figure 89, Figure 90, and Figure 91.



NOTE 1 MR22 OP[1:0] = 10<sub>B</sub>: RDQS\_t and RDQS\_c enabled.

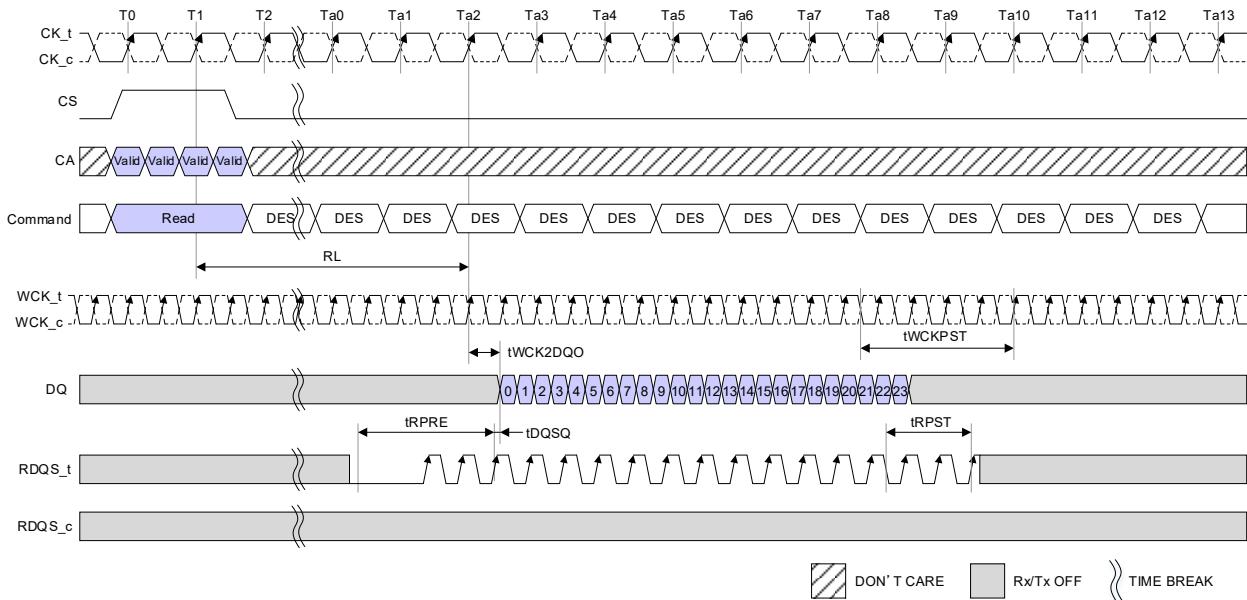
NOTE 2 WCK2CK in Sync state: WCK2CK Always on mode.

NOTE 3 tWCK2CK is 0 ps in this instance.

NOTE 4 BL=24, tPRE = 2tWCK (Static) + 2tWCK (Toggle), tPST = 2.5tWCK, tWPST = 4.5tWCK

**Figure 89 – Read Timing with Differential RDQS Mode**

### 7.5.1.3.2 RDQS Related Functionalities (cont'd)



NOTE 1 MR22 OP[1:0] = 01<sub>B</sub>: RDQS\_t enabled and RDQS\_c disabled.

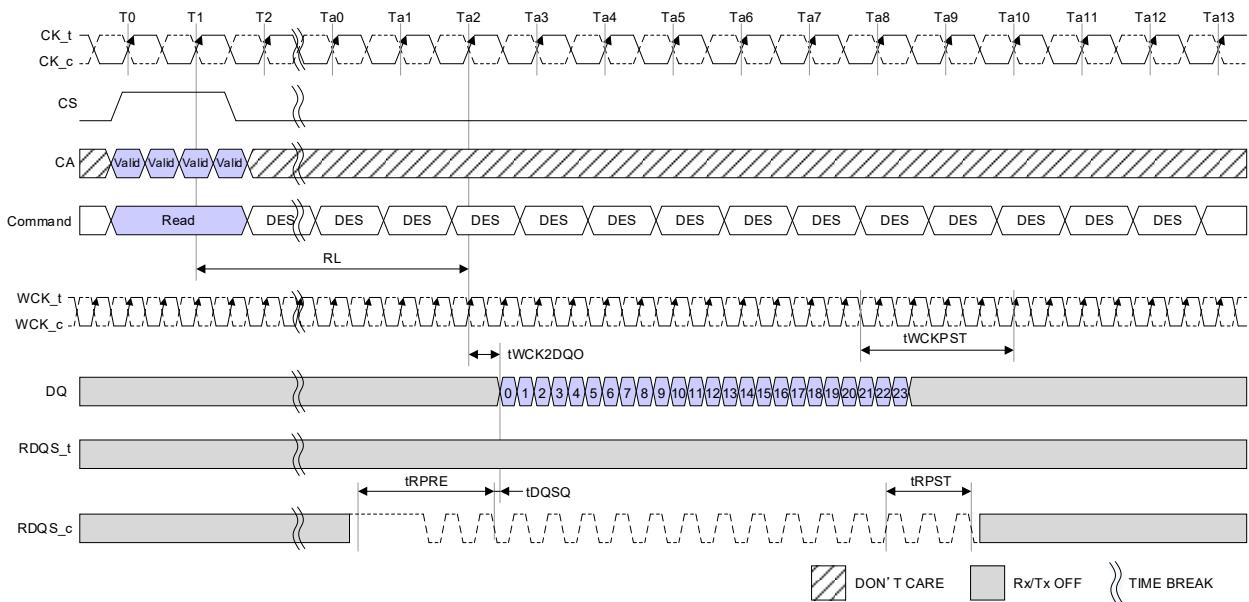
NOTE 2 WCK2CK in Sync state: WCK2CK Always on mode.

NOTE 3 tWCK2CK is 0 ps in this instance.

NOTE 4 BL=24, tPRE = 2tWCK (Static) + 2tWCK (Toggle), tRPST = 2.5tWCK, tWCKPST = 4.5tWCK

**Figure 90 – Read Timing with Single-ended RDQS\_t Mode**

### 7.5.1.3.2 RDQS Related Functionalities (cont'd)



NOTE 1 MR22 OP[1:0] = 11<sub>B</sub>: RDQS\_t disabled and RDQS\_c enabled.

NOTE 2 WCK2CK in Sync state: WCK2CK Always on mode.

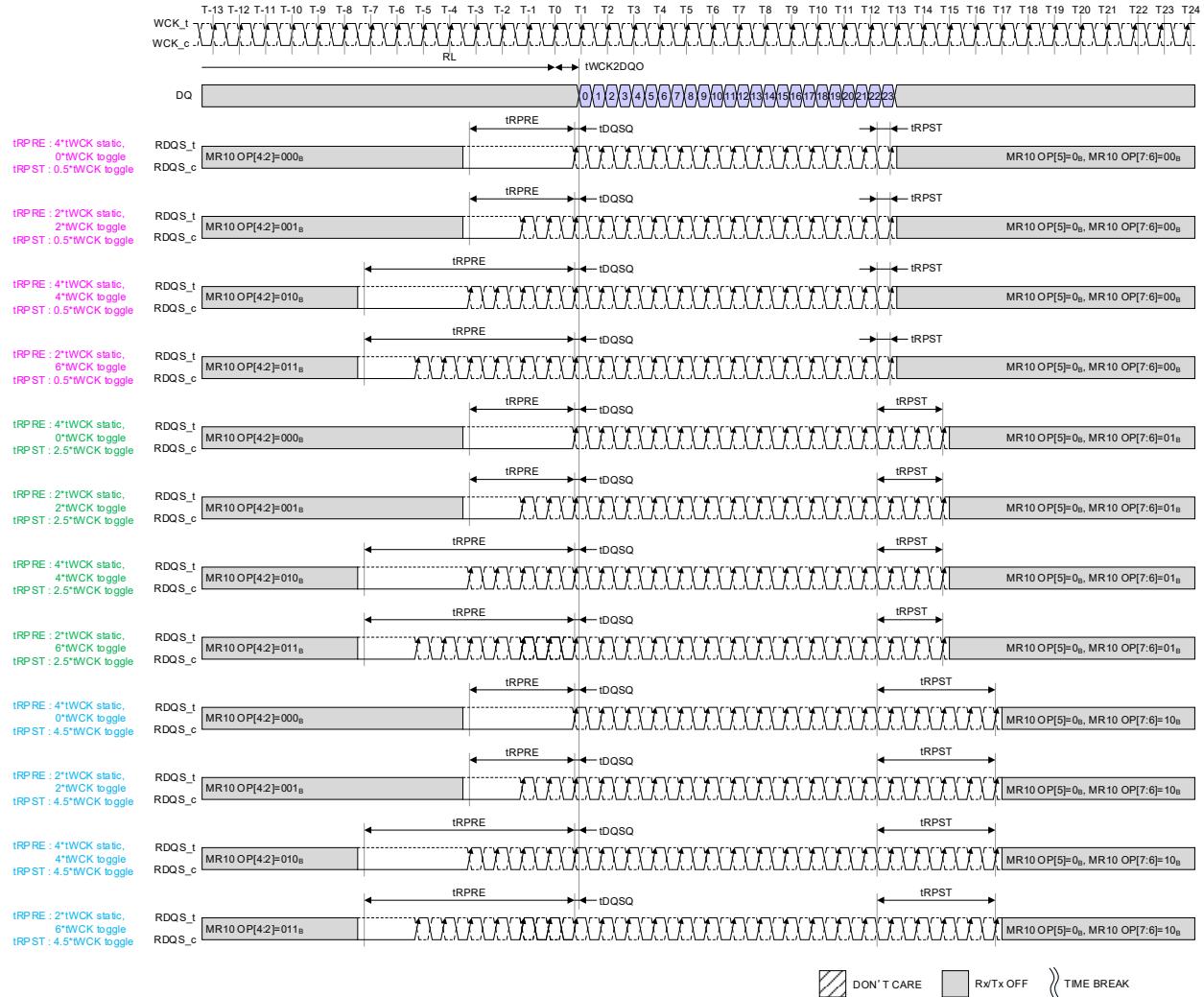
NOTE 3 tWCK2CK is 0 ps in this instance.

NOTE 4 BL=24, tPRE = 2tWCK (Static) + 2tWCK (Toggle), tRPST = 2.5tWCK, tWCKPST = 4.5tWCK

**Figure 91 – Read Timing with Single-ended RDQS\_c Mode**

### 7.5.1.3.3 RDQS Pre Shift

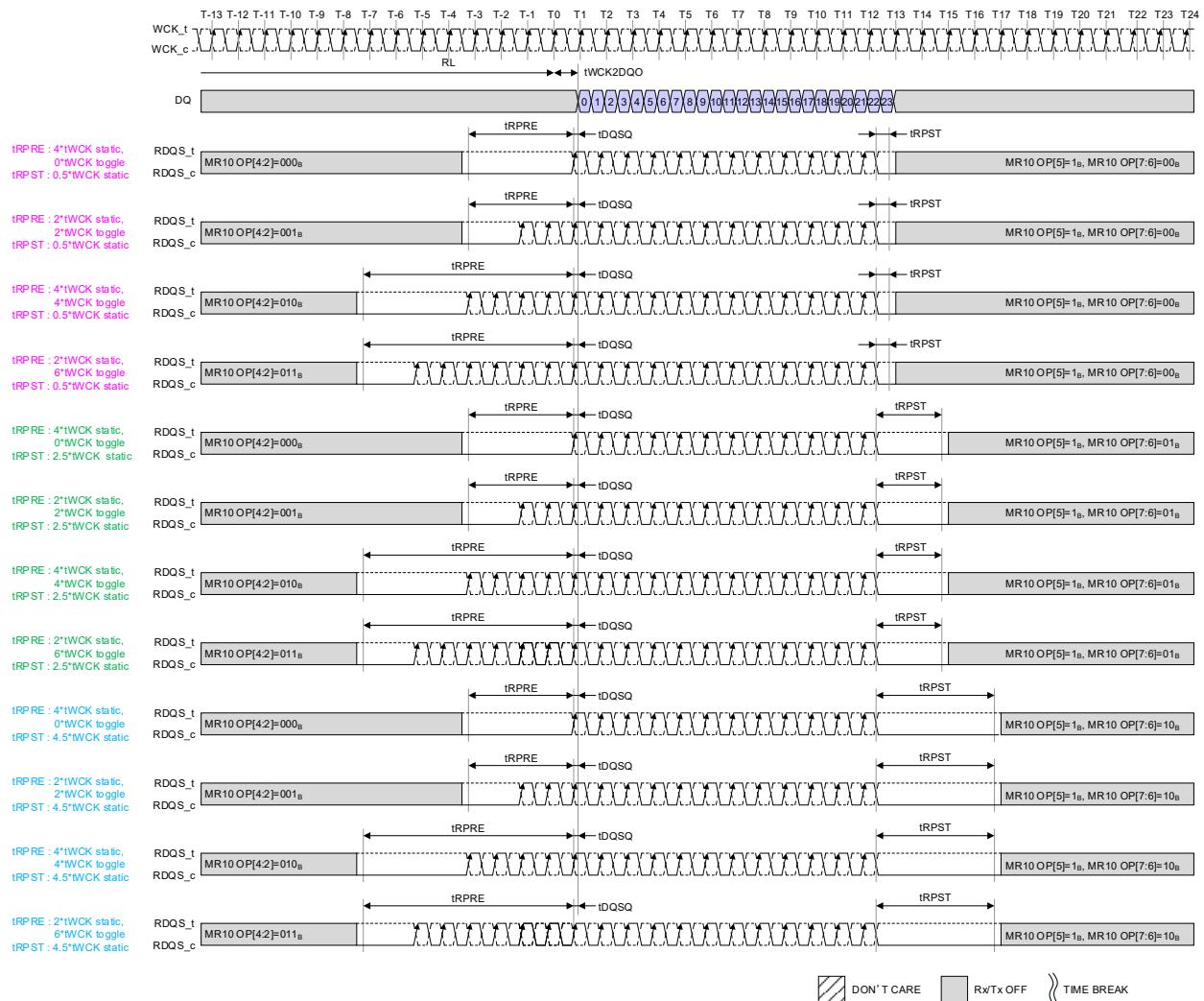
LPDDR6 SDRAM supports programmable option to drive RDQS early by nWCK for low power host architecture to compensate extra delay on the path of RDQS propagation path compared to DQ.



NOTE 1 RDQS Pre-Shift: MR10 OP[0]=0<sub>b</sub>; 0\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=0<sub>b</sub>; 1:1 ratio

Figure 92 – RDQS Read Preamble and Toggle Postamble with Pre-Shift = 0\*tWCK

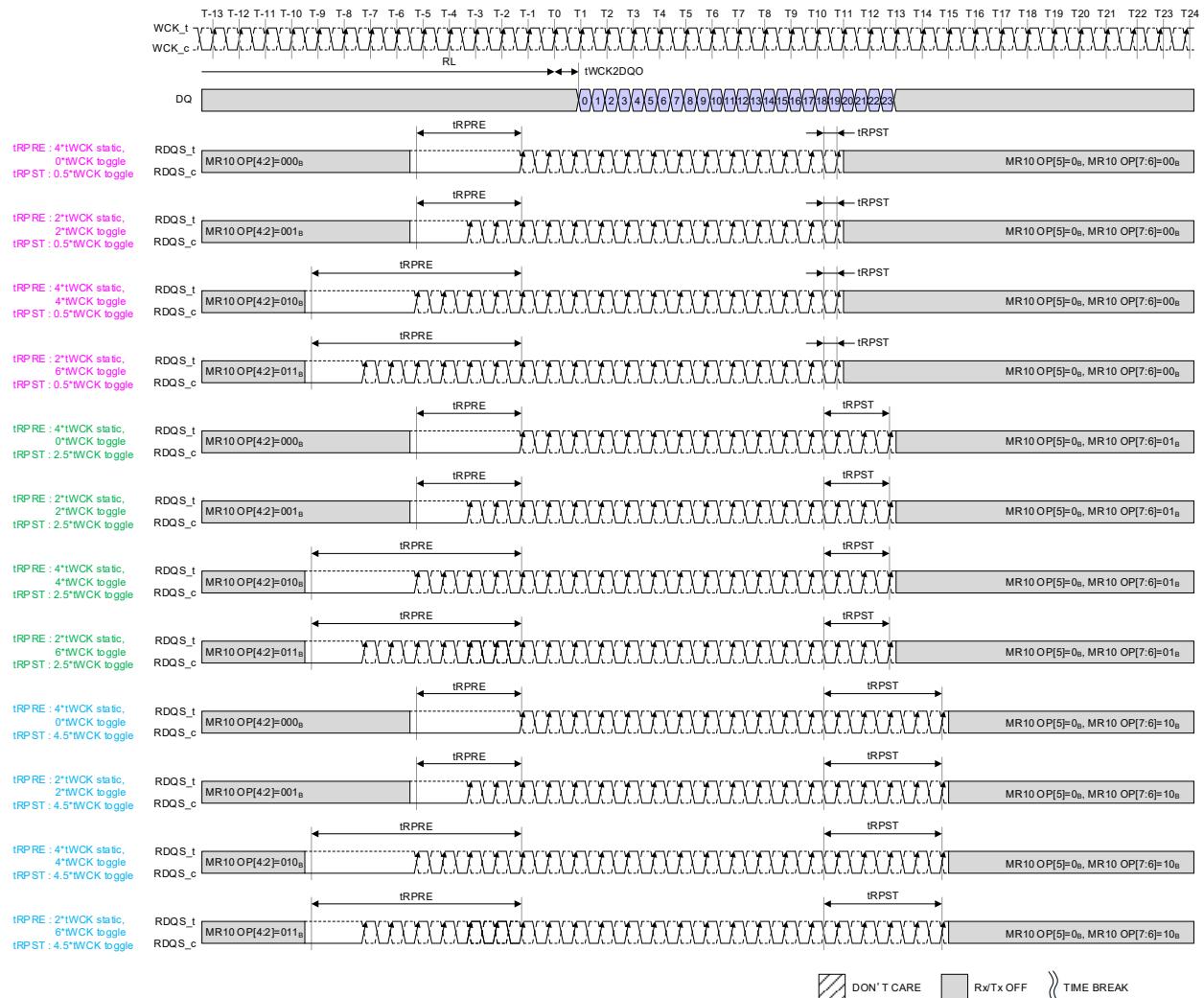
### 7.5.1.3.3 RDQS Pre Shift (cont'd)



NOTE 1 RDQS Pre-Shift: MR10 OP[0]=0<sub>B</sub>: 0\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=0<sub>B</sub>: 1:1 ratio

**Figure 93 – RDQS Read Preamble and Static Postamble with Pre-Shift = 0\*tWCK**

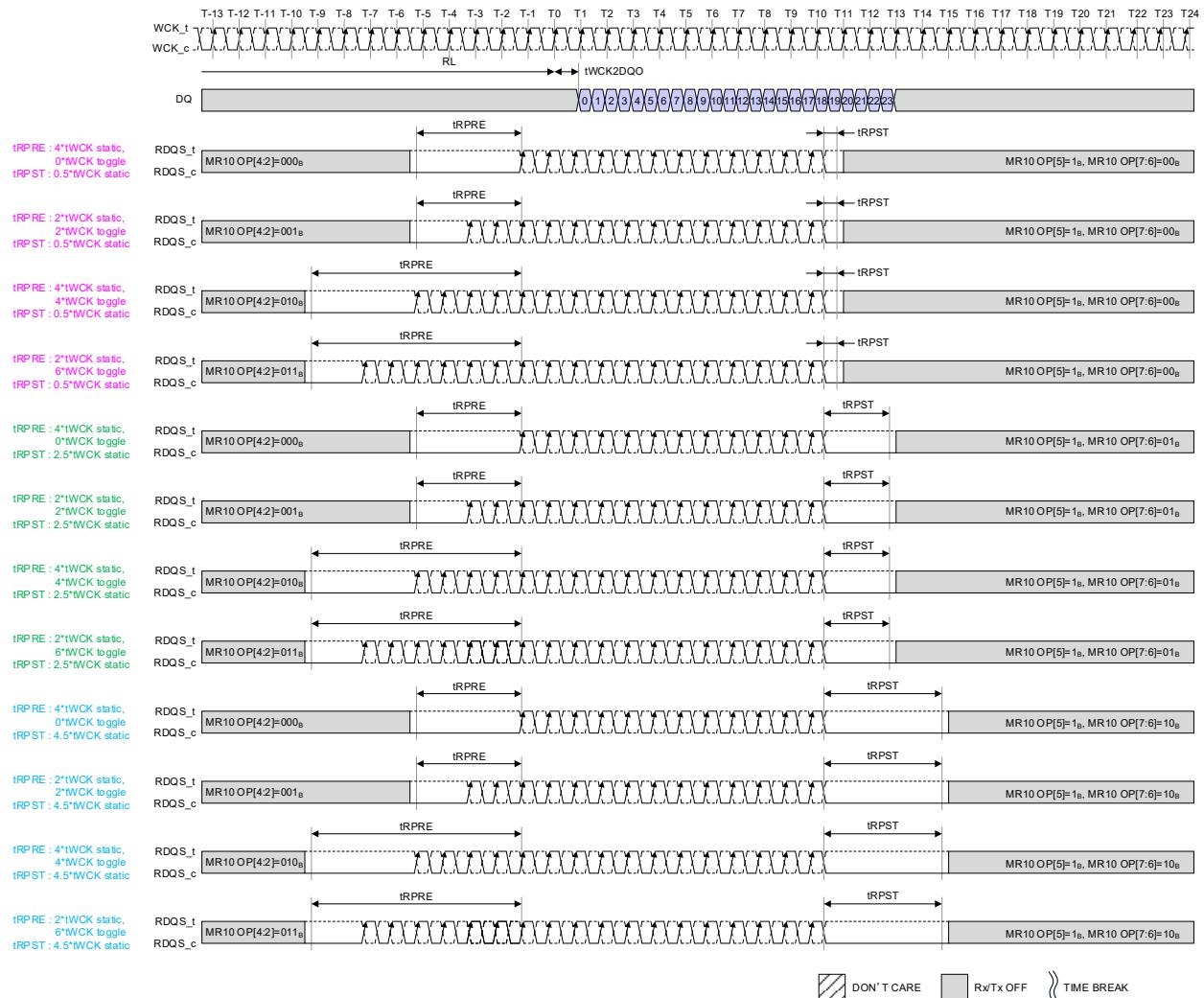
### 7.5.1.3.3 RDQS Pre Shift (cont'd)



NOTE 1 RDQS Pre-Shift: MR10 OP[0]=1<sub>b</sub>: 2\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=0<sub>b</sub>: 1:1 ratio

**Figure 94 – RDQS Read Preamble and Toggle Postamble with Pre-Shift = 2\*tWCK**

### 7.5.1.3.3 RDQS Pre Shift (cont'd)

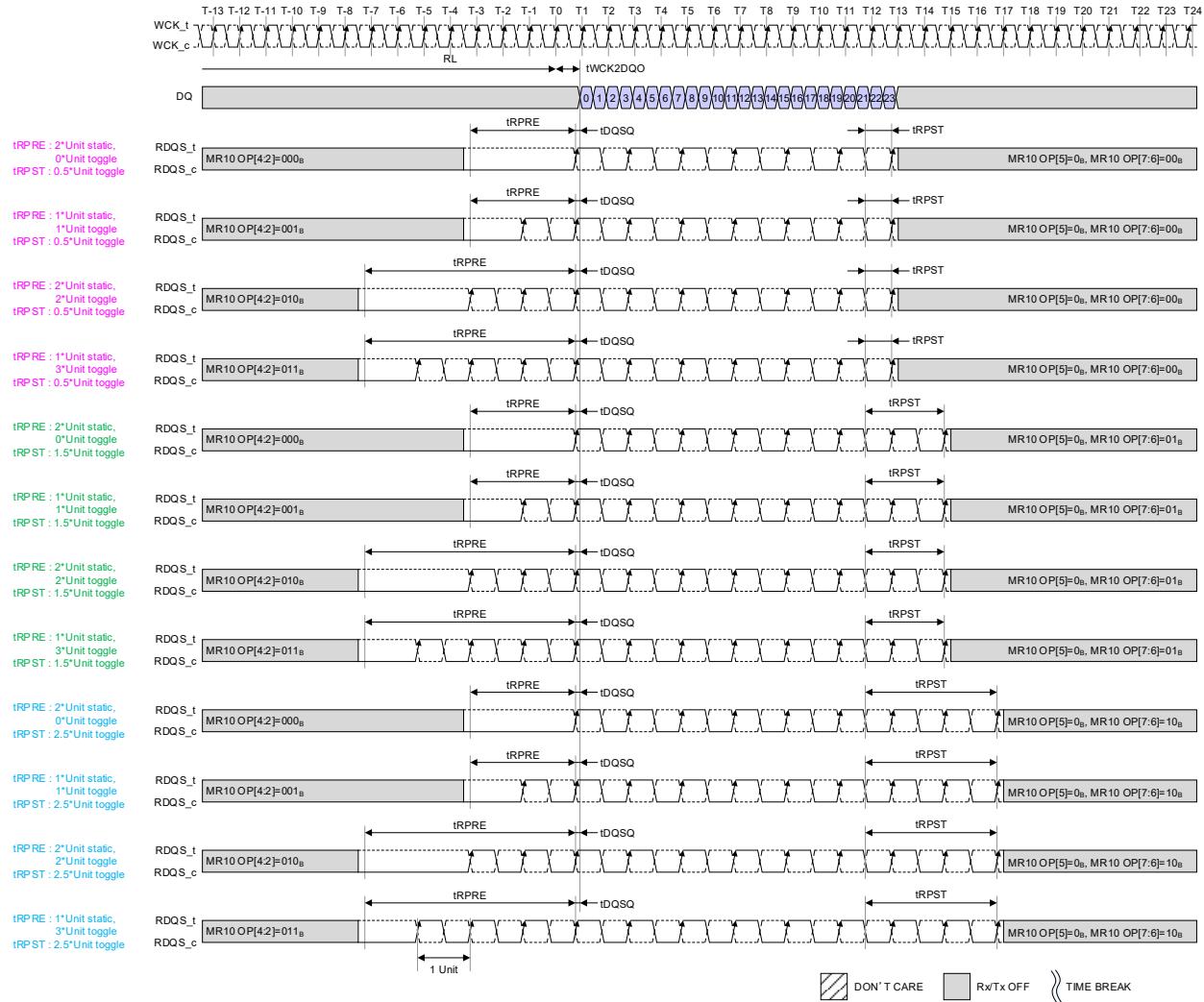


NOTE 1 RDQS Pre-Shift:  $MR10\ OP[0]=1_B$ :  $2^*tWCK$ ,  
RDQS to WCK Ratio:  $MR10\ OP[1]=0_B$ : 1:1 ratio

Figure 95 – RDQS Read Preamble and Static Postamble with Pre-Shift =  $2^*tWCK$

### 7.5.1.3.4 RDQS Half Rate Toggle Setting

RDQS RT (RDQS to WCK Ratio) is programmed in MR10 OP[1].

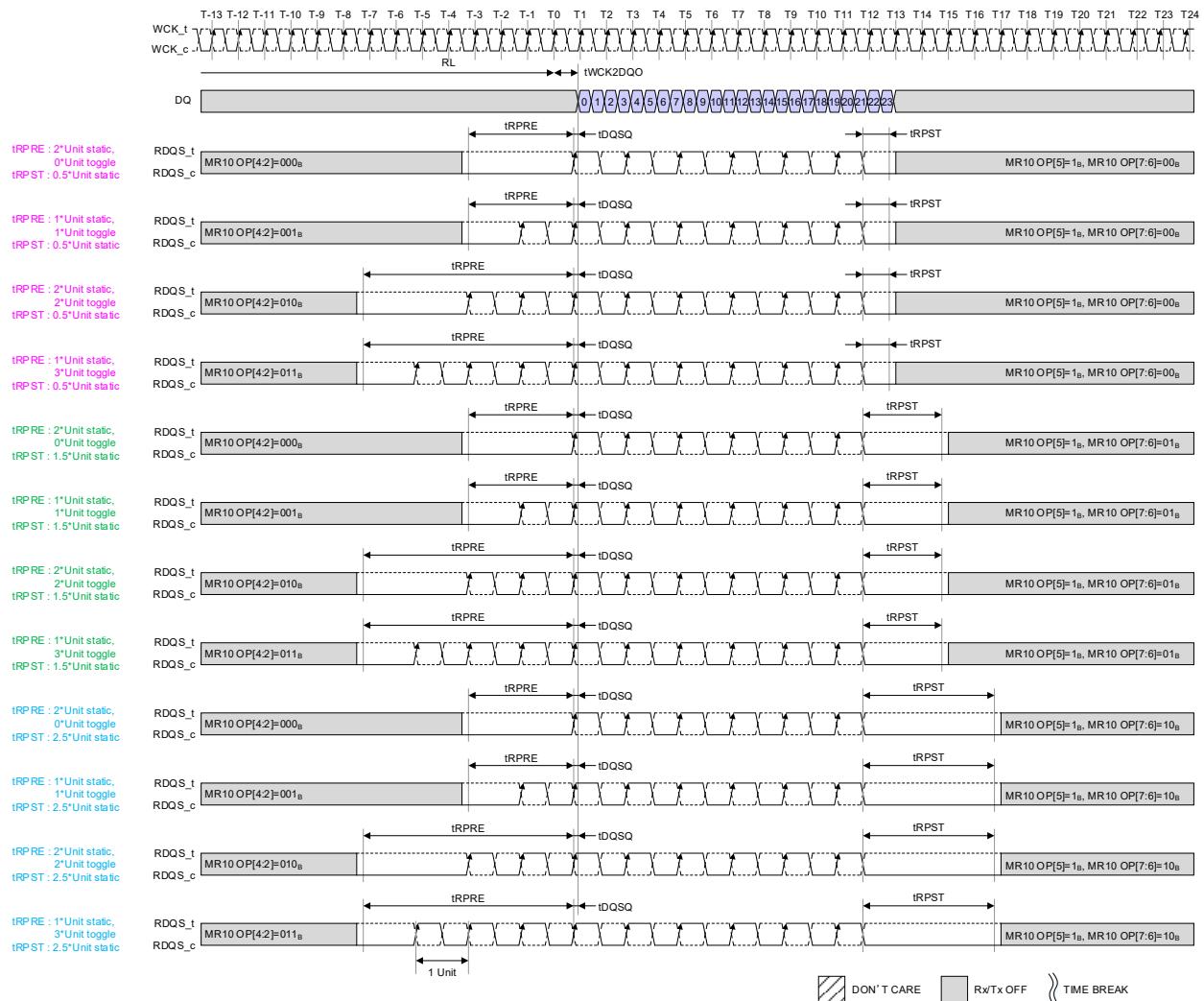


NOTE 1 RDQS 1 Unit = 2tWCK.

NOTE 2 RDQS Pre-Shift: MR10 OP[0]=0<sub>b</sub>: 0\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=1<sub>b</sub>: 2:1 ratio

Figure 96 – RDQS Read Preamble and Toggle Postamble with Pre-Shift = 0\*tWCK

#### 7.5.1.3.4 RDQS Half Rate Toggle Setting (cont'd)

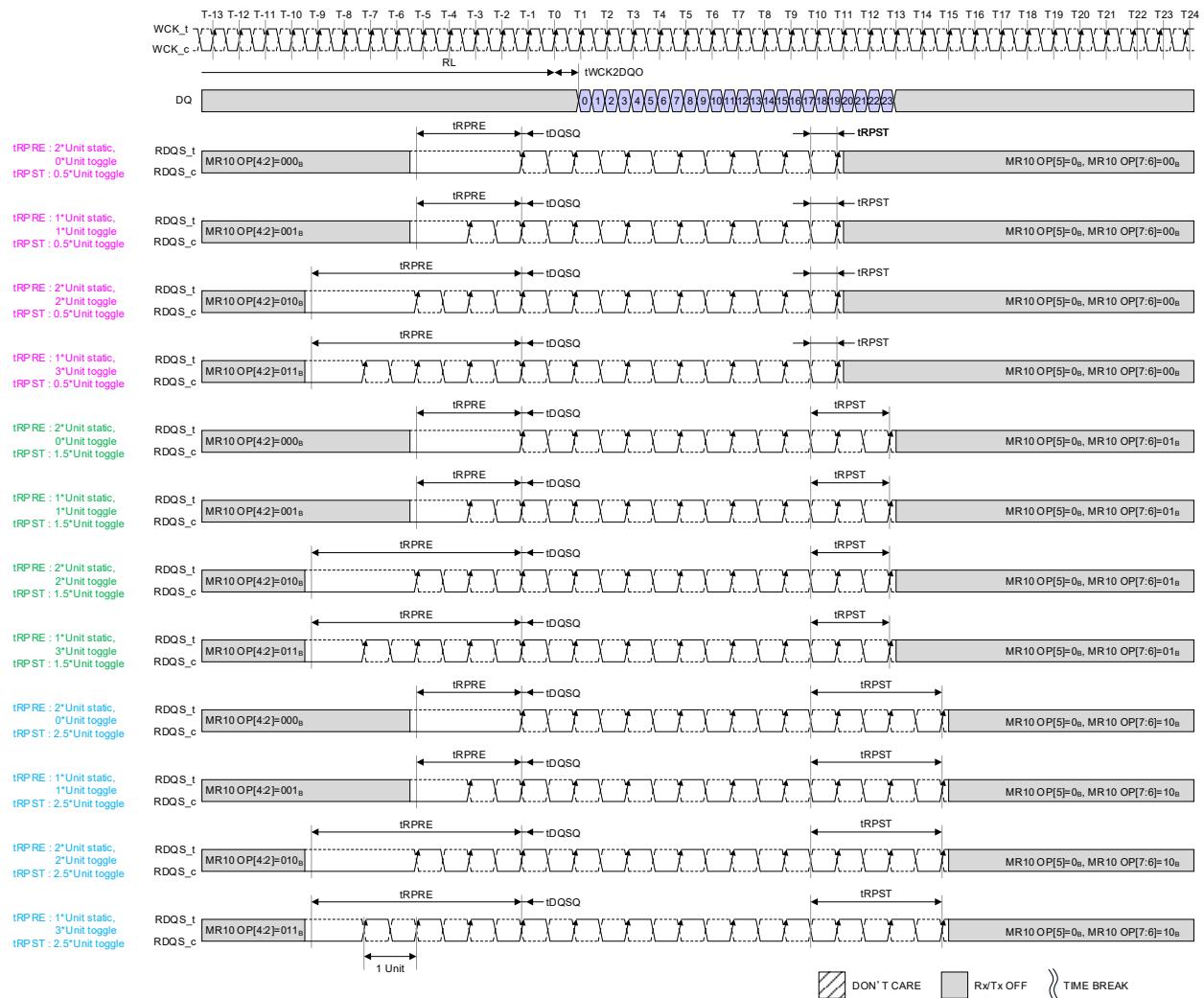


NOTE 1 RDQS 1 Unit = 2tWCK.

NOTE 2 RDQS Pre-Shift: MR10\_OP[0]=0<sub>B</sub>: 0\*tWCK,  
RDQS to WCK Ratio: MR10\_OP[1]=1<sub>B</sub>: 2:1 ratio

Figure 97 – RDQS Read Preamble and Static Postamble with Pre-Shift = 0\*tWCK

### 7.5.1.3.4 RDQS Half Rate Toggle Setting (cont'd)

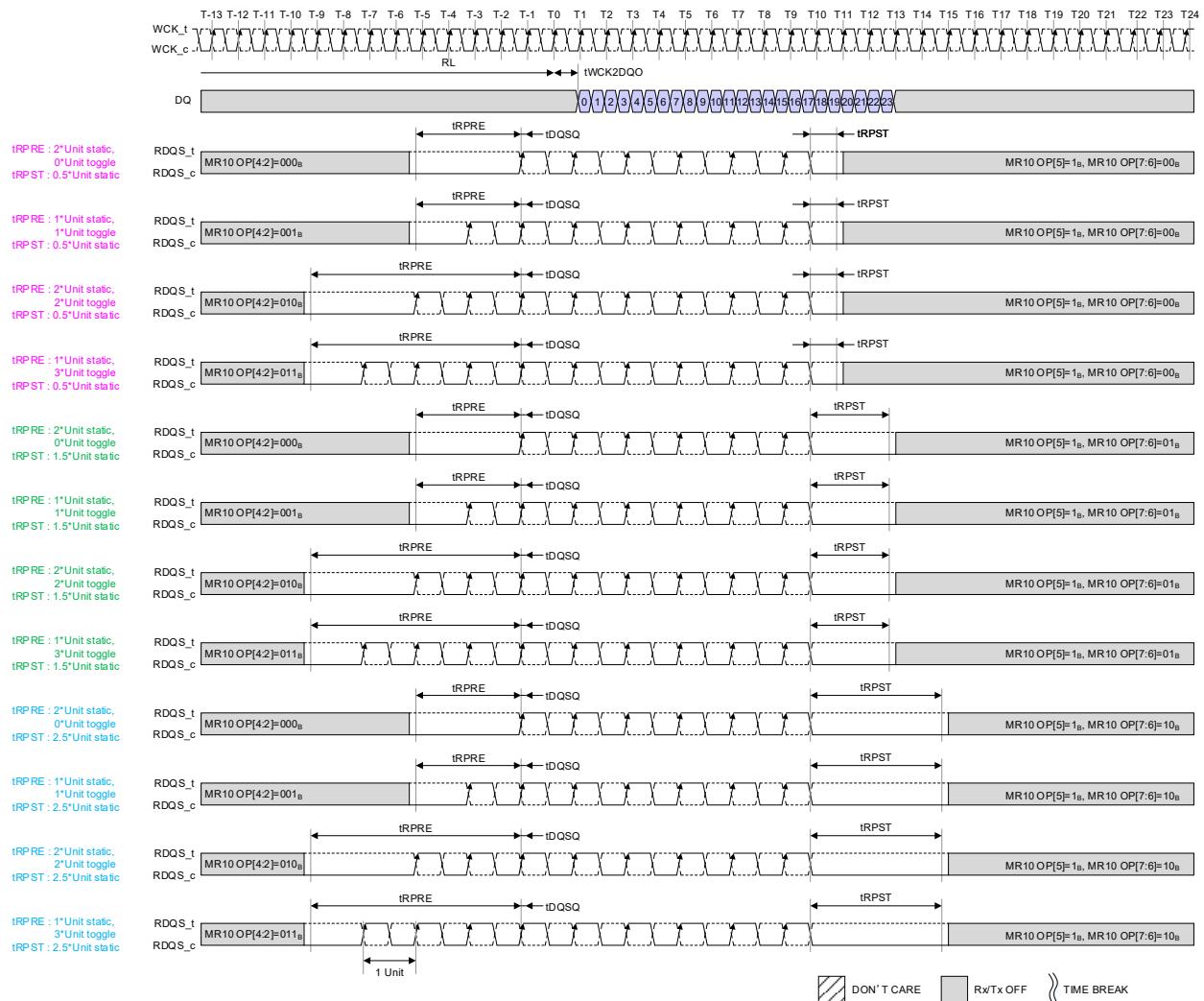


NOTE 1 RDQS 1 Unit = 2tWCK.

NOTE 2 RDQS Pre-Shift: MR10 OP[0]=1B: 2\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=1B: 2:1 ratio

Figure 98 – RDQS Read Preamble and Toggle Postamble with Pre-Shift = 2\*tWCK

#### 7.5.1.3.4 RDQS Half Rate Toggle Setting (cont'd)



NOTE 1 RDQS 1 Unit = 2tWCK.

NOTE 2 RDQS Pre-Shift: MR10 OP[0]=1<sub>B</sub>: 2\*tWCK,  
RDQS to WCK Ratio: MR10 OP[1]=1<sub>B</sub>: 2:1 ratio

Figure 99 – RDQS Read Preamble and Static Postamble with Pre-Shift = 2\*tWCK

### 7.5.1.3.5 RDQS Pattern Definition

Need to Update

**Table 282 – RDQS Pattern Definition**


### 7.5.1.3.6 Mode Registers for RDQS

The length and type of RDQS pre-amble can be determined by MR10 OP [4:2]. The length of RDQS post-amble can be determined by MR10 OP [7:6]. The specific number is TBD. RDQS mode configuration can also be changed by MR22 OP [1:0]. When MR22 OP [1:0] =00<sub>B</sub>, RDQS mode will not be supported, and SOC should latch the read data with its own internal clock. Single-ended RDQS mode and differential RDQS mode can be selected by setting OP [1:0] to 01<sub>B</sub>, 10<sub>B</sub>, and 11<sub>B</sub> each.

**Table 283 – RDQS Timing Parameters**

Parameter	Symbol	Min/Max	Value	Unit	Note
READ preamble	tRPRE	Min	TBD	tWCK	
READ post amble	tRPST	Min	TBD	tWCK	
RDQS_c low impedance time from CK_t, CK_c	tLZ (DQS)	Min	TBD	ps	
RDQS_c high impedance time from CK_t, CK_c	tHZ (DQS)	Max	TBD	ps	
RDQS-DQ skew	tDQSQ	Max	TBD	ps	

## 7.5.2 Write Operation

After a bank has been activated, the Write Operation causes LPDDR6 SDRAM to take in input data and write to its array. The Write Operation is initiated by the Write Command during which the beginning column address and Bank/Bank group address for the data to be taken into the array is provided. The data is received by the SDRAM on its DQ pins WL cycles after the Write Command.

LPDDR6 SDRAM requires a WCK post-amble after completing all write DQ bursts. The length of WCK post-amble can be set by mode register.

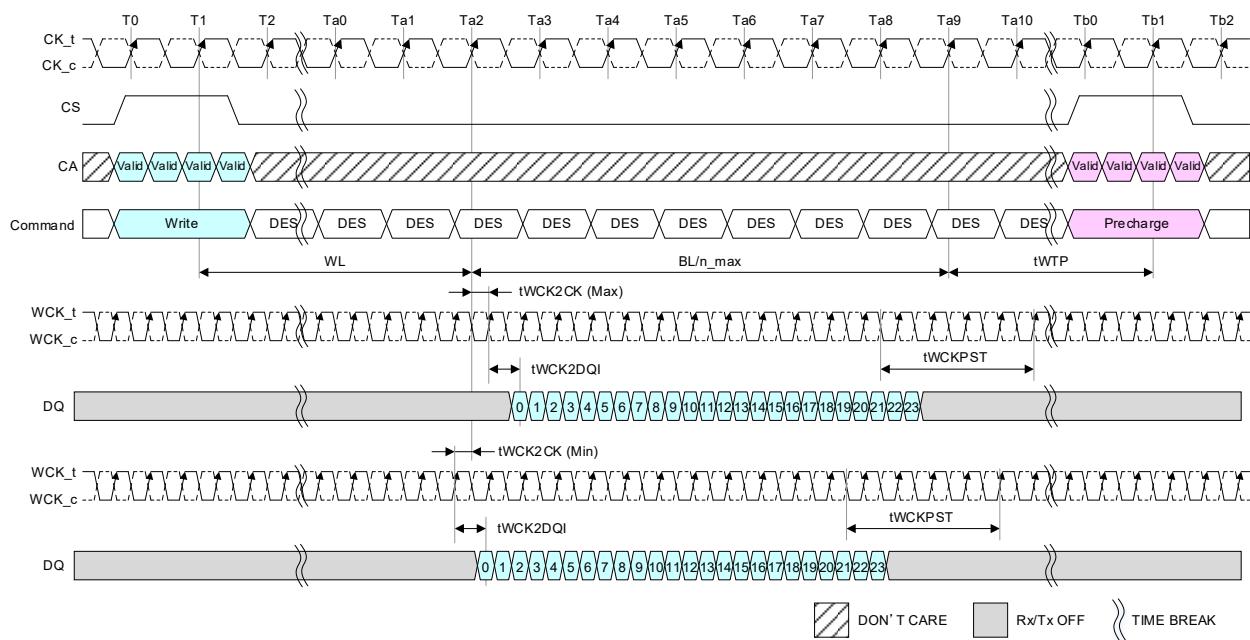
### 7.5.2.1 Burst Write Operation

An LPDDR6 SDRAM requires to be in WCK2CK synchronization state before the internal write operation starts and WCK post-amble is needed after all write DQ burst.

Refer to clause 7.3.1 - WCK2CK Synchronization operation for detail on WCK2CK synchronization and WCK postamble.

### 7.5.2.1.1 Write Timing

A WRITE command is initiated with CS, and CA[3:0] asserted to the proper state at the rising and falling edges of CK, as defined by the Command Truth Table, Table 254. LPDDR6 SDRAM write command does not support burst ordering, so that the starting column burst address is always aligned with a 32B boundary. The write latency (WL) is defined from the 2nd rising edge of the CK\_t that starts a write command to the rising edge of the CK\_t from which ( $t_{WCK2CK} + t_{WCK2DQI}$ ) is measured. The first valid “latching” edge of WCK is required to be driven WL \* tCK +  $t_{WCK2CK}$  after the rising edge of CK\_t that completes a write command. The LPDDR6 SDRAM uses an un-matched WCK-DQ path for lower power, so the WCK is required to arrive at the SDRAM ball prior to the DQ signal by the amount of  $t_{WCK2DQI}$ . The WCK is required to be trained to arrive at the DQ pad center-aligned with the DQ-data. The DQ-data is required to be held for tDIVW (data input valid window) and the WCK is required to be periodically trained to stay centered in the tDIVW window to compensate for timing changes due to temperature and voltage variation. Burst data is captured by the SDRAM on successive edges of WCK until the 24 or 48 bit data burst is complete. The WCK is required to remain active (toggling) for tWCKPST (WCK postamble) after the completion of the burst WRITE. After a burst WRITE operation, tWTP is required to be satisfied before a PRECHARGE command to the same bank can be issued. Pin input timings are measured relative to the crosspoint of WCK\_t and WCK\_c.



NOTE 1 WCK2CK Sync state.

NOTE 2 BL=24,  $t_{WCKPST}=4.5nWCK(Toggle)$

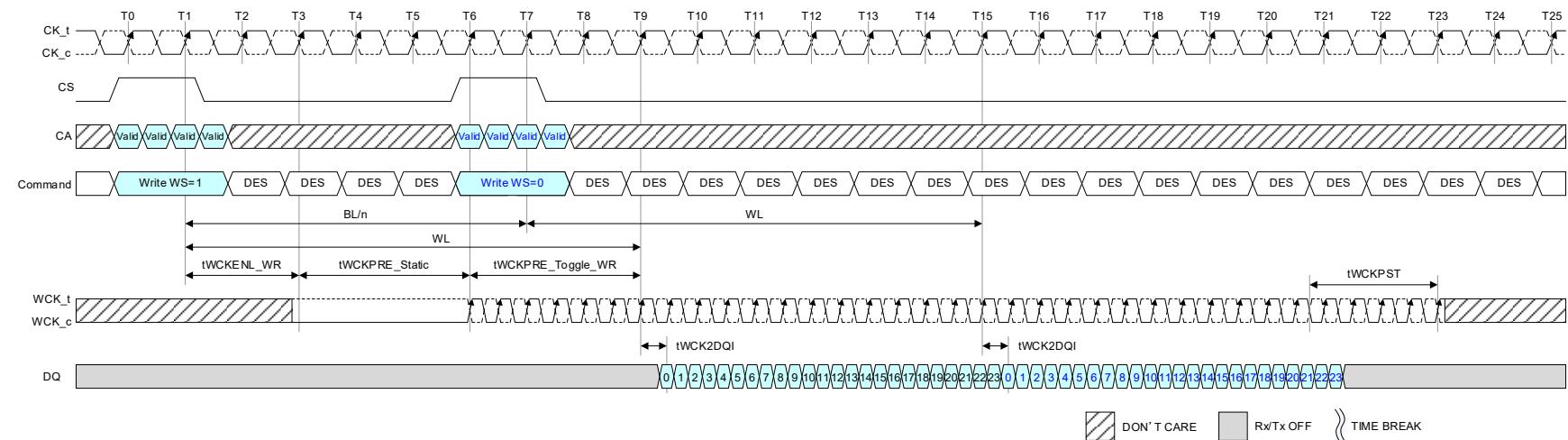
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 100 – Burst Write Operation

### 7.5.2.1.2 Write to Write Operation without Additional WCK2CK-sync

Figure 101 shows timing diagram of back to back write operation with BL/n. First Write command should be with WS=1, making the SDRAM in WCK2CK-sync state. Second Write command is not required WS=1, because the WCK2CK-sync state continues until WL + BL/n\_min + RD(tWCKPST/tCK).

Additionally, issuing WCK2CK synchronization command which operand: WS=1 is prohibited during WCK2CK sync state. Therefore WS=1 at second Write command is illegal.

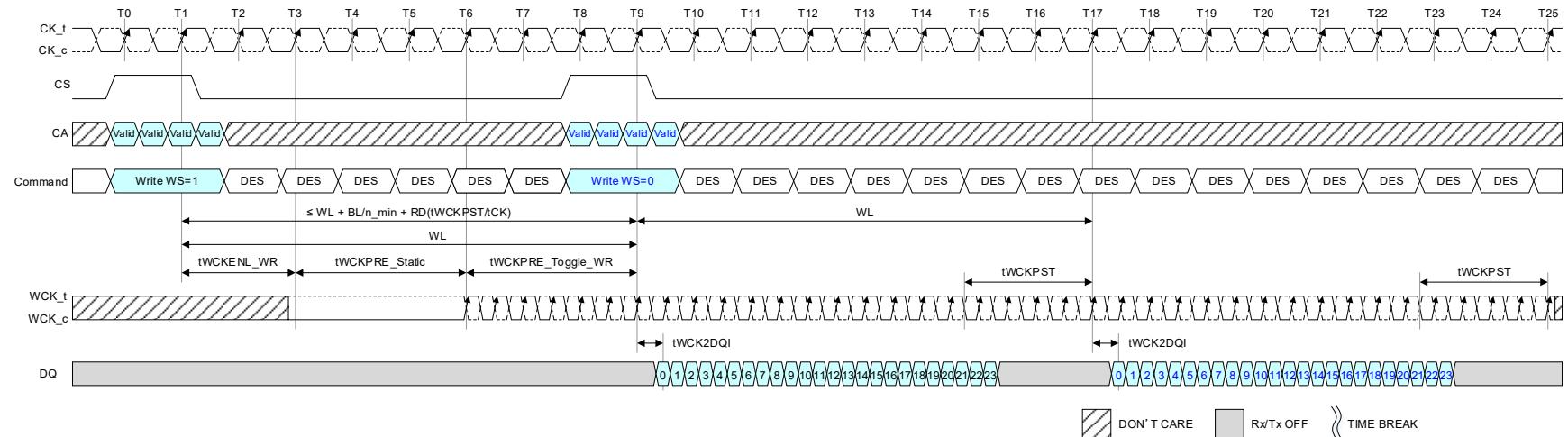


- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 2 tWCK2CK is 0 ps in this instance.
- NOTE 3 tWCKENL\_WR=2, tWCKPRE\_Static=3, tWCKPRE\_Toggle\_WR=3, WL=8, BL=24, tWCKPST=4.5tWCK

**Figure 101 – Back to Back Write Operation with BL/n**

### 7.5.2.1.2 Write to Write Operation without Additional WCK2CK-sync (cont'd)

When the command gap between two Write commands is larger than  $BL/n$  and equal or less than  $WL + BL/n_{min} + RD(tWCKPST/tCK)$ , a WS=1 in second Write command is not required and illegal, due to SDRAM is still in WCK2CK-sync state at second Write command issued.



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

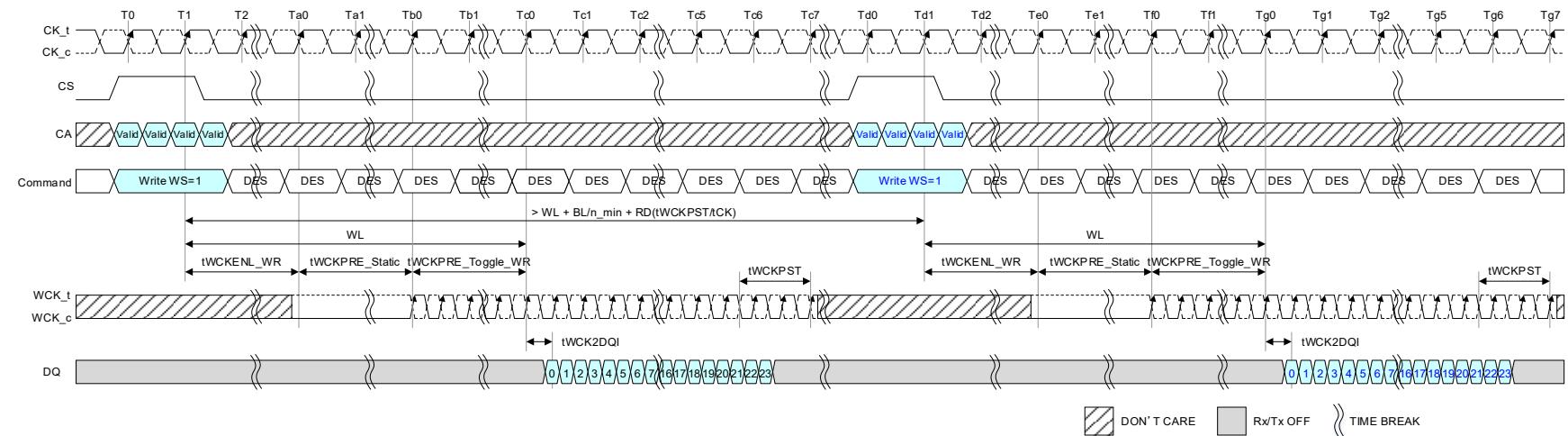
NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 tWCKENL\_WR=2, tWCKPRE\_Static=3, tWCKPRE\_Toggle\_WR=3, WL=8, BL=24, tWCKPST=4.5tWCK

Figure 102 – Back to Back Write Operation without Additional WCK2CK Sync Sequence

### 7.5.2.1.3 Write to Write Operation with Additional WCK2CK-sync

When the command gap between two write commands is larger than  $WL + BL/n_{min} + RD(tWCKPST/tCK)$ , a new WCK2CK synchronization sequence is required. Figure 103 shows the case when the command gap between two write commands is larger than  $WL + BL/n_{max} + RD(tWCKPST/tCK)$ .



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

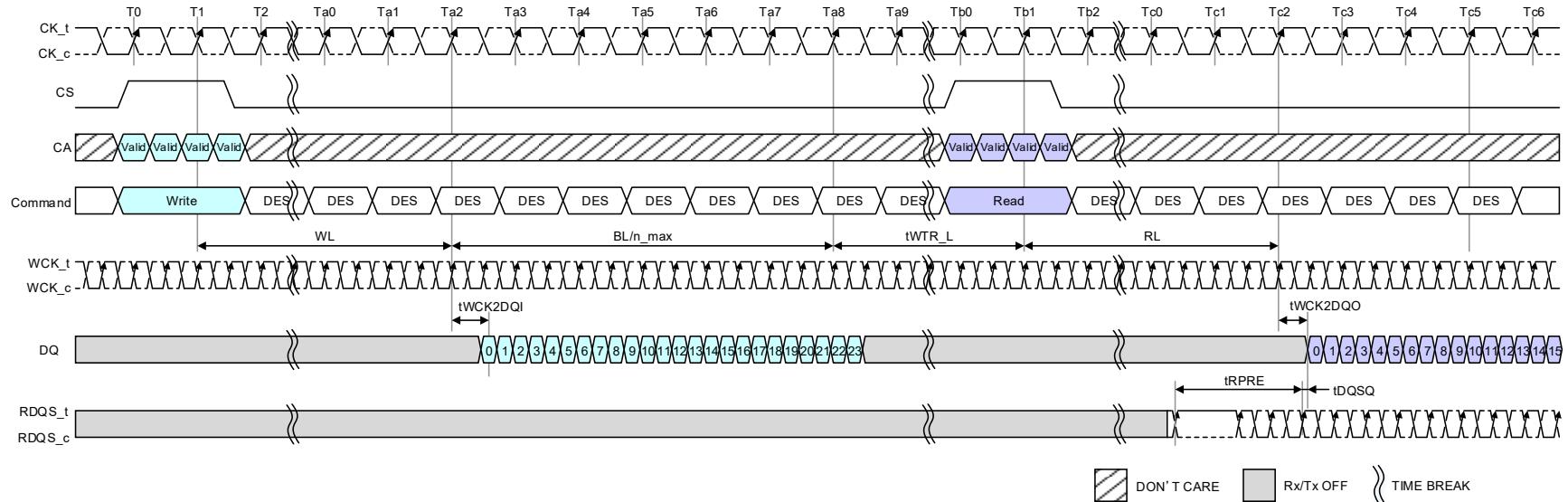
NOTE 2 tWCK2CK is 0 ps in this instance.

NOTE 3 BL=24, tWCKPST=2.5tWCK

Figure 103 – Back to Back Write Operation Requiring a New WCK2CK Sync Sequence

#### 7.5.2.1.4 Write Operation followed by Read Operation

When a read command follows a write command, the minimum gap between two commands is defined as  $\min(tWTR\_S/L)$ .  $tWTR\_L$  (Same BG) /  $tWTR\_S$  (Different BG) is measured from the rising edge of the CK\_t of 2nd command that satisfies WL + BL/n\_max +  $tWTR\_L$  (Same BG) / WL + BL/n\_min +  $tWTR\_S$  (Different BG) respectively after a write command to the following read command.



NOTE 1 WCK2CK Sync state: WCK2CK Always on mode.

NOTE 2  $tWCK2CK$  is 0 ps in this instance.

NOTE 3  $BL=24$

NOTE 4 DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 104 – Write Operation followed by Read Operation: Read and Write to the Same BG

### 7.5.3 Read and Read-to-Precharge Latencies

Latencies related to Read timing are measured from the second rising edge of CK\_t of the Read command. The Read Latencies depend on the settings of DVFSL, Read Link protection, and Efficiency mode Disable/Enable.

For each MR1 OP[4:0] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

**Table 284 – Read Latencies Tables Summary**

Table	Link protection	DVFSL
Table 269	Disable	Disable
Table 270	Enable	Disable
Table 271	Disable	Enable
Table 272	Enable	Enable

### 7.5.3.1 Read and Read-to-Precharge Latencies (cont'd)

**Table 285 – Read Latencies for Link Protection is Disabled and DVFSL is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRTP [nCK]
					Set 0	Set 1	Set 2	
00000 <sub>B</sub>	80	1067	20	267	7	7	8	TBD
00001 <sub>B</sub>	1067	1600	267	400	9	10	11	TBD
00010 <sub>B</sub>	1600	2133	400	533	12	13	14	TBD
00011 <sub>B</sub>	2133	2750	533	688	15	17	18	TBD
00100 <sub>B</sub>	2750	3200	688	800	17	19	21	TBD
00101 <sub>B</sub>	3200	3750	800	938	20	22	24	TBD
00110 <sub>B</sub>	3750	4267	938	1067	23	25	28	TBD
00111 <sub>B</sub>	4267	4800	1067	1200	26	28	31	TBD
01000 <sub>B</sub>	4800	5500	1200	1375	30	32	35	TBD
01001 <sub>B</sub>	5500	6400	1375	1600	34	37	41	TBD
01010 <sub>B</sub>	6400	7500	1600	1875	40	44	48	TBD
01011 <sub>B</sub>	7500	8533	1875	2133	46	50	54	TBD
01100 <sub>B</sub>	8533	9600	2133	2400	52	56	62	TBD
01101 <sub>B</sub>	9600	10667	2400	2667	56	62	68	TBD
01110 <sub>B</sub>	10667	11733	2667	2933	TBD	TBD	TBD	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD	TBD	TBD	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD	TBD	TBD	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Read DBI	Static/Dynamic Efficiency mode	Apply
Disable	Disable	Set 0
Enable	Disable	Set 1
Disable	Enable	Set 1
Enable	Enable	Set 2

### 7.5.3.1 Read and Read-to-Precharge Latencies (cont'd)

**Table 286 – Read Latencies for Link Protection is Enabled and DVFSL is Disabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRTP [nCK]
					Set 0	Set 1	
00000 <sub>B</sub>	80	1067	20	267	7	8	TBD
00001 <sub>B</sub>	1067	1600	267	400	11	11	TBD
00010 <sub>B</sub>	1600	2133	400	533	14	15	TBD
00011 <sub>B</sub>	2133	2750	533	688	17	19	TBD
00100 <sub>B</sub>	2750	3200	688	800	20	22	TBD
00101 <sub>B</sub>	3200	3750	800	938	23	25	TBD
00110 <sub>B</sub>	3750	4267	938	1067	26	28	TBD
00111 <sub>B</sub>	4267	4800	1067	1200	29	32	TBD
01000 <sub>B</sub>	4800	5500	1200	1375	33	36	TBD
01001 <sub>B</sub>	5500	6400	1375	1600	39	42	TBD
01010 <sub>B</sub>	6400	7500	1600	1875	46	50	TBD
01011 <sub>B</sub>	7500	8533	1875	2133	52	56	TBD
01100 <sub>B</sub>	8533	9600	2133	2400	58	64	TBD
01101 <sub>B</sub>	9600	10667	2400	2667	64	70	TBD
01110 <sub>B</sub>	10667	11733	2667	2933	TBD	TBD	TBD
01111 <sub>B</sub>	11733	12800	2933	3200	TBD	TBD	TBD
10000 <sub>B</sub>	12800	14400	3200	3600	TBD	TBD	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Static/Dynamic Efficiency mode	Apply
Disable	Set 0
Enable	Set 1

### 7.5.3.1 Read and Read-to-Precharge Latencies (cont'd)

**Table 287 – Read Latencies for Link Protection is Disabled and DVFSL is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency			nRTP [nCK]
					Set 0	Set 1	Set 2	
00000 <sub>B</sub>	80	1067	20	267	7	8	9	TBD
00001 <sub>B</sub>	1067	1600	267	400	10	11	12	TBD
00010 <sub>B</sub>	1600	2133	400	533	14	15	16	TBD
00011 <sub>B</sub>	2133	2750	533	688	17	19	21	TBD
00100 <sub>B</sub>	2750	3200	688	800	20	22	24	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Read DBI	Static/Dynamic Efficiency mode	Apply
Disable	Disable	Set 0
Enable	Disable	Set 1
Disable	Enable	Set 1
Enable	Enable	Set 2

### 7.5.3.1 Read and Read-to-Precharge Latencies (cont'd)

**Table 288 – Read Latencies for Link Protection is Enabled and DVFSL is Enabled**

MR1 OP[4:0]	Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	Read Latency		nRTP [nCK]
					Set 0	Set 1	
00000 <sub>B</sub>	80	1067	20	267	8	9	TBD
00001 <sub>B</sub>	1067	1600	267	400	12	13	TBD
00010 <sub>B</sub>	1600	2133	400	533	15	17	TBD
00011 <sub>B</sub>	2133	2750	533	688	19	21	TBD
00100 <sub>B</sub>	2750	3200	688	800	22	24	TBD

NOTE 1 The LPDDR6 SDRAM device should not be operated at a frequency above the upper frequency limit, or below the lower frequency limit, shown for each RL, or nRTP value.

NOTE 2 Some operating features can affect Read Latency:

Static/Dynamic Efficiency mode	Apply
Disable	Set 0
Enable	Set 1

#### 7.5.4 Write Latency

Latencies related to Write timing are measured from the second rising edge of CK\_t of the Write command.

For each MR1 OP[4:0] setting, device operation at less than the CK lower limit or higher than the CK upper limit is illegal.

**Table 289 – Write Latency**

MR1 OP[4:0]	Data Rate Range [Mbps]		CK Frequency Range [MHz]		WL		Unit
	Lower Limit (>)	Upper Limit ( $\leq$ )	Lower Limit (>)	Upper Limit ( $\leq$ )	Set A	Set B	
00000 <sub>B</sub>	80	1067	20	267	4	5 4	nCK
00001 <sub>B</sub>	1067	1600	267	400	6	7	nCK
00010 <sub>B</sub>	1600	2133	400	533	8	10	nCK
00011 <sub>B</sub>	2133	2750	533	688	8	13	nCK
00100 <sub>B</sub>	2750	3200	688	800	10	15	nCK
00101 <sub>B</sub>	3200	3750	800	938	12	18	nCK
00110 <sub>B</sub>	3750	4267	938	1067	12	21	nCK
00111 <sub>B</sub>	4267	4800	1067	1200	14	24	nCK
01000 <sub>B</sub>	4800	5500	1200	1375	16	28	nCK
01001 <sub>B</sub>	5500	6400	1375	1600	18	32	nCK
01010 <sub>B</sub>	6400	7500	1600	1875	20	38	nCK
01011 <sub>B</sub>	7500	8533	1875	2133	22	44	nCK
01100 <sub>B</sub>	8533	9600	2133	2400	24	50	nCK
01101 <sub>B</sub>	9600	10667	2400	2667	26	54	nCK
01110 <sub>B</sub>	10667	11733	2667	2933	TBD	TBD	nCK
01111 <sub>B</sub>	11733	12800	2933	3200	TBD	TBD	nCK
10000 <sub>B</sub>	12800	14400	3200	3600	TBD	TBD	nCK

### 7.5.5 Data Bus Inversion (DBI-DC) Function

LPDDR6 SDRAM supports the function of Data Bus inversion. Its details are shown below.

LPDDR6 device supports Data Bus Inversion (DBI-DC) function for Write and Read operation.

LPDDR6 device supports DBI-DC function with two bytes granularity.

DBI-DC function during Read can be enabled or disabled through MR3 OP[0].

DBI-DC function during Write can be enabled or disabled through MR3 OP[1].

LPDDR6 device supports Data Bus Inversion function via 16 metadata bits per 256 data bits in a data packet and sampled in Write operation or driven in Read operation. The metadata bits assignment is indicated in the data packet format (refer to clause 2.4)

### 7.5.5.1 Reference Data Packet Format

Generic data packet format assumes the below table. I[15:0] is DBI control bits when DBI is enabled.

**Table 290 – LPDDR6 Data Packet Format when DBI is Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	FIXL	FIXL	FIXL	FIXL	D144	D145	D146	D147	D192	D193	D194	D195	I0	I1	I2	I3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	FIXL	FIXL	FIXL	FIXL	D148	D149	D150	D151	D196	D197	D198	D199	I4	I5	I6	I7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	FIXL	FIXL	FIXL	FIXL	D168	D169	D170	D171	D216	D217	D218	D219	I8	I9	I10	I11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	FIXL	FIXL	FIXL	FIXL	D172	D173	D174	D175	D220	D221	D222	D223	I12	I13	I14	I15

#### **7.5.5.1 Reference Data Packet Format (cont'd)**

**Table 291 – LPDDR6 Data Packet Format when System Meta and DBI are Enabled**

	Beat																							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	D0	D1	D2	D3	D48	D49	D50	D51	D96	D97	D98	D99	D128	D129	D130	D131	D176	D177	D178	D179	D224	D225	D226	D227
DQ1	D4	D5	D6	D7	D52	D53	D54	D55	D100	D101	D102	D103	D132	D133	D134	D135	D180	D181	D182	D183	D228	D229	D230	D231
DQ2	D8	D9	D10	D11	D56	D57	D58	D59	D104	D105	D106	D107	D136	D137	D138	D139	D184	D185	D186	D187	D232	D233	D234	D235
DQ3	D12	D13	D14	D15	D60	D61	D62	D63	D108	D109	D110	D111	D140	D141	D142	D143	D188	D189	D190	D191	D236	D237	D238	D239
DQ4	D16	D17	D18	D19	D64	D65	D66	D67	M0	M1	M2	M3	D144	D145	D146	D147	D192	D193	D194	D195	I0	I1	I2	I3
DQ5	D20	D21	D22	D23	D68	D69	D70	D71	M4	M5	M6	M7	D148	D149	D150	D151	D196	D197	D198	D199	I4	I5	I6	I7
DQ6	D24	D25	D26	D27	D72	D73	D74	D75	D112	D113	D114	D115	D152	D153	D154	D155	D200	D201	D202	D203	D240	D241	D242	D243
DQ7	D28	D29	D30	D31	D76	D77	D78	D79	D116	D117	D118	D119	D156	D157	D158	D159	D204	D205	D206	D207	D244	D245	D246	D247
DQ8	D32	D33	D34	D35	D80	D81	D82	D83	D120	D121	D122	D123	D160	D161	D162	D163	D208	D209	D210	D211	D248	D249	D250	D251
DQ9	D36	D37	D38	D39	D84	D85	D86	D87	D124	D125	D126	D127	D164	D165	D166	D167	D212	D213	D214	D215	D252	D253	D254	D255
DQ10	D40	D41	D42	D43	D88	D89	D90	D91	M8	M9	M10	M11	D168	D169	D170	D171	D216	D217	D218	D219	I8	I9	I10	I11
DQ11	D44	D45	D46	D47	D92	D93	D94	D95	M12	M13	M14	M15	D172	D173	D174	D175	D220	D221	D222	D223	I12	I13	I14	I15

### 7.5.5.1.1 Metadata bits Behavior with Write Related Commands

**Table 292 – Metadata Bits Pin Behavior by Command and Support Function Setting for Write Related Commands**

Function			Metadata Bits Output Behavior	
System Meta MR92 OP[7]	Write DBI MR3 OP[1] MR93, MR94	Write Link EDC/ECC MR23 OP[1:0]	Write	Write FIFO CMD
Disable	Disable	Disable	M[15:0] and I[15:0] are ignored	Follows FIFO Definition
Disable	Disable	Enable	I[15:0] are sampled as Write Link ECC data, Fixed to low input.(M[15:0] are ignored)	Follows FIFO Definition
Disable	Enable	Disable	I[15:0] are sampled as DBI data, Fixed to low input.(M[15:0] are ignored)	Follows FIFO Definition
Disable	Enable	Enable	Prohibited setting	Prohibited setting
Enable	Disable	Disable	Fixed to low input.(I[15:0] are ignored), M[15:0] are sampled as System meta data	Follows FIFO Definition
Enable	Disable	Enable	I[15:0] are sampled as Write Link ECC data, M[15:0] are sampled as System meta data	Follows FIFO Definition
Enable	Enable	Disable	I[15:0] are sampled as DBI data, M[15:0] are sampled as System meta data	Follows FIFO Definition
Enable	Enable	Enable	Prohibited setting	Prohibited setting
<b>NOTE 1</b> Explanation of terminology in the cells: - Fixed low input: The input level is fixed to LOW. - Follows FIFO Definition: Metadata bits behavior follows WCK-DQ (FIFO) training definition. Write DBI and/or Write Link ECC functions are disabled regardless of MR setting. See 4.2.9 for details. - Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time. - DBI data input: I[15:0] is treated as DBI signal and it indicates whether LPDDR6 SDRAM needs to invert the Write data received on DQs within two bytes. The SDRAM inverts Write data received on the DQ inputs in case DBI input data was sampled HIGH, or leaves the Write data non-inverted in case DBI input data was sampled LOW. Total count of '1' data bits on each two-bytes section in a data packet, the Write data received on the DQ inputs, should less than or equal to eighth during Write DBI is enabled.				
<b>NOTE 2</b> In case Enhanced Write DBI function is enabled (MR3 Op[1]=1 <sub>B</sub> , MRW operations to MR93 and MR94 with non-default values), each DBI bit selects one of two Mode Registers (0 <sub>B</sub> for MR93[0:7], 1 <sub>B</sub> for MR94[0:7]) for enhanced Write DBI operations. The selected Mode Register's 8bit operands are applied to bit-wise XOR operations with corresponding Write data bits.				

### 7.5.5.1.2 Metadata bits Behavior with Read and MRR Command

**Table 293 – Metadata Bits Behavior by Command and Support Function Setting for Read and MRR Command**

Function			Metadata bits Output Behavior	
System Meta MR92 OP[7]	Read DBI MR3 OP[0]	Read Link EDC/ECC MR23 OP[2]	Read	Mode Register Read
Disable	Disable	Disable	Fixed low output	Fixed low output
Disable	Disable	Enable	I[15:0] are as Read Link ECC data output, M[15:0] are fixed low output	Valid data output
Disable	Enable	Disable	I[15:0] are as DBI data output, M[15:0] are fixed low output	Fixed low output
Disable	Enable	Enable	Prohibited setting	Prohibited setting
Enable	Disable	Disable	I[15:0] are fixed low output, M[15:0] are as System meta output	Fixed low output
Enable	Disable	Enable	I[15:0] are as Read Link ECC data output, M[15:0] are as System meta output	Valid data output
Enable	Enable	Disable	I[15:0] are as DBI data output, M[15:0] are as System meta output	Fixed low output
Enable	Enable	Enable	Prohibited setting	Prohibited setting
NOTE 1 Explanation of terminology in the cells.				
<ul style="list-style-type: none"> <li>- Follows Link ECC Definition: Metadata bits behavior follows Link ECC definition. See 7.8.21 for details.</li> <li>- Prohibited setting: Corresponding command issuing is prohibited in this mode register setting or enabling these functions are prohibited at the same time.</li> <li>- Valid data output: High or low data is outputted, and these output data are meaningless.</li> <li>- Fixed low output: The output level is fixed to LOW.</li> <li>- DBI data output: The LPDDR6 SDRAM inverts Read data on its DQ outputs associated within a two-bytes section and drives DBI data output HIGH when the number of '1' data bits within a given two-byte section is greater than eight; otherwise, the SDRAM does not invert the read data and drives DBI data LOW.</li> </ul>				

### 7.5.5.2 Write Data Bus Inversion Function

LPDDR6 SDRAM supports the function of Write Data Bus Inversion. Its details are shown below:

LPDDR6 device supports Enhanced Write Data Bus Inversion function for Write operation. The Write DBI function is based on a two-byte granularity. Refer to LPDDR6 DQ packet definition.

The Enhanced DBI-DC function during Write can be enabled or disabled through MR3 OP[1]. DBI signal is a part of LPDDR6 DQ packet and each DBI bit is mapped to corresponding Write Data Bytes as followings.

**Table 294 – DBI Bit vs. DQ Byte Mapping**

DBI bit	Corresponding Write Data Bytes
DBI 0	D[0:15]
DBI 1	D[16: 31]
DBI 2	D[32: 47]
DBI 3	D[48: 63]
DBI 4	D[64: 79]
DBI 5	D[80: 95]
DBI 6	D[96: 111]
DBI 7	D[112: 127]
DBI 8	D[128:143]
DBI 9	D[144: 159]
DBI 10	D[160: 175]
DBI 11	D[176: 191]
DBI 12	D[192: 207]
DBI 13	D[208: 223]
DBI 14	D[224: 239]
DBI 15	D[240: 255]

In case the Write DBI function is enabled, each DBI bit selects one of two Mode Registers (0b for MR93 OP[7:0], 1b for MR94 OP[7:0]) for enhanced Write DBI operations. The selected Mode Register's 8bit operands are applied to bit-wise XOR operations with corresponding Write data bits. If users do not program MR93 and MR94 (Write Only), the enhanced DBI function is equivalent to conventional DBI-DC operations.

Default values of MR93: MR93 OP[7:0]=00000000b

Default values of MR94: MR94 OP[7:0]=11111111b

### 7.5.5.2 Write Data Bus Inversion Function (cont'd)

**Table 295 – Enhanced DBI Operation Example**

Selected MR Operands	Corresponding Two Bytes Data Bits	Enhanced DBI Operations (Bitwise XOR)
OP[0]	D0	$Op[0] \text{ xor } D0$
OP[1]	D1	$Op[1] \text{ xor } D1$
OP[2]	D2	$Op[2] \text{ xor } D2$
OP[3]	D3	$Op[3] \text{ xor } D3$
OP[4]	D4	$Op[4] \text{ xor } D4$
OP[5]	D5	$Op[5] \text{ xor } D5$
OP[6]	D6	$Op[6] \text{ xor } D6$
OP[7]	D7	$Op[7] \text{ xor } D7$
OP[0]	D8	$Op[0] \text{ xor } D8$
OP[1]	D9	$Op[1] \text{ xor } D9$
OP[2]	D10	$Op[2] \text{ xor } D10$
OP[3]	D11	$Op[3] \text{ xor } D11$
OP[4]	D12	$Op[4] \text{ xor } D12$
OP[5]	D13	$Op[5] \text{ xor } D13$
OP[6]	D14	$Op[6] \text{ xor } D14$
OP[7]	D15	$Op[7] \text{ xor } D15$

## 7.5.6 System Meta Function Mode

### 7.5.6.1 Features

LPDDR6 SDRAMs support a system meta mode for write and read operations as an option to systems. As specified in a write or read DQ packet, 2Byte meta per 32Byte data is stored or retrieved along with normal WRITE (WR-S, WR-L) or READ (RD-S, RD-L) commands. In case the system meta mode is enabled (MR92 OP[7]=1b) by a host, a part of 2KByte page in a bank array carves out automatically and used for meta data storage from/to correspond meta registers in a DRAM IO block. When the system meta mode is disabled, all available memory space could be allocated for normal write or read operations. The host system must handle the validity of metadata stored in meta registers using appropriate Meta-Write and/or Meta-Read commands.

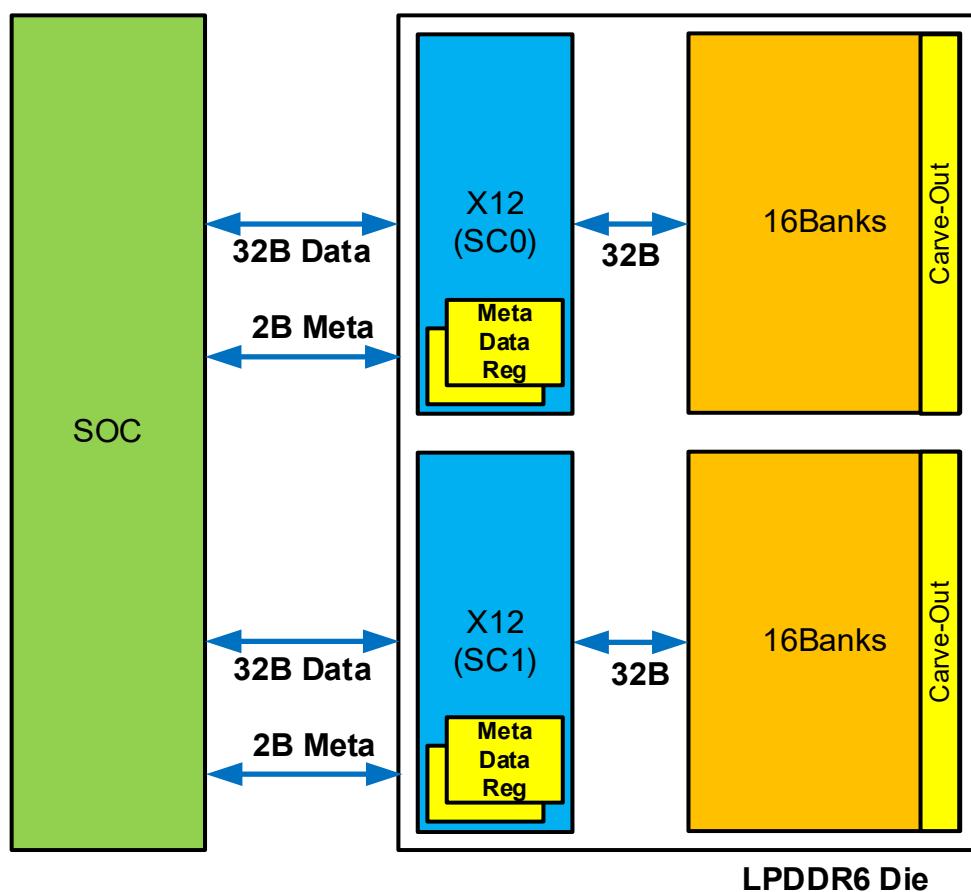


Figure 105 – System Meta Mode Diagram Example

### 7.5.6.2 Bank Array Carve Out Configuration

LPDDR6 SDRAM has a 2,048Bytes page which is addressed by 6bit Column Address (C[5:0], 0x00 ~0x3F). If the system mode is enabled (MR92 OP[7]=1b), each 2,048Byte page in a bank is split into two parts, normal data space (15/16 of page, 0x00 ~0x3B) and meta data space (1/16 of page, 0x3C~0x3F). Table 296 describes column addresses vs. designated meta registers mapping and configuration.

Table 296 — LPDDR6 Meta Column Address Translation Table

Column Address of 32Byte Data	Meta Data Register (MDR) Configuration
0x00	2Byte Meta (0x00)
0x01	2Byte Meta (0x01)
~	~
0x0E	2Byte Meta (0x0E)
0x0F	2Byte Meta (0x0F)
0x10	2Byte Meta (0x10)
0x11	2Byte Meta (0x11)
~	~
0x1E	2Byte Meta (0x1E)
0x1F	2Byte Meta (0x1F)
0x20	2Byte Meta (0x20)
0x21	2Byte Meta (0x21)
~	~
0x2E	2Byte Meta (0x2E)
0x2F	2Byte Meta (0x2F)
0x30	2Byte Meta (0x30)
0x31	2Byte Meta (0x31)
~	~
0x3B	2Byte Meta (0x3B)
N/A	2Byte (RFU)
NOTE 1 0x00~0x3F: Hexadecimal column address range of 2Kbyte page.	
NOTE 2 MDR (Meta Data Register)	
NOTE 3 One Meta Data Register is assigned to each bank (total 16 MDR per Sub-Channel).	
NOTE 4 A Meta Data Register can be mapped to one of 4 column addresses (0x3C, 0x3D, 0x3E, 0x3F) by system users.	

### 7.5.6.3 Meta Registers Configuration in Sub-Channel IO Block

LPDDR6 SDRAM sub-channel IO block (X12 DQs) includes total 16 Meta Data Registers (MDR0 ~MDR15). One meta register is assigned to each bank and designated to carve out column addresses (0x3C, 0x3D, 0x3E, 0x3F) for meta. Each 32Byte meta register stores sixteen 2Byte meta from associated sixteen column addresses except “0x3F”. Refer to Figure 106 about meta data registers configuration.

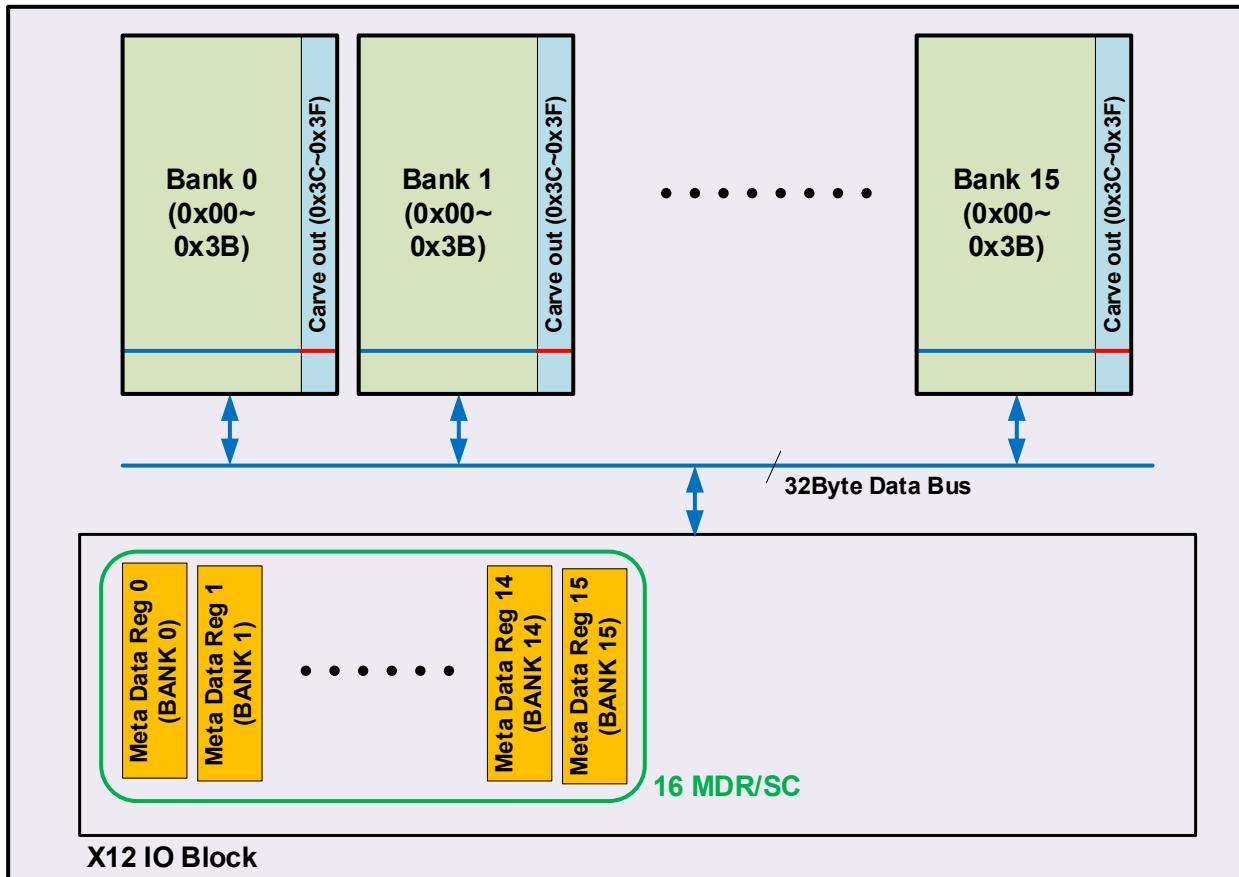


Figure 106 – 16 Meta Data Registers in a Sub-Channel Diagram Example

#### 7.5.6.4 Meta-Write and Meta-Read Operations

When Write or Read commands are issued to an LPDDR6 SDRAM device, Meta-Write/Meta-Read commands can be distinguished from normal Write/Read commands by PAMM segment hit or miss in a target bank and associated column address (C[5:2]). Meta-Write/Meta-Read operations shall be executed by WR-S/RD-S commands with C[5:0]=0x3C~0x3F. Issuing WR-L/RD-L commands with C[5:0]=0x3C~0x3F is prohibited. The flow chart in Figure 107 describes how an LPDDR6 device distinguishes Meta-Write/Read commands from normal Write/Read commands.

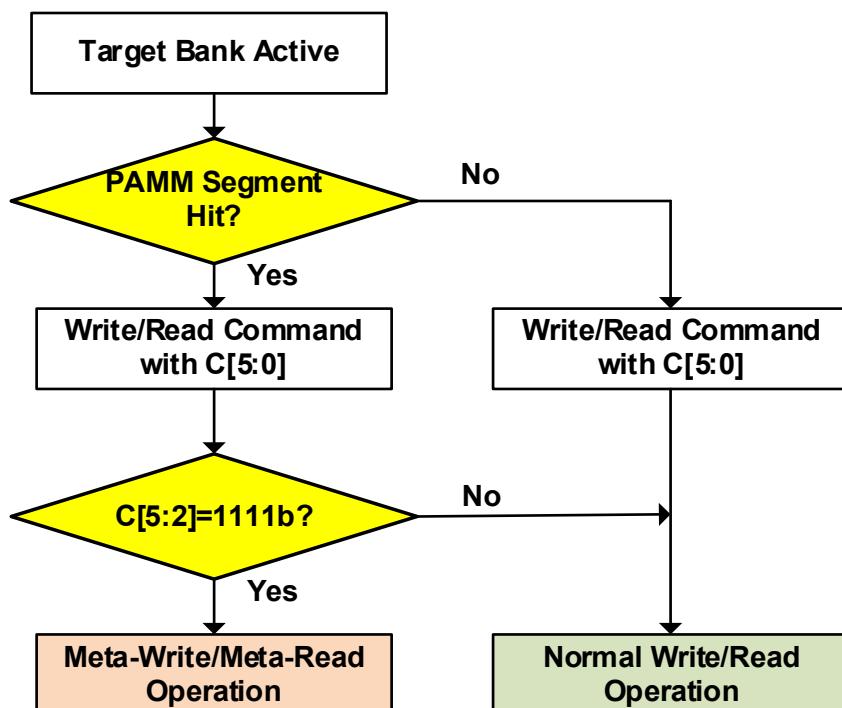


Figure 107 – Meta Write/Read Command Decoding Flow Chart

#### 7.5.6.4 Meta-Write and Meta-Read Operations (cont'd)

The following is Meta-Write/Meta-Read behavior:

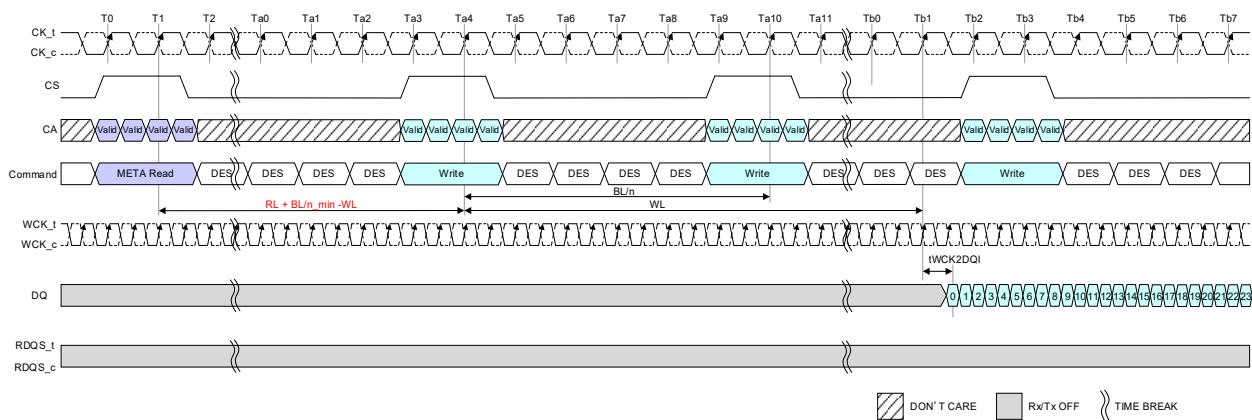
- During Meta-Write and Meta-Read operations, DQ transaction is not associated.
- Meta-Write/Meta-Read operation can execute regardless of whether WCK2CK SYNC is ON or OFF.
- Dynamic Non-target ODT is not applied to a Meta-Write command.

**Table 297 – Meta-Write/Meta-Read Behavior with or without WCK2CK SYNC**

Current WKC2CK SYNC Status	Next Command		Operation
	Command	WS Operand	
SYNC OFF	WR-S/WR-L/RD-S/RD-L	"H"	Allowed
	WR-M/RD-M		Allowed
	WR-S/WR-L/RD-S/RD-L	"L"	Not Allowed
	WR-M/RD-M		Allowed
SYNC ON	WR-S/WR-L/RD-S/RD-L	"H"	Not Allowed
	WR-M/RD-M		Not Allowed
	WR-S/WR-L/RD-S/RD-L	"L"	Allowed
	WR-M/RD-M		Allowed

#### 7.5.6.5 System Meta Mode Function Timing Diagram Examples

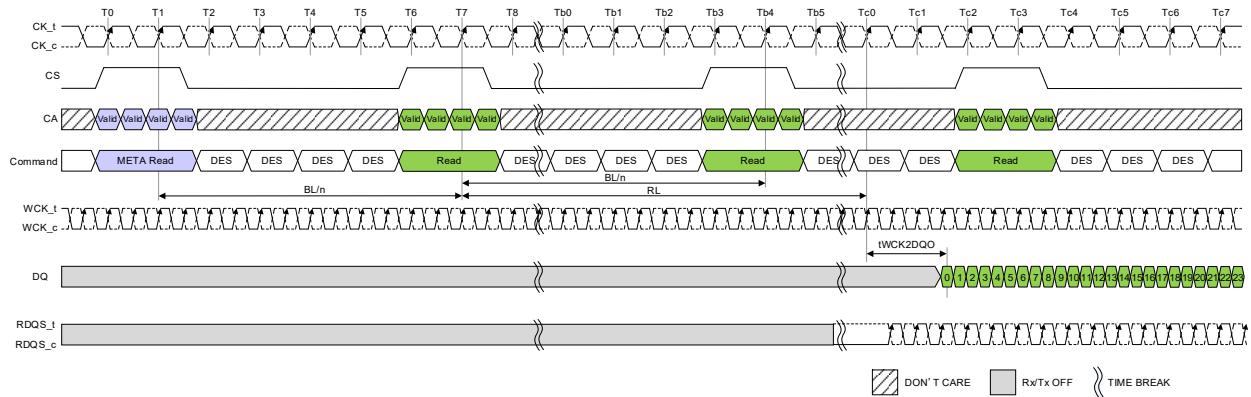
A Meta-Read command selects one of four carve-out column addresses (0x3C ~ 0x3F) in the target bank and transfers a 32Byte data to a corresponding meta data register. The next Write command executes 32Byte data write operation to the target bank and 2Byte meta data write operation to the associated meta data register. Meta-Write and Meta-Read commands timing constraints are different depending on bank and rank relationship (same rank/same BG, same rank/different BG, different rank). Refer to Meta Mode Command Timing Constraints.



**Figure 108 – Meta Read and Write Operations Timing Diagram Example (Same Rank, Different BG)**

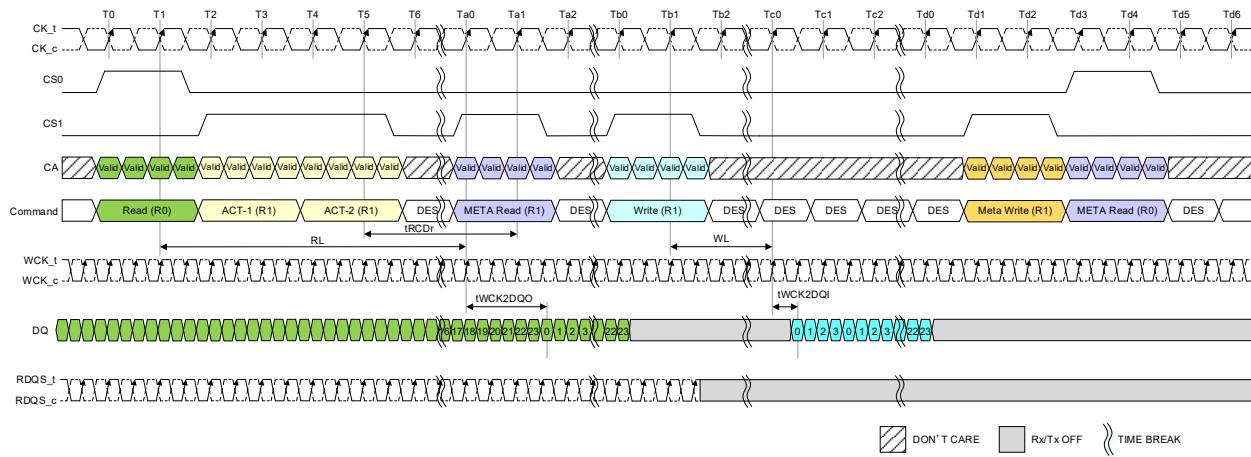
### 7.5.6.5 System Meta Mode Function Timing Diagram Examples (cont'd)

A Meta-Read command selects one of four carve-out column addresses (0x3C ~ 0x3F) in the target bank and transfers a 32Byte data to a corresponding meta data register. The next Read command executes 32Byte data read operation from the target bank and 2Byte meta data read operation from the associated meta data register. As specified in LPDDR6 DQ packet structure, 32Byte data and 2Byte meta data are transmitted to a host.



**Figure 109 – Meta Read and Read Operations Timing Diagram Example (Same Rank, Same BG)**

A Meta-Write and a Meta-Read operations are not associated with DQ bus transactions. Therefore, the Meta-Write and the Meta-Read commands can be issued while other rank's DQ bus transaction. As shown in Figure 110, an Active (ACT-1 and ACT-2) and a Meta-Read commands for Rank 1 (CS1) are issued while Read operations for Rank 0 (CS0) continue. Meta-Write and Meta-Read commands for different ranks require 2nCK timing constraints. Refer to 8.10 Meta Mode Command Timing Constraints.



**Figure 110 – Dual Rank Meta Read and Meta Write Operations Timing Diagram Example (Different Rank)**

### 7.5.6.6 Partial Array Meta Mode

#### 7.5.6.6.1 PAMM Segment Enablement

The LPDDR6 SDRAM adopts flexible meta mode scheme. A segment in each bank for 4BG/4BK (BK0 ~BK15) bases sub-channel of the LPDDR6 SDRAM can be independently configured whether a Meta Mode operation is taking place. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the meta segment enablement status of each segment up to 8 segments. For segment enablement bit assignments, see Mode Register 95.

The enablement bit to the meta segment controls the Meta Mode operation of entire memory within the segment. When the segment is enabled via MRW(MR 95 OP[7:0]), a Meta Mode operation to the entire segment is executed. To enable a Meta Mode operation to the segment, a coupled enablement bit must be programmed, "Valid".

**Table 298 – Example of Meta Segment Enablement in LPDDR6 SDRAM**

	Meta Segment (MR95)	BK 0	BK 1	BK 2	BK 3	BK 4	BK 5	BK 6	BK 7	BK 8	BK 9	BK 10	BK 11	BK 12	BK 13	BK 14	BK 15
Segment 0	0																
Segment 1	0																
Segment 2	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	
Segment 3	0																
Segment 4	0																
Segment 5	0																
Segment 6	0																
Segment 7	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	

NOTE 1 This table illustrates an example. Memory Carve-Out and Meta operations are valid only to segment 2 and segment 7.

NOTE 2 V: Valid

## 7.6 Refresh Operation

### 7.6.1 Refresh Command

The REFRESH command is initiated with CS HIGH, CA[2:0] HIGH at the 1st rising edge of the clock and CA[1:0] LOW at the 2nd falling edge of the clock. All-bank REFRESH is initiated with CA[3] HIGH at the 1st rising edge of the clock, and Dual-bank REFRESH is initiated with CA[3] LOW at the 1st rising edge of the clock.

A Dual-bank REFRESH command (REFdb) is performed to two sets of bank group addresses ("BG0/1", "dBG0/1") and one set of bank address ("BA0/1") as transferred on CA[3:0] at the 2nd rising edge (R2) and the 2nd falling edge (F2) of the clock. A Dual-bank REFRESH command (REFdb) to the 16 banks can be issued in any BG order. e.g., REFdb commands may be issued in the following order: (0,4)-(9,13)-(8,12)-(2,6)-(1,5)-(10,14)-(3,7)-(11,15). After the 16 banks have been refreshed using eight Dual-bank REFRESH commands, the controller can send another set of Dual-bank REFRESH commands in the same order or a different order. e.g., REFdb commands are issued in the following order that is different from the previous order: (3,11)-(6,14)-(1,9)-(8,12)-(0,4)-(7,15)-(2,10)-(5,13). One of the possible orders can also be a sequential round robin: (0,8)-(1,9)-(2,10)-(3,11)-(4,12)-(5,13)-(6,14)-(7,15). It is illegal to send a Dual-bank REFRESH command to the same bank unless all 16 banks have been refreshed using the Dual-bank REFRESH command. Also, it is illegal to issue a REFdb command with BG0/1 equal to dBG0/1. The count of 8 REFdb commands starts with the first REFdb command after a synchronization event.

The bank count is synchronized between the controller and the SDRAM by resetting the bank count to zero. Synchronization can occur upon issuing a RESET\_n or at every exit from self-refresh. REFab command also synchronizes the counter between the controller and SDRAM to zero. The SDRAM device can be placed in self-refresh, or a REFab command can be issued at any time without cycling through all banks using Dual-bank REFRESH command. After the bank count is synchronized to zero, the controller can issue Dual-bank REFRESH commands in any order as described in the previous paragraph.

A REFab command issued when the bank counter is not zero will reset the bank counter to zero and the DRAM will perform refreshes to all banks as indicated by the row counter. If another refresh command (REFab or REFdb) is issued after the REFab command, then it uses an incremented value of the row counter. Table 299 shows examples of both bank and refresh counter increment behavior.

### 7.6.1 Refresh Command (cont'd)

**Table 299 – Bank and Refresh Counter Increment Behavior**

#	SUB #	Command	dBG1	dBG0	BG1	BG0	BA1	BA0	Refresh Bank #	Bank Counter #	Ref Counter # (Row Address #)
0	0	Reset, SRX or REFab									To 0
1	1	REFdb	1	0	0	0	0	0	0/8	0 to 1	n
2	2	REFdb	1	0	0	0	0	1	1/9	1 to 2	
3	3	REFdb	1	0	0	0	1	0	2/10	2 to 3	
4	4	REFdb	1	0	0	0	1	1	3/11	3 to 4	
5	5	REFdb	1	1	0	1	0	0	4/12	4 to 5	
6	6	REFdb	1	1	0	1	0	1	5/13	5 to 6	
7	7	REFdb	1	1	0	1	1	0	6/14	6 to 7	
8	8	REFdb	1	1	0	1	1	1	7/15	7 to 0	
9	1	REFdb	0	1	0	0	0	0	0/4	0 to 1	
10	2	REFdb	1	1	1	0	0	1	9/13	1 to 2	
• • •											
15	7	REFdb	0	1	0	0	1	1	3/7	6 to 7	n+1
16	8	REFdb	1	1	1	0	1	1	11/15	7 to 0	
17	1	REFdb	1	0	0	0	0	0	0/8	0 to 1	
18	2	REFdb	1	0	0	0	0	1	1/9	1 to 2	n+2
19	3	REFdb	1	0	0	0	1	0	2/10	2 to 3	
20	0	REFab	V	V	V	V	V	V	0~15	To 0	
21	1	REFdb	1	0	0	0	1	0	2/10	0 to 1	n+3
22	2	REFdb	1	1	0	1	0	1	5/13	1 to 2	

### 7.6.1 Refresh Command (cont'd)

A bank must be idle before it can be refreshed. The controller must track the bank pair being refreshed by the REFdb REFRESH command.

The REFdb command must not be issued to the device until the following conditions are met:  
tRFCab has been satisfied after the prior REFab command.

tdbR2dbR has been satisfied after the prior REFdb command.

tRP has been satisfied after the prior PRECHARGE command to that bank.

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than the one affected by the REFdb command).

The target bank pair is inaccessible during Dual-bank REFRESH cycle time (tRFCdb). However, other banks not being refreshed within the device are accessible and can be addressed during the cycle. During the REFdb operation, any of the non-refreshing banks can be maintained in an active state or accessed by a READ or a WRITE command. When the Dual-bank REFRESH cycle has completed, the affected bank pair will be in the idle state.

After issuing REFdb, these conditions must be met:

- tRFCdb must be satisfied before issuing a REFab command.
- tRFCdb must be satisfied before issuing an ACTIVATE command to the same bank or bank pair.
- tdbR2act must be satisfied before issuing an ACTIVATE command to a different non-refreshing bank.
- tdbR2dbR must be satisfied before issuing another REFdb command.

An all-bank REFRESH command (REFab) issues a REFRESH command to all banks. All banks must be idle when REFab is issued (for instance, by issuing a PRECHARGE-ALL command prior to issuing an all-bank REFRESH command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. The REFab command must not be issued to the device until the following conditions have been met:

- tRFCab has been satisfied following the prior REFab command.
- tRFCdb has been satisfied following the prior REFdb command.
- tRP has been satisfied following the prior PRECHARGE command.

When an all-bank refresh cycle is completed, all banks will be idle. After issuing REFab:

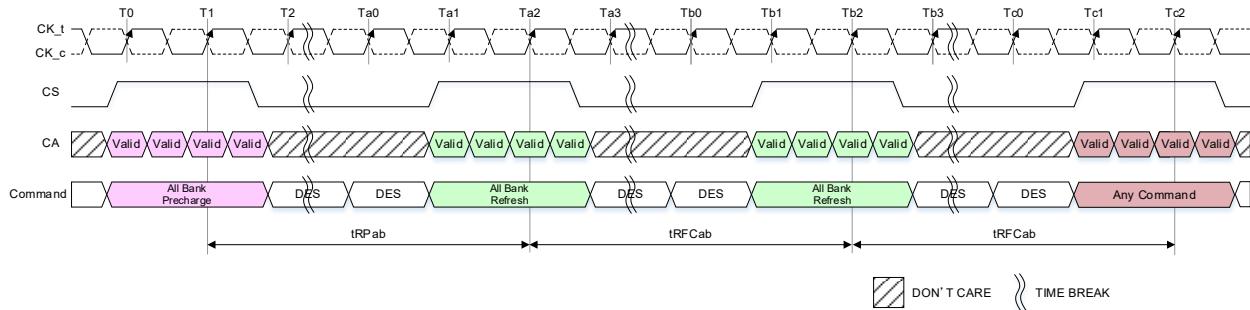
- tRFCab latency must be satisfied before issuing an ACTIVATE command.
- tRFCab latency must be satisfied before issuing a REFab or REFdb command.

### 7.6.1 Refresh Command (cont'd)

**Table 300 – REFRESH Command Scheduling Separation Requirements**

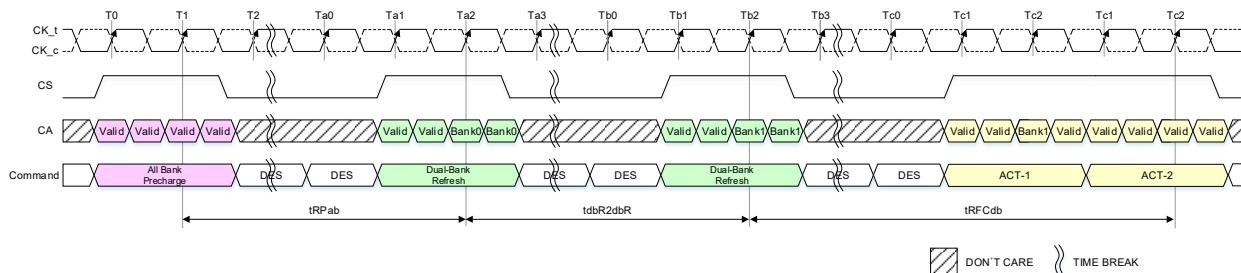
Symbol	Minimum Delay From	To	Note
tRFCab	REFab	REFab	
		Activate command to any bank	
		REFdb	
tRFCdb	REFdb	REFab	
		Activate command to same bank as REFdb	
tdbr2act	REFdb	Activate command to different bank than REFdb	
tRRD	Activate	REFdb	1
		Activate command to different bank than prior Activate command	
tdbR2dbR	REFdb	REFdb	
NOTE 1 A bank must be in the idle state before it is refreshed, so following an ACTIVATE command REFab is prohibited; REFdb is supported only if it affects a bank that is in the idle state.			
NOTE 2 "Same bank" and "different bank" here indicate "same bank pair" and "different bank pair", respectively. Please refer to "Refresh Bank#" row in Table 299 - Bank and Refresh counter increment behavior for further information.			

### 7.6.1 Refresh Command (cont'd)



- NOTE 1 Only DES, NOP, PDE, CAS(WS\_AON), CAS(WS\_OFF), MRR, MPC, RFF, WFF, and MRW commands are allowed after Refresh command is registered until tRFCab(min) expires. However, PARC:MR25 OP[6] setting change by MRW command is prohibited during tRFCab(min) period.
- NOTE 2 If MR25 OP[6]=1<sub>B</sub>: PARC Enable, MRW command to set PASR: MR27 OP[7:0] is prohibited until tRFCab(min) expires.
- NOTE 3 If any command is Activate, the end point of tRFCab is 2<sup>nd</sup> rising edge of CK\_t of ACT-2. Refer to Figure 112.

**Figure 111 – All-Bank Refresh Operation**



- NOTE 1 Operation to banks other than the banks being refreshed are supported during tRFCdb period.
- NOTE 2 PARC:MR25 OP[6] setting change by MRW command is prohibited during tRFCdb(min) and tdbR2dbR(min) period.
- NOTE 3 If MR25 OP[6]=1<sub>B</sub>: PARC Enable, MRW command to set PASR: MR27 OP[7:0] is prohibited until tRFCdb(min) and tdbR2dbR(min) expires.

**Figure 112 – Dual-Bank Refresh Operation**

### 7.6.1 Refresh Command (cont'd)

In general, a Refresh command needs to be issued to the LPDDR6 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the LPDDR6 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed and maximum number of pulled-in or postponed REF command is dependent on the refresh rate. This is described in Table 301.

In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to  $9 \times tREFI$ . A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to  $9 \times tREFI$ . At any given time, a maximum of 16 REF commands can be issued within  $2 \times tREFI$ . Self-Refresh Mode may be entered with a maximum of 8 Refresh commands being postponed. After exiting Self-Refresh Mode with one or more Refresh commands postponed, additional Refresh commands may be postponed to the extent that the total number of postponed Refresh commands (before and after the Self-Refresh) will never exceed 8. During Self-Refresh Mode, the number of postponed or pulled-in REF commands does not change.

### **7.6.1 Refresh Command (cont'd)**

**Table 301 – REFRESH Command Timing Constraints**<sup>1,2,3</sup>

MR4 OP[4:0]	Maximum Refresh Multiplier	Effective Refresh Interval tREFIe	Max. No. of Pulled-In or Postponed REFab	Max. Interval Between Two REFab	Max Number of REFab in a 'Burst'	'Burst' Interval Definition	Per-bank Refresh
00000B	Low temp. Limit	N/A	N/A	N/A	N/A	N/A	N/A
00001B	8 x	8x tREFI	1	2 x tREFIe	16	2 x tREFI	1/8 of REFab
00010B	6 x	6 x tRFFI	1	2 x tREFIe	16	2 x tREFI	1/8 of REFab
00011B	4 x	4 x tREFI	2	3 x tREFIe	16	2 x tREFI	1/8 of REFab
00100B	3.3 x	3.3 x tREFI	2	3 x tREFIe	16	2 x tREFI	1/8 of REFab
00101B	2.5 x	2.5 x tREFI	3	4 x tREFIe	16	2 x tREFI	1/8 of REFab
00110B	2.0 x	2.0 x tREFI	4	5 x tREFIe	16	2 x tREFI	1/8 of REFab
00111B	1.7 x	1.7 x tREFI	5	6 x tREFIe	16	2 x tREFI	1/8 of REFab
01000B	1.3 x	1.3 x tREFI	6	7 x tREFIe	16	2 x tREFI	1/8 of REFab
01001B	1 x	1 x tREFI	8	9 x tREFIe	16	2 x tREFI	1/8 of REFab
01010B	0.7 x	0.7 x tREFI	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
01011B	0.5 x	0.5 x tREFI	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
01100B	0.25 x, no de-rating	0.25 x tREFI, no de-rating	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
01101B	0.25 x, with de-rating	0.25 x tREFI, with de-rating	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
01110B	0.125 x, no de-rating	0.125 x tREFI, no de-rating	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
01111B	0.125 x, with de-rating	0.125 x tREFI, with de-rating	8	9 x tREFIe	16	max(2xtREFIe, 16xtRFCab)	1/8 of REFab
11111B	SDRAM High temperature operating limit exceeded	N/A	N/A	N/A	N/A	N/A	N/A

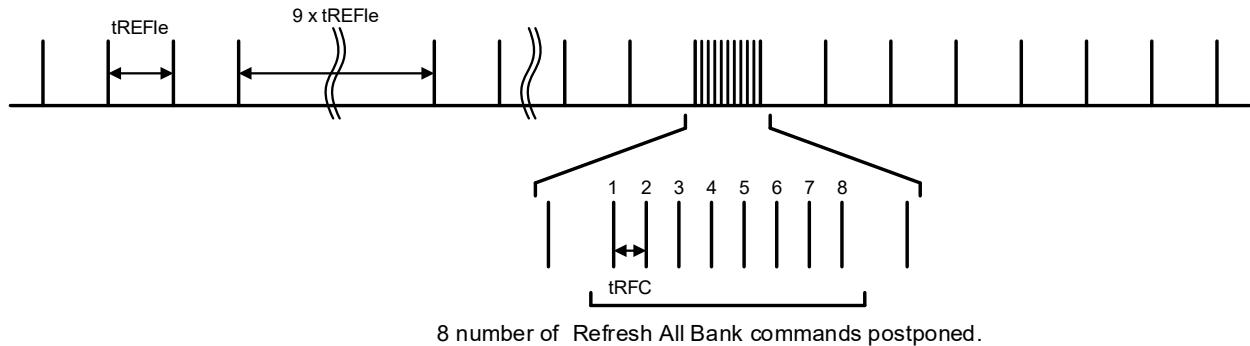
**NOTE 1** For any thermal transition phase where Refresh mode is transitioned, DRAM will support the previous postponed refresh requirement provided the number of postponed refreshes is monotonically reduced to meet the new requirement. However, the pulled-in refresh commands in previous thermal phase are not applied in new thermal phase. Entering new thermal phase, the controller must count the number of pulled-in refresh commands as zero, regardless of remaining pulled-in refresh commands in previous thermal phase.

**NOTE 2** LPDDR6 devices are refreshed properly if memory controller issues refresh commands with same or shorter refresh period than reported by MR4 OP[4:0]. If shorter refresh period is applied, the corresponding requirements from table apply. For example, When MR4 OP[4:0]=00001B, controller can be in any refresh multiplier from 8 to 0.25. When MR4 OP[4:0]=00010B, the only prohibited refresh rate is 8 \* tREFI.

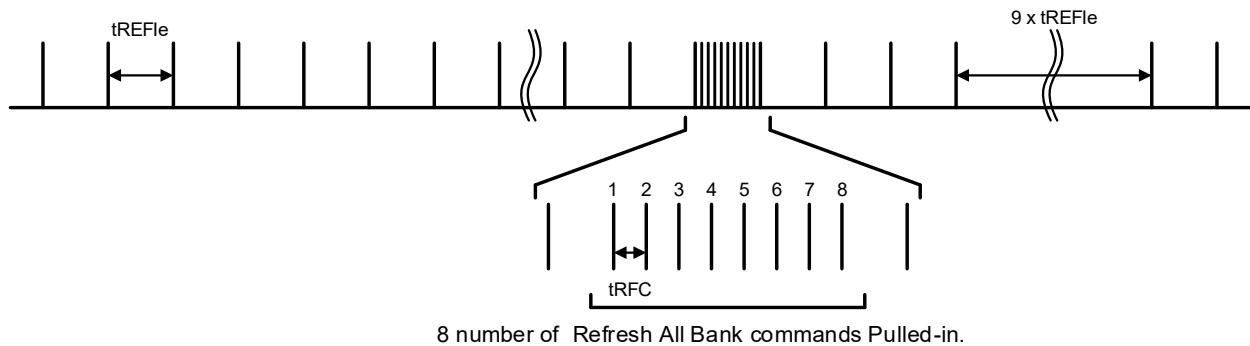
**NOTE 3** As long as the requirements specified in this table are satisfied, issuing extra refresh commands over the specification is allowed. The extra refresh commands are executed in the same manner as the normal refresh commands; however, the extra refresh command does not count as the postponed or pulled-in refresh command. Refer to Figure 115 for more information.

### 7.6.1 Refresh Command (cont'd)

The following figures describe postponed and pulled-in all-bank Refresh commands.



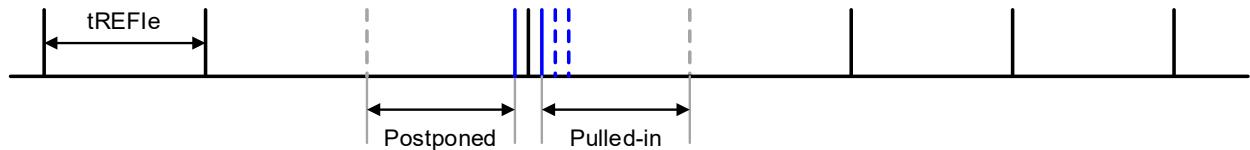
**Figure 113 – Postponing Refresh Commands (Example)**



**Figure 114 – Pulling-in Refresh Commands (Example)**

The Refresh commands issued beyond "Maximum number of pulled-in or postponed REFab" and/or "substituting postponed/pulled-in refresh" in one burst is acceptable. Although it is executed as the normal Refresh command internally, the extra refresh command does not count as postponed/ pulled-in refresh command.

- Periodic Refresh
- - - Postponed/Pulled-in Refresh
- Substituting Refresh
- - - Extra Refresh



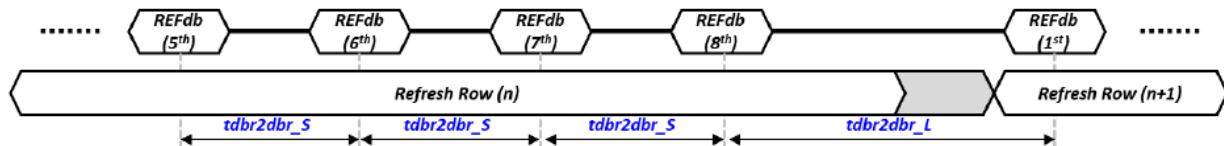
**Figure 115 – Extra Refresh (Example)**

### 7.6.2 Dual tdbR2tdbR Parameter

LPDDR6 supports a pair of dual-bank refresh to dual-bank refresh timing parameters, tdbR2dbR\_S, and tdbR2tbR\_L, in order to allow for improved efficiency in managing dual-bank refresh operation at the refresh rates under high temperature conditions.

tdbR2dbR\_S is applied when the dual-bank refresh is targeted at the different dual-bank pair of the same row address (i.e., same refresh counter) as the previous dual-bank refresh.

tdbR2dbR\_L is applied when the dual-bank refresh is targeted at the dual-bank pair of a different row address (i.e., different refresh counter) than the previous dual-bank refresh.



### **7.6.3 Refresh Requirement**

**Table 302 – Refresh Requirement Parameters**

#### 7.6.4 Optimized Refresh

LPDDR6 SDRAM supports Optimized Refresh operation, and the memory controller can choose to enable or disable Optimized Refresh mode via MR25 OP[7].

The use of Self Refresh mode introduces the possibility of missing an internally timed refresh event when Self Refresh Exit is registered. To address this, it is required that upon exit from Self Refresh at least one REFRESH command (1 all-bank or 8 dual-bank) is issued before entry into a subsequent Self Refresh. However, this refresh operation can be managed in an optimal manner if the memory controller supports Optimized Refresh described in Figure 116. The SDRAM also handles the internal Self Refresh with its own refresh timer.

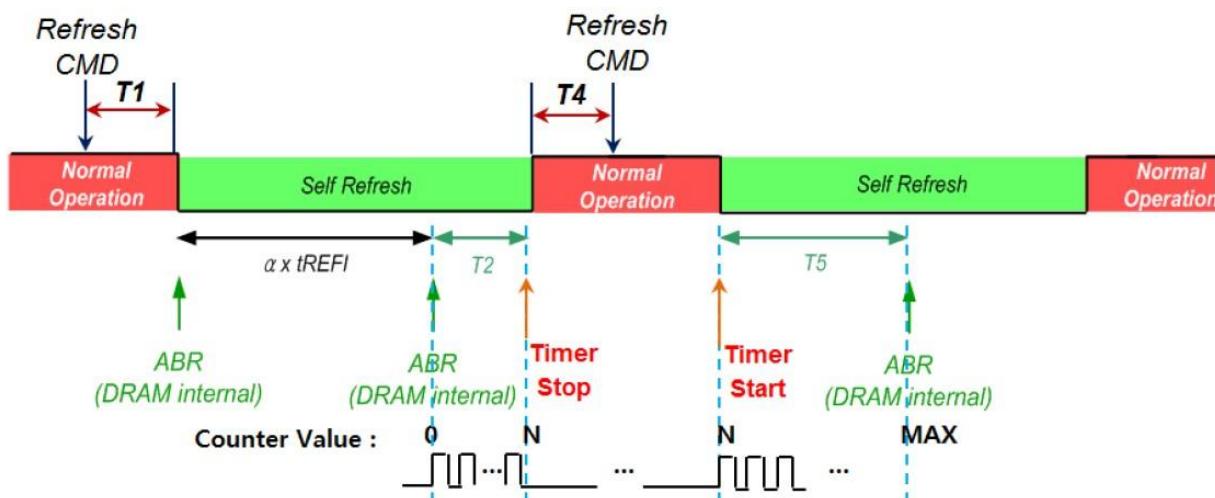
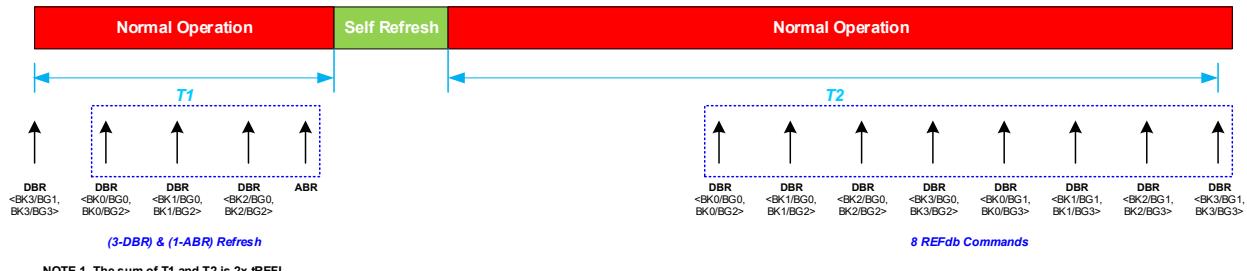


Figure 116 – Optimized Refresh Operation

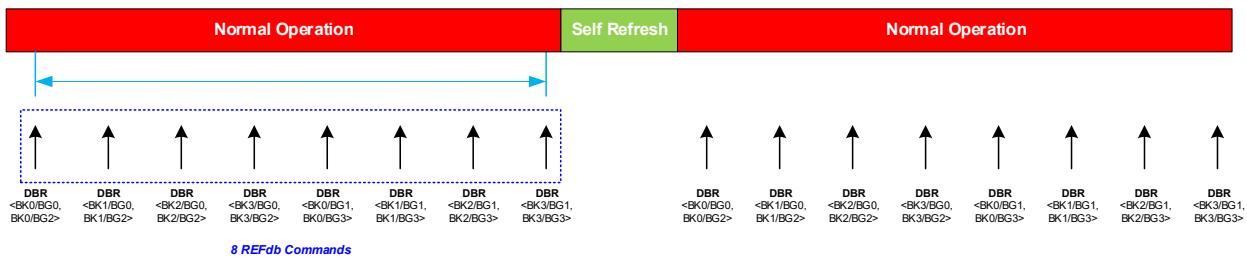
When this feature is enabled, upon exit from Self Refresh mode, LPDDR6 SDRAM freezes and stores the refresh timer value. Upon entering Self Refresh mode, the SDRAM resumes the refresh timer from the stored value and increments it to the next value, so that it can operate ABR only when the refresh timer expires in Self Refresh mode. If the memory controller can track the passage of time (T1 and T4 in Figure 116) for tREFI out of Self Refresh time period, it is up to the memory controller to determine when to issue refresh command (1 all-bank or 8 dual-bank). Refresh commands meeting tREFI condition, as determined by the memory controller tracking, are counted towards regular refresh commands required by the tREFI interval and affect the postponed or pulled-in refresh commands.

The bank count synchronized between the controller and the SDRAM resets to zero at every exit from Self Refresh. Therefore, an incomplete set of dual-bank REFRESH before Self-refresh entry is not included in REFRESH commands for Optimized Refresh operation. It is recommended to execute a complete set of dual-bank REFRESH commands (8 dual-bank REFRESH commands) for efficient Optimized Refresh operation.

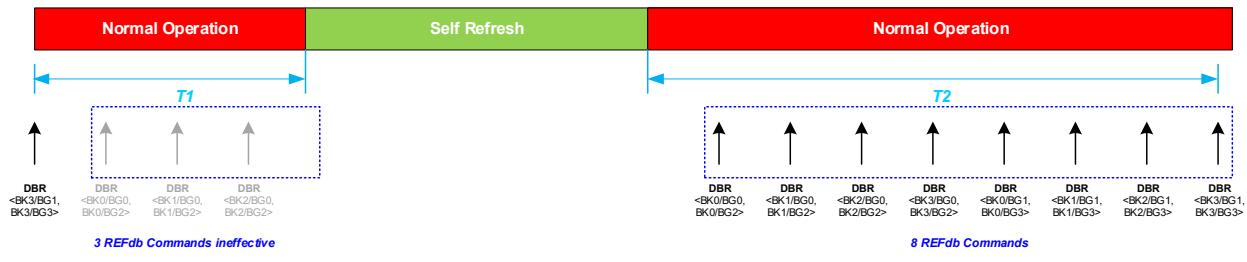
#### 7.6.4 Optimized Refresh (cont'd)



**Figure 117 – Optimized Refresh Operation Example for REFab (Completion of the Bank Count by One REFab Command)**



**Figure 118 – Optimized Refresh Operation Example for REFdb (Completion of the Bank Count by 8 REFdb Commands)**



**Figure 119 – Inefficient Optimized Refresh Operation Example**

### 7.6.5 Self Refresh Operation

The Self Refresh command can be used to retain data in the LPDDR6 SDRAM without external Refresh command. The device has a built-in timer to accommodate Self Refresh operation. The Self Refresh is entered by Self Refresh Entry Command defined by configuring CS HIGH and CA[2:0] LOW at the 1st rising edge of the clock and CS don't care, CA[0] LOW, CA[1] HIGH, and CA[2] LOW at the 1st falling edge of the clock. If Self Refresh command is issued with CA[3] HIGH at the 1st falling edge of the clock, Self-Refresh Command is initiated with Power Down status. Self-Refresh command is only allowed when READ, MRR, RFF or RDC data burst is completed; in other words, Read postamble must be completed and SDRAM must be in idle state.

During Self Refresh mode, all input pins of SDRAM are activated and CS ODT and CA ODT states are maintained according to the setting of its mode register, as well as NT ODT. If external clock is running, SDRAM can accept the following commands: PDE, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW. However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during Self Refresh mode.

LPDDR6 SDRAM can operate in Self Refresh in both the standard and elevated temperature ranges.

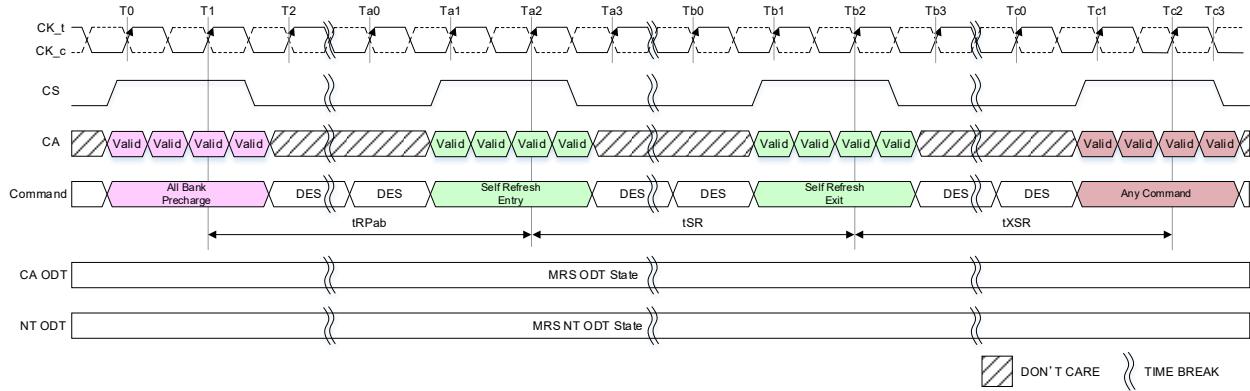
SDRAM will also manage Self Refresh power consumption when the operating temperature changes.

For proper Self Refresh operation, power supply pins (VDD1, VDD2C, VDD2D and VDDQ) are required to be at valid levels. However, VDDQ may be turned off during Self-Refresh with Power Down after tESPD is satisfied.

Prior to exiting Self-Refresh with Power Down, VDDQ is required to be within specified limits. The minimum time that the SDRAM is required to remain in Self Refresh mode is tSRmin. Once Self Refresh Exit is registered, only MRR, CAS(WS\_AON), CAS(WS\_OFF), WFF, RFF, RDC, DES, MPC, MRW are allowed until tXSR is satisfied. However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during tXSR(min).

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when Self Refresh Exit is registered. Upon exit from Self Refresh, it is required that at least one REFRESH command (1 all-bank or 8 per-2-bank) is issued before entry into a subsequent Self Refresh. This REFRESH command is not included in the count of regular refresh commands required by the tREFI interval and does not modify the postponed or pulled-in refresh counts; the REFRESH command does count toward the maximum refreshes permitted within 2 x tREFI.

### 7.6.5 Self Refresh Operation (cont'd)



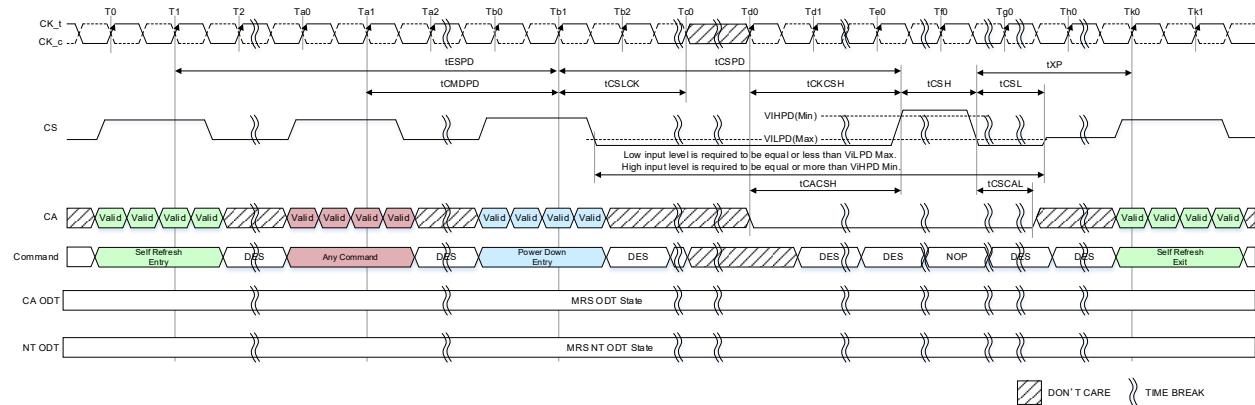
NOTE 1 PDE, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW are allowed during Self Refresh. However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during Self Refresh mode.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 120 – Self Refresh Entry/Exit Timing**

### 7.6.5.1 Power Down Entry and Exit during Self Refresh

Entering/Exiting Power Down Mode is allowed during Self Refresh mode in SDRAM. The related timing parameters between Self Refresh Entry/Exit and Power Down Entry/Exit are shown in Figure 121. The power-down state is asynchronously exited when CS toggles HIGH (VIHPD). The AC parameters related to the Power Down are defined in clause 7.7. The operation by the command issued prior to PDE is required to be completed before changing clock frequency, stopping clock, or turning off VDDQ.



**NOTE 1** PDE, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, MRW are allowed during Self Refresh (No Power Down). However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during Self Refresh mode.

The operation by the command issued prior to Power Down Entry (PDE) is required to be completed before changing clock frequency, stopping clock, or turning off VDDQ.

**NOTE 2** Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

**NOTE 3** The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHPD(Min).

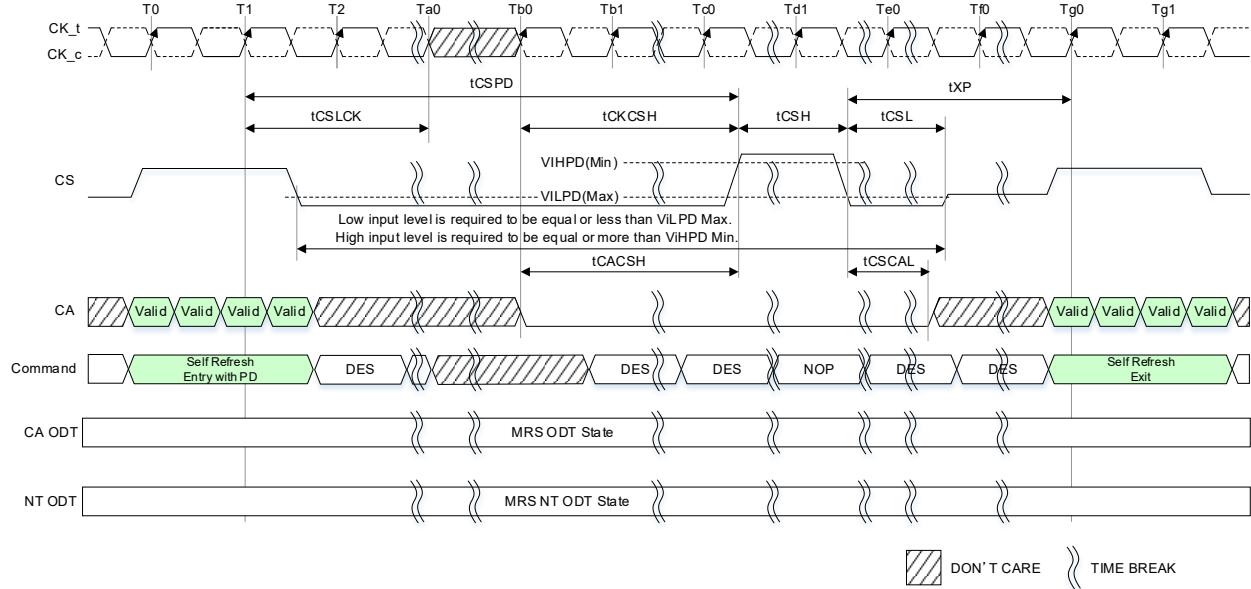
**NOTE 4** The start point of tCSL/tXP and the end point of tCSL are crossover points of VILPD(Max).

**NOTE 5** DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated as "don't care."

**Figure 121 – Self Refresh Entry/Exit Timing with Power Down Entry/Exit**

### 7.6.5.1 Power Down Entry and Exit during Self Refresh (cont'd)

If Self Refresh command is issued with CA[3] HIGH at the falling edge of the 1st clock, Self-Refresh Command is initiated with Power Down status.



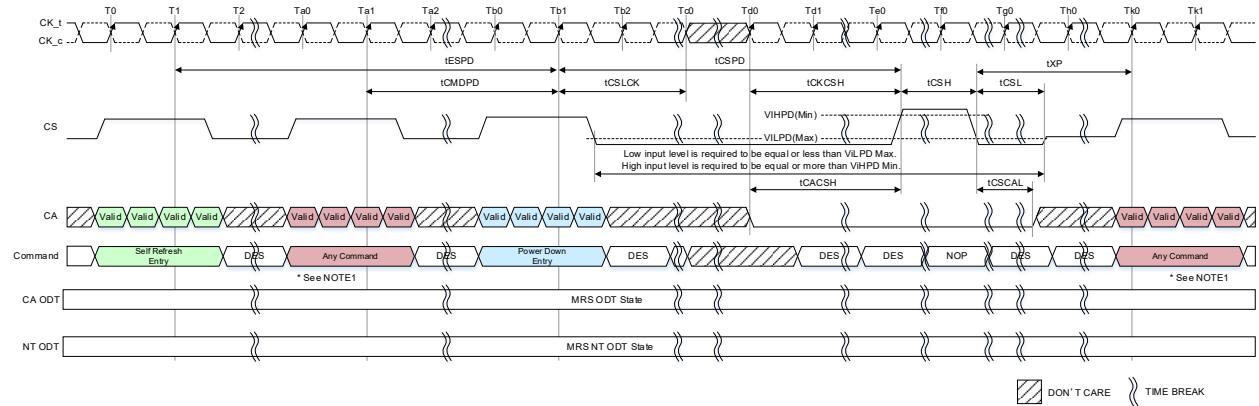
**NOTE 1** Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

**NOTE 2** DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated as "don't care."

**Figure 122 – Timing for Self Refresh Entry with PD Set HIGH**

### 7.6.5.2 Command Input Timing after Power Down Exit during Self Refresh

Command input timings after Power Down Exit during Self Refresh mode are shown in Figure 123.



**NOTE 1** PDE, MRR, CAS, DES, SRX, MPC, RFF, WFF, RDC, and MRW are allowed during Self Refresh (No Power Down). However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during Self Refresh mode.

The operation by the command issued prior to Power Down Entry (PDE) is required to be completed before changing clock frequency, stopping clock, or turning off VDDQ.

**NOTE 2** Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock is stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

**NOTE 3** DES commands are shown for ease of illustration; other commands may be valid at these times where the CA input is indicated as "don't care."

**Figure 123 – Command Input Timing after Power Down Exit during Self Refresh**

### 7.6.5.3 Clock Stop Timing during Self Refresh

Clock input can be stopped during Self Refresh mode. When stopping clock, CS and CK input must abide by the following requirements:

- CS shall be held LOW.
- CK\_t shall be held LOW and CK\_c shall be held HIGH.

Other conditions that must be observed are defined in clause 7.8.6.2: Input Clock Stop. Refer to the following figures for Clock stop and restart timing.

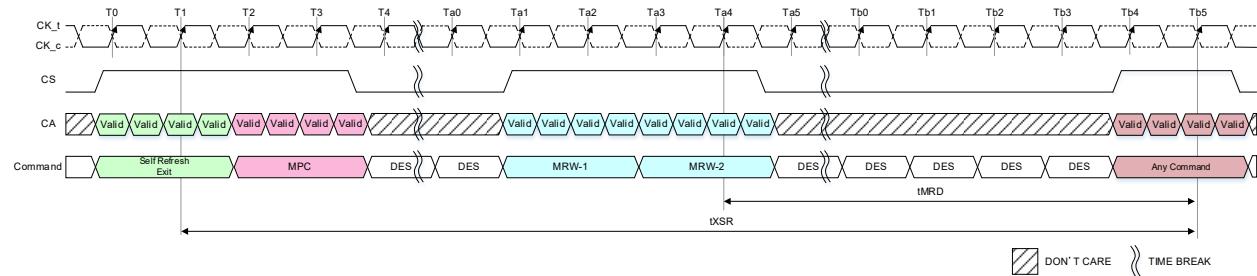
### 7.6.5.4 Self Refresh AC Timing Table

Table 303 – Self Refresh AC Timing

Parameters	Symbol	Min/ Max	Value	Unit	Note
Self Refresh Timing					
Delay from SRE command to PDE	tESPD	Min.	2	nCK	
Minimum Self Refresh Time (Entry to Exit)	tSR	Min.	Max(15ns, 4nCK)	ns	
Exit Self Refresh to Valid commands	tXSR	Min.	tRFCab + Max(7.5ns, 4nCK)	ns	
Valid Clock Requirement after SRE	tSRECK	Min.	Max(5ns, 3nCK)	ns	
Valid Clock Requirement before Valid Command	tCKSSR	Min.	2 x tCK + tXP	ns	

### 7.6.5.5 MRR, MRW, RFF, WFF, RDC, and MPC Commands during tXSR

Mode Register Read (MRR), Mode Register Write (MRW), Write FIFO (WFF), Read FIFO (RFF), Read DQ Calibration (RDC), and Multi-Purpose Command (MPC) can be issued during tXSR period.



**NOTE 1** MPC and MRW command are shown in this figure, any combination of CAS(WS\_AON), CAS(WS\_OFF), MRR, MRW, WFF, RFF, RDC and MPC are allowed during tXSR(min) period.

However, PASR: MR27 OP[7:0], Optimized Refresh mode: MR25 OP[7], and PARC: MR25 OP[6] setting change by MRW command is prohibited during tXSR(min) period.

**NOTE 2** Any command also includes CAS(WS\_AON), CAS(WS\_OFF), MRR, MRW, WFF, RFF, RDC and all MPC command.

**NOTE 3** DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 124 – MRR, MRW, WFF, RFF, RDC, and MPC Commands Issuing Timing during tXSR**

**Table 304 – Self Refresh Exit (SRX) Command Timing Constraints**

Current Command	Next Command	Timing Constraints (nCK)	
		Min	Max
Self Refresh Exit (SRX)	MODE REGISTER READ (MRR)	2	-
	MODE REGISTER WRITE-1 (MRW-1)	2	-
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal
	WRITE FIFO (WFF)	2	-
	READ FIFO (RFF)	2	-
	READ DQ CALIBRATION (RDC)	2	-
	MULTI PURPOSE COMMAND (MPC)	2	-

## 7.6.6 Partial Array Self Refresh (PASR)

### 7.6.6.1 PASR Segment Masking

A segment in every bank of the LPDDR6 SDRAM can be independently configured to mask Self Refresh operation. One mode register unit of 8 bits, accessible via MRW command, is assigned to program the segment masking status of each segment with support of up to 8 segments. For segment masking bit assignments, refer to MR27 definition.

The mask bit to the segment controls refreshes operation of the entire memory within the segment. When a segment is masked via MRW (MR27 OP[7:0]), Self Refresh operation to the entire segment is blocked, and data retention in the segment is not guaranteed in Self Refresh mode. To enable refresh operation to the segment, the coupled mask bit must be programmed "unmasked."

Users must be aware that data retention is also not guaranteed for the Activation Counters within the masked segments. This means that the Activation Counters will be in an unknown state, which may lead to unexpected triggering of Alert Back-off protocol during normal operation following PASR-enabled Self Refresh.

**Table 305 – Example of Segment Masking Use in LPDDR6 SDRAM<sup>1</sup>**

	Segment Mask (MR27)	All Banks
Segment 0	0	
Segment 1	0	
Segment 2	1	M
Segment 3	0	
Segment 4	0	
Segment 5	0	
Segment 6	0	
Segment 7	1	M

NOTE 1 This table illustrates an example when refresh operation to Segment 2 and Segment 7 are masked.

### 7.6.6.2 Partial Array Refresh Control (PARC)

LPDDR6 SDRAM supports Partial Array Refresh Control (PARC) to reduce IDD5 power consumption.

If PARC MR25 OP[6]=1<sub>B</sub>, LPDDR6 SDRAM skips refresh operation of the segments configured by PASR Segment Mask: MR27 OP[7:0] when All-bank or Dual-bank Refresh command is received.

When the segment is masked via MRW (MR27 OP[7:0]) and MR25 OP[6]=1<sub>B</sub>, Self Refresh and Refresh operation to the entire segment is blocked, and data retention in the segment is not guaranteed in Normal Refresh and Self Refresh mode. Activate command to the masked segments is illegal. MR27 OP[7:0] and MR25 OP[6] can be changed only when all banks are in idle state.

## 7.7 Power Down

### 7.7.1 Power-Down Entry and Exit

Power-Down is entered by issuing Power-Down Entry Command.

Power-Down Entry Command must not be issued while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- Write
- VRCG High Current mode Entering/Exiting via MRW

Also, LPDDR6 SDRAM cannot be placed in Power Down state during following state and until those modes have completely terminated. (Self Refresh Entry with Power Down Entry command is contained in Power Down Entry command. See Command Truth Table for detail).

- In Enhanced RDQS Training Mode: MR46 OP[0]=1<sub>B</sub>
- In RDQS Toggle Mode: MR46 OP[1]=1<sub>B</sub>
- In WCK2CK Leveling Mode: MR16 OP[2]=1<sub>B</sub>
- In CBT: Command Bus Training Mode/ CST CS Training Mode: MR16 OP[5:4]≠00<sub>B</sub>
- In changing Physical Mode Register by Frequency Set Point function
- In PPR: Post Package Repair Mode: MR41 OP[4]=1<sub>B</sub>
- From DCM start command to DCM stop command
- VREF(CA) Value setting via MRW: MR12 OP[6:0]
- VREF(DQ) Value setting via MRW: MR14 OP[6:0]
- VREF(CS) Value setting via MRW: MR15 OP[6:0]

Power down entry command is not allowed to be the next command of Write FIFO (WFF) command.

Power-Down Entry Command can be issued while any other operations such as row activation, Precharge, Auto Precharge or Refresh are in progress. The Power-Down IDD specification will not be applied until such operations are complete. Power-Down entry and exit are shown in Figure 125.

LPDDR6 supports dynamic write NT-ODT function, there are two power down mode according to dynamic write NT-ODT enable/disable (MR20 OP[5:3]).

When dynamic write NT-ODT is disabled(MR20 OP[5:3]=000<sub>B</sub>), entering Power-down mode deactivates the input and output buffers, excluding CS and Reset\_n.

When dynamic write NT-ODT is enabled(MR20 OP[5:3]≠000<sub>B</sub>), entering Power-down mode deactivates the input and output buffers, excluding CS, CK\_t/c, CA[0] and Reset\_n.

In case of dynamic write NT-ODT is disabled, entering Power-Down mode deactivates the input and output buffers, excluding CS and Reset\_n. Clock input is required after Power-Down Entry Command is issued, this timing period is defined as tCSLCK. Power-Down Entry Command will result in deactivation of all input receivers except CS and Reset\_n after tCSLCK has expired. In Power-Down mode, CS must be held LOW and all other input signals except Reset\_n are “Don’t Care”. CS LOW is required to be maintained until tCSPDmin is satisfied. During Power Down mode, CS Rx input level applies Asynchronous mode definition.

In case of dynamic write NT-ODT is enabled, entering Power-Down mode deactivates the input and output buffers, excluding CS, CK\_t/c, CA[0] and Reset\_n. Therefore, valid Clock input is required.

### 7.7.1 Power-Down Entry and Exit (cont'd)

VDDQ can be turned off during Power-Down mode. Prior to exiting Power-Down mode, VDDQ is required to be within its minimum/maximum operating range. Vref(CA) update timing (TBD ns) is required after the voltage (VDDQ) ramp up is completed for reliable operation.

No refresh operations are performed in Power-Down mode except Self-Refresh Power-Down. The maximum duration in Power-Down mode is only limited by the refresh requirements outlined in the Refresh command section.

When dynamic write NT-ODT is disabled ( $MR20\ OP[5:3]=000_B$ ), The Power-Down state is asynchronously exited when CS toggles. Power-Down Entry command can be re-issued with  $tXP_{min} + tCKSNC_{min} + 1nCK$  after CS goes LOW, however CK sync is required. A valid, executable command can be applied with Power-Down exit latency  $tXP_{min} + tCKSNC_{min} + 1nCK$  after CS goes LOW, CK sync is required in this case too.

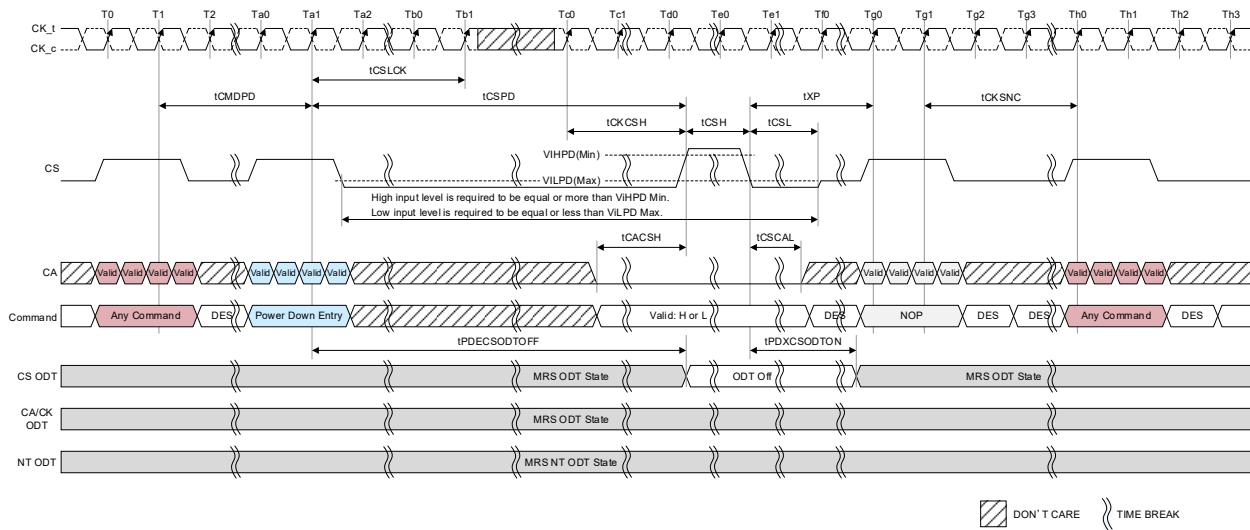
Clock frequency change or Clock Stop is inhibited during tCMDPD, tCSLCK, tCKCSH, tXP, tMRWPD, tZQPD, tOSCPD, tERQX, and tFC periods.

If Power-Down occurs when all banks are idle, this mode is referred to as idle Power-Down. If Power-Down occurs when there is a row active in any bank, this mode is referred to as active Power-Down. And if Power-Down occurs when Self Refresh is in progress, this mode is referred to as Self Refresh Power-Down in which the internal refresh is continuing in the same way as Self Refresh mode.

When CA, CK and/or CS ODT is enabled via Mode Register setting, the rank providing ODT will continue to terminate CA, CK bus in all DRAM states including Power-Down. CS ODT state goes OFF ignoring MRS ODT state after Power-Down Entry is issued and returns to MRS ODT state with Power-Down Exit.

When dynamic write NT-ODT is enabled( $MR20\ OP[5:3]\neq000_B$ ), Power-down state is synchronously exited by Power-down exit command.

### 7.7.1 Power-Down Entry and Exit (cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover point of VIHPD(Min).

NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover points of VILPD(Max).

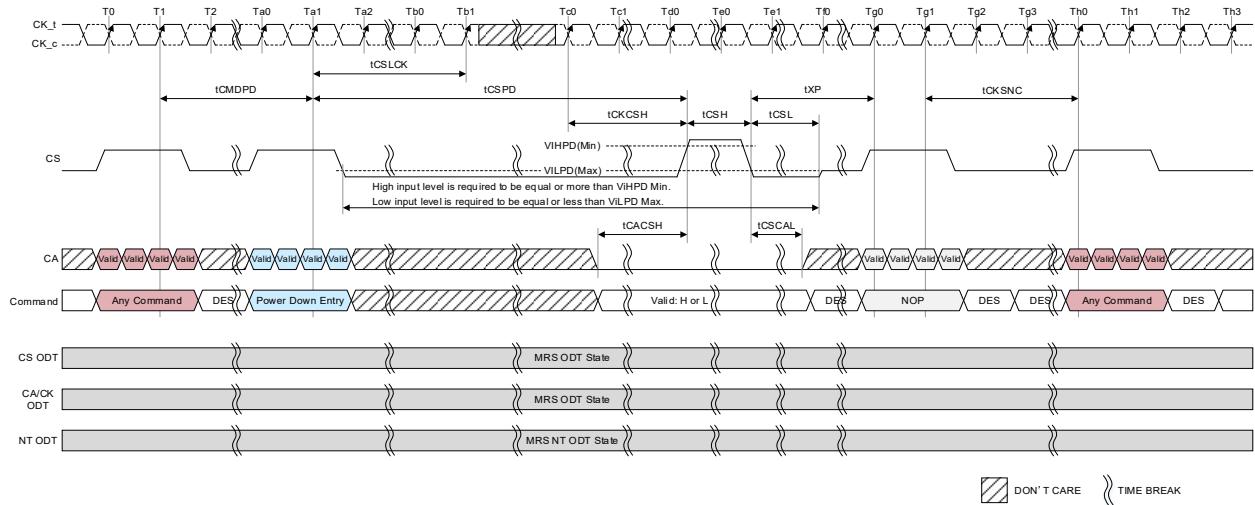
NOTE 5 Power Down Entry command can be issued at Th0.

NOTE 6 CA input is required be Low during tCSH.

NOTE 7 CS ODT behavior option on Power Down is set to disable: MR23 OP[4]=0B.

**Figure 125 – Basic Power-Down Entry and Exit Timing: CS ODT is Enabled and CS ODT Behavior Option on Power Down, Dynamic Write NT-ODT is Disabled**

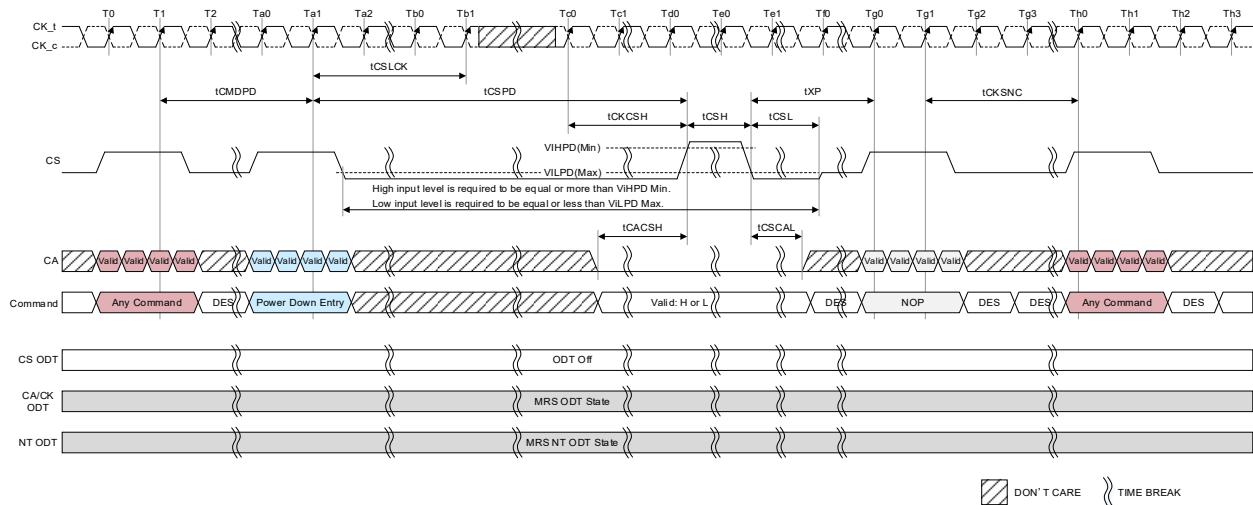
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover points of VIHPD(Min).
- NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover points of VILPD(Max).
- NOTE 5 Power Down Entry command can be issued at Th0.
- NOTE 6 CA input is required be Low during tCSH.
- NOTE 7 CS ODT behavior option on Power Down is set to disable: MR23 OP[4]=1B.

**Figure 126 – Basic Power-Down Entry and Exit Timing: CS ODT, CS ODT Behavior Option on Power Down is Enabled and Dynamic Write NT-ODT is Disabled**

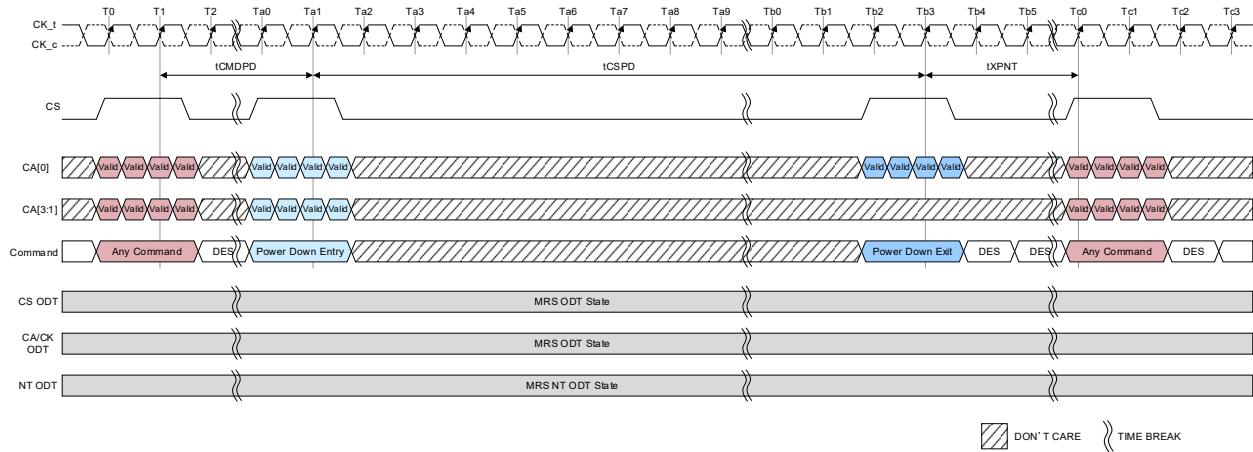
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 2 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 3 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover points of VIHPD(Min).
- NOTE 4 The start point of tCSL/tXP and the end point of tCSL are crossover points of VILPD(Max).
- NOTE 5 Power Down Entry command can be issued at Th0.
- NOTE 6 CA input is required be Low during tCSH.

**Figure 127 – Basic Power-Down Entry and Exit Timing: CS ODT and Dynamic Write NT-ODT is Disabled**

### 7.7.1 Power-Down Entry and Exit (cont'd)



NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.

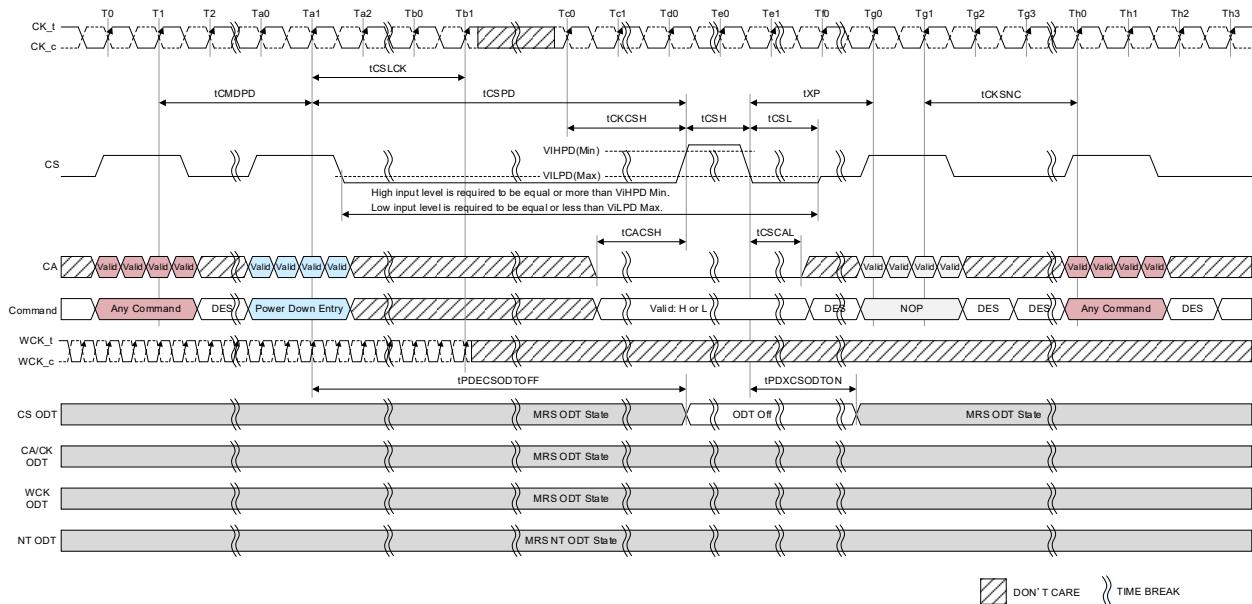
NOTE 2 CK Sync is continued during Power Down.

NOTE 3 During Power Down, CS ODT follows MR17 OP[5:3] regardless of setting for CS ODT behavior option on Power Down: MR23 OP[4].

NOTE 4 CS input is required to keep to low level during Power Down.

**Figure 128 – Basic Power-Down Entry and Exit Timing: Dynamic Write NT-ODT is Enabled**

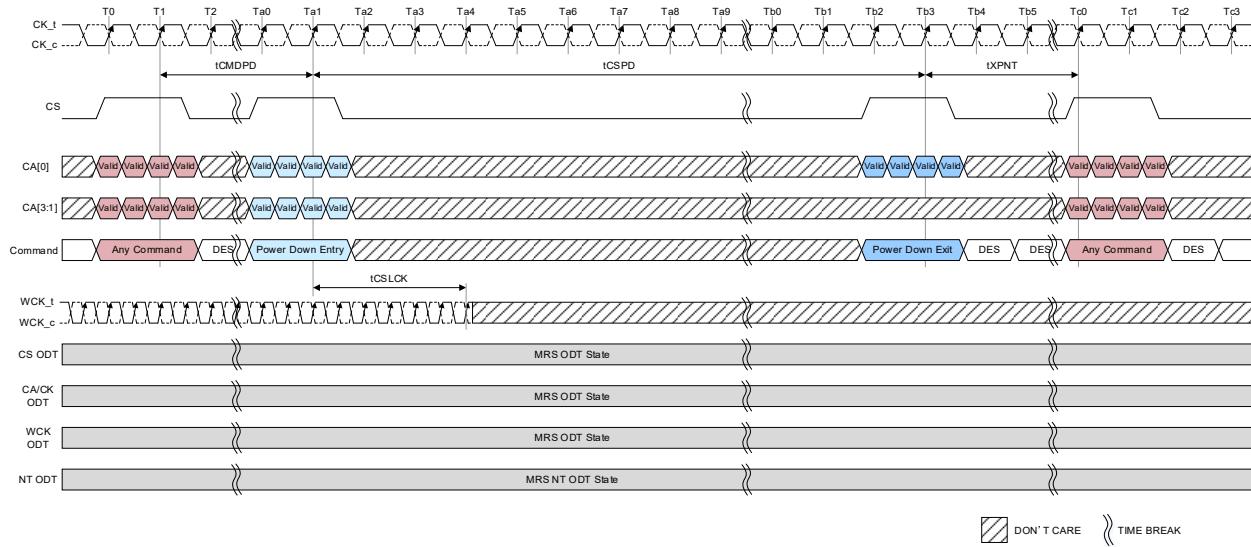
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 2 tWCK2CK is 0 ps in this instance.
- NOTE 3 Input clock frequency can be changed or the input clock can be stopped or floated after tCSLCK is satisfied and during Power Down, provided that upon exiting Power Down, the clock stable and within specified limits for a minimum of tCKCSH of stable clock prior to Power Down exit and clock frequency is between the minimum and maximum specified frequency for the speed grade in use.
- NOTE 4 WCK input is required to be continued at least the end of tCSLCK.
- NOTE 5 The start point of tCSH and the end point of tCSPD/tCKCSH are crossover points of VIHPD(Min).
- NOTE 6 The start point of tCSL/tXP and the end point of tCSL are crossover points of VILPD(Max).
- NOTE 7 Power Down Entry command can be issued at Th0.
- NOTE 8 CA input is required be Low during tCSH.
- NOTE 9 CS ODT behavior option on Power Down is set to disable: MR23 OP[4]=0B.

**Figure 129 – Basic Power-Down Entry and Exit Timing during WCK2CK Sync State:  
Dynamic Write NT-ODT is Disabled**

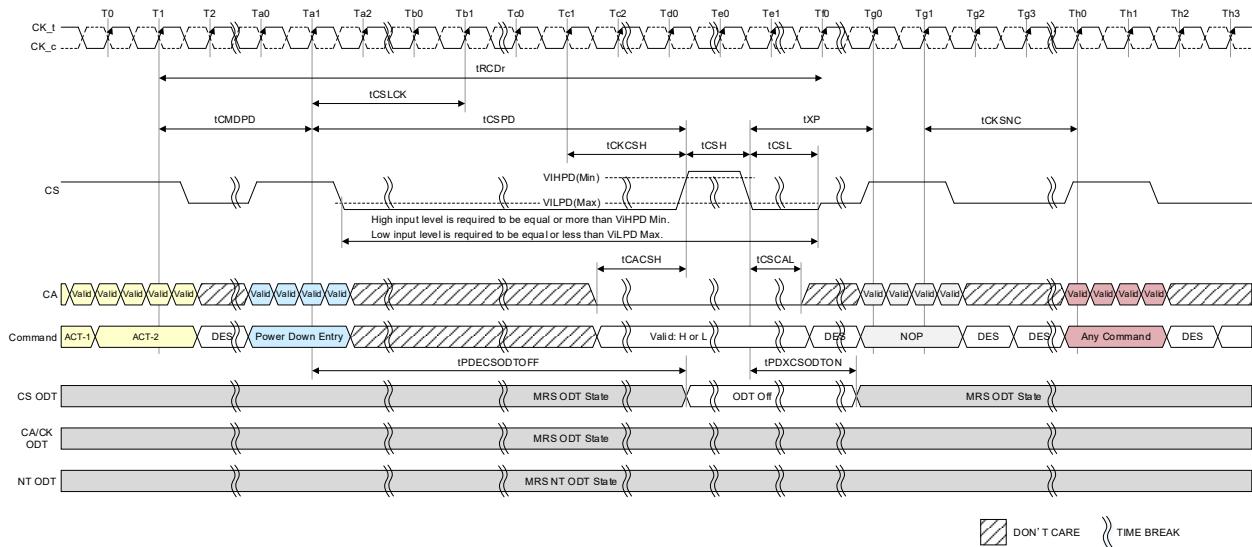
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 DES commands are shown for ease of illustration; other commands may be valid at these times.  
 NOTE 2 CK Sync is continued during Power Down.  
 NOTE 3 tWCK2CK is 0 ps in this instance.  
 NOTE 4 WCK input is required to be continued at least the end of tCSLCK.  
 NOTE 5 During Power Down, CS ODT follows MR17 OP[5:3] regardless of setting for CS ODT behavior option on Power Down: MR23 OP[4].  
 NOTE 6 CS input is required to keep to low level during Power Down.

**Figure 130 – Basic Power-Down Entry and Exit Timing during WCK2CK Sync State:  
Dynamic Write NT-ODT is Enabled**

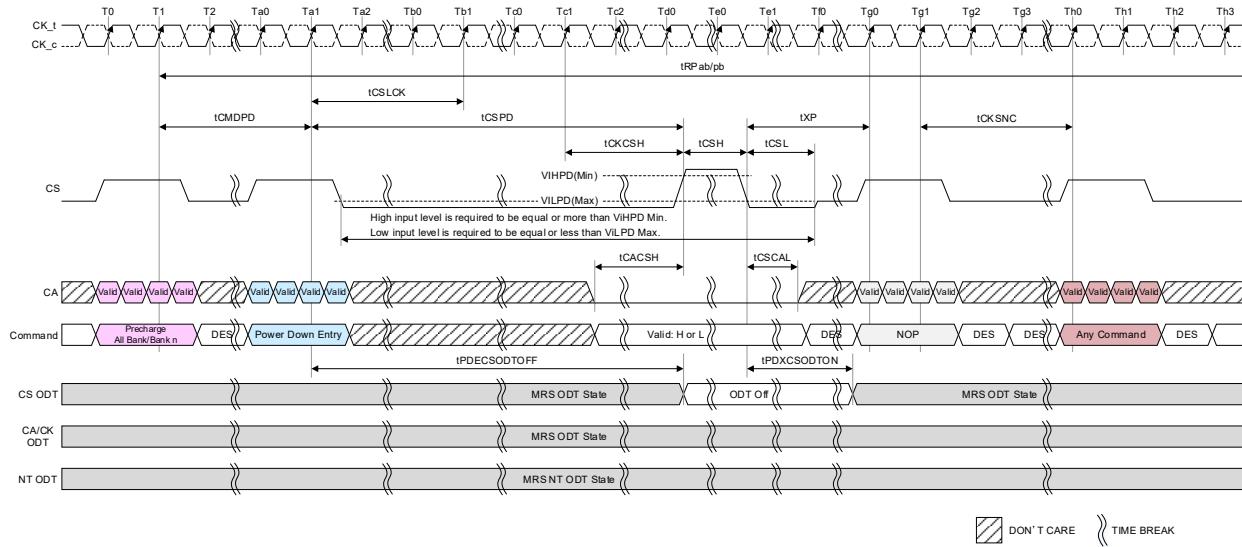
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 Power down exit command (CS High) can be issued if tCSPD is satisfied. There is no dependency for power down exit command on tRCDr. Even though Dynamic Write NT-ODT is enabled, the same situation as Dynamic Write NT-ODT is disabled.
- NOTE 2 Sum of tCMDPD, tCSPD, tCSH, and tXP (tXPNT) is always longer than tRCDr(min) and tRCDw(min).
- NOTE 3 tRCDr and tRCDw are required to be met, if clock is to be stopped or floated after Power Down Entry. Even in this case, tCSLCK is required to be met.

**Figure 131 – Activate to Power Down Entry without Clock Stop/Frequency Change:  
Dynamic Write NT-ODT is Disabled**

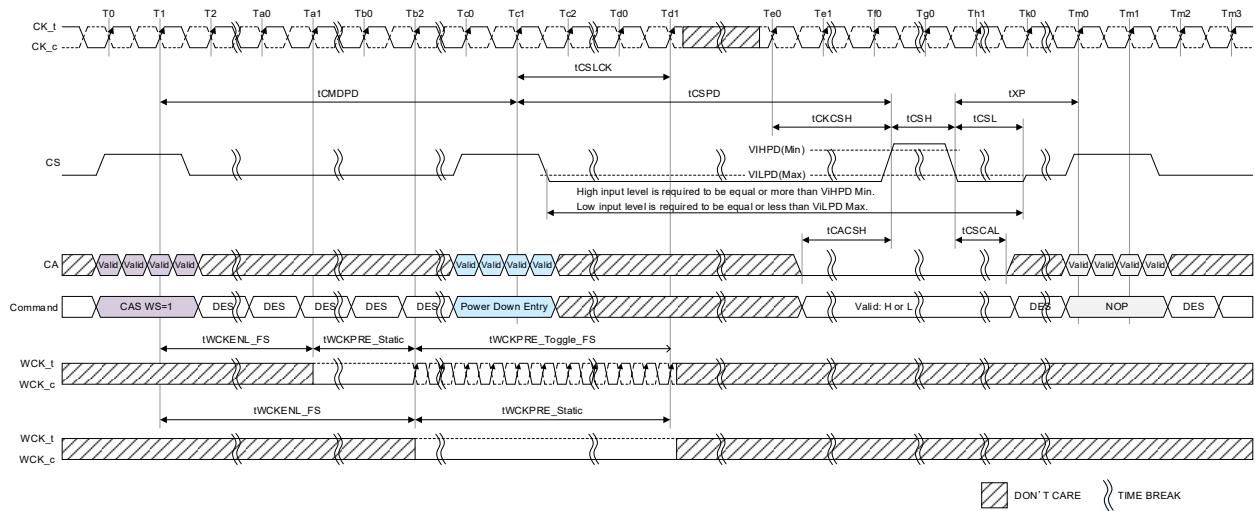
### 7.7.1 Power-Down Entry and Exit (cont'd)



- NOTE 1 Power down exit command (CS High) can be issued if tCSPD is satisfied. There is no dependency for power down exit command on tRPab/pb.  
Even though Dynamic Write NT-ODT is enabled, the same situation as Dynamic Write NT-ODT is disabled.
- NOTE 2 Sum of tCMDPD, tCSPD, tCSH, tXP (tXPNT), 1nCK and tCKSNC is seldom longer than tRPab/pb(min).
- NOTE 3 tRPab/pb(min) is required to be met, if clock is to be stopped or floated after Power Down Entry.

**Figure 132 – All/Per Bank Precharge to Power Down Entry without Clock Stop/Frequency Change: Dynamic Write NT-ODT is Disabled**

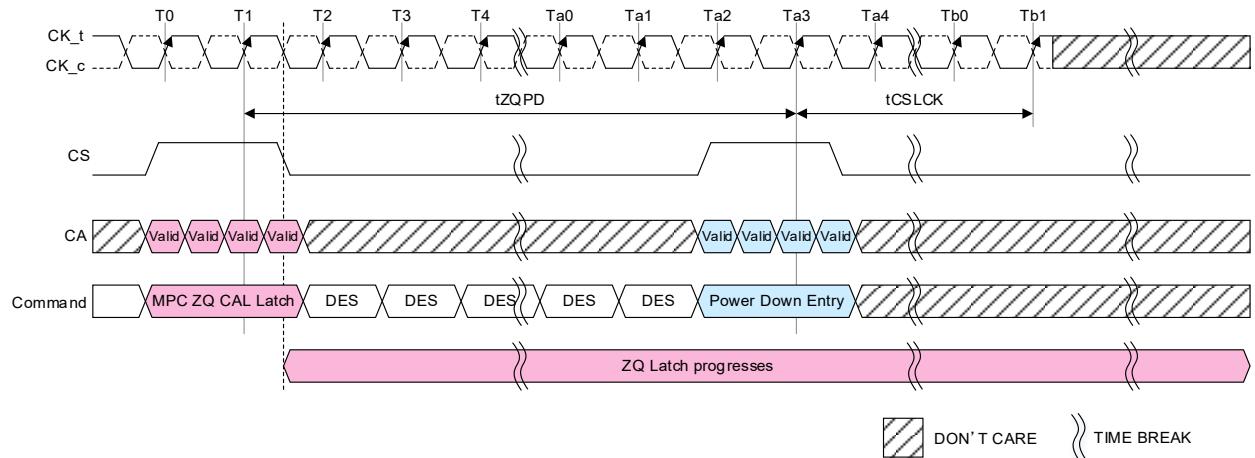
### 7.7.1 Power-Down Entry and Exit (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 WCK input is required to be continued at least the end of tCSLCK.

**Figure 133 – CAS(WS) to Power Down Entry: Dynamic Write NT-ODT is Disabled**

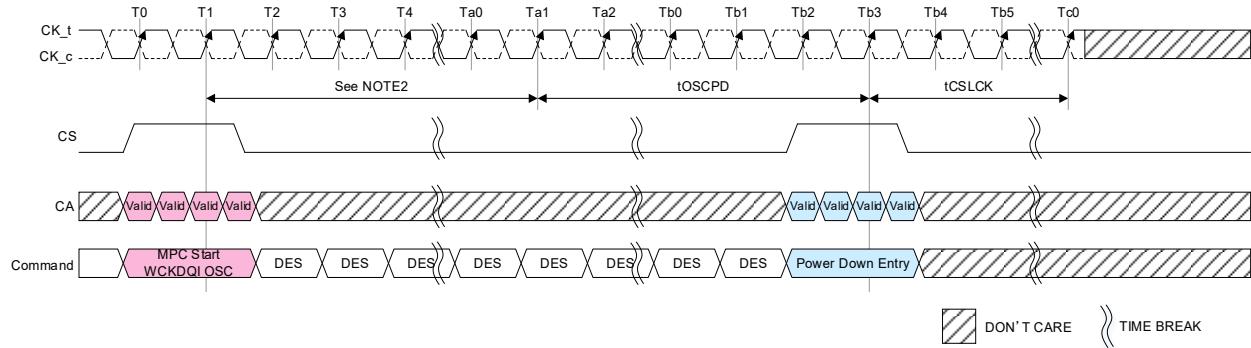


NOTE 1 ZQ Latch continues if Power Down Entry Command is issued after tZQPD is satisfied.

**Figure 134 – Multi Purpose Command for ZQ Latch Command to Power-Down Entry**

### 7.7.1 Power-Down Entry and Exit (cont'd)

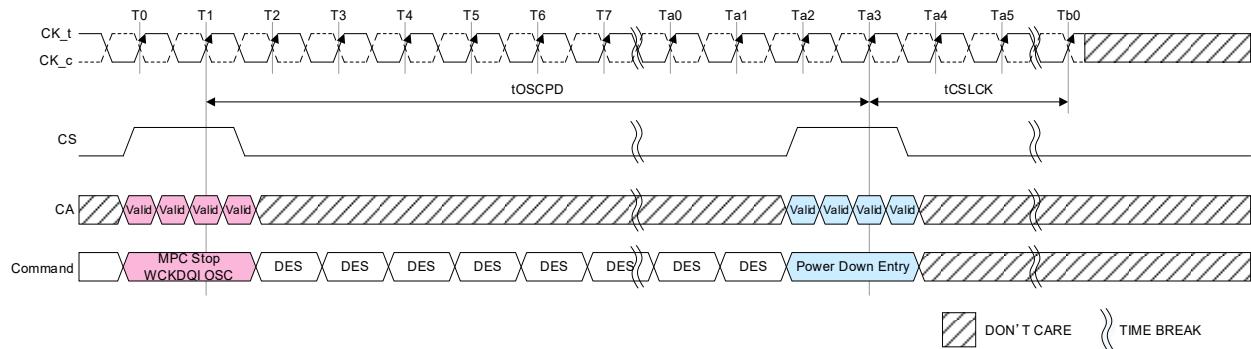
Power Down Entry command can be issued after tCMDPD is satisfied, even though the Oscillator is running. However, in this case, the value of Oscillator Count in MR35/MR36 and MR38/MR39 will be lost. If the value of Oscillator Count in Mode Register would like to be retained, the entering power down timing should be satisfied a following timing.



NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]≠00000000<sub>B</sub>.

NOTE 2 Setting counts of WCK2DQI interval timer run time setting: MR37 OP[7:0]

**Figure 135 – MPC for Start WCK2DQI Interval Oscillator to Power-Down Entry**

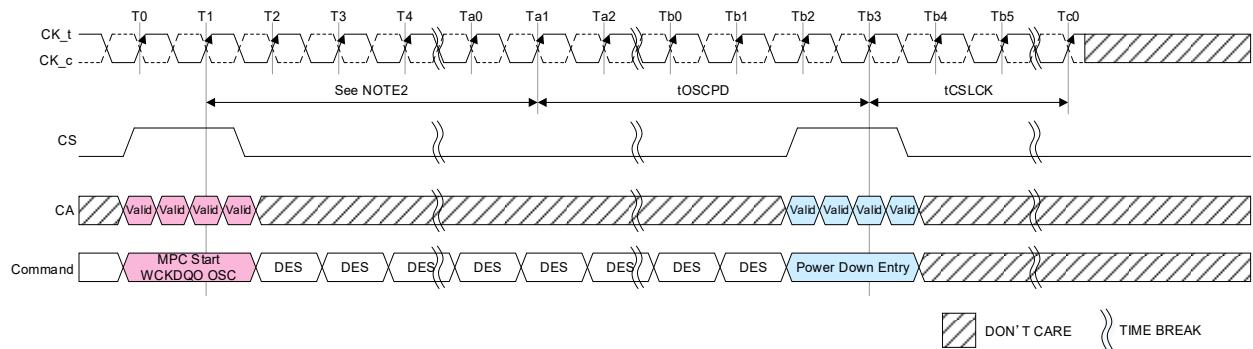


NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]=00000000<sub>B</sub>.

NOTE 2 If WCK2DQI interval timer run stop to automatic is not set: MR37 OP[7:0]=00000000<sub>B</sub>, Stop WCK2DQI Interval Oscillator command is required before Power down Entry for preventing OSC result contamination and saving OSC operating power.

**Figure 136 – MPC for Stop WCK2DQI Interval Oscillator to Power-Down Entry**

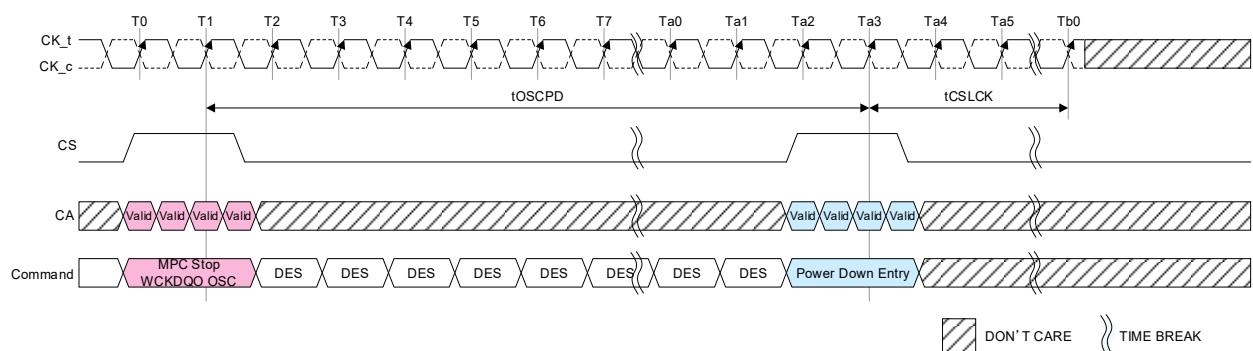
### 7.7.1 Power-Down Entry and Exit (cont'd)



NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]≠00000000<sub>B</sub>.

NOTE 2 Setting counts of WCK2DQO interval timer run time setting: MR40 OP[7:0]

**Figure 137 – MPC for Start WCK2DQO Interval Oscillator to Power-Down Entry**



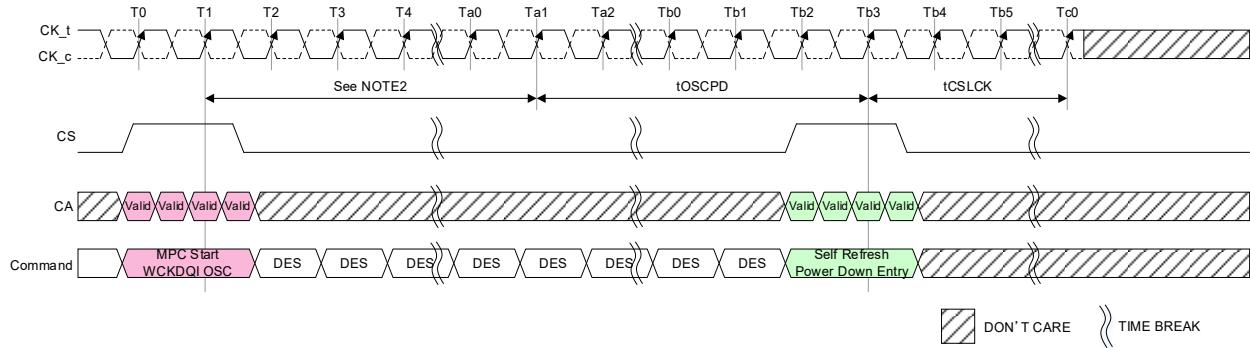
NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]=00000000<sub>B</sub>.

NOTE 2 If WCK2DQO interval timer run stop to automatic is not set: MR40 OP[7:0]=00000000<sub>B</sub>, Stop WCK2DQO Interval Oscillator command is required before Power down Entry for preventing OSC result contamination and saving OSC operating power.

**Figure 138 – MPC for Stop WCK2DQO Interval Oscillator to Power-Down Entry**

### 7.7.1 Power-Down Entry and Exit (cont'd)

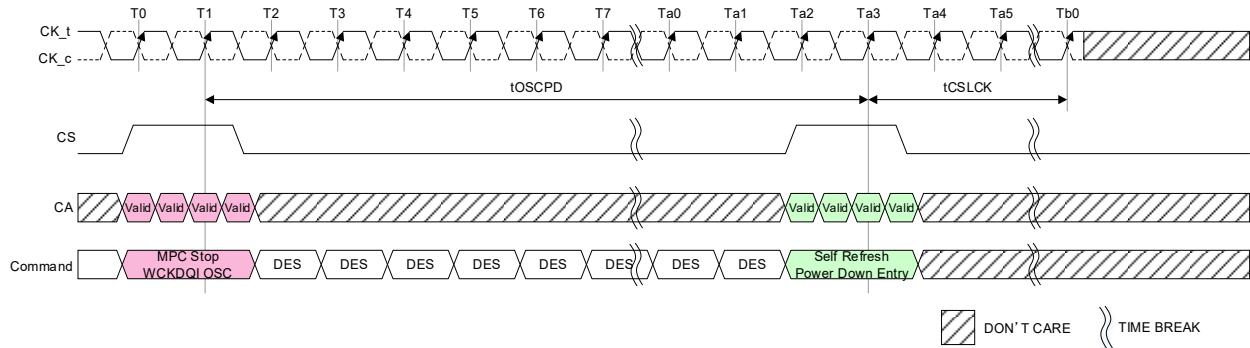
Self Refresh Entry with Power Down Entry command can also be issued after tCMDPD is satisfied, even though the Oscillator is running. However, in this case, the value of Oscillator Count in MR35/MR36 and MR38/MR39 will be lost. If the value of Oscillator Count in Mode Register needs to be retained, the entering Self Refresh Entry with Power Down timing should satisfy the following timing.



NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]≠00000000B.

NOTE 2 Setting counts of WCK2DQI interval timer run time setting: MR37 OP[7:0]

**Figure 139 – MPC for Start WCK2DQI Interval Oscillator to Self Refresh with Power-Down Entry**

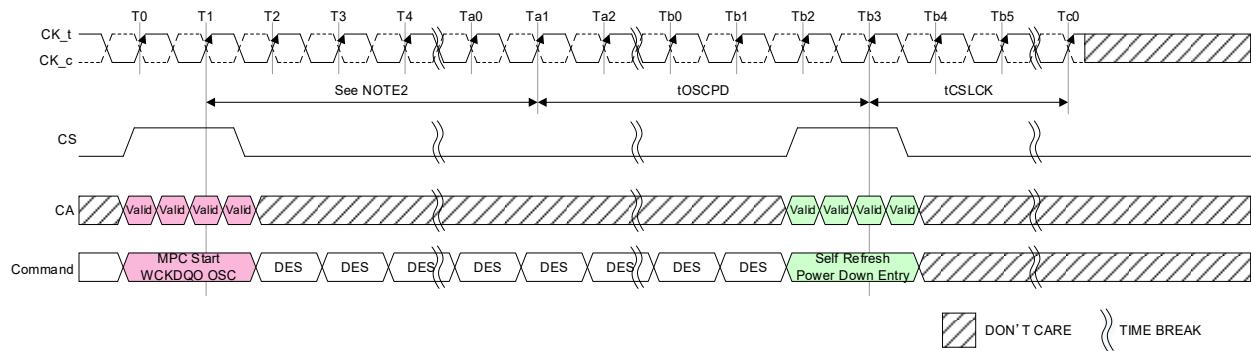


NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]=00000000B.

NOTE 2 If WCK2DQI interval timer run stop to automatic is not set: MR37 OP[7:0]=00000000B, Stop WCK2DQI Interval Oscillator command is required before Self Refresh with Power Down Entry for preventing OSC result contamination and saving OSC operating power.

**Figure 140 – MPC for Stop WCK2DQI Interval Oscillator to Self Refresh with Power-Down Entry**

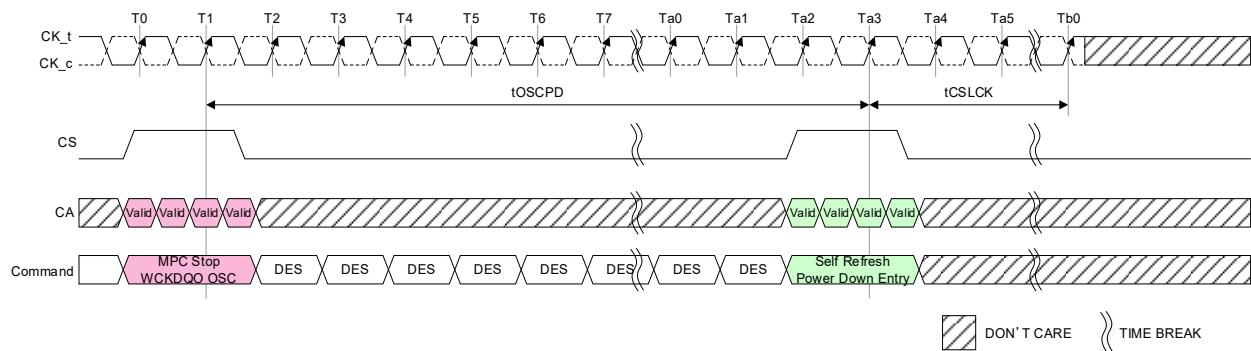
### 7.7.1 Power-Down Entry and Exit (cont'd)



NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]≠00000000B.

NOTE 2 Setting counts of WCK2DQO interval timer run time setting: MR40 OP[7:0]

**Figure 141 – MPC for Start WCK2DQO Interval Oscillator to Self Refresh with Power-Down Entry**



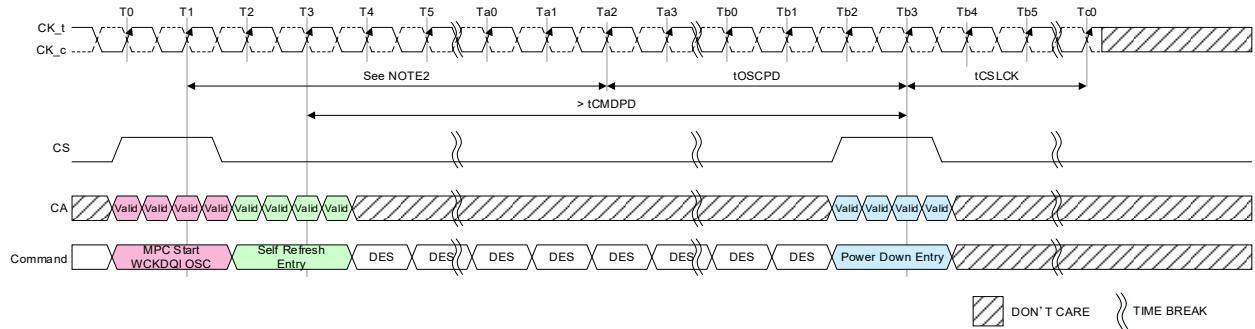
NOTE 1 WCK2DQO interval timer run time setting: MR40 OP[7:0]=00000000B.

NOTE 2 If WCK2DQO interval timer run stop to automatic is not set: MR40 OP[7:0]=00000000B, Stop WCK2DQO Interval Oscillator command is required before Self Refresh with Power Down Entry for preventing OSC result contamination and saving OSC operating power.

**Figure 142 – MPC for Stop WCK2DQO Interval Oscillator to Self Refresh with Power-Down Entry**

### 7.7.1 Power-Down Entry and Exit (cont'd)

If the values of Oscillator Count in MR35/MR36 and MR38/MR39 need to be retained, the delay time from OSC Start/Stop command to Power Down Entry command should satisfy the timing defined in Figure 135 to Figure 138 even though during Self Refresh State.



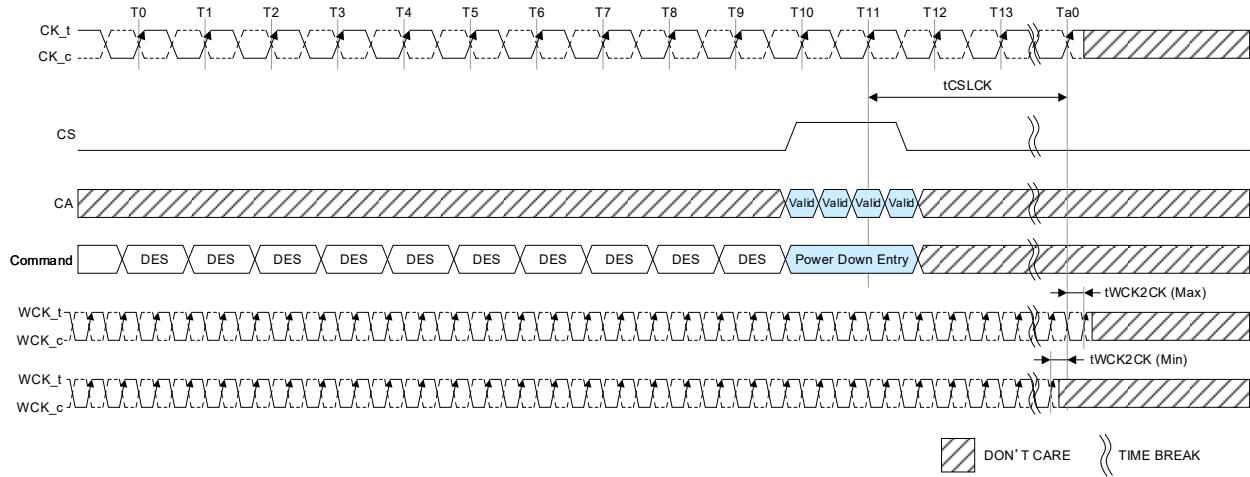
NOTE 1 WCK2DQI interval timer run time setting: MR37 OP[7:0]≠00000000B.

NOTE 2 Setting counts of WCK2DQI interval timer run time setting: MR37 OP[7:0]

**Figure 143 – MPC for Start WCK2DQI Interval Oscillator to Power-Down Entry during Self Refresh**

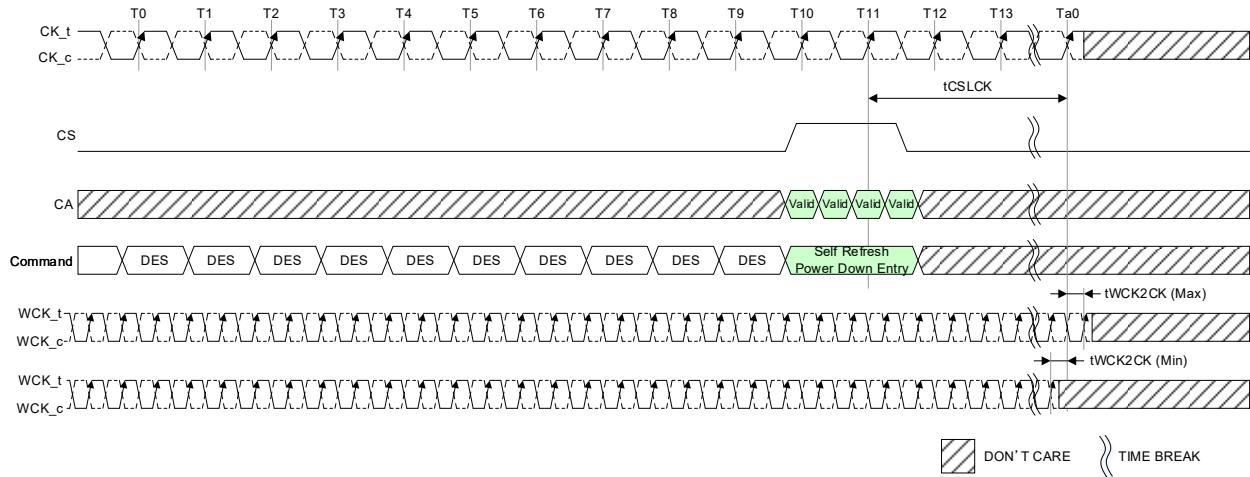
### 7.7.1.1 WCK Input Signal Stop Timing

The WCK input signal stop timing after Power Down and Self Refresh with Power down when WCK Always On mode: MR22 OP[5]=1<sub>B</sub> is as shown in Figure 144 and Figure 145.



NOTE 1 The input Clock and Write Clock can be stopped after tCSLCK is satisfied.

**Figure 144 – Power Down Entry to CK and WCK Stop Timing**



NOTE 1 The input Clock and Write Clock can be stopped after tCSLCK is satisfied.

**Figure 145 – Self Refresh with Power Down Entry to CK and WCK Stop Timing**

### 7.7.1.1 WCK Input Signal Stop Timing (cont'd)

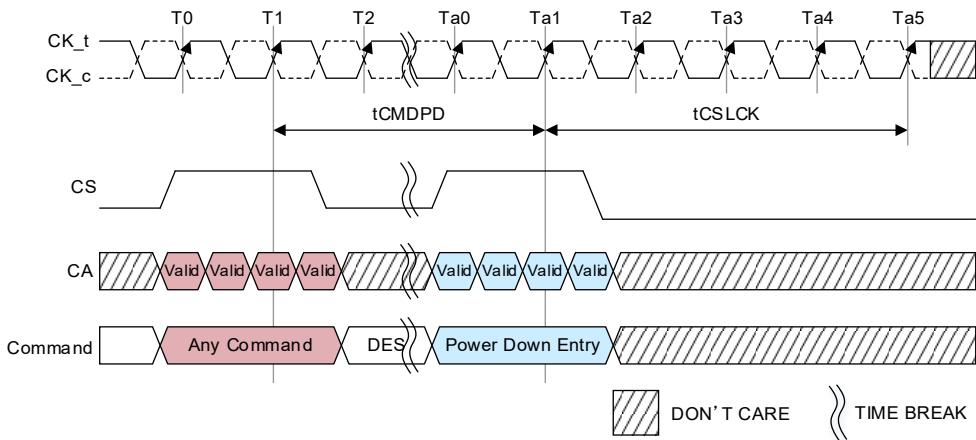
Table 306 and Table 307 apply to both Dynamic Write NT-ODT disable and enable case.

**Table 306 – Power Down AC Timing**

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Power-Down Timing					
Delay time from PDE to CS goes High	tCSPD	Min.	10.0ns + 1tCK	ns	1,2
Delay from valid command to PDE	tCMDPD	Min.	Max(1.75ns, 4nCK)	ns	
Valid Clock Requirement after PDE	tCSLCK	Min.	Max(5ns, 4nCK)	ns	1
Valid Clock Requirement before CS goes High	tCKCSH	Min.	Max(1.75ns, 4nCK)	ns	
Valid Low Requirement for CA before CS goes High	tCACSH	Min	1.75ns	ns	
Exit Power-Down to next NOP command delay	tXP	Min.	Max(7ns, 4nCK)	ns	1
Minimum CS High Pulse width @ PDX	tCSH	Min.	3	ns	
Minimum CS Low Duration time @ PDX	tCSL	Min.	4	ns	
Minimum CA Low Duration time @ PDX	tCSCAL	Min.	1.75	ns	
Delay from MRW command to PDE	tMRWPD	Min.	Max(14ns, 6nCK)	ns	1, 3
Delay from ZQ Calibration Latch Command to PDE	tZQPD	Min.	4nCK	ns	
Delay from MPC OSC Start/Stop Command to PDE	tOSCPD	Min.	Max(40ns,8nCK)	ns	
Delay from PD Entry to CS ODT OFF	tPDECSODTOFF	Max.	10ns + 1tCK	ns	2
Delay from Power Down Exit to CS ODT ON	tPDXCSODTON	Max.	Max(6ns, 2nCK)	-	
Power-Down Exit (PDX-NT) to next valid command delay	tXPNT	Min.	Max(10ns, 4nCK)	ns	1

**Table 306 — Power Down AC Timing (cont'd)**

NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK).  
For example, tCSLCK will not expire until CK has toggled through at least 4 full cycles( $4 \cdot tCK$ ) and 5 ns has transpired.  
The case for which 4nCK is applied to is shown below.



- NOTE 2 The tCK value is required to follow the operating frequency of when the PDE command is issued.
- NOTE 3 A following MR change defined Table 308 applies special delay time.  
 VREF(CS): MR15 OP[6:0]  
 VREF(CA): MR12 OP[6:0]  
 VREF(DQ[11:0]): MR14 OP[6:0]  
 VRCG: MR13 OP[3]
- NOTE 4 Power down AC timing is unaffected by System Meta mode and Dynamic/ Static Efficiency mode setting (Enable/Disable).

### 7.7.1.1 WCK Input Signal Stop Timing (cont'd)

**Table 307 — Power Down Entry Command Timing Constraint**

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
ACT-2	Power Down Entry	tCMDPD	-	
All Bank Precharge		nACU + tCMDPD	-	
Per Bank Precharge		nACU + tCMDPD	-	
Read (ODT Disable)		RL+RU(tWCK2DQO(max)/tCK)+BL/n_max+RU(tWCKPST/tCK)	-	1,7
Read with AP (ODT Disable)		Max((RL+RU(tWCK2DQO(max)/tCK)+BL/n_max+RU(tWCKPST/tCK)),(nRTP+nACU+tCMDPD))	-	7
Read (ODT Enable)		ODTLon_RD+RU(tODT_RDon(max)/tCK)+2nCK	-	1,2
Read with AP (ODT Enable)		Max((ODTLon_RD+RU(tODT_RDon(max)/tCK)+2nCK),(nRTP+nACU+tCMDPD))	-	3
Write		WL + RU(tWCK2DQI(max)/tCK) + BL/n_max + nWTP + nACU	-	4,8,9
Write with AP		WL + RU(tWCK2DQI(max)/tCK) + BL/n_max + nWTP + nACU + tCMDPD	-	5,8,9
Mode Register Read (ODT Disable)		RL+RU(tWCK2DQO(max)/tCK)+BL/n_max+RU(tWCKPST/tCK)	-	7
Mode Register Read (ODT Enable)		ODTLon_RD+RU(tODT_RDon(max)/tCK)+2nCK	-	
Mode Register Write-2		tMRWPD	-	
CAS(WS=1)		tCMDPD	-	10
CAS(WS_OFF=1)		tCMDPD	-	
CAS(WS=0, WS_OFF=0)		tCMDPD	-	
MPC ZQCAL Latch		tZQPD	-	
MPC Start WCK2DQI OSC		WCK2DQI interval timer run time setting + tOSCPD (When WCK2DQI timer stops automatically.)	-	
MPC Stop WCK2DQI OSC		tOSCPD (When WCK2DQI timer stop by OSC stop command.)	-	
MPC Start WCK2DQO OSC		WCK2DQO interval timer run time setting + tOSCPD (When WCK2DQO timer stops automatically.)	-	
MPC Stop WCK2DQO OSC		tOSCPD (When WCK2DQO timer stop by OSC stop command.)	-	

**Table 307 – Power Down Entry Command Timing Constraint (cont'd)**

NOTE 1	Read and Read with AP to Power-Down Entry timing also applies following case. - Read FIFO command to Power Down entry command - Read DQ Calibration command to Power Down entry command - Mode Register Read command to Power Down entry command
NOTE 2	Including Meta-Read command. Refer to System Meta Function Mode: 7.5.6 for detail.
NOTE 3	Including Meta-Read with Precharge command. Refer to System Meta Function Mode: 7.5.6 for detail.
NOTE 4	Including Meta-Write command. Refer to System Meta Function Mode: 7.5.6 for detail.
NOTE 5	Including Meta-Write with Precharge command. Refer to System Meta Function Mode: 7.5.6 for detail.
NOTE 6	Power Down Entry Command Timing Constraint is unaffected by System Meta mode and Efficiency mode setting (Enable/Disable). As well as Static Efficiency mode.
NOTE 7	tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR11 OP[6]: WCK Frequency Mode setting. MR11 OP[6]=0 <sub>B</sub> : tWCK2DQO_LF(max) MR11 OP[6]=1 <sub>B</sub> : tWCK2DQO_HF(max).
NOTE 8	tWCK2DQI(max) is applied tWCK2DQI_LF(max) or tWCK2DQI_HF(max) depending on MR11 OP[6]: WCK Frequency Mode setting. MR11 OP[6]=0 <sub>B</sub> : tWCK2DQI_LF(max) MR11 OP[6]=1 <sub>B</sub> : tWCK2DQI_HF(max).
NOTE 9	This Timing is applied regardless of DQ ODT Disable/Enable setting: MR19 OP[2:0].
NOTE 10	WCK input is required to be continued at least the end of tCSLCK.

**Table 308 – Special Timing to Mode Register Write to Power Down Entry**

Current Command	Next Command	Timing Constraints (Min)	Note
MRW to VREF(CS) Setting	Power Down Entry	tVREFCS_Long(max) = 250 ns + 0.5tCK tVREFCS_Short(max) = 200 ns + 0.5tCK tVREFCS_Weak(max) = 1 ms	
MRW to VREF(CA) Setting		tVREFCA_Long(max) = 250 ns + 0.5tCK tVREFCA_Short(max) = 200 ns + 0.5tCK tVREFCA_Weak(max) = 1 ms	
MRW to VREF(DQ) Setting		tVREFDQ_Long(max) = 250 ns + 0.5tCK tVREFDQ_Short(max) = 200 ns + 0.5tCK tVREFDQ_Weak(max) = 1 ms	
MRW to VRCG Enable		VRCG_ENABLE(max) = 150 ns	
MRW to VRCG Disable		tVRCG_DISABLE(max) = 100 ns	

## 7.8 Other Operation

### 7.8.1 Mode Register Read

The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR6 SDRAM registers. The MRR command is initiated with CS and CA[3:0] in the proper state as defined by the Command Truth Table, Table 254. The mode register address operands (MA[7:0]) allow the user to select one of 256 registers. The mode register contents are available on the first 12 UI's data bits of DQ[7:0] after RL + tWCK2DQO following the MRR command. Subsequent data bits contain valid but undefined content. WCK is toggled for the duration of the Mode Register Read burst. MRR has a command burst length 24.

MRR operation must not be interrupted.

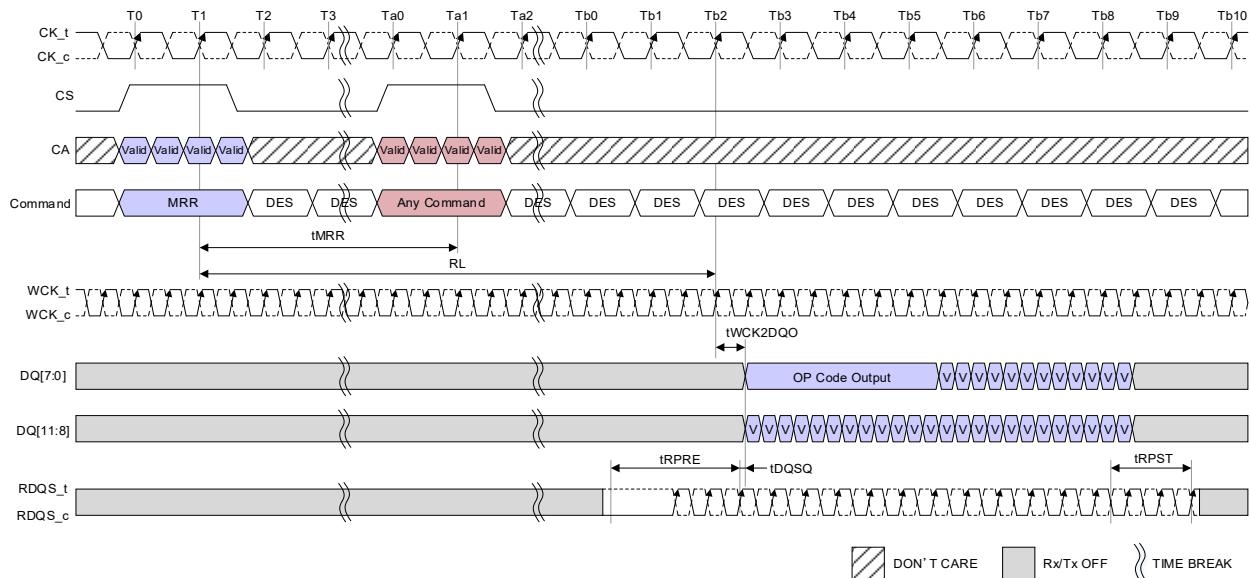
Mode Register Read behavior regarding Efficiency mode is defined in other sections.

**Table 309 – DQ Output Mapping**

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
DQ0	OP0												V											
DQ1	OP1												V											
DQ2	OP2												V											
DQ3	OP3												V											
DQ4	OP4												V											
DQ5	OP5												V											
DQ6	OP6												V											
DQ7	OP7												V											
DQ[11:8]	V												V											

NOTE 1 MRR data is extended to first 12 UI's for SDRAM controller to sample data easily.  
NOTE 2 "V" means "H" or "L" (a defined logic level).  
NOTE 3 The read preamble and postamble of MRR are the same as normal read operation.

### 7.8.1 Mode Register Read (cont'd)



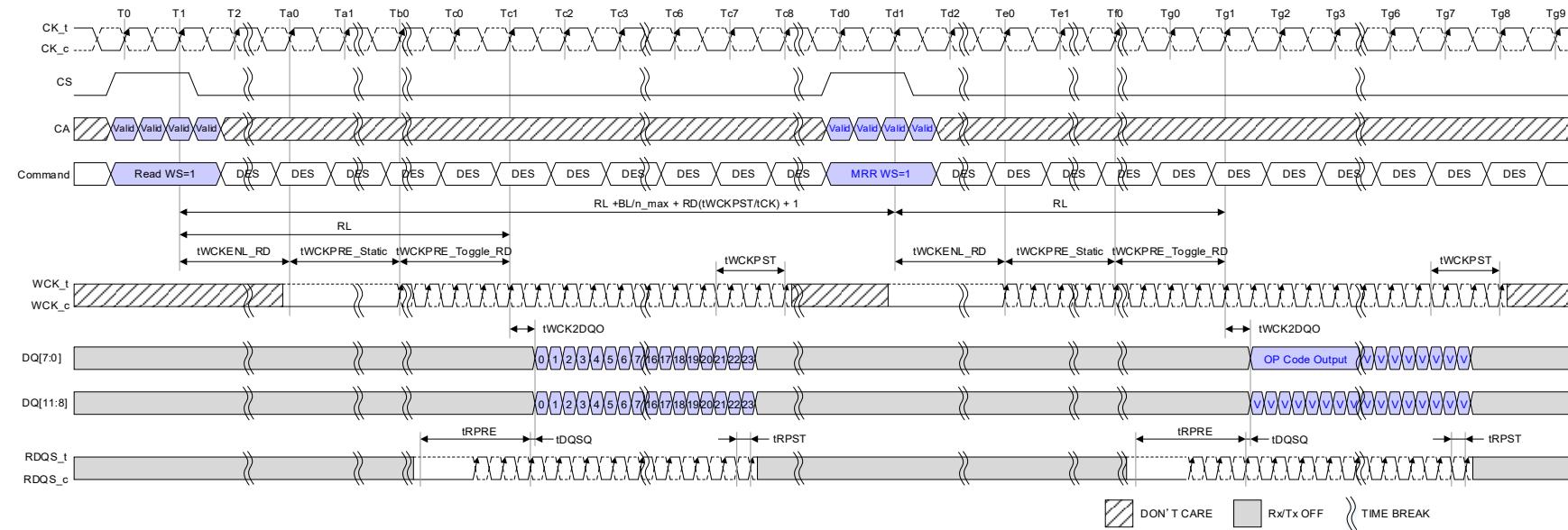
- NOTE 1 WCK2CK Sync state (WCK Always On mode).
- NOTE 2 tWCK2CK is 0 ps in this instance.
- NOTE 3 BL=24, tRPRE=2tWCK (Static) + 2tWCK (Toggle), tRPST=2.5tWCK(Toggle)
- NOTE 4 Only DES is allowed during tMRR period.
- NOTE 5 There are some exceptions about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints: Table 399 for details.
- NOTE 6 DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.
- NOTE 7 tWCK2CK is 0 ps in this instance.

Figure 146 – Mode Register Read Operation

### 7.8.1.1 MRR after Read and Write Command

After a prior Read and Read with AP Command, the MRR command shall not issue earlier than the period defined by MRR/MRW Timing Constraints: Table 399.

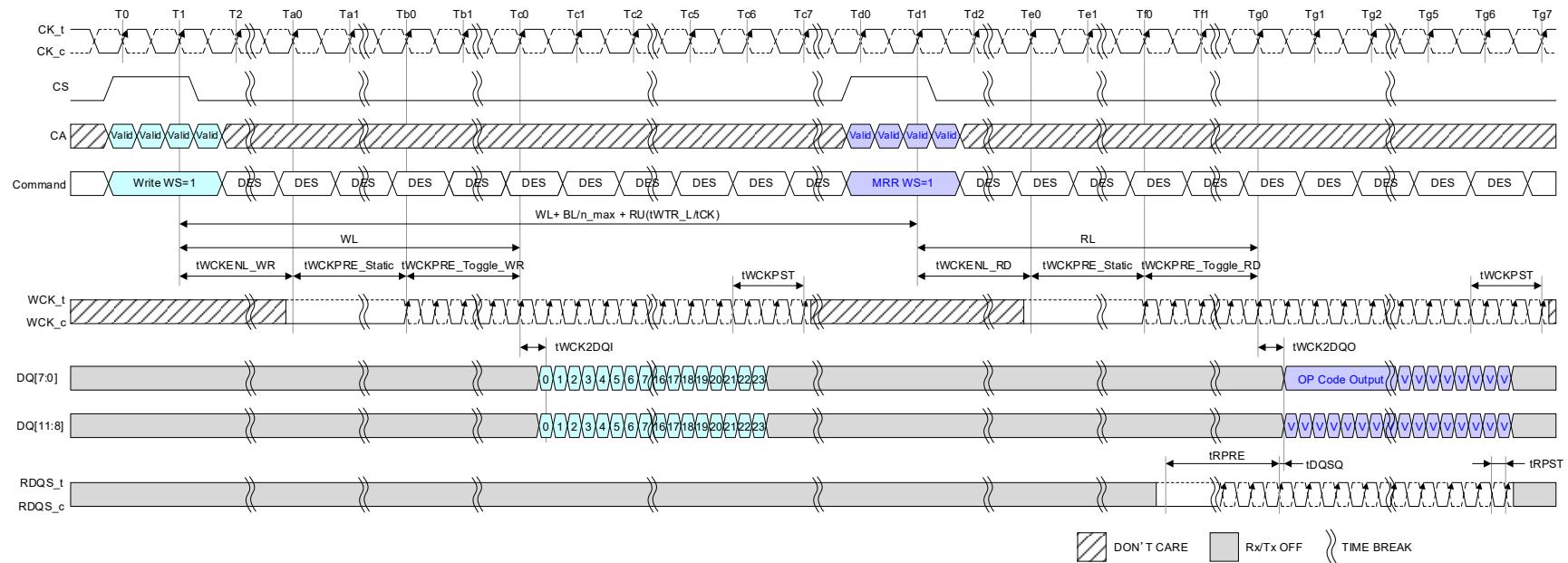
In a similar way MRR command shall not issue the period defined by MRR/MRW Timing Constraints: Table 399 after a prior Write, Write with AP and Write FIFO command in order to avoid the collision of Read and Write burst data on SDRAM's internal Data bus.



- NOTE 1 The minimum number of clock cycles from the burst READ command to the MRR command is  $RL + BL/n_{max} + RD(tWCKPST/tCK) + 1nCK$ . The timing variable "BL/n\_max" is defined in the effective burst length table.
- NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 3 tWCK2CK is 0 ps in this instance.
- NOTE 4 BL=24, tWCKPST=2.5tWCK

**Figure 147 – Read to MRR Timing**

### 7.8.1.1 MRR after Read and Write Command (cont'd)

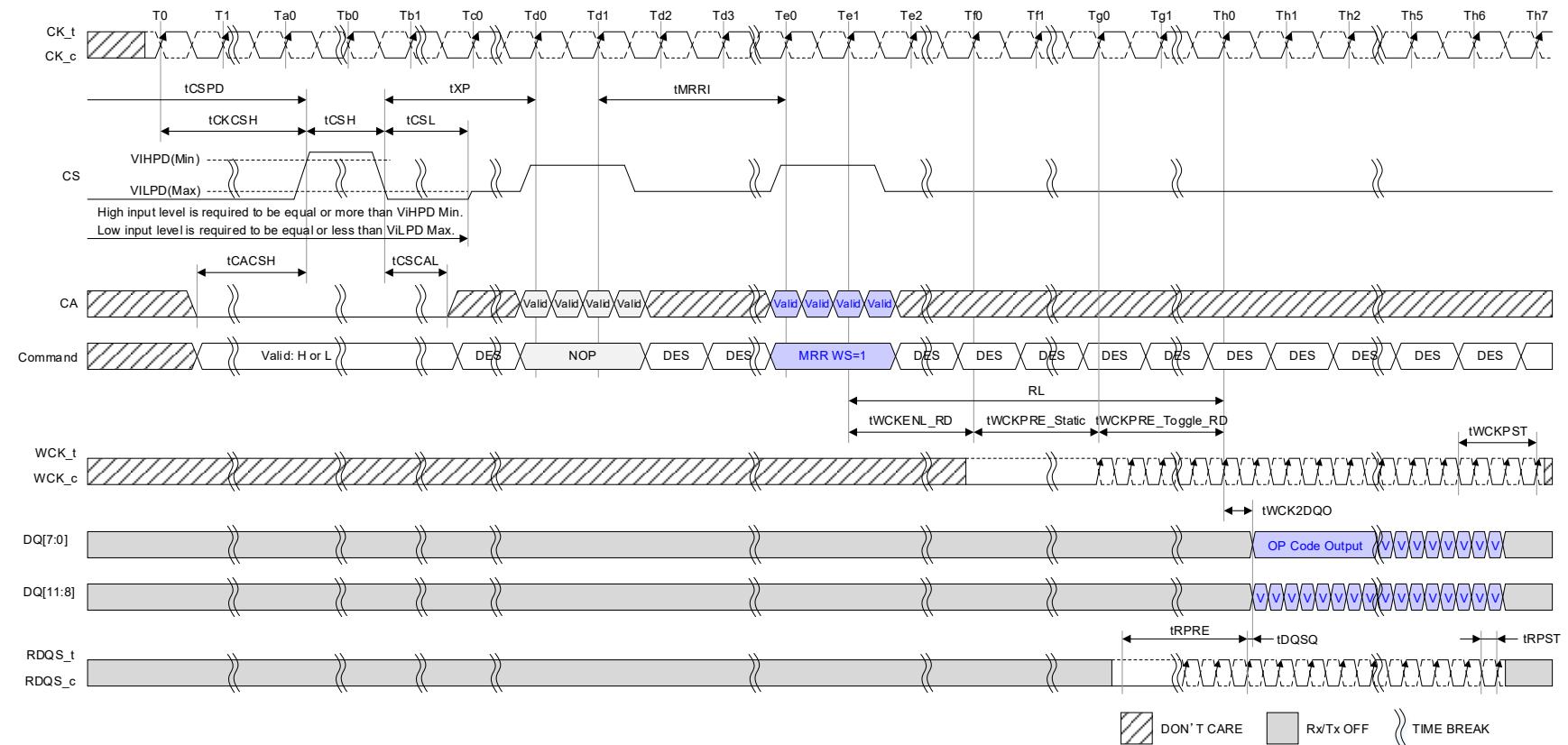


- NOTE 1 NOTE 1 The minimum number of clock cycles from the burst write command to the MRR command is  $WL + BL/n_{max} + RU(tWTR\_L/tCK)$ . The timing variable "BL/n<sub>max</sub>" is defined in the effective burst length table.
- NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.
- NOTE 3 tWCK2CK is 0 ps in this instance.
- NOTE 4 BL=24, tWCKPST=2.5tWCK

Figure 148 – Write to MRR Timing

### 7.8.1.2 MRR after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time is required to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode.



NOTE 1 tMRRI contains tCKSNC.

NOTE 2 Even if using CAS(WS=1) and MRR(WS=0) combination, need to satisfy tMRRI from CK\_t second rising edge of NOP command to issue MRR command.

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 4 tWCK2CK is 0 ps in this instance.

Figure 149 – MRR after Power-Down Exit

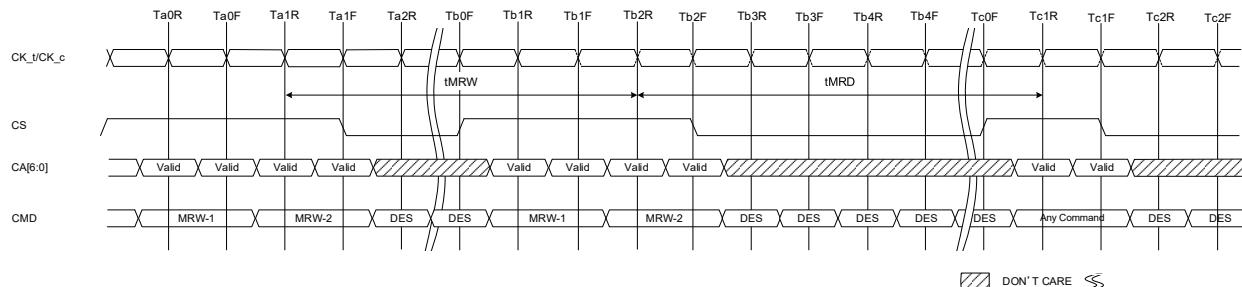
### 7.8.1.2 MRR after Power-Down Exit (cont'd)

**Table 310 – Mode Register Read/Write AC Timing**

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min.	TBD	ns	1
MODE REGISTER READ command period	tMRR	Min.	12	nCK	
MODE REGISTER WRITE command period	tMRW	Min.	Max (10ns, 4nCK)	ns	
Mode register set command delay	tMRD	Min.	Max (14ns, 4nCK)	ns	
NOTE 1 tMRRI contains tCKSNC.					

### 7.8.2 Mode Register Write

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CS and CA[6:0] to valid levels as defined in Table 254. The mode register address and the data written to the mode registers is contained in CA[6:0]. The Mode Register Write command is composed of two commands, MRW-1 command and MRW-2 command. However, MRW-1 command must be followed by MRW-2 command. The MRW command period is defined by tMRW. The Mode Register Write command to read-only registers have no impact on the functionality of the device.



NOTE 1 Only DES command is allowed during tMRW and tMRD periods.

**Figure 150 – Mode Register Write Timing**

**Table 311 – Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)**

Current State	Command	Intermediate State	Next State
		SDRAM	SDRAM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading	Bank(s) Active
	MRW	Mode Register Writing	Bank(s) Active

### **7.8.2.1 Mode Register Write control for Efficiency Mode**

Will update MRW with Efficiency mode.

### **7.8.3 Frequency Set Point**

Frequency Set Points (FSP) allow the LPDDR6 SDRAM CA Bus to be switched between 3 differing operating frequencies, with changes in voltage swings and termination values, without ever being in an untrained state which could result in a loss of communication to the SDRAM. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These tripled registers form 3 sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the DRAM operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for a selected Frequency Set-Point without affecting the LPDDR6-SDRAM's current operation. Once all necessary parameters have been written to the selected Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

### 7.8.3 Frequency Set Point (cont'd)

Parameters which have 3 physical registers controlled by FSP-WR and FSP-OP include:

**Table 312 – Mode Register Function with 3 Physical Registers (TBD)**

MR#	Operand	Function	Note
MR1	OP[3]	CK mode	
	OP[7:4]	WL (Write Latency)	
MR2	OP[3:0]	RL (Read latency) and nRBTP(READ burst end to PRECHARGE delay)	
	OP[7:4]	nWR(Write Recovery for Auto Precharge commands)	
MR3	OP[2:0]	PDDS (Pull-Down Drive Strength)	
	OP[4:3]	BK/BG-ORG (Bank/Bank Group Organization)	
	OP[5]	WLS (Write Latency Set)	
	OP[6]	DBI RD (DBI Read select)	
	OP[7]	DBI WR (DBI Write select)	
MR10	OP[0]	RDQS Postamble mode	
	OP[1]	RDQS PRE 2 (RD Pre-amble Length)	
	OP[3:2]	WCK PST (WCK Post-amble Length)	
	OP[5:4]	RDQS PRE (RD Pre-amble Length)	
	OP[7:6]	RDQS PST (RD Post-amble Length)	
MR11	OP[2:0]	DQ ODT (DQ Bus Receiver On-Die Termination)	
	OP[3]	NT-ODT Enable (Non Target ODT Enable)	
	OP[6:4]	CA ODT (CA Bus Receiver On-Die Termination)	
	OP[7]	CS ODT OP (CS ODT behavior option)	
MR12	OP[6:0]	V <sub>REF</sub> (CA) (V <sub>REF</sub> (CA) Setting)	
MR14	OP[6:0]	V <sub>REF</sub> (DQ[7:0]) (V <sub>REF</sub> (DQ[7:0]) Setting)	
MR15	OP[6:0]	V <sub>REF</sub> (DQ[15:8]) (V <sub>REF</sub> (DQ[15:8]) Setting)	
MR17	OP[2:0]	SeC ODT (Controller ODT Value for VOH calibration)	
	OP[3]	ODTD CK (CK ODT termination)	
	OP[4]	ODTD CS (CS ODT termination)	
	OP[5]	ODTD CA (CA ODT termination)	
MR18	OP[2:0]	WCK-ODT	
	OP[3]	WCK FM (WCK Frequency Mode)	
	OP[4]	WCK-ON (WCK always ON mode)	
	OP[7]	CKR (WCK to CK frequency ratio)	
MR19	OP[1:0]	DVFSC (VDD2 Dynamic Voltage and Frequency Scaling Core)	
	OP[3:2]	DVFSQ (VDDQ Dynamic Voltage and Frequency Scaling VDDQ)	
	OP[4]	WCK2DQ OSC-FM	
	OP[7:6]	CS ODT (CS termination)	
MR20	OP[1:0]	RDQS (Read-DQS)	
	OP[3:2]	WCK mode	
MR22	OP[5:4]	WECC (Write-link ECC Control)	
	OP[7:6]	RECC (Read-link ECC Control)	
MR24	OP[2:0]	DFE Quantity for Lower Byte (DFEQL)	
	OP[6:4]	DFE Quantity for Upper Byte (DFEQU)	
MR30	OP[3:0]	DCA for Lower Byte (DCAL)	
	OP[7:4]	DCA for Upper Byte (DCAU)	
MR41	OP[0]	Per-pin DFE Control (PDFEC)	
	OP[7:5]	NT-DQ-ODT (Non Target DQ Bus Receiver On-Die Termination)	
MR58	OP[1:0]	DQ Up Emphasis LB (DQ pull-up pre-emphasis lower Byte)	
	OP[3:2]	DQ Dn Emphasis LB (DQ pull-down pre-emphasis lower Byte)	
	OP[5:4]	DQ Up Emphasis UB (DQ pull-up pre-emphasis upper Byte)	
	OP[7:6]	DQ Dn Emphasis UB (DQ pull-down pre-emphasis upper Byte)	
MR69	OP[3:0]	Read DCA for Lower Byte (RDCAL)	
	OP[7:4]	Read DCA for Upper Byte (RDCAU)	
See Mode Register Definition section for more details.			

### 7.8.3 Frequency Set Point (cont'd)

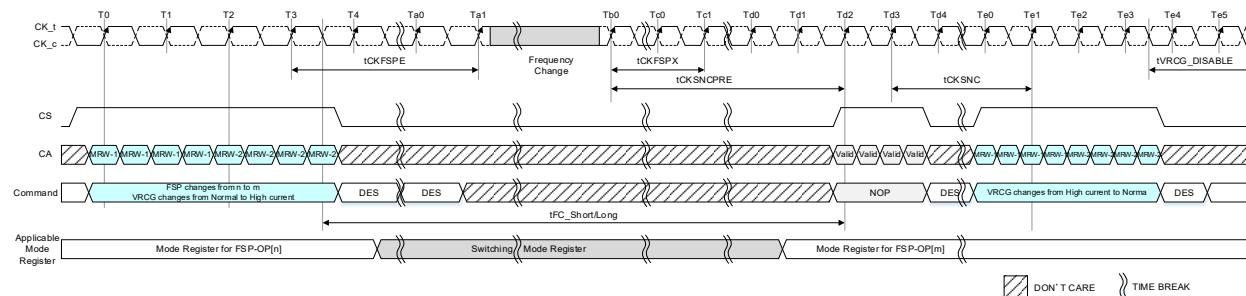
Table 313 shows how the 3 mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

**Table 313 – Relation between MR Setting and DRAM Operation**

Function	MR# and Operand	Data	Operation	Note		
FSP-WR	MR16 OP[1:0]	00 <sub>B</sub> (Default)	Data write to Mode Register N for FSP-OP[0] by MRW Command. Data read from Mode Register N for FSP-OP[0] by MRR Command.	1		
		01 <sub>B</sub>	Data write to Mode Register N for FSP-OP[1] by MRW Command. Data read from Mode Register N for FSP-OP[1] by MRR Command.			
		10 <sub>B</sub>	Data write to Mode Register N for FSP-OP[2] by MRW Command. Data read from Mode Register N for FSP-OP[2] by MRR Command.			
FSP-OP	MR16 OP[3:2]	00 <sub>B</sub> (Default)	SDRAM operates with Mode Register N for FSP-OP[0] setting.	2		
		01 <sub>B</sub>	SDRAM operates with Mode Register N for FSP-OP[1] setting.			
		10 <sub>B</sub>	SDRAM operates with Mode Register N for FSP-OP[2] setting.			
NOTE 1 FSP-WR stands for Frequency Set Point Write/Read.						
NOTE 2 FSP-OP stands for Frequency Set Point Operating Point.						

#### 7.8.3.1 Frequency Set Point Update Timing

The Frequency set point update timing is shown in Figure 151. When changing the frequency set point via MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into VREF Fast Response (high current) mode at the same time. After Frequency change time(tFC) is satisfied. VRCG can be changed into Normal Operation mode via MR16 OP[6].



NOTE 1 The Clock frequency change should be made during the 'frequency change' timing (Ta1 to Tb0).

For more information, refer to 7.8.6 Input Clock Stop and Frequency Change.

NOTE 2 From the rising edge of CK\_t (at cycle T4) until the rising edge of CK\_t at the end of tCKFSPX timing (Tc1), Only DES command is allowed and CS should keep Low.

**Figure 151 – Frequency Set Point Switching Timing**

### 7.8.3.1 Frequency Set Point Update Timing (cont'd)

**Table 314 – Frequency Set Point AC Timing Table**

Item	Symbol	Min/Max	Value	Unit	Notes		
Frequency Set Point parameters							
Frequency Set Point Switching Time	tFC_Short	Min	200	ns	1,2		
	tFC_Long	Min	250	ns	1,2		
Valid Clock Requirement after Entering FSP Change	tCKFSPE	Min	max(7.5ns, 4nCK)		-		
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	Min	max(7.5ns, 4nCK)		-		
NOTE 1	Frequency Set Point Switching Time depends on value of V <sub>REF</sub> (CA) setting: MR12 OP[6:0] of FSP-OP 0, 1 and 2 and V <sub>REF</sub> (CS) setting : MR15 OP[6:0] of FSP-OP 0, 1 and 2. The details are shown in Table 315. Additionally, change of Frequency Set Point may affect V <sub>REF</sub> (DQ) setting. Settling time of V <sub>REF</sub> (DQ) level is same as V <sub>REF</sub> (CA) level.						
NOTE 2	tCK for this timing is the tCK value of the operating frequency when the MRW is issued.						

**Table 315 – tFC Value Mapping**

Application	Step Size	
	From FSP -OP0	To FSP-OP1
tFC_Short	Base	A single step size increment/decrement
tFC_Long	Base	Equal to or more than 2 step size increment/decrement
NOTE 1 Changing from FSP-OPx to FSP-OPy is also supported.		

Table 316 provides an example of tFC value mapping when FSP-OP moves from OP0 to OP1.

**Table 316 – tFC Value Mapping Example**

Case	From/To	FSP-OP: MR16 OP[3:2]	V <sub>REF</sub> (CA) Setting: MR12: OP[6:0]	Application	Note		
1	From	00	0001100	tFC_Short	1		
	To	01	0001101				
2	From	00	0001000	tFC_Long	2		
	To	01	0101000				
NOTE 1 A single step size increment/decrement for V <sub>REF</sub> (CA) Setting Value.							
NOTE 2 Equal to or more than 2 step size increment/decrement for V <sub>REF</sub> (CA) Setting Value.							

### 7.8.3.1 Frequency Set Point Update Timing (cont'd)

The LPDDR6-SDRAM defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR6 SDRAM to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point, Figure 152. See Command Bus Training section for more details on this training mode.

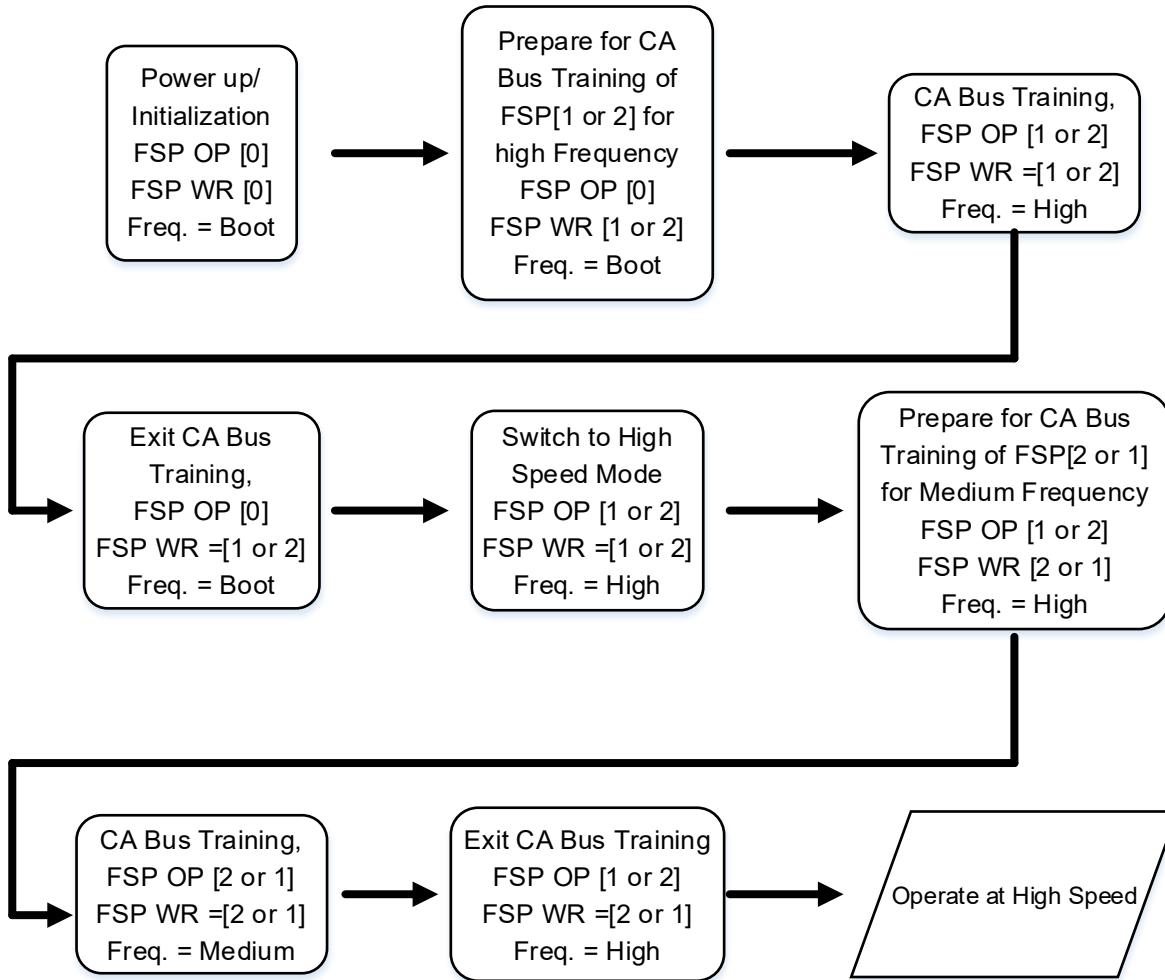
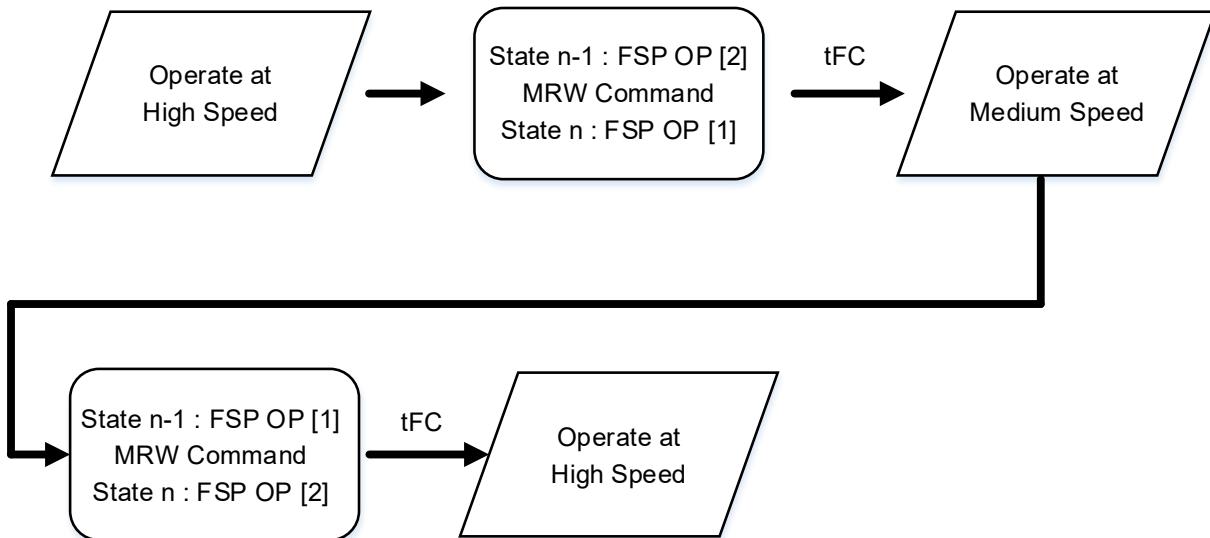


Figure 152 – Training 3 Frequency Set-Points

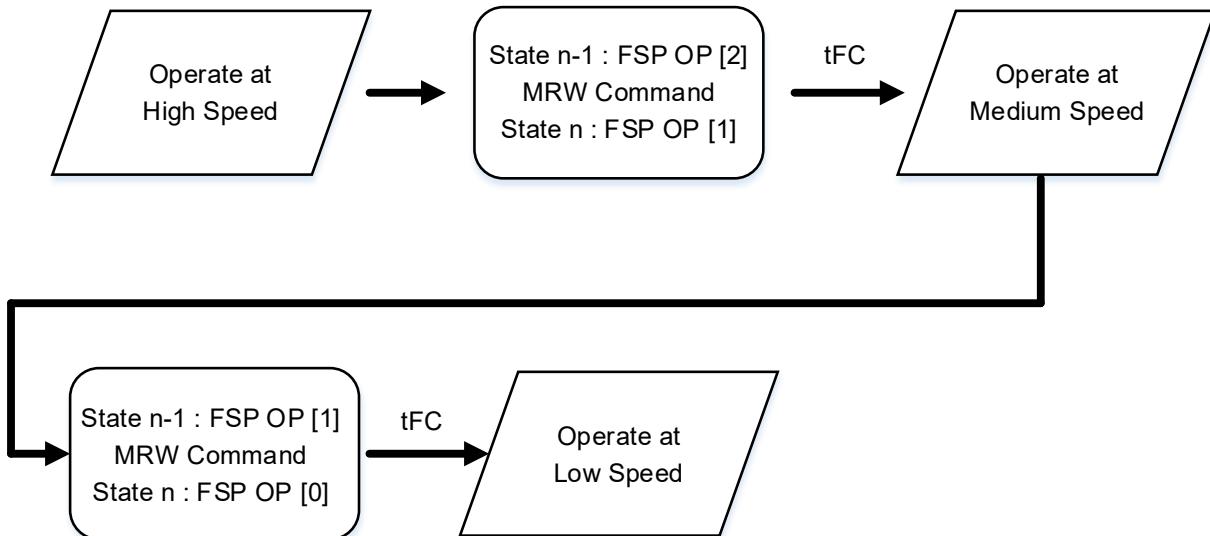
### 7.8.3.1 Frequency Set Point Update Timing (cont'd)

Once all Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 153).



**Figure 153 – Switching Between Two Trained Frequency Set-Points (Example)**

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously trained values (in particular the VREF(CA) calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 154).



**Figure 154 – Switching to a Third Trained Frequency Set-Point (Example)**

## 7.8.4 On-Die Termination (ODT)

### 7.8.4.1 On-Die Termination for Command/Address Bus

Command/Address ODT (On-Die Termination) is a feature of the LPDDR6 SDRAM that allows the SDRAM to turn on/off termination resistance for CK\_t, CK\_c, and CA[3:0] signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the Command/Address ODT feature is shown in Figure 155.

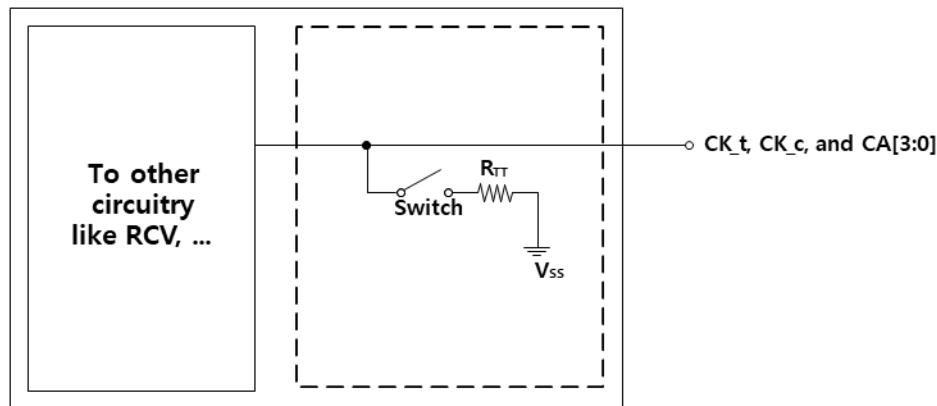


Figure 155 – Functional Representation of Command/Address Bus ODT

#### 7.8.4.1.1 ODT Mode Register and ODT State Table for Command/Address Bus

Command/Address ODT termination values are set and enabled via MR18. The CA bus (CA[3:0]) and the Clock (CK\_t, CK\_c) ODT resistance values are set by MR18 OP[5:3] and MR18 OP[2:0], respectively. The default state for the CA bus and the Clock is ODT disabled.

CA and CK ODT of the device are designed to enable one rank (termination for one rank and un-termination for other ranks) or multi ranks (balanced termination for all ranks) to terminate the entire command bus in the multi-rank system. For this reason, the rank providing CA, CK ODT via MR18 setting will continue to terminate CA, CK bus in all DRAM states including Power-Down Mode.

In the multi-rank/channel system, the device usually shares the CA/CK bus, and the un-terminated die needs to know the ODT status of other shared dies when the termination status of CA/CK bus is different from each other. LPDDR6 SDRAM uses MR25 setting to decide the buffer type for power optimization. MR25 OP[4] is set to notify CK ODT status of other shared dies, MR25 OP[5] is set to notify CA ODT status of other shared dies.

Example: when CK and CA ODT status is different from each other (e.g., CK termination, CA un-termination) and MR25 OP[5] is disabled, the un-terminated CA input buffer use the fixed level reference voltage (TBD).

### 7.8.4.1.2 ODT Mode Register and ODT Characteristics for Command/Address Bus

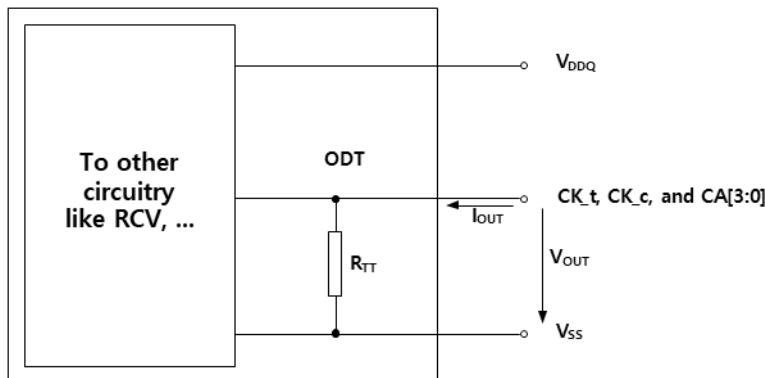


Figure 156 – On Die Termination for Command/Address Bus

Table 317 – ODT DC Electrical Characteristics, Assuming RZQ = 240 Ω ±1% over the Entire Operating Temperature Range after Proper ZQ Calibration

MR18 OP[5:3] MR18 OP[2:0]	RTT	Vout	Min	Nom	Max	Unit	Note
001	240Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ	1,2,3
010	120Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/2	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/2	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/2	1,2,3
011	80Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/3	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/3	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/3	1,2,3
100	60Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/4	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/4	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/4	1,2,3
101	48Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/5	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/5	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/5	1,2,3
110	40Ω	VOLdc = 0.2*VDDQ	0.8	1.0	1.1	RZQ/6	1,2,3
		VOMdc = 0.5*VDDQ	0.9	1.0	1.1	RZQ/6	1,2,3
		VOHdc = 0.75*VDDQ	0.9	1.0	1.3	RZQ/6	1,2,3
Mismatch CA-CA within CLK group		0.5*VDDQ	-		2	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see TBD.

NOTE 2 Pull-Down ODT resistors are recommended to be calibrated at 0.5\*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown, e.g., calibration at 0.2\* VDDQ and 0.75\*VDDQ.

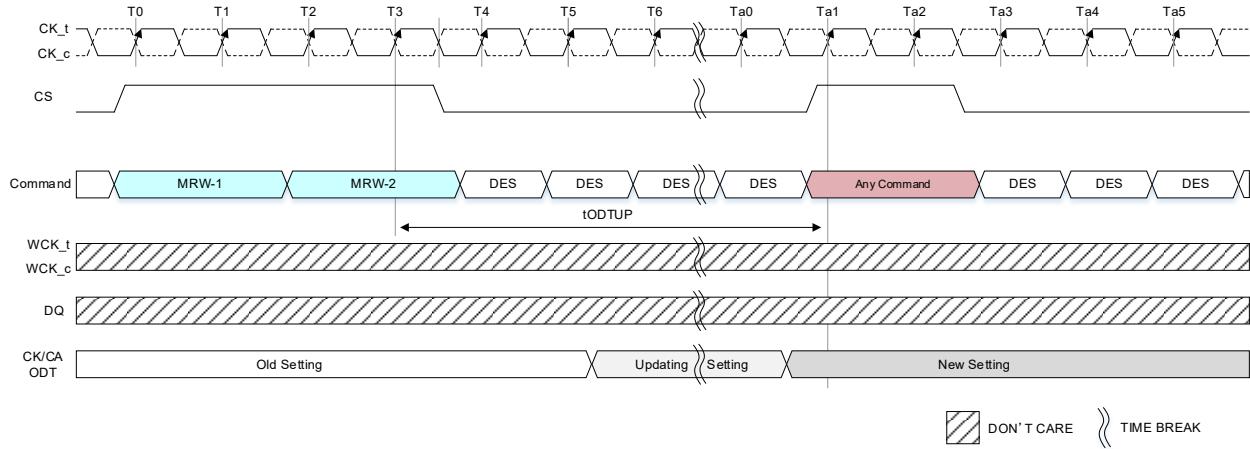
NOTE 3 Measurement definition for RTT : TBD.

NOTE 4 CA to CA mismatch within clock group (CA) variation for a given component including CK\_t and CK\_c (characterized).

$$\text{CA - CA(Mismatch)} = \frac{\text{RTT(max)} - \text{RTT(min)}}{\text{RTT(avg)}}$$

### 7.8.4.1.3 ODT Update Time for Clock and Command/Address

ODT update time for Clock and Command/Address Bus after Mode Register set are shown in Figure 157.

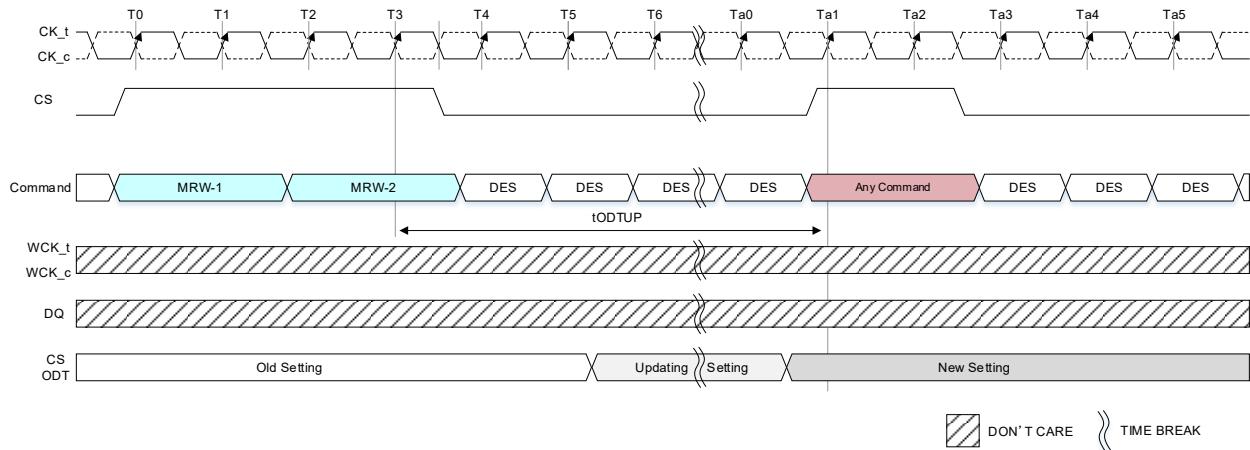


NOTE 1 CS input shall be required to be low during tODTUP period.

**Figure 157 – ODT for Clock and Command/Address Setting Update Timing**

### 7.8.4.1.4 ODT Update Time for CS

ODT update time for CS after Mode Register set are shown in Figure 158.



NOTE 1 CS input shall be required to be low during tODTUP period.

**Figure 158 – ODT for CS Setting Update Timing**

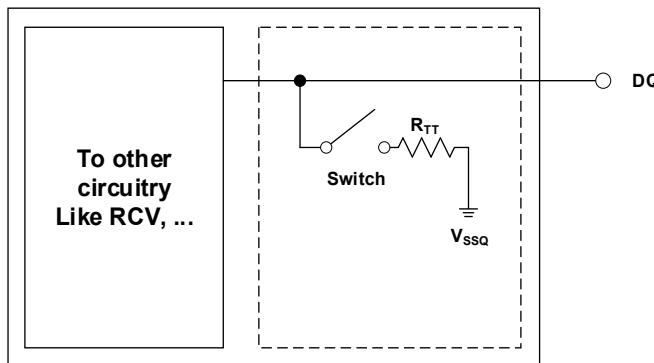
**Table 318 – ODT Command/Address Bus AC Timing Parameter**

Speed		ALL Operation Frequency		Unit
Parameter	Symbol	MIN	MAX	
ODT C/A Value Update Time	tODTUP	-	250	ns

#### 7.8.4.2 On-Die Termination for Data Bus

Data Bus ODT (On-Die Termination) is a feature of the LPDDR6 SDRAM that allows the SDRAM to turn on/off termination resistance for each DQ signal when using the pin as an input. The ODT feature is designed to improve signal integrity of the memory channel by allowing the SDRAM controller to turn on and off termination resistance for any target SDRAM devices during Write operation.

The Data Bus ODT feature is off and cannot be supported in Power-Down and Self-Refresh states. A simple functional representation of the SDRAM ODT feature is shown in Figure 159.



**Figure 159 – Functional Representation of Data Bus ODT**

##### 7.8.4.2.1 ODT Mode Register for Data Bus

The Data Bus ODT mode is enabled if MR19 OP[2:0] are non-zero. In this case, the value of RTT is determined by their setting.

The ODT Mode is disabled if MR19 OP[2:0]=000<sub>B</sub>.

##### 7.8.4.2.2 Asynchronous ODT for Data Bus

Although ODT Mode is enabled via MR19 OP[2:0], DRAM ODT is basically Hi-Z. DRAM ODT state is automatically turned ON asynchronously based on the Write command that the SDRAM samples. After the write burst is complete, DRAM ODT state is automatically turned OFF asynchronously.

Following timing parameters apply when DRAM ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODTOff,min, tODTOff,max

ODTLon is a synchronous parameter, and it is the latency from the Write or Write FIFO command (2nd rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on.

Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Write FIFO command (2nd rising edge of the clock).

#### 7.8.4.2.2 Asynchronous ODT for Data Bus (cont'd)

ODT<sub>Off</sub> is a synchronous parameter, and it is the latency from the Write or Write FIFO command (2nd rising edge of the clock) to t<sub>ODT<sub>Off</sub></sub> reference. ODT<sub>Off</sub> latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODT<sub>Off</sub> latency. Minimum RTT turn-off time (t<sub>ODT<sub>Off</sub>,min</sub>) is the point in time when the device termination circuit starts to turn off the ODT resistance. Maximum ODT turn-off time (t<sub>ODT<sub>Off</sub>,max</sub>) is the point in time when the on-die termination has reached high impedance. t<sub>ODT<sub>Off</sub>,min</sub> and t<sub>ODT<sub>Off</sub>,max</sub> are measured once ODT<sub>Off</sub> latency is satisfied from the Write or Write FIFO command (2nd rising edge of the clock).

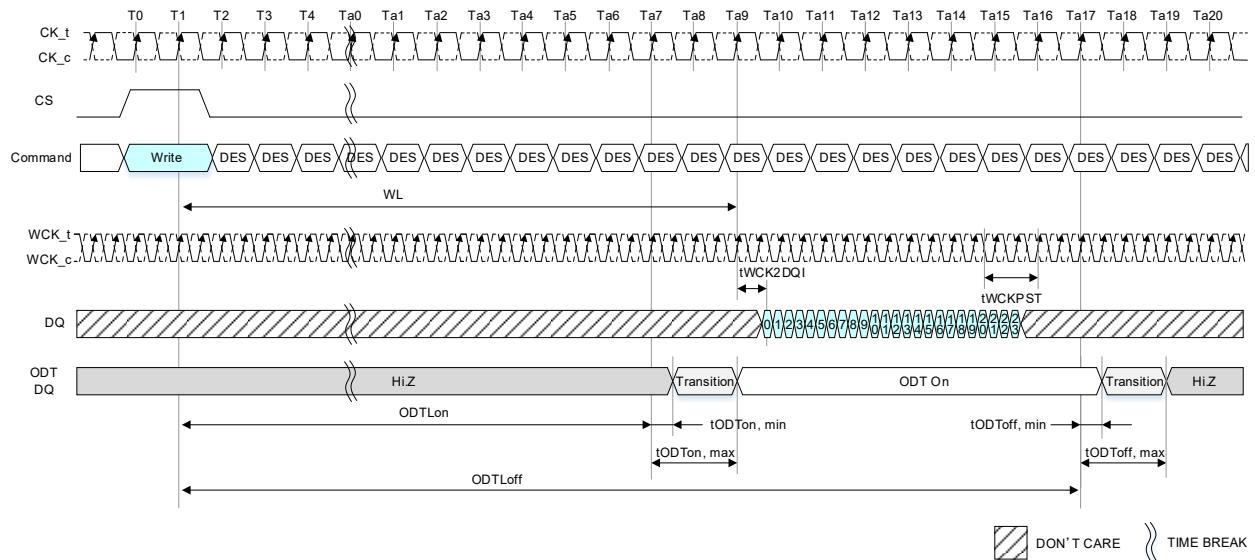
**Table 319 – ODT<sub>On</sub> and ODT<sub>Off</sub> Latency Values**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODT <sub>On</sub> [nCK]	ODT <sub>Off</sub> (WL + BL/n_min + RU(tWCK2DQI(max)/tCK)) [nCK]		
				ALL mode	BL24	BL48
1067	20	267	WL-1	TBD	TBD	TBD
1600	267	400	WL-2	TBD	TBD	TBD
2133	400	533	WL-2	TBD	TBD	TBD
2750	533	688	WL-3	TBD	TBD	TBD
3200	688	800	WL-3	TBD	TBD	TBD
3750	800	938	WL-4	TBD	TBD	TBD
4267	938	1067	WL-4	TBD	TBD	TBD
4800	1067	1200	WL-5	TBD	TBD	TBD
5500	1200	1375	WL-5	TBD	TBD	TBD
6400	1375	1600	WL-6	TBD	TBD	TBD
7500	1600	1875	WL-7	TBD	TBD	TBD
8533	1875	2133	WL-8	TBD	TBD	TBD
9600	2133	2400	WL-9	TBD	TBD	TBD
10667	2400	2667	WL-10	TBD	TBD	TBD
11733	2667	2933	WL-11	TBD	TBD	TBD
12800	2933	3200	WL-12	TBD	TBD	TBD
14400	3200	3600	WL-13	TBD	TBD	TBD

**Table 320 – Asynchronous ODT Turn-On and Turn-Off Timing**

Parameter	ALL Operation Frequency	Unit
t <sub>ODT<sub>On</sub>,min</sub>	1.5	ns
t <sub>ODT<sub>On</sub>,max</sub>	3.5	ns
t <sub>ODT<sub>Off</sub>,min</sub>	1.5	ns
t <sub>ODT<sub>Off</sub>,max</sub>	3.5	ns

### 7.8.4.2.2 Asynchronous ODT for Data Bus (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

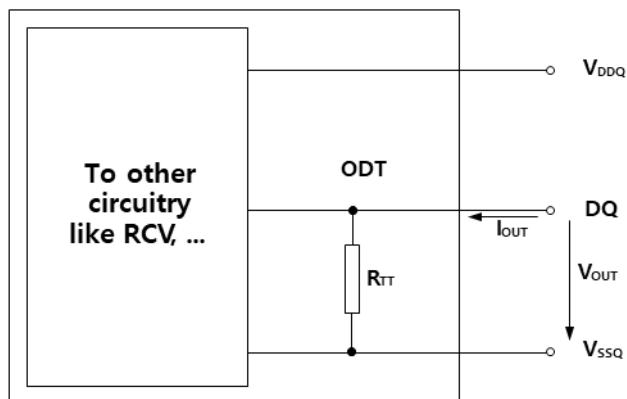
NOTE 2 ODTLon=WL-2, ODTLoff=WL+8

NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 160 – Asynchronous ODTon/ODToff Timing**

### 7.8.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus

On-Die Termination effective resistance RTT is defined by MR19 P[2:0]. ODT is applied to the DQ pins. A functional representation of the on-die termination is shown in Figure 161.



**Figure 161 – On Die Termination for Data Bus**

#### **7.8.4.2.3 ODT Mode Register and ODT Characteristics for Data Bus (cont'd)**

**Table 321 – ODT DC Electrical Characteristics, Assuming RZQ = 240 Ω ± 1% over the Entire Operating Temperature Range after Proper ZQ Calibration**

### 7.8.4.3 On-Die Termination for WCK\_t and WCK\_c

WCK ODT (On-Die Termination) is a feature of the LPDDR6 SDRAM that allows the SDRAM to turn on/off termination resistance for WCK\_t and WCK\_c signals without the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for DRAM devices via Mode Register setting. A simple functional representation of the DRAM ODT feature is shown in Figure 162.

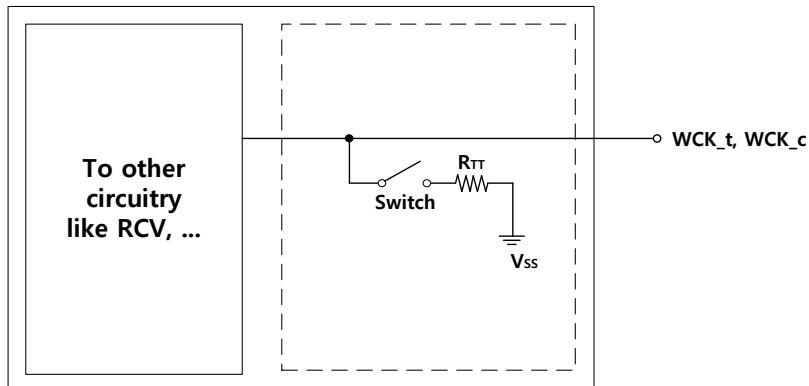


Figure 162 – Functional Representation of WCK ODT

#### 7.8.4.3.1 ODT Mode Register for WCK\_t/c

The WCK ODT termination values are set and enabled via MR19 OP[5:3]. The default state for the WCK is ODT disabled. The WCK ODT of the device always maintains the present ODT status.

#### 7.8.4.3.2 ODT during WCK2CK Training

If the WCK ODT is enabled by MR19 OP[5:3] in WCK2CK training mode, DRAM always provides the termination on WCK\_t/WCK\_c signals with the pre-defined ODT value via MR19 OP[5:3]. DQ termination is always off in WCK2CK training mode.

#### 7.8.4.4 ODT Mode Register and ODT Characteristics for CS

CS ODT (On-Die Termination) is a feature of the LPDDR6 SDRAM that allows the DRAM to turn on/off termination resistance for CS signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on with specific RZQ value and off termination resistance for any target DRAM devices via Mode Register setting. A simple functional representation of the CS ODT feature is shown in Figure 163.

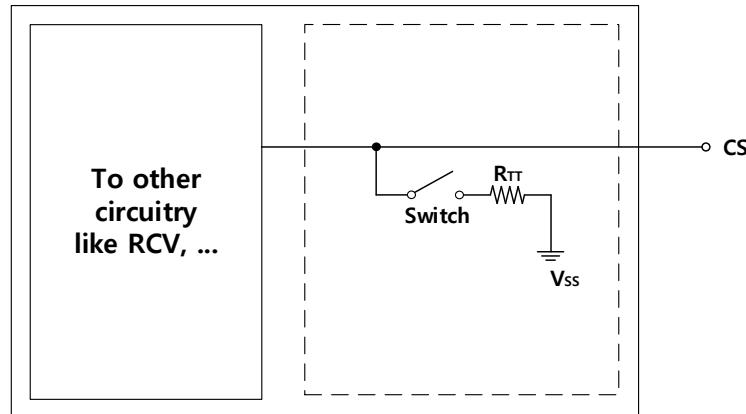
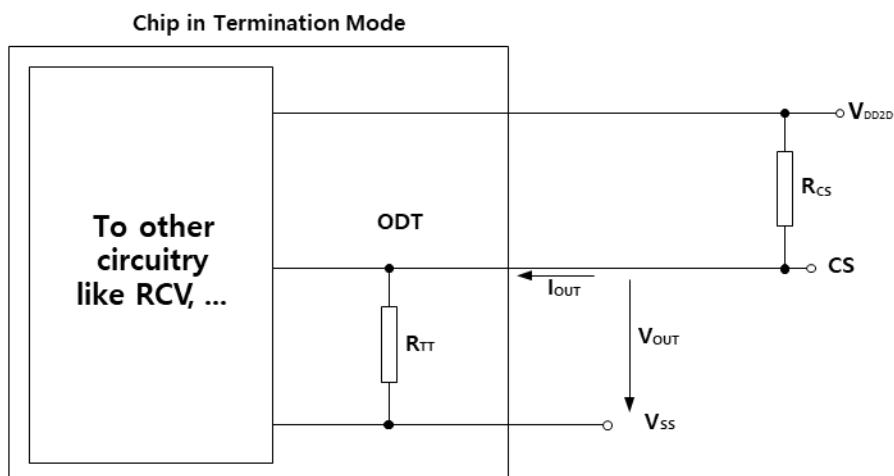


Figure 163 – Functional Representation of CS

#### 7.8.4.4.1 ODT Mode Register and ODT Characteristics for CS

On-Die Termination effective resistance RTT of the CS pin is enabled and determined by MR17 OP[5:3]. The Vout level is driven from the VDD2D with VDDQ-based ZQ codes. The CS ODT is not allowed in VDDQ power rail. A functional representation of the on-die termination is shown in Figure 164.



**Figure 164 – On Die Termination for CS**

**Table 322 – CS ODT DC Electrical Characteristics, Assuming RZQ = 240 Ω ± 1% over the Entire Operating Temperature Range after a Proper ZQ Calibration**

MR17 OP[5:3]	RTT	Rcs	Min	Nom	Max	Unit	Note
001	240Ω	40 ohm	1.0	-	2.3	RZQ	1,2,3
		60 ohm	1.0	-	2.1	RZQ	1,2,3
010	120Ω	40 ohm	1.0	-	2.2	RZQ/2	1,2,3
		60 ohm	1.0	-	2.0	RZQ/2	1,2,3
011	80Ω	40 ohm	1.0	-	2.1	RZQ/3	1,2,3
		60 ohm	1.0	-	1.9	RZQ/3	1,2,3
100	60Ω	40 ohm	1.0	-	2.0	RZQ/4	1,2,3
		60 ohm	1.0	-	1.8	RZQ/4	1,2,3
101	48Ω	40 ohm	1.0	-	1.9	RZQ/5	1,2,3
		60 ohm	1.0	-	1.7	RZQ/5	1,2,3
110	40Ω	40 ohm	1.0	-	1.8	RZQ/6	1,2,3
		60 ohm	1.0	-	1.6	RZQ/6	1,2,3

### 7.8.5 Non-target DRAM ODT

LPDDR6 SDRAM supports the Non-target DRAM ODT function for DQ and RDQS pins to improve signal integrity in 2-rank configurations. A simple DRAM ODT configuration at Read and Write operation is shown in Figure 165. The Non-target DRAM ODT function is enabled when its ODT value in MR20 OP[2:0] is set to any configuration other than 000<sub>B</sub> (disabled). The Non-target DRAM ODT is activated in all states. Non-target ODT-enabled pins should be driven Low in the standby mode to avoid unnecessary leakage current.

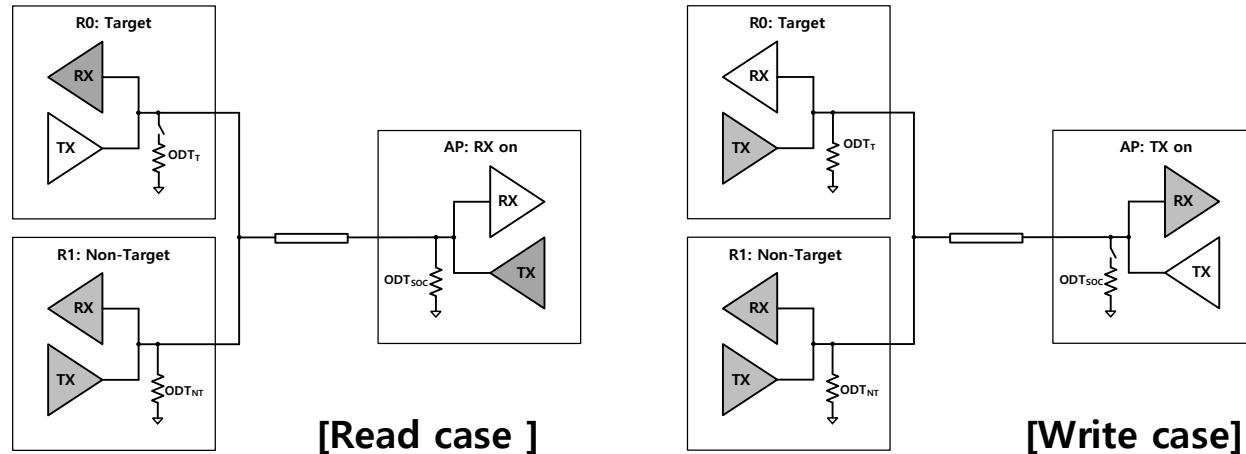


Figure 165 – DRAM ODT Configuration of Non-target DRAM ODT Mode

Table 323 – Non-target and Target ODT Status for Different DRAM States

Current DRAM State	Non-Target DRAM	Target DRAM	Note
Power Down	Enable (MR20 OP[2:0])	Enable (MR20 OP[2:0])	
Self-Refresh Power Down	Enable (MR20 OP[2:0])	Enable (MR20 OP[2:0])	
Pre-charge/ Active Standby	Enable (MR20 OP[2:0])	Enable (MR20 OP[2:0])	
Write/ Write FIFO	Enable (MR20 OP[2:0]) <sup>1</sup>	Enable (MR19 OP[2:0])	1
Read/ Read FIFO/ Read DQ Calibration/ MRR	Enable (MR20 OP[2:0])	PDDS/PUDS	
Meta-Write	Enable (MR20 OP[2:0])	Enable (MR20 OP[2:0])	2
Meta-Read	Enable (MR20 OP[2:0])	Enable (MR20 OP[2:0])	
NOTE 1	When Dynamic Write NT-ODT is enabled (MR20 OP[5:3]≠000 <sub>B</sub> ) and Write NT-ODT command is issued to the non-target rank, the non-target rank ODT value is superseded by the ODT value configured in DQ WR NT-ODT (MR20 OP[5:3]) during Write operation.		
NOTE 2	Meta-Write command does not support Dynamic Write NT-ODT function. During Meta-Write operation, the non-target rank maintains the NT-ODT values of DQ NT-ODT (MR20 OP[2:0]) regardless of DQ WR NT-ODT setting (MR20 OP[5:3]).		

### 7.8.5.1 Non-target DRAM ODT Control

In Non-Target ODT (NT-ODT) mode, Target DRAM ODT and Non-Target DRAM ODT can be set by MR19 OP[2:0] and MR20 OP[2:0], respectively, and the possible combination is shown in Table 326 and Table 327.

When using the NT-ODT function, the following must be taken into consideration: 1) in Write operation, vDIVW and VDIHL\_AC specification of DQ must be satisfied, and 2) in Read operation, since the SDRAM calibrates Pull-up strength to satisfy VOH specification according to SoC ODT of MR17 OP[2:0], the SoC ODT MR should be configured such that it follows the equivalent resistance of NT-ODT (MR20 OP[2:0]) and ODT of SoC Rx. NT-ODT should be disabled in case that VRO is enabled by MR13 OP[2]. Refer to Table 324 for more information.

Once the NT-ODT feature is enabled, termination by NT-ODT for DQ and RDQS pins are sustained until disabling NT-ODT or resetting the SDRAM, except for the following cases.

- DQ
  - duration for which input receiver is turned on (Write operation for example)
  - duration for which output driver is turned on (Read operation for example)
- RDQS\_t
  - RDQS\_t disabled via MR setting
  - duration for which output driver is turned on
- RDQS\_c
  - RDQS\_c disabled via MR setting
  - duration for which output driver is turned on

Additionally, it is required that the following Mode Registers are configured with the same setting for the SDRAMs connected to the same data bus when enabling NT-ODT:

- Write Link ECC (MR23 OP[0]) or Write Link EDC (MR23 OP[1])
- Read Link ECC/EDC (MR23 OP[2])
- EDBI-WR (MR3 OP[1])
- DBI-RD (MR3 OP[0])
- RDQS (MR22 OP[1:0])

### 7.8.5.1 Non-target DRAM ODT Control (cont'd)

**Table 324 – Normal Mode vs. NT-ODT Mode for Write Operation**

Mode	Target Rank ODT	Non-Target Rank ODT	Equivalent ODT of 2-Rank DRAM
Normal Mode	MR19 OP[2:0] (ODT <sub>T</sub> )	Disabled (MR20 OP[2:0]=000 <sub>B</sub> and MR20 OP[5:3]=000 <sub>B</sub> )	ODT <sub>T</sub>
NT-ODT Mode	MR19 OP[2:0] (ODT <sub>T</sub> )	MR20 OP[2:0] or MR20 OP[5:3] (ODT <sub>NT</sub> )	ODT <sub>T</sub>    ODT <sub>NT</sub>
NT-ODT Mode	Disabled (MR19 OP[2:0]=000 <sub>B</sub> )	MR20 OP[2:0] or MR20 OP[5:3] (ODT <sub>NT</sub> )	ODT <sub>NT</sub>
NOTE 1 When Dynamic Write NT-ODT is enabled (MR20 OP[5:3]≠000 <sub>B</sub> ) and Write NT-ODT command is issued to the non-target rank, the non-target rank ODT value (ODT <sub>NT</sub> ) is superseded by the ODT value configured in DQ WR NT-ODT (MR20 OP[5:3]) during Write operation.			

**Table 325 – Normal Mode vs. NT-ODT Mode for Read Operation**

Mode	Non-Target Rank ODT	SoC Rx ODT	Equivalent ODT for RD operation	MR17 OP[2:0] (SoC ODT for DRAM Pull-Up Cal.)
Normal Mode	Disable (MR20 OP[2:0]=000 <sub>B</sub> )	ODT <sub>SOC</sub>	ODT <sub>SOC</sub>	ODT <sub>SOC</sub>
NT-ODT Mode	MR20 OP[2:0] (ODT <sub>NT</sub> )	ODT <sub>SOC</sub>	ODT <sub>NT</sub>    ODT <sub>SOC</sub>	ODT <sub>NT</sub>    ODT <sub>SOC</sub> <sup>1</sup>
NOTE 1 Since SoC ODT of MR17 can only support RZQ/n (n=1,2,3,4,5,6), (ODT <sub>NT</sub>   ODT <sub>SOC</sub> ) should be either RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.				

### 7.8.5.1 Non-target DRAM ODT Control (cont'd)

Table 326 shows all combinations that equivalent ODT is RZQ/1, RZQ/2, RZQ/3, RZQ/4, RZQ/5, or RZQ/6.

**Table 326 – Combination of Target ODT, Non-target ODT, and SoC ODT  
(NT-ODT Enabled Case: MR20 OP[2:0]≠000<sub>B</sub>)**

ODT <sub>NT</sub> (MR20 OP[2:0])	ODT <sub>T</sub>	ODT <sub>SoC</sub>	Write <sup>1</sup> (ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> )	Read (SoC ODT MR17 OP[2:0])
RZQ/1	RZQ/1	Disabled	RZQ/2	RZQ/1
	RZQ/2	RZQ/1	RZQ/3	RZQ/2
	RZQ/3	RZQ/2	RZQ/4	RZQ/3
	RZQ/4	RZQ/3	RZQ/5	RZQ/4
	RZQ/5	RZQ/4	RZQ/6	RZQ/5
	Disabled	RZQ/5	RZQ/1	RZQ/6
RZQ/2	RZQ/1	Disabled	RZQ/3	RZQ/2
	RZQ/2	RZQ/1	RZQ/4	RZQ/3
	RZQ/3	RZQ/2	RZQ/5	RZQ/4
	RZQ/4	RZQ/3	RZQ/6	RZQ/5
	Disabled	RZQ/4	RZQ/2	RZQ/6
RZQ/3	RZQ/1	Disabled	RZQ/4	RZQ/3
	RZQ/2	RZQ/1	RZQ/5	RZQ/4
	RZQ/3	RZQ/2	RZQ/6	RZQ/5
	Disabled	RZQ/3	RZQ/3	RZQ/6
RZQ/4	RZQ/1	Disabled	RZQ/5	RZQ/4
	RZQ/2	RZQ/1	RZQ/6	RZQ/5
	Disabled	RZQ/2	RZQ/4	RZQ/6
RZQ/5	RZQ/1	Disabled	RZQ/6	RZQ/5
	Disabled	RZQ/1	RZQ/5	RZQ/6
RZQ/6	Disabled	Disabled	RZQ/6	RZQ/6
NOTE 1 When Dynamic Write NT-ODT is enabled (MR20 OP[5:3]≠000 <sub>B</sub> ) and Write NT-ODT command is issued to the non-target rank, the non-target rank ODT value (ODT <sub>NT</sub> ) during Write operation is superseded by the ODT value configured in DQ WR NT-ODT (MR20 OP[5:3]).				

### 7.8.5.1 Non-target DRAM ODT Control (cont'd)

**Table 327 – Combination of Target ODT, Non-target ODT, and SoC ODT  
(NT-ODT Disabled and Dynamic Write NT-ODT Disable Case: MR20 OP[2:0]=000<sub>B</sub> and  
MR20 OP[5:3]=000<sub>B</sub>)**

ODT <sub>NT</sub>	ODT <sub>T</sub>	ODT <sub>SOC</sub>	Write (ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> )	Read (SoC ODT MR17 OP[2:0])
Disabled	RZQ/1	RZQ/1	RZQ/1	RZQ/1
		RZQ/2		RZQ/2
		RZQ/3		RZQ/3
	RZQ/2	RZQ/4	RZQ/2	RZQ/4
		RZQ/5		RZQ/5
		RZQ/6		RZQ/6
	RZQ/3	RZQ/1	RZQ/3	RZQ/1
		RZQ/2		RZQ/2
		RZQ/3		RZQ/3
		RZQ/4		RZQ/4
		RZQ/5		RZQ/5
		RZQ/6		RZQ/6
	RZQ/4	RZQ/1	RZQ/4	RZQ/1
		RZQ/2		RZQ/2
		RZQ/3		RZQ/3
		RZQ/4		RZQ/4
		RZQ/5		RZQ/5
		RZQ/6		RZQ/6
	RZQ/5	RZQ/1	RZQ/5	RZQ/1
		RZQ/2		RZQ/2
		RZQ/3		RZQ/3
		RZQ/4		RZQ/4
		RZQ/5		RZQ/5
		RZQ/6		RZQ/6
	RZQ/6	RZQ/1	RZQ/6	RZQ/1
		RZQ/2		RZQ/2
		RZQ/3		RZQ/3
		RZQ/4		RZQ/4
		RZQ/5		RZQ/5
		RZQ/6		RZQ/6

### 7.8.5.1 Non-target DRAM ODT Control (cont'd)

**Table 328 – Combination of Target ODT, Non-target ODT, and SoC ODT  
(NT-ODT Disabled and Dynamic Write NT-ODT Enabled Case: MR20 OP[2:0]=000<sub>B</sub> and  
MR20 OP[5:3]≠000<sub>B</sub>)**

ODT <sub>NT</sub> (MR20 OP[5:3])	ODT <sub>T</sub>	ODT <sub>SOC</sub>	Write (ODT <sub>eq</sub> =ODT <sub>NT</sub> // ODT <sub>T</sub> )	Read (SoC ODT MR17 OP[2:0])
RZQ/1	RZQ/1	Disabled	RZQ/2	Disabled
	RZQ/2	RZQ/1	RZQ/3	RZQ/1
	RZQ/3	RZQ/2	RZQ/4	RZQ/2
	RZQ/4	RZQ/3	RZQ/5	RZQ/3
	RZQ/5	RZQ/4	RZQ/6	RZQ/4
	Disabled	RZQ/5	RZQ/1	RZQ/5
RZQ/2	RZQ/1	Disabled	RZQ/3	Disabled
	RZQ/2	RZQ/1	RZQ/4	RZQ/1
	RZQ/3	RZQ/2	RZQ/5	RZQ/2
	RZQ/4	RZQ/3	RZQ/6	RZQ/3
	Disabled	RZQ/4	RZQ/2	RZQ/4
RZQ/3	RZQ/1	Disabled	RZQ/4	Disabled
	RZQ/2	RZQ/1	RZQ/5	RZQ/1
	RZQ/3	RZQ/2	RZQ/6	RZQ/2
	Disabled	RZQ/3	RZQ/3	RZQ/3
RZQ/4	RZQ/1	Disabled	RZQ/5	Disabled
	RZQ/2	RZQ/1	RZQ/6	RZQ/1
	Disabled	RZQ/2	RZQ/4	RZQ/2
RZQ/5	RZQ/1	Disabled	RZQ/6	Disabled
	Disabled	RZQ/1	RZQ/5	RZQ/1
RZQ/6	Disabled	Disabled	RZQ/6	Disabled

### 7.8.5.2 Dynamic Write NT-ODT Control

In certain applications, it is more desirable to configure different NT-ODT settings for Write and Read operation to improve SI. LPDDR6 provides a method that allows for individual NT-ODT values for Write and Read operation.

The dynamic control of NT-ODT during Write operation is enabled with a unique CS assertion pattern to the non-target rank when Write and Write FIFO commands are issued to the target-rank. More specifically, when a Write or Write FIFO command is issued, CS for the non-target rank should be asserted "H" at R1 of the command clock and de-asserted "L" for R2 to control NT-ODT settings (a normal Write command to the target rank is defined such that CS is asserted "H" for both R1 and R2 of the command clock). Refer to clause 7.1. Command Truth Table for more information.

When this feature is enabled via DQ WR NT-ODT (MR20 OP[5:3]) and initiated with the CS assertion pattern, the NT-ODT values follow the mode register setting in MR20 OP[5:3] during Write operation. In any other states than when Write-related operation is in progress, the non-target DRAM maintains the NT-ODT values based on DQ NT-ODT MR20 OP[2:0].

When it is disabled (MR20 OP[5:3]=000<sub>B</sub>), CS for the non-target rank must be kept "L" when Write or Write FIFO command is issued.

Dynamic Write NT-ODT feature, when enabled, maintains its operation during the power-down state. Since the aforementioned CS assertion pattern is used to control the NT-ODT settings, the normal CS toggle pattern cannot be used to bring the non-target device from the power-down state. Hence, Power Down Exit (PDX-NT) command is defined for power-down exit initiation of the non-target device. It is initiated with CS "H" at R1 and R2 of the command clock with CA[0] "V" at R1, F1, R2, and F2. This command is only valid when Dynamic Write NT-ODT feature is enabled.

Since the non-target DRAM must now monitor additional command pins, increased power-down current will be observed when this feature is enabled. In order to reduce the number of pins awake during the power-down state, the SDRAM may turn off all command address pins except for CA[0], which is necessary to determine the duration for which Write NT-ODT is active (BL24 or BL48). Hence, it is prohibited to issue the CS pattern of "H" at R1 and "L" at R2 of the command clock to a power-downed device with Dynamic Write NT-ODT enabled, as it may trigger an unintended Write NT-ODT operation.

### 7.8.5.3 Asynchronous NT-ODT

The NT-ODT is enabled by MR20 OP[2:0], and the target ODT of the SDRAM is controlled by Write-related commands such as Write and Write FIFO commands or Read-related commands such as Read, Mode Register Read, Read DQ Calibration, and Read FIFO commands. The ODT of each device is turned on with the NT-ODT value stored in DQ NT-ODT MR20 OP[2:0]. When Write or Read command is issued to the target device, the ODT of the target DRAM is controlled according to timing parameters such as ODTLon\_(RD\_DQ/RDQS), tODT\_(RD)on, ODTLoff\_(RD\_DQ/RDQS), and tODT\_(RD)off.

Following timing parameters apply when DRAM NT-ODT mode is enabled.

- ODTLon, tODTon,min, tODTon,max
- ODTLoff, tODTOff,min, tODTOff,max
- ODTLon\_RD, tODT\_RDon,min, tODT\_RDon,max
- ODTLoff\_RD, tODT\_RDoff,min, tODT\_RDoff,max

In case that Dynamic NT-ODT is enabled, when Write or Write FIFO command is issued to the target device, the ODT of the non-target device is dynamically turned on with the NT-ODT value stored in MR20 OP[5:3] (DQ WR NT-ODT) regardless of the NT-ODT setting of MR20 OP[2:0] (DQ NT-ODT). It is controlled according to the same set of timing parameters that affect the ODT of the target device upon Write command, such as ODTLon, tODTon, ODTLoff, and tODTOff.

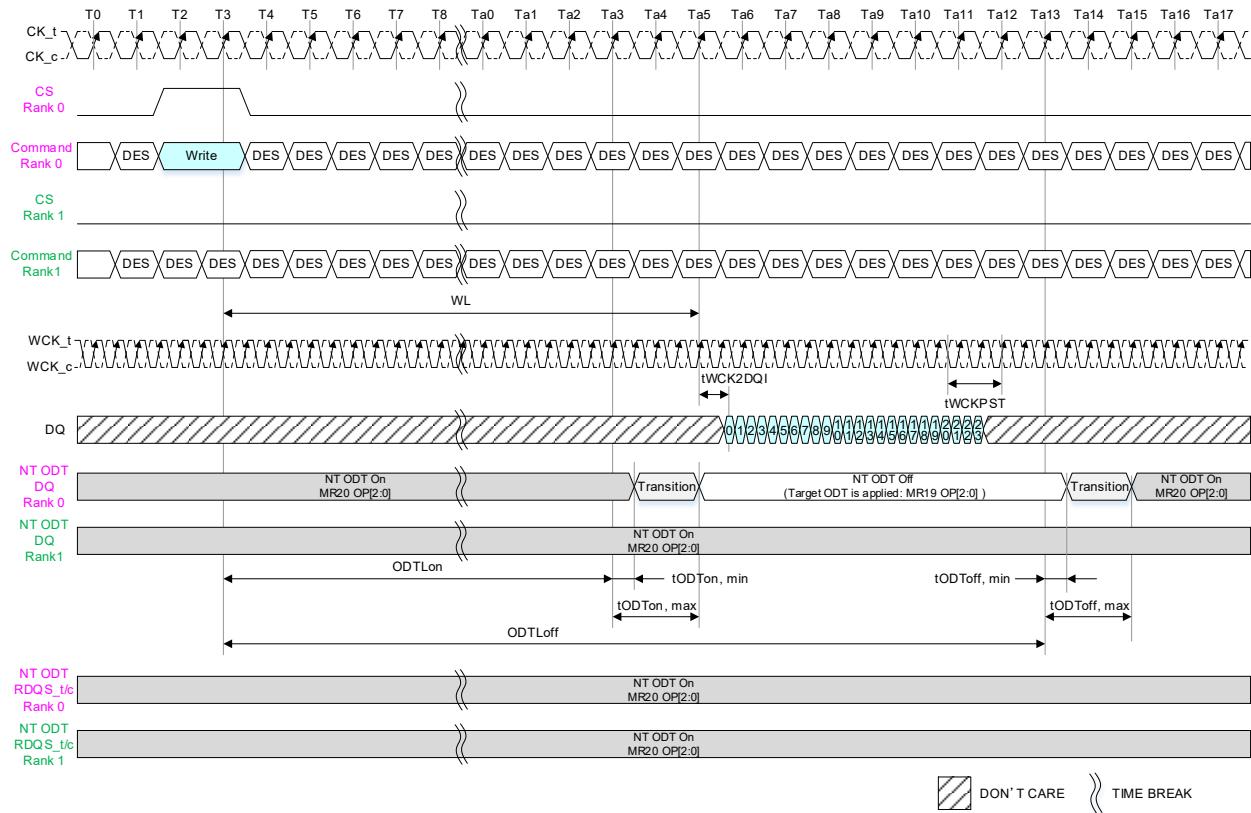
#### 7.8.5.3.1 NT-ODT Behavior for Write Operation

ODTLon is a synchronous parameter, and it is the latency from the Write or Write FIFO command (2nd rising edge of the clock) to tODTon reference. ODTLon latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTLon latency. Minimum RTT turn-on time (tODTon,min) is the point in time when the device termination circuit leaves high impedance state, and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (tODTon,max) is the point in time when the ODT resistance is fully on. tODTon,min and tODTon,max are measured once ODTLon latency is satisfied from the Write or Write FIFO command.

ODTlOff is a synchronous parameter, and it is the latency from the Write or Write FIFO command (2nd rising edge of the clock) to tODTOff reference. ODTlOff latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODTlOff latency. Minimum RTT turn-off time (tODTOff,min) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (tODTOff,max) is the point in time when the on-die termination has reached high impedance. tODTOff,min and tODTOff,max are measured once ODTlOff latency is satisfied from the Write or Write FIFO command (2nd rising edge of the clock).

In Non-target DRAM ODT enabled mode, ODT timings (ODTLon and ODTlOff) are referenced to the Write command, and the ODT value in the target rank is updated within tODTon,max as shown in Figure 166. After the Write operation, the target ODT value returns to the pre-defined non-target DRAM ODT value within tODTOff,max.

### 7.8.5.3.1 NT-ODT Behavior for Write Operation (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

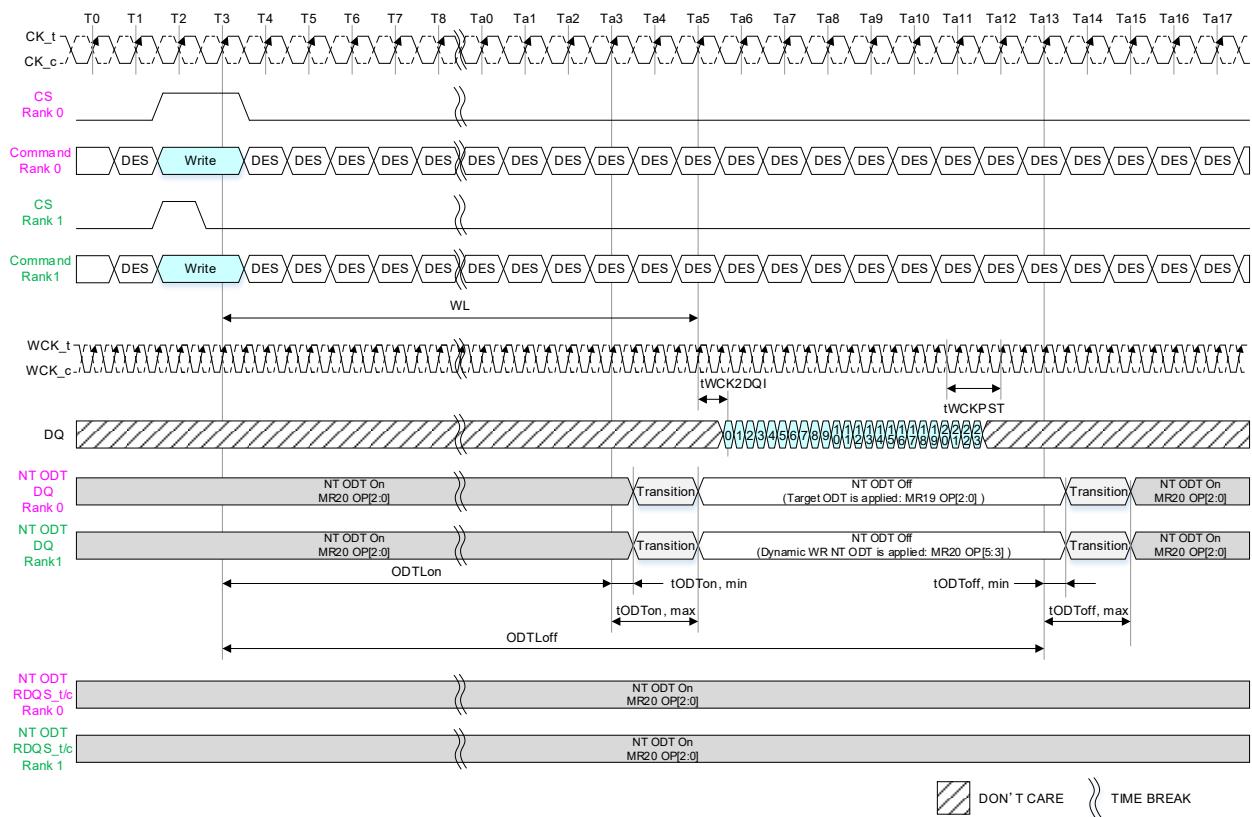
NOTE 2 ODTLon=WL-2, ODTLoff=WL+8

NOTE 3 Write Link ECC or Write Link EDC is not enabled.

**Figure 166 – ODT, NT-ODT Timing for Write Operation:  
Dynamic Write NT-ODT Disabled (MR20 OP[5:3]=000<sub>B</sub>)**

#### **7.8.5.3.1 NT-ODT Behavior for Write Operation (cont'd)**

In case that Dynamic Write NT-ODT mode is enabled and Write NT-ODT command is issued to the non-target rank, ODT timings (ODTLon and ODTLoff) are referenced to the Write command, and the ODT value in the non-target rank is updated within tODTTon,max as shown in Figure 167. After the Write operation, the non-target ODT value returns to the pre-defined non-target DRAM ODT value within tODTOff,max if NT-ODT is enabled (MR20 OP[2:0]≠000<sub>B</sub>). Otherwise, if NT-ODT is disabled (MR20 OP[2:0]=000<sub>B</sub>), the non-target ODT is turned off and reaches high impedance state within tODTOff,max.



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 ODTL<sub>on</sub>=WL-2, ODTL<sub>off</sub>=WL+8

**NOTE 3** Write Link ECC or Write Link EDC is not enabled.

NOTE 4 NT-ODT is enabled ( $MR20\ OP[2:0]\neq 000_B$ ).

**Figure 167 – ODT, NT-ODT Timing for Write Operation:  
Dynamic Write NT-ODT Enabled ( $MR20\ OP[5:3]\neq000_B$ )**

### 7.8.5.3.1 NT-ODT Behavior for Write Operation (cont'd)

**Table 329 – ODTLon and ODTLoff Latency Values for Write**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLon [nCK]	ODTLoff (WL + BL/n_min + RU(tWCK2DQI(max)/tCK)) [nCK]	
			ALL mode	BL24	BL48
1067	20	267	WL-1	WL+7	WL+13
1600	267	400	WL-2	WL+7	WL+13
2133	400	533	WL-2	WL+7	WL+13
2750	533	688	WL-3	WL+7	WL+13
3200	688	800	WL-3	WL+7	WL+13
3750	800	938	WL-4	WL+7	WL+13
4267	938	1067	WL-4	WL+7	WL+13
4800	1067	1200	WL-5	WL+8	WL+14
5500	1200	1375	WL-5	WL+7	WL+13
6400	1375	1600	WL-6	WL+7	WL+13
7500	1600	1875	WL-7	WL+8	WL+20
8533	1875	2133	WL-8	WL+8	WL+20
9600	2133	2400	WL-9	WL+8	WL+20
10667	2400	2667	WL-10	WL+8	WL+20
11733	2667	2933	WL-11	TBD	TBD
12800	2933	3200	WL-12	TBD	TBD
14400	3200	3600	WL-13	TBD	TBD

**Table 330 – Asynchronous NT-ODT Turn-On and Turn-Off Timing for Write**

Parameter	ALL Operation Frequency	Unit
tODTon,min	1.5	ns
tODTon,max	3.5	ns
tODToff,min	1.5	ns
tODToff,max	3.5	ns

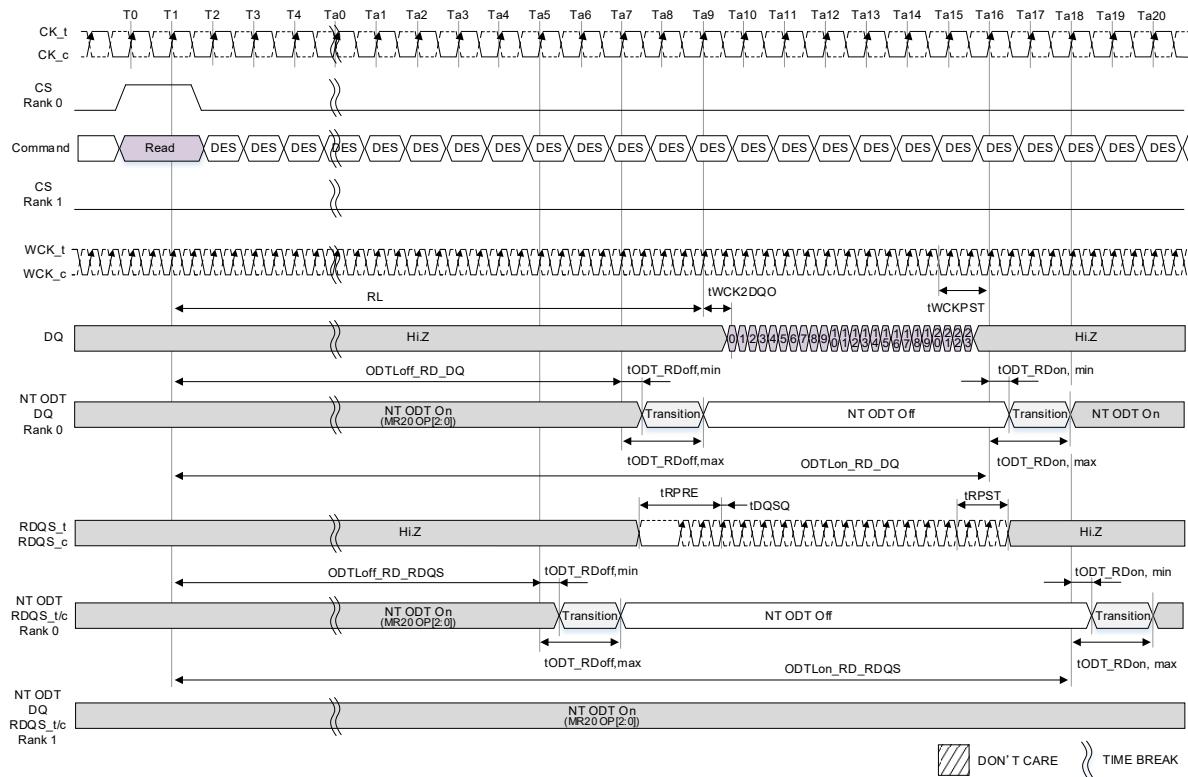
### 7.8.5.3.2 NT-ODT Behavior for Read Operation

ODT<sub>Off</sub>\_RD\_DQ/RDQS is a synchronous parameter, and it is the latency from the Read command (2nd rising edge of the clock) to t<sub>ODT</sub>\_RD<sub>Off</sub> reference. ODT<sub>Off</sub>\_RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODT<sub>Off</sub>\_RD\_DQ/RDQS latency. Minimum RTT turn-off time (t<sub>ODT</sub>\_RD<sub>Off,min</sub>) is the point in time when the device termination circuit starts to turn off the NT-ODT resistance. Maximum NT-ODT turn-off time (t<sub>ODT</sub>\_RD<sub>Off,max</sub>) is the point in time when the on-die termination has reached high impedance. t<sub>ODT</sub>\_RD<sub>Off,min</sub> and t<sub>ODT</sub>\_RD<sub>Off,max</sub> are measured once ODT<sub>Off</sub>\_RD\_DQ/RDQS latency is satisfied from the Read command.

ODT<sub>On</sub>\_RD\_DQ/RDQS is a synchronous parameter, and it is the latency from the Read command (2nd rising edge of the clock) to t<sub>ODT</sub>\_RD<sub>On</sub> reference. ODT<sub>On</sub>\_RD\_DQ/RDQS latency is a fixed latency value for each operation frequency range. Each operation frequency range has a different ODT<sub>On</sub>\_RD\_DQ/RDQS latency. Minimum RTT turn-on time (t<sub>ODT</sub>\_RD<sub>On,min</sub>) is the point in time when the device termination circuit leaves high impedance state, and NT-ODT resistance begins to turn on. Maximum RTT turn-on time (t<sub>ODT</sub>\_RD<sub>On,max</sub>) is the point in time when the ODT resistance is fully on. t<sub>ODT</sub>\_RD<sub>On,min</sub> and t<sub>ODT</sub>\_RD<sub>On,max</sub> are measured once ODT<sub>On</sub>\_RD\_DQ/RDQS latency is satisfied from the Read command.

In Non-target DRAM ODT enabled mode, ODT timings (ODT<sub>Off</sub>\_RD\_DQ/RDQS and ODT<sub>On</sub>\_RD\_DQ/RDQS) are referenced to the Read command, and the ODT value in the target rank is disabled within t<sub>ODT</sub>\_RD<sub>Off,max</sub> as shown in Figure 168. After the Read operation, the ODT state returns to the pre-defined Non-target DRAM ODT value within t<sub>ODT</sub>\_RD<sub>On,max</sub>.

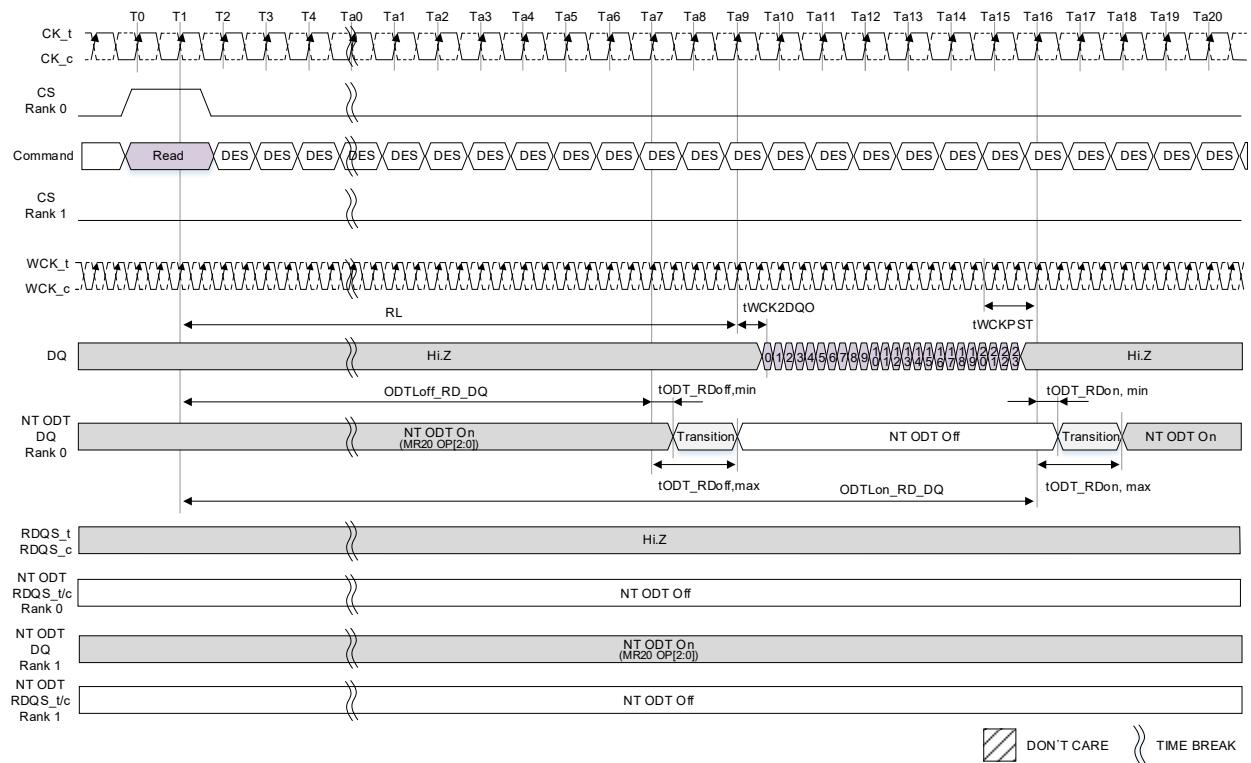
### **7.8.5.3.2 NT-ODT Behavior for Read Operation (cont'd)**



NOTE 1 tWCK2CK is 0 ps in this instance.

**Figure 168 – NT-ODT Timing for Read Operation**

### 7.8.5.3.2 NT-ODT Behavior for Read Operation (cont'd)



NOTE 1 tWCK2CK is 0 ps in this instance.

**Figure 169 – NT-ODT Timing for Read Operation: RDQS Disabled**

### 7.8.5.3.2 NT-ODT Behavior for Read Operation (cont'd)

**Table 331 — ODTLon\_RD\_DQ and ODTLoff\_RD\_DQ Latency Values for Read**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLoff_RD_DQ [nCK]	ODTLon_RD_DQ (RL + BL/n_min + RU(tWCK2DQO(max)/tCK)) [nCK]	
				ALL mode	BL24
1067	20	267	RL-1	RL+7	RL+13
1600	267	400	RL-2	RL+7	RL+13
2133	400	533	RL-2	RL+8	RL+14
2750	533	688	RL-3	RL+8	RL+14
3200	688	800	RL-3	RL+8	RL+14
3750	800	938	RL-4	RL+8	RL+14
4267	938	1067	RL-4	RL+9	RL+15
4800	1067	1200	RL-5	RL+9	RL+15
5500	1200	1375	RL-5	RL+9	RL+15
6400	1375	1600	RL-6	RL+9	RL+15
7500	1600	1875	RL-7	RL+10	RL+22
8533	1875	2133	RL-8	RL+10	RL+22
9600	2133	2400	RL-9	RL+10	RL+22
10667	2400	2667	RL-10	RL+11	RL+23
11733	2667	2933	RL-11	TBD	TBD
12800	2933	3200	RL-12	TBD	TBD
14400	3200	3600	RL-13	TBD	TBD

**Table 332 — ODTLon\_RD\_RDQS and ODTLoff\_RD\_RDQS Latency Values for Read with RDQS Enabled and RDQS PS (MR10 OP[0])=0<sub>B</sub> and RDQS PRE (MR10 OP[4:2])=000<sub>B</sub>, 001<sub>B</sub>**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTLoff_RD_RDQS [nCK]	ODTLon_RD_RDQS (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2) [nCK]	
				ALL mode	BL24
1067	20	267	RL-3	RL+9	RL+15
1600	267	400	RL-4	RL+9	RL+15
2133	400	533	RL-4	RL+10	RL+16
2750	533	688	RL-5	RL+10	RL+16
3200	688	800	RL-5	RL+10	RL+16
3750	800	938	RL-6	RL+10	RL+16
4267	938	1067	RL-6	RL+11	RL+17
4800	1067	1200	RL-7	RL+11	RL+17
5500	1200	1375	RL-7	RL+11	RL+17
6400	1375	1600	RL-8	RL+11	RL+17
7500	1600	1875	RL-9	RL+12	RL+24
8533	1875	2133	RL-10	RL+12	RL+24
9600	2133	2400	RL-11	RL+12	RL+24
10667	2400	2667	RL-12	RL+13	RL+25
11733	2667	2933	RL-13	TBD	TBD
12800	2933	3200	RL-14	TBD	TBD
14400	3200	3600	RL-15	TBD	TBD

### 7.8.5.3.2 NT-ODT Behavior for Read Operation (cont'd)

**Table 333 – ODTLon\_RD\_RDQS and ODTloff\_RD\_RDQS Latency Values for Read with RDQS Enabled and RDQS PS (MR10 OP[0])=0<sub>B</sub> and RDQS PRE (MR10 OP[4:2])=010<sub>B</sub>, 011<sub>B</sub>**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTloff_RD_RDQS [nCK]	ODTLon_RD_RDQS (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2) [nCK]		
				ALL mode	BL24	BL48
9600	2133	2400	RL-13	RL+12	RL+24	
10667	2400	2667	RL-14	RL+13	RL+25	
11733	2667	2933	RL-15	TBD	TBD	
12800	2933	3200	RL-16	TBD	TBD	
14400	3200	3600	RL-17	TBD	TBD	

**Table 334 – ODTLon\_RD\_RDQS and ODTloff\_RD\_RDQS Latency Values for Read with RDQS Enabled and RDQS PS (MR10 OP[0])=1<sub>B</sub> and RDQS PRE (MR10 OP[4:2])=000<sub>B</sub>, 001<sub>B</sub>**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTloff_RD_RDQS [nCK]	ODTLon_RD_RDQS (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2 -1) [nCK]		
				ALL mode	BL24	BL48
9600	2133	2400	RL-12	RL+11	RL+23	
10667	2400	2667	RL-13	RL+12	RL+24	
11733	2667	2933	RL-14	TBD	TBD	
12800	2933	3200	RL-15	TBD	TBD	
14400	3200	3600	RL-16	TBD	TBD	

**Table 335 – ODTLon\_RD\_RDQS and ODTloff\_RD\_RDQS Latency Values for Read with RDQS Enabled and RDQS PS (MR10 OP[0])=1<sub>B</sub> and RDQS PRE (MR10 OP[4:2])=010<sub>B</sub>, 011<sub>B</sub>**

Data Rate (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	ODTloff_RD_RDQS [nCK]	ODTLon_RD_RDQS (RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + 2 -1) [nCK]		
				ALL mode	BL24	BL48
9600	2133	2400	RL-14	RL+11	RL+23	
10667	2400	2667	RL-15	RL+12	RL+24	
11733	2667	2933	RL-16	TBD	TBD	
12800	2933	3200	RL-17	TBD	TBD	
14400	3200	3600	RL-18	TBD	TBD	

**Table 336 – Asynchronous NT-ODT Turn-On and Turn-Off Timing for Read**

Parameter	ALL Operation Frequency	Unit
tODT_RDon,min	1.5	ns
tODT_RDon,max	3.5	ns
tODT_RDoff,min	1.5	ns
tODT_RDoff,max	3.5	ns

## 7.8.6 Input Clock Stop and Frequency Change

### 7.8.6.1 Input Clock Frequency Change

LPDDR6 SDRAM supports input clock frequency change under the following conditions:

- tCK(abs)min is met for each clock cycle.
- Refresh requirements apply during clock frequency change.
- All banks are required to be idle state.
- SDRAM state is required to be Idle, Dual Bank Refresh or All Bank Refresh.
- Any Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The certain timing conditions such as tRP, tMRW, and tMRR have been met prior to changing the frequency.
- CS shall be held LOW during clock frequency change.
- The LPDDR6 SDRAM is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of (2 x tCK + tXP).
- WCK2CK-Sync state is expired, or WCK2CK-Sync OFF state in case of WCK always On mode.
- Target ODT turn off time (ODTLooff) plus extra 4 clocks and NT-ODT turn on time (ODTLon\_RD, ODTLon\_RD\_DQ, ODTLon\_RD\_RDQS) plus extra 4 clocks are satisfied.

After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

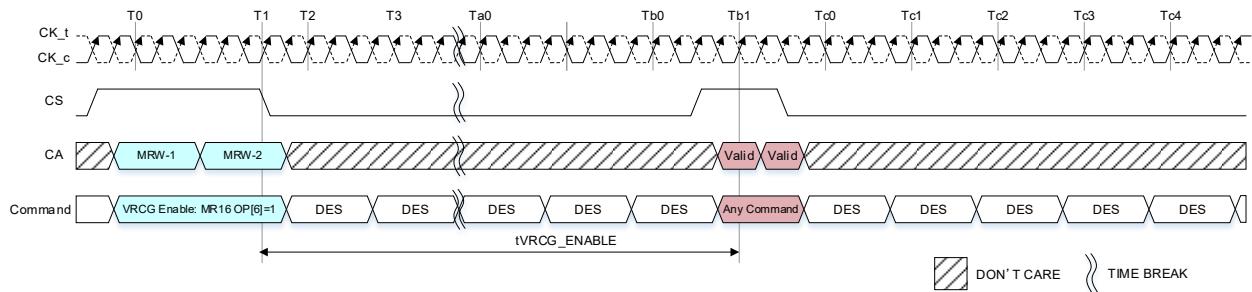
### 7.8.6.2 Input Clock Stop

LPDDR6 SDRAM supports clock stop under the following conditions:

- CK\_t is held LOW and CK\_c is held HIGH during clock stop.
- CS shall be held LOW during clock stop.
- Refresh requirements apply during clock stop.
- All banks are required to be idle state.
- SDRAM state is required to be Idle, Dual Bank Refresh or All Bank Refresh.
- The certain timing conditions such as tRP, tMRW, tMRR, tZQLAT, etc., have been met prior to stopping the clock.
- Read with auto precharge and write with auto precharge commands need extra 4 clock cycles in addition to the related timing constraints, nWR and nRTP, to complete the operations as shown in Figure TBD.
- REFab, REFdb, SRX and ZQcal Start commands are required to have Max(9ns,6nCK) additional clocks prior to stopping the clock as shown in Figure TBD.
- The LPDDR6 SDRAM is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of (2 x tCK + tXP).
- WCK2CK-Sync state is expired, or WCK2CK-Sync OFF state in case of WCK always On mode.
- Target ODT turn off time (ODTLooff) plus extra 4 clocks and NT-ODT turn on time (ODTLon\_RD, ODTLon\_RD\_DQ, ODTLon\_RD\_RDQS) plus extra 4 clocks are satisfied.

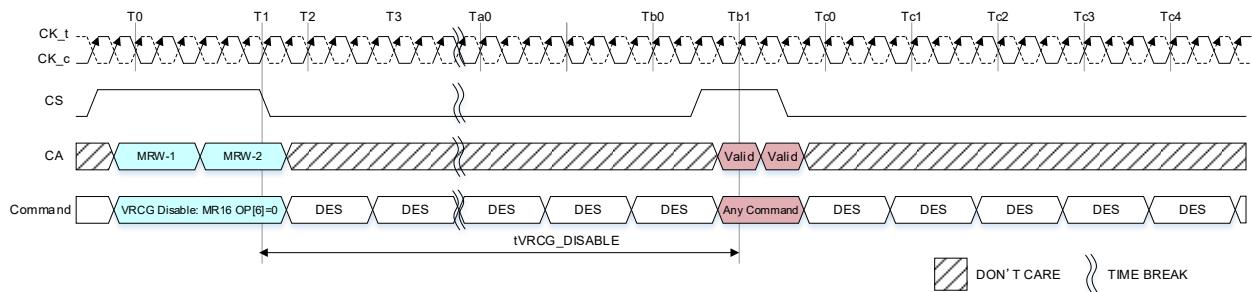
### 7.8.7 VREF Current Generator(VRCG)

LPDDR6 SDRAM VREF current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal VREF(DQ) and VREF(CA) levels during training and when changing frequency set points during operation. The high current mode is enabled by setting MR16 OP[6]=1<sub>B</sub>. Only Deselect commands may be issued until tVRCG\_ENABLE is satisfied. tVRCG\_ENABLE timing is shown in Figure 170.



**Figure 170 – VRCG Enable Timing**

VRCG high current mode is disabled by setting MR16 OP[6]=0<sub>B</sub>. Only Deselect commands may be issued until tVRCG\_DISABLE is satisfied. tVRCG\_DISABLE timing is shown in Figure 171.



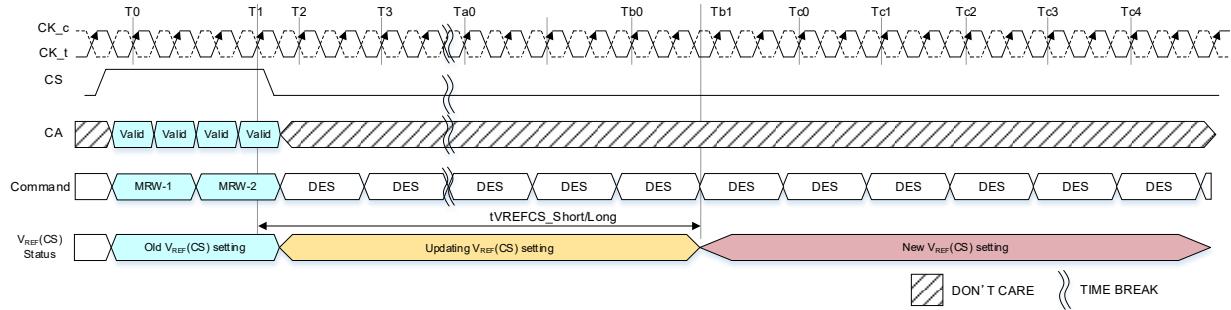
**Figure 171 – VRCG\_DISABLE Timing**

**Table 337 – VRCG Enable/Disable Timing Input Leakage Current**

Parameter	Symbol	Min	Max	Unit	Notes
VREF High Current Mode Enable Time	tVRCG_ENABLE	-	150	Ns	
VREF High Current Mode Disable Time	tVRCG_DISABLE	-	100	ns	

### 7.8.8 VREF(CS) Update Timing

In case of VRGCG is high current mode: MR13 OP[3]=1<sub>B</sub>, LPDDR6 VREF(CS) setting time which update by MRW command is shown in Figure 172.

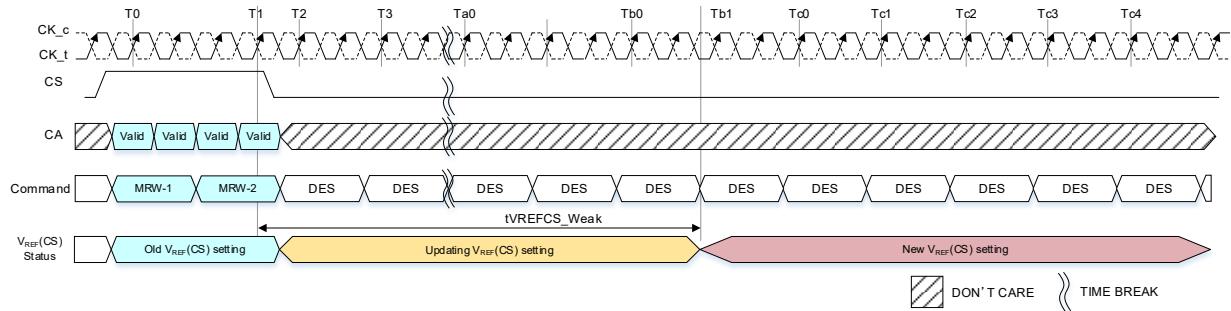


NOTE 1 VRGCG (VREF Current Generator): MR13 OP[3]=1<sub>B</sub>.

NOTE 2 Only DES Command is allowed till tVREFCS\_Short/Long is satisfied.

**Figure 172 – VREF(CS) Update Timing: VRGCG is High Current Mode**

In case of VRGCG is Normal operation: MR13 OP[3]=0<sub>B</sub>, LPDDR6 VREF(CS) setting time which update by MRW command is shown in Figure 173.



NOTE 1 VRGCG (VREF Current Generator): MR13 OP[3]=0<sub>B</sub>.

NOTE 2 Only DES Command is allowed till tVREFCS\_Weak is satisfied.

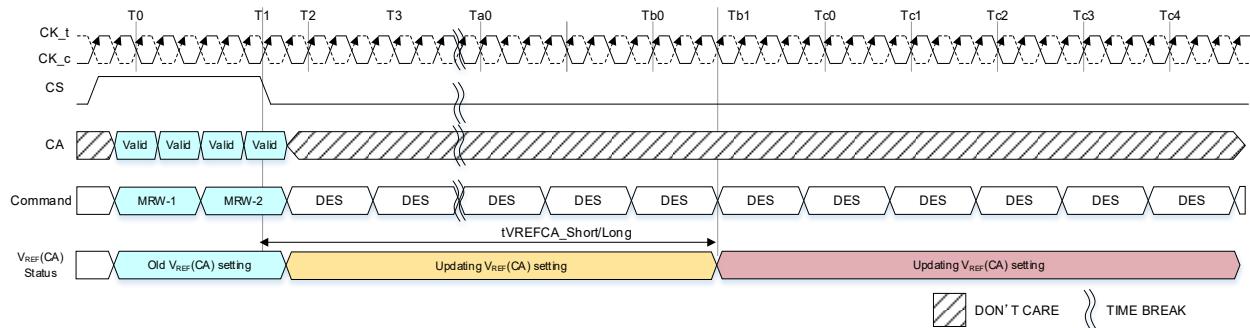
**Figure 173 – VREF(CS) Update Timing: VRGCG is Normal Operation**

**Table 338 – VREF(CS) Update Timing AC Timing Table<sup>5</sup>**

Item	Symbol	Min/Max	Value	Unit	Notes
V <sub>REF</sub> (CS) update parameters					
V <sub>REF</sub> (CS) update timing	tVREFCS_Short	Min	200+0.5tCK	ns	1,2,3
	tVREFCS_Long	Min	250+0.5tCK	ns	1,2,4
	tVREFCS_Weak	Min	1	ms	6
NOTE 1 VREF(CS) update timing depends on value of VREF(CS) setting: MR12 OP[6:0].					
NOTE 2 The value is assumed that VRGCG is setting High current mode: MR13 OP[3]=1 <sub>B</sub> .					
NOTE 3 tCK for this timing is the tCK value of the operating frequency when the MRW is issued.					
NOTE 4 VREFCS_Short is for a single step size increment/decrement change in VREF(CS) voltage.					
NOTE 5 VREFCS_Long is for at least 2 step sizes increment/decrement change including up to VREFmin to VREFmax or VREFmax to VREFmin change in VREF(CS) voltage.					
NOTE 6 The value is assumed that VRGCG is setting Normal Operation: MR13 OP[3]=0 <sub>B</sub> .					

### 7.8.9 VREF(CA) Update Timing

In case of VRCG is high current mode: MR16 OP[6]=1<sub>B</sub>, LPDDR6 VREF(CA) setting time which update by MRW command is shown in Figure 174.

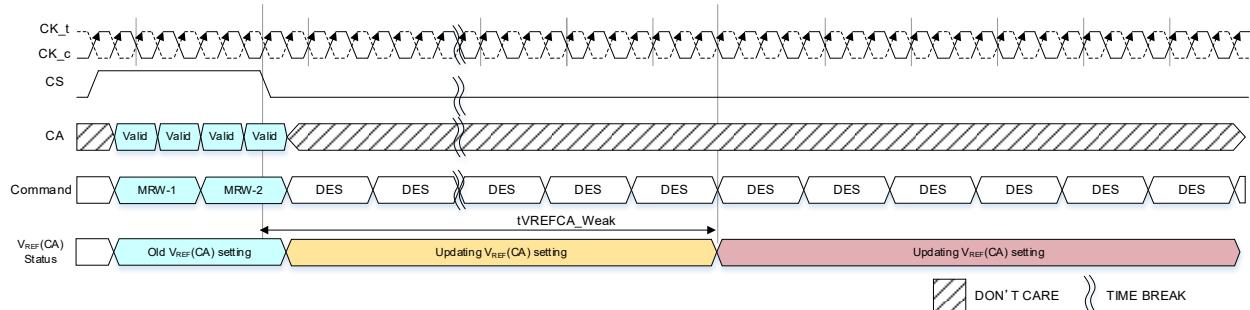


NOTE 1 VR<sub>CG</sub> (VREF Current Generator): MR16 OP[6]=1<sub>B</sub>.

**NOTE 2** Only DES Command is allowed till tVREFCA\_Short/Long is satisfied.

**Figure 174 – VREF(CA) Update Timing: VRCG is High Current Mode**

In case of VRCG is Normal operation: MR16 OP[6]=0<sub>B</sub>, LPDDR6 VREF(CA) setting time which update by MRW command is shown in Figure 175.



NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=0B.

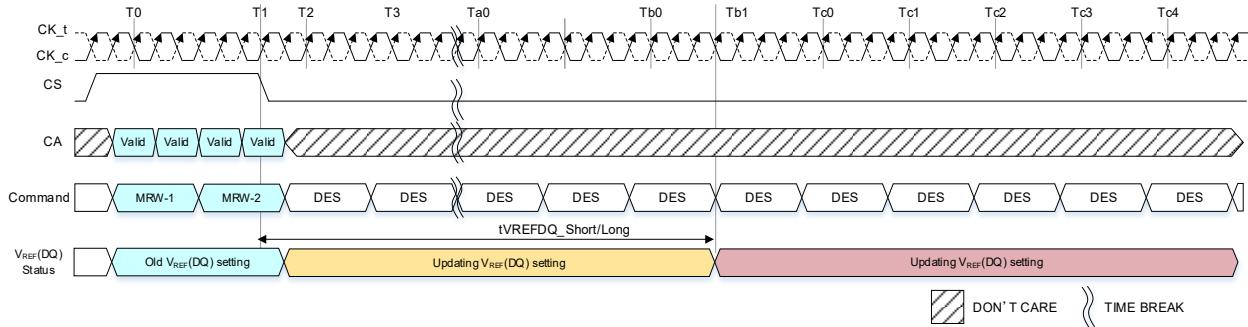
**NOTE 2** Only DES Command is allowed till tVREFCA Weak is satisfied.

**Figure 175 – VREF(CA) Update Timing: VRCG is High Normal Operation**

**Table 339 – VREF(CA) Update Timing AC Timing Table<sup>5</sup>**

### 7.8.10 VREF(DQ) Update Timing

In case of VRCG is high current mode: MR16 OP[6]=1<sub>B</sub>, LPDDR6 VREF(DQ) setting time which update by MRW command is shown in Figure 176.



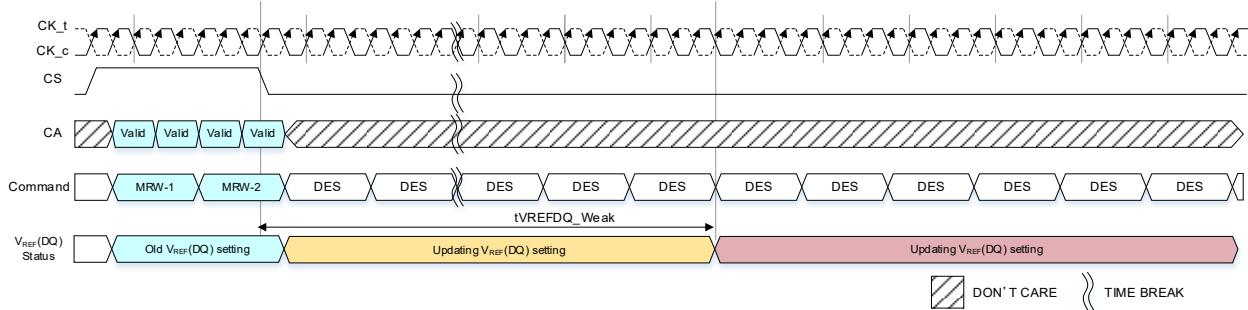
NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=1<sub>B</sub>.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3 The WCK and Data input is prohibited till the tVREFDQ\_Short/Long period is satisfied.

**Figure 176 – VREF(DQ) Update Timing: VRCG is High Current Mode**

In case of VRCG is at Normal operation: MR16 OP[6]=0<sub>B</sub>, LPDDR6 VREF(DQ) setting time which update by MRW command is shown in Figure 177.



NOTE 1 VRCG (VREF Current Generator): MR16 OP[6]=0<sub>B</sub>.

NOTE 2 DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 3 The WCK and Data input is prohibited till the tVREFDQ\_Weak period is satisfied.

**Figure 177 – VREF(DQ) Update Timing: VRCG is High Normal Operation**

### 7.8.10 VREF(DQ) Update Timing (cont'd)

**Table 340 – VREF(DQ) Update Timing AC Timing Table<sup>5</sup>**

Item	Symbol	Min/ Max	Data Rate (Mbps)												Unit	Notes										
			5 3	1 0	1 6	2 1	2 7	3 2	3 7	4 2	4 8	5 5	6 0	6 4												
<b>V<sub>REF</sub>(DQ) update parameters</b>																										
V <sub>REF</sub> (DQ) update timing	tVREFDQ_Short	Min	200+0.5tCK										ns	1,2,3												
	tVREFDQ_Long	Min	250+0.5tCK										ns	1,2,4												
	tVREFDQ_Weak	Min	1										ms	6												
NOTE 1	V <sub>REF</sub> (DQ) update timing depends on value of V <sub>REF</sub> (DQ) setting: MR14 OP[6:0] and MR15 OP[6:0].																									
NOTE 2	The value is assumed that VRCG is setting High current mode: MR16 OP[6]=1 <sub>B</sub> .																									
NOTE 3	tCK for this timing is the tCK value of the operating frequency when the MRW is issued.																									
NOTE 4	VREFDQ_Short is for a single step size increment/decrement change in V <sub>REF</sub> (DQ) voltage.																									
NOTE 5	VREFDQ_Long is for at least 2 step sizes increment/decrement change including up to V <sub>REFmin</sub> to V <sub>REFmax</sub> or V <sub>REFmax</sub> to V <sub>REFmin</sub> change in V <sub>REF</sub> (DQ) voltage.																									
NOTE 6	The value is assumed that VRCG is setting Normal Operation: MR16 OP[6]=0 <sub>B</sub> .																									

### 7.8.11 Thermal Offset

Because of their tight thermal coupling with the LPDDR6 device, hot spots on an SOC can induce thermal gradients across the LPDDR6 device. As these hot spots may not be located near the device thermal sensor, the devices' temperature compensated self-refresh circuit may not generate enough refresh cycles to guarantee memory retention. To address this shortcoming, the controller can provide a thermal offset that the memory uses to adjust its TCSR circuit to ensure reliable operation.

This offset is provided through MR13 OP[1:0]. This temperature offset may modify refresh behavior. It will take a max of 200  $\mu$ s to have the change reflected in MR4 OP[4:0]. If the induced thermal gradient from the device temperature sensor location to the hot spot location of the controller is larger than 15 °C, then self-refresh mode will not reliably maintain memory contents.

To accurately determine the temperature gradient between the memory thermal sensor and the induced hot spot, the memory thermal sensor location must be provided to the LPDDR6 memory controller.

### 7.8.12 Temperature Sensor and Temperature Gradient

LPDDR6 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing de-rating is required in the elevated temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device TOPER may be used to determine whether operating temperature requirements are being met.

LPDDR6 devices shall monitor device temperature and update MR4 according to tTSI. Device temperature status bits shall be no older than tTSI. MR4 will be updated even when device is in self refresh state.

When using the temperature sensor, the actual device case temperature may be higher than the TOPER specification that applies for the standard or elevated temperature ranges. For example, TCASE may be above 85 °C when MR4[4:0] equals 'b01001. LPDDR6 devices shall allow for 2 °C temperature margin between the point at which the device updates the MR4 value and the point at which the controller reconfigures the system accordingly. In the case of tight thermal coupling of the memory device to external hot spots, the maximum device temperature might be higher than what is indicated by MR4.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2 °C.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

$$\text{TempGradient} \times (\text{ReadInterval} + \text{tTSI} + \text{SysRespDelay}) \leq 2 \text{ °C}$$

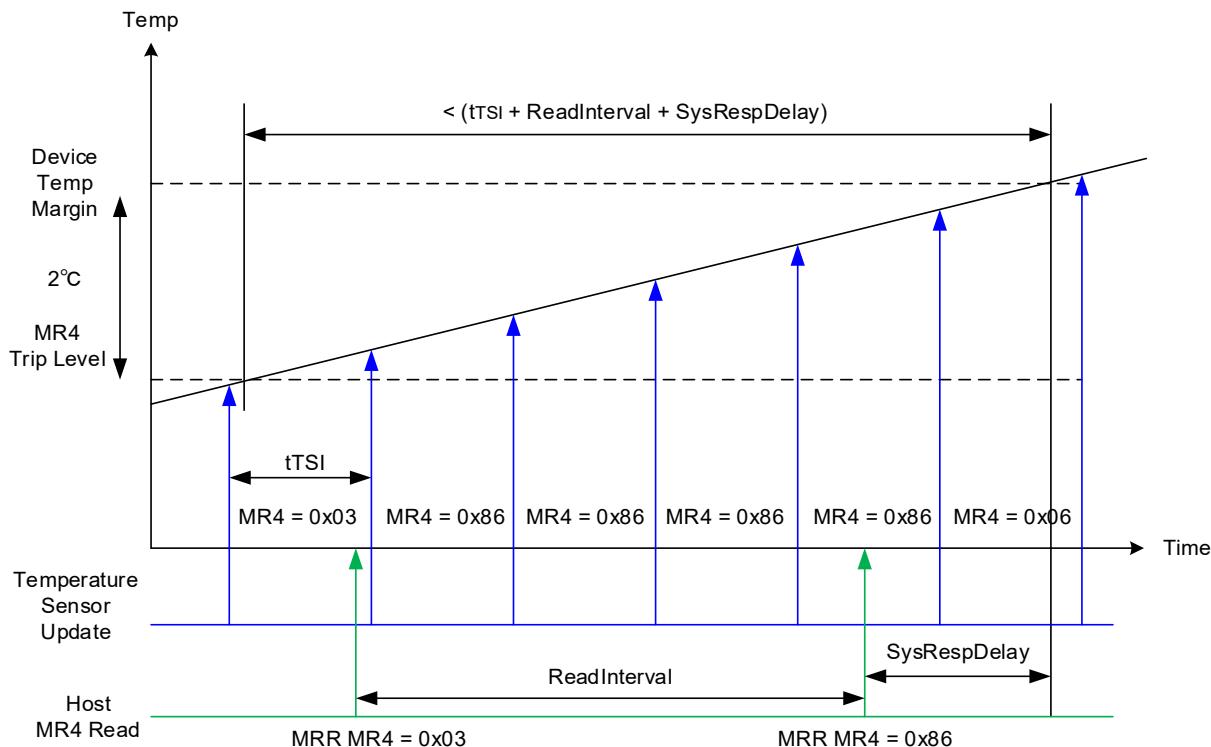
### 7.8.12 Temperature Sensor and Temperature Gradient (cont'd)

**Table 341 – Temperature Sensor**

Parameter	Symbol	Max/ Min	Value	Unit	Note
System Temperature Gradient	TempGradient	Max	System Dependent	°C/s	
MR4 Read Interval	ReadInterval	Max	System Dependent	ms	
Temperature Sensor Interval	tTSI	Max	32	ms	
System Response Delay	SysRespDelay	Max	System Dependent	ms	
Device Temperature Margin	TempMargin	Max	2	°C	

For example, if TempGradient is 10 °C/s and the SysRespDelay is 1 ms:

$(10 \text{ °C/s}) \times (\text{ReadInterval} + 32 \text{ ms} + 1 \text{ ms}) \leq 2 \text{ °C}$ . In this case, ReadInterval shall be no greater than 167 ms.



**Figure 178 – Temp Sensor Timing**

### 7.8.13 Multi-Purpose Command

LPDDR6 SDRAM uses the MPC command to issue commands about ZQ calibration, CK SYNC Off and WCK2DQx Interval Oscillator. The MPC command is initiated with CS and CA[3:0] asserted to the proper state at the crossing points of CK\_t and CK\_c, as defined in TBD. The MPC command has eight operands (OP[7:0]) that are decoded to execute specific commands in the SDRAM. OP[7] is a special bit that is decoded on the first crossing point of CK\_t and CK\_c of the MPC command.

The MPC command supports the following functions:

- Start WCK2DQI Interval Oscillator
- Stop WCK2DQI Interval Oscillator
- Start WCK2DQO Interval Oscillator
- Stop WCK2DQO Interval Oscillator
- ZQ CAL Latch
- CK SYNC Off

**Table 342 – MPC Command Definition**

SDRAM COMMAND	CS	DDR COMMAND PIN				CK_t edge	Notes	
		CA0	CA1	CA2	CA3			
MULTI PURPOSE COMMAND (MPC)	H	H	L	L	L/PAR	R1	1, 2	
	X	H	L	H	V	F1		
	H	OP4	OP5	OP6	OP7	R2		
	X	OP0	OP1	OP2	OP3	F2		
NOTE 1 LPDDR6 commands are two clock cycles long and defined by the states of CS at the 1st and 2nd rising edge (R1, R2) of clock and CA[3:0] at the 1st rising edge (R1), the 1st falling edge (F1), the 2nd rising edge (R2) and the 2nd falling edge (F2) of clock. Note that some operations such as ACTIVATE and MODE REGISTER WRITE require two commands to initiate.								
NOTE 2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CK_t, CK_c and CA[3:0] can be floated.								
NOTE 3 MPC to MPC command timing constraints is 4nCK.								

**Table 343 – MPC Command Definition for OP[7:0]**

Function	Operand	Data	Notes
Commands	OP[7:0]	10000001 <sub>B</sub> : Start WCK2DQI Interval Oscillator 10000010 <sub>B</sub> : Stop WCK2DQI Interval Oscillator 10000011 <sub>B</sub> : Start WCK2DQO Interval Oscillator 10000100 <sub>B</sub> : Stop WCK2DQO Interval Oscillator 10000101 <sub>B</sub> : Reserved 10000110 <sub>B</sub> : ZQ CAL Latch 10010000 <sub>B</sub> : CK SYNC Off All Others: Reserved	

### 7.8.14 WCK2DQ Interval Oscillator

As voltage and temperature change on the SDRAM die, the WCK clock tree delay will shift and may require re-training.

The LPDDR6-SDRAM includes an internal CK based WCK2DQx Interval Oscillator to measure the amount of delay over a given time interval (determined by the controller), allowing the controller to compare the trained delay value to the delay value seen at a later time. The CK based WCK2DQx Interval Oscillator will provide the controller with important information regarding the need to re-train, and the magnitude of potential error in WCK clock tree.

To provide low power interval oscillator to user, the WCK2DQx Interval Oscillator counts the number of CK cycles, not the number of WCK cycles.

The WCK2DQx Interval Oscillator is started by issuing an MPC [Start WCK2DQx Osc] which will start an internal ring oscillator. A counter is implemented to count the number of times a signal propagates through a replica of the WCK clock tree during the established time interval.

The WCK2DQx Interval Oscillator may be stopped by issuing an MPC [Stop WCK2DQx Osc] or the controller may instruct the SDRAM to count for a specific number of clocks and then stop automatically.

When the WCK2DQx Interval Oscillator is stopped by either method, the result of the oscillator counter is automatically stored in MR35/MR36 and MR38/MR39.

WCK2DQI Interval Oscillator and WCK2DQO Interval Oscillator cannot be operated simultaneously. After completing WCK2DQI (or WCK2DQO) Interval Oscillator operation, WCK2DQO (or WCK2DQI) Interval Oscillator Start MPC can be issued. To track tWCK2DQx variation of different WCK frequency modes (MR11 OP[6]), user can specify WCK2DQx oscillator for WCK low or high frequency mode via MR11 OP[6]. When operating in WCK low frequency mode (MR11 OP[6]=0<sub>B</sub>), WCK2DQx oscillator for WCK high frequency mode (MR11 OP[6]=1<sub>B</sub>) can be enabled and vice versa.

The controller may adjust the accuracy of the result by running the WCK2DQx Interval Oscillator for shorter (less accurate) or longer (more accurate) duration. The accuracy of the result for a given temperature and voltage is determined by the following equation:

$$\text{WCK2DQx Interval Oscillator Granularity Error} = \frac{2 * (\text{WCK2DQx Delay})}{\text{Run Time}}$$

Where: Run Time = Total time between start and stop commands  
WCK2DQ delay = the value of the WCK clock tree delay (tWCK2DQ min/max)

Additional matching error must be included, which is the difference between WCK training circuit and the actual WCK clock tree across voltage and temperature.

Therefore, the total accuracy of the WCK2DQx Interval Oscillator counter is given by:

$$\text{WCK2DQx Interval Oscillator Accuracy} = 1 - \text{Granularity Error} - \text{Matching Error}$$

#### 7.8.14 WCK2DQ Interval Oscillator (cont'd)

The result of the WCK2DQx Interval Oscillator is defined as the number of CK cycles which reflects WCK Clock tree Delays that are counted during the run time determined by the controller.

The result for WCK2DQI is stored in MR35 OP[7:0] and MR36 OP[7:0], and that for WCK2DQO is also stored in MR38 OP[7:0] and MR39 OP[7:0]. MR35 and MR38 contain the least significant bits (LSB) of the result for WCK2DQI and WCK2DQO, respectively. MR36 and MR39 contain the most significant bits (MSB) of the result for WCK2DQI and WCK2DQO, respectively.

MR35 and MR36 are overwritten by the SDRAM when an MPC-1 [Stop WCK2DQI Osc] command is received. Similarly, for a WCK2DQI stop command, MR38 and MR39 are also overwritten when SDRAM receives MPC-1 [Stop WCK2DQO Osc] command.

The SDRAM counter will count to its maximum value ( $=2^{16}$ ) and stop. If the maximum value is read from the mode registers, then the memory controller must assume that the counter overflowed the register and discard the result. The longest "run time" for the oscillator that will not overflow the counter registers can be calculated as follows:

$$\text{Longest WCK2DQI Run Time Interval} = 216 * t_{WCK2DQ} \text{ (min)} = 216 * \text{TBD} = \text{TBD}$$

$$\text{Longest WCK2DQO Run Time Interval} = 216 * t_{WCK2DQ} \text{ (min)} = 216 * \text{TBD} = \text{TBD}$$

#### 7.8.14.1 Interval Oscillator Matching Error

The interval oscillator matching error is defined as the difference between the WCK training circuit (interval oscillator) and the actual WCK clock tree across voltage and temperature.

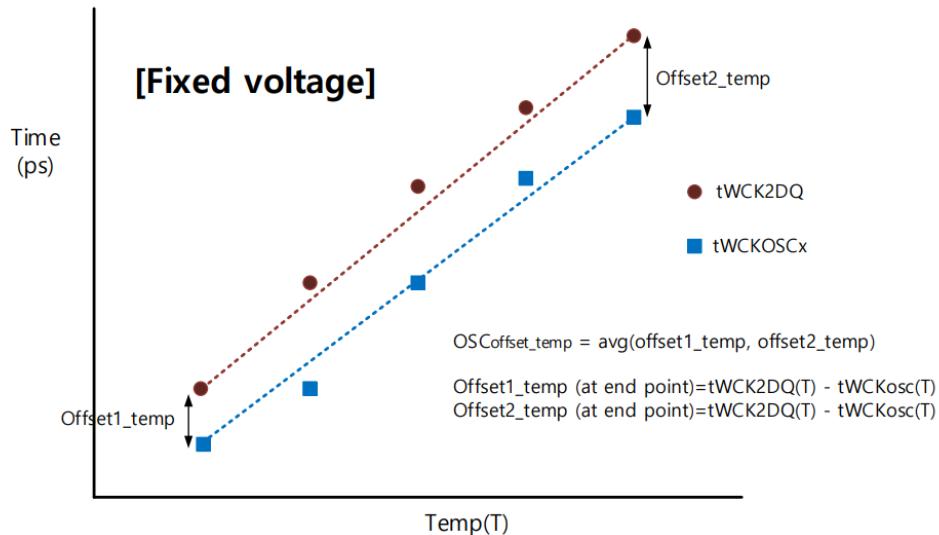


Figure 179 – Interval Oscillator Offset\_Temp

- OSC<sub>Match\_temp</sub>:  $\text{OSC}_{\text{Match\_temp}} = [\text{tWCK2DQ}_{(T)} - \text{tWCKosc}_{(T)} - \text{OSC}_{\text{offset\_temp}}]$
- tWCKosc(T):  $\text{tWCKosc } (T) = \frac{\text{RunTime}}{2*\text{count}}$

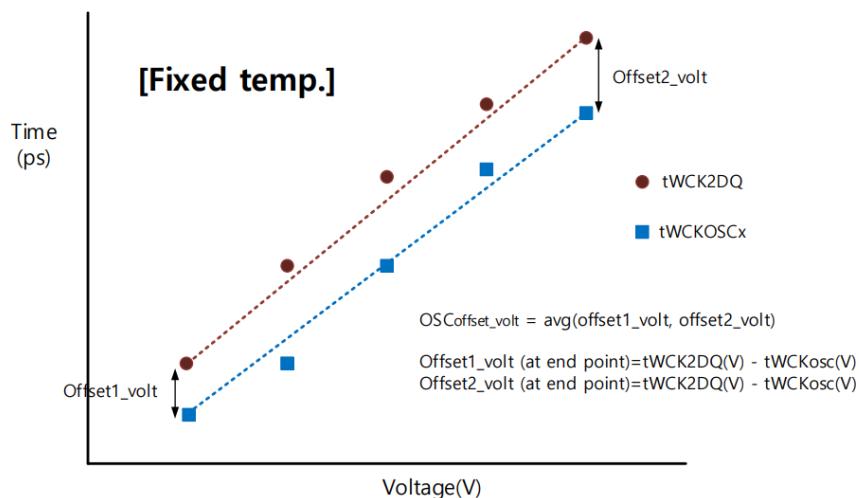


Figure 180 – Interval Oscillator Offset\_Volt

- OSC<sub>Match\_volt</sub>:  $\text{OSC}_{\text{Match\_volt}} = [\text{tWCK2DQ}_{(V)} - \text{tWCKosc}_{(V)} - \text{OSC}_{\text{offset\_volt}}]$
- tWCKosc(V):  $\text{tWCKosc } (V) = \frac{\text{RunTime}}{2*\text{count}}$

### 7.8.14.1 Interval Oscillator Matching Error (cont'd)

**Table 344 – WCK Oscillator Matching Error Specification for HF Mode**

Parameter	Symbol	$\leq 6400$ Mbps		7500/8533		9600/12800		Units	Note
		Min	Max	Min	Max	Min	Max		
Write WCK Oscillator Matching Error: Voltage variation	WOSC <sub>Match_volt</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,2,3,5
Write WCK Oscillator Matching Error: Temperature variation	WOSC <sub>Match_temp</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,2,3,5
Write WCK Oscillator Offset for Voltage variation	WOSC <sub>offset_volt</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	2,5
Write WCK Oscillator Offset for Temperature variation	WOSC <sub>offset_temp</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	2,5
Read WCK Oscillator Matching Error: Voltage variation	ROSC <sub>Match_volt</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,2,3,6
Read WCK Oscillator Matching Error: Temperature variation	ROSC <sub>Match_temp</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,2,3,6
Read WCK Oscillator Offset for Voltage variation	ROSC <sub>offset_volt</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	2,6
Read WCK Oscillator Offset for Temperature variation	ROSC <sub>offset_temp</sub>	TBD	TBD	TBD	TBD	TBD	TBD	ps	2,6
NOTE 1 The WOSCmatch or ROSCmatch is the matching error between the actual WCK and WCK interval oscillator over voltage and temp. NOTE 2 This parameter will be characterized or guaranteed by design. NOTE 3 The input stimulus for tWCK2DQ will be consistent over voltage and temp conditions. NOTE 4 tWCK2DQ (V, T) delay will the average of WCK to DQ delay over the runtime period. NOTE 5 The matching error and offset of WOSC is from WCK2DQI interval oscillator. NOTE 6 The matching error and offset of ROSC is from WCK2DQO interval oscillator. NOTE 7 For Elevated, Automotive Grade 1/2/3 temperature range, please contact venders for temperature variation specs.									

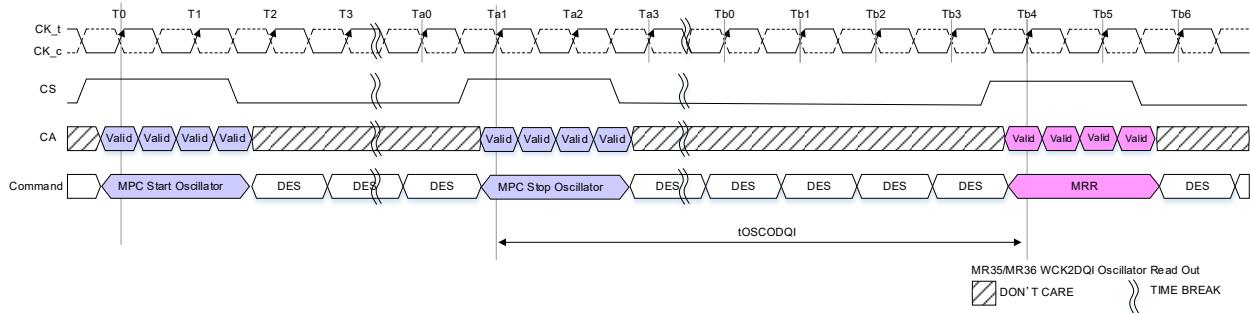
**Table 345 – WCK Oscillator Matching Error Specification for LF Mode**

Parameter	Symbol	Min	Max	Unit	Notes
Write WCK Oscillator Matching Error: Voltage variation	WOSC <sub>Match_volt</sub>	TBD	TBD	ps	1,2,3,5
Write WCK Oscillator Error: Temperature variation	WOSC <sub>Match_temp</sub>	TBD	TBD	ps	1,2,3,5
Write WCK Oscillator Offset: Voltage variation	WOSC <sub>offset_volt</sub>	TBD	TBD	ps	2,5
Write WCK Oscillator Offset: Temperature variation	WOSC <sub>offset_temp</sub>	TBD	TBD	ps	2,5
Read WCK Oscillator Matching Error: Voltage variation	ROSC <sub>Match_volt</sub>	TBD	TBD	ps	1,2,3,6
Read WCK Oscillator Error: Temperature variation	ROSC <sub>Match_temp</sub>	TBD	TBD	ps	1,2,3,6
Read WCK Oscillator Offset: Voltage variation	ROSC <sub>offset_volt</sub>	TBD	TBD	ps	2,6
Read WCK Oscillator Offset: Temperature variation	ROSC <sub>offset_temp</sub>	TBD	TBD	ps	2,6
NOTE 1 The WOSCmatch or ROSCmatch is the matching error between the actual WCK and WCK interval oscillator over voltage and temp. NOTE 2 This parameter will be characterized or guaranteed by design. NOTE 3 The input stimulus for tWCK2DQ will be consistent over voltage and temp conditions. NOTE 4 tWCK2DQ(V, T) delay will the average of WCK to DQ delay over the runtime period. NOTE 5 The matching error and offset of WOSC is from WCK2DQI interval oscillator. NOTE 6 The matching error and offset of ROSC is from WCK2DQO interval oscillator.					

## 7.8.14.2 WCK2DQI/O Interval Oscillator Readout Timing

### 7.8.14.2.1 WCK2DQI Interval Oscillator

WCK2DQI interval Oscillator Stop to its counting value readout timing is shown in Figure 181 and Figure 182.

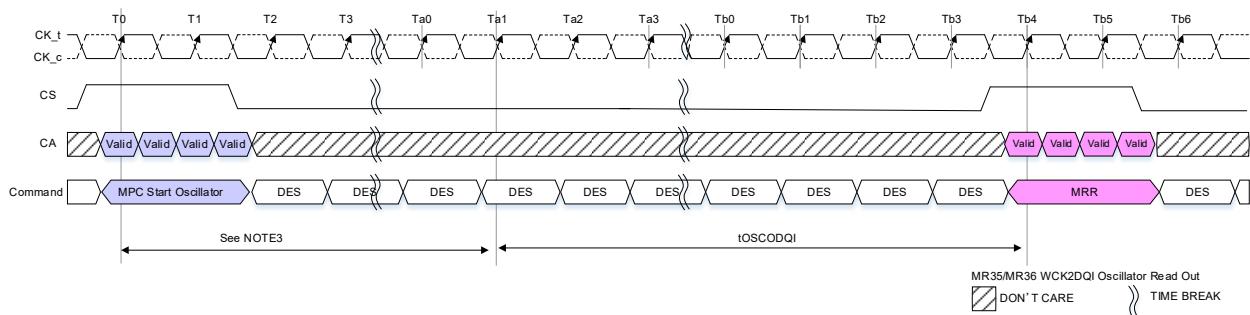


NOTE 1 The combination of 'MPC: Start Oscillator' and 'MPC: Stop Oscillator' is follows Start WCK2DQI Interval oscillator and stop WCK2DQI interval oscillator.

NOTE 2 WCK2DQI interval run time : MR37 OP [7:0]=00000000<sub>B</sub>.

NOTE 3 DES Commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 181 – In Case of WCK2DQI Interval Oscillator is Stopped by MPC Command**



NOTE 1 The combination of 'MPC: Start Oscillator' and 'MPC: Stop Oscillator' is follows Start WCK2DQI Interval oscillator and stop WCK2DQI interval oscillator.

NOTE 2 WCK2DQI interval run time : MR37 OP [7:0]=00000000<sub>B</sub>.

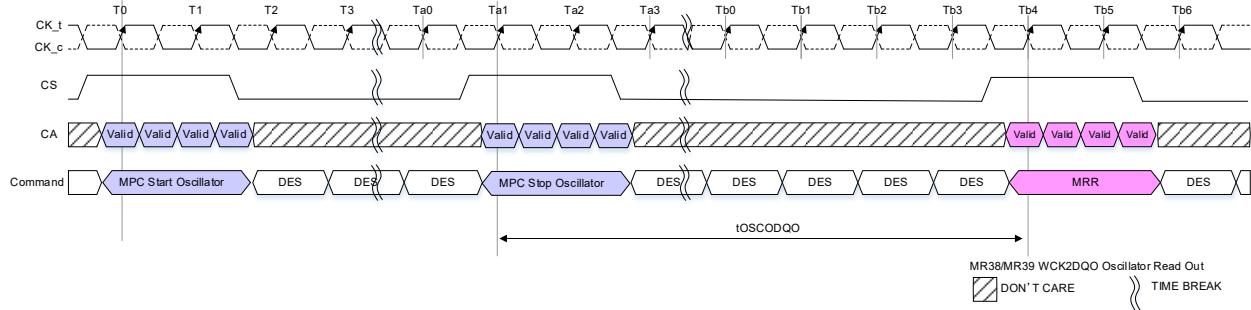
NOTE 3 Setting counts of MR37 for WCK2DQI interval Oscillator.

NOTE 4 DES Commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 182 – In Case of WCK2DQI Interval Oscillator is Stopped by Interval Timer**

### 7.8.14.2.2 WCK2DQO Interval Oscillator

WCK2DQO interval Oscillator Stop to its counting value readout timing is shown in Figure 183 and Figure 184.

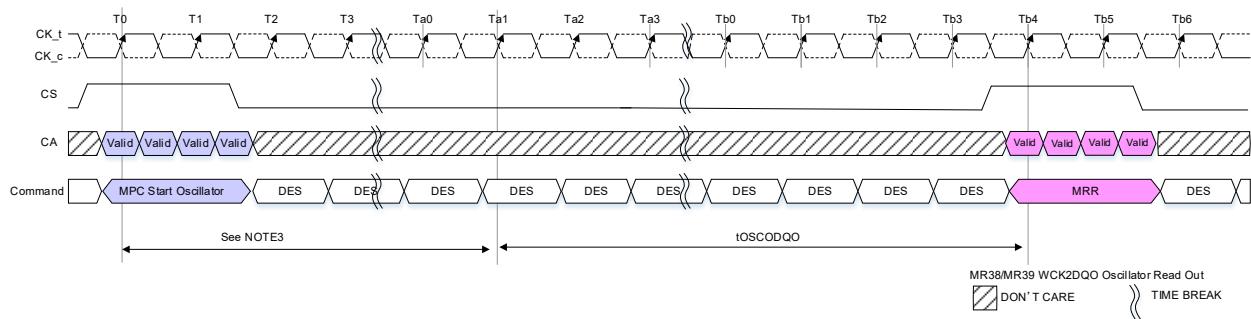


**NOTE 1** The combination of 'MPC: Start Oscillator' and 'MPC: Stop Oscillator' is as following Start WCK2DQO Interval oscillator and stop WCK2DQO interval oscillator.

**NOTE 2** WCK2DQO interval run time: MR40 OP [7:0]=00000000<sub>B</sub>.

**NOTE 3** DES Commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 183 – In Case of WCK2DQO Interval Oscillator is Stopped by MPC Command**



**NOTE 1** The combination of 'MPC: Start Oscillator' and 'MPC: Stop Oscillator' is as following Start WCK2DQO Interval oscillator and stop WCK2DQO interval oscillator.

**NOTE 2** WCK2DQO interval run time: MR40 OP [7:0]=00000000<sub>B</sub>.

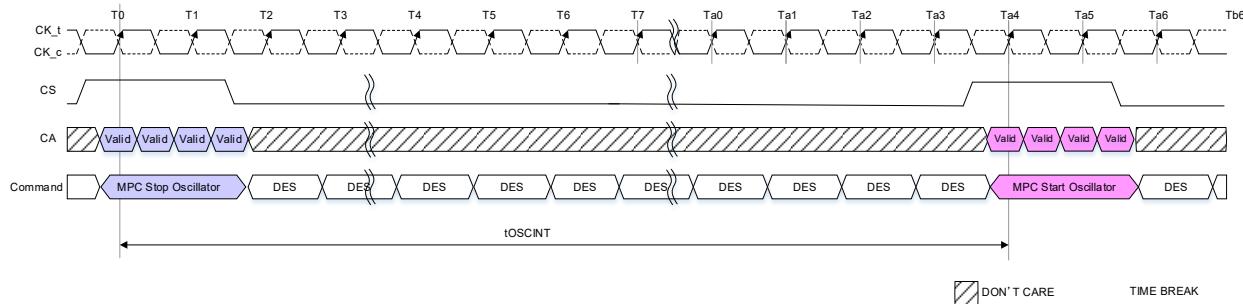
**NOTE 3** Setting counts of MR40 for WCK2DQO interval Oscillator.

**NOTE 4** DES Commands are shown for ease of illustration; other commands may be valid at these times.

**Figure 184 – In Case of WCK2DQO Interval Oscillator is Stopped by Interval Timer**

### 7.8.14.3 WCK2DQI(O) Interval Oscillator Start/Stop Command Constraints

WCK2DQI/WCK2DQO Interval Oscillator Start/Stop Command Constraints is shown in Figure 185.



NOTE 1 This parameter applies to following combination.

- MPC Stop WCK2DQI Interval Oscillator to MPC Start WCK2DQO Interval Oscillator.
- MPC Stop WCK2DQO Interval Oscillator to MPC Start WCK2DQI Interval Oscillator.
- MPC Stop WCK2DQI Interval Oscillator to MPC Start WCK2DQI Interval Oscillator.
- MPC Stop WCK2DQO Interval Oscillator to MPC Start WCK2DQO Interval Oscillator.

**Figure 185 – WCK2DQI/WCK2DQO Interval Oscillator Start/Stop Command Constraints Timing**

**Table 346 – WCK2DQI/WCK2DQO Interval Oscillator AC Timing**

Parameter	Symbol	Min/Max	Value	Units	Notes
Delay time from Stop WCK2DQI Interval Oscillator command to Mode Register Readout from MR35/MR36	tOSCODQI	Min	TBD	ns	1
Delay time from Stop WCK2DQO Interval Oscillator command to Mode Register Readout from MR38/MR39	tOSCODQO	Min	TBD	ns	2
Delay time from MPC OSC Stop command to MPC OSC Start command	tOSCINT	Min	TBD	ns	
NOTE 1 Issuing all Mode Register Read (MRR) command except for MR35/MR36 is allowed in tOSCODQI period.					
NOTE 2 Issuing all Mode Register Read (MRR) command except for MR38/MR39 is allowed in tOSCODQO period.					

### 7.8.15 DVFSQ Mode

LPDDR6 devices can allow VDDQ to be ramped during operation including Read and Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Some guidelines are:

If operation of the LPDRAM will be halted during the VDDQ voltage ramp.

1. The device must be placed in power-down mode or CS held low until the voltage ramp is complete.
2. Re-calibration is recommended before high-speed operation at VDDQ=0.5 V nominal after ramping the VDDQ level.
3. FSP change to appropriate new settings should occur before operation at the new level

If operation of the LPDRAM during the VDDQ voltage ramp is intended

1. The LPDRAM should be operated at settings and speeds suitable for the lowest VDDQ level.
2. Operation with ODT disabled is highly recommended, and generally required for VDDQ levels below 0.5 V nominal.
3. The VDDQ voltage ramp should always be equal or slower than the specified limits
4. Recommended to set VRCG enabled to ensure internal Vref tracking of the changing VDDQ level.
5. Re-calibration is recommended before high-speed operation at VDDQ=0.5v nominal after ramping the VDDQ level.
6. FSP change to appropriate new settings should occur before higher-speed operation at the new level.

### 7.8.16 Post Package Repair (PPR)

The repair process is irrevocable so great care should be exercised when using. With PPR, LPDDR6 SDRAM can correct 1 Row per bank. The controller should prevent unintended PPR mode entry and repair. Before start PPR, dynamic efficiency mode should be disabled.

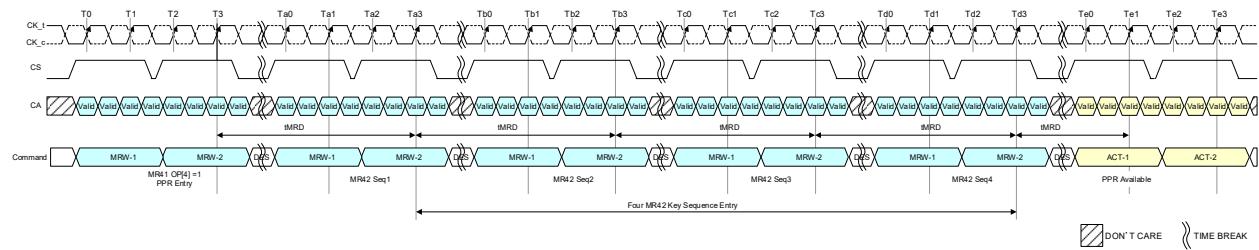
The availability of PPR for each bank is readable via MR43 OP[7:0] and MR44 OP[7:0] respectively. When static efficiency mode is enabled, mode register read should be issued with valid SC (sub-channel op).

**Table 347 – MR43 OP[7:0] and MR44 OP[7:0] Register Information**

Function	Register Type	Operand	Data	Notes
PPR Resource Bank Group 0 / Bank 0	Read-only	MR43 OP[0]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 0 / Bank 1		MR43 OP[1]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 0 / Bank 2		MR43 OP[2]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 0 / Bank 3		MR43 OP[3]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 1 / Bank 0		MR43 OP[4]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 1 / Bank 1		MR43 OP[5]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 1 / Bank 2		MR43 OP[6]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 1 / Bank 3		MR43 OP[7]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 2 / Bank 0		MR44 OP[0]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 2 / Bank 1		MR44 OP[1]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 2 / Bank 2		MR44 OP[2]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 2 / Bank 3		MR44 OP[3]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 3 / Bank 0		MR44 OP[4]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 3 / Bank 1		MR44 OP[5]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 3 / Bank 2		MR44 OP[6]	0B: PPR Resource is not available 1B: PPR Resource is available	
PPR Resource Bank Group 3 / Bank 3		MR44 OP[7]	0B: PPR Resource is not available 1B: PPR Resource is available	

### 7.8.16.1 Guard Key Protection

Entry into PPR is protected through a sequential MRS guard key to prevent unintentional PPR programming. The PPR guard key requires a sequence of four MRW commands to be issued immediately after entering PPR, as shown in Figure 186. The guard key sequence is entered in the specified order as stated below and shown in Table 348. Any interruptions of the guard key sequence by other MRW/MRR commands or non-MR commands such as ACT, WR, RD, REFab, and REFdb are not allowed. Since interruption of the guard key entry is not allowed, if the guard key is not entered in the required order or is interrupted by other commands intentionally, it should be asserted Reset\_n, followed immediately by the reset and initialization procedure. If the guard key is not entered in the required order or an incorrect guard key is entered unintentionally, the SDRAM will capture the wrong guard key and PPR mode will not execute. Even in this case, asserting Reset\_n, and then doing the reset and initialization procedure is required at the end of PPR procedure. The SDRAM does not provide an error indication if an incorrect PPR guard key sequence is entered.



NOTE 1 Only DES commands are allowed during tMRD.

Figure 186 – Guard Key Timing Diagram

Table 348 – Guard Key Encoding for MR42

Command	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR42 Seq1	1	1	0	0	1	1	1	1
MR42 Seq2	0	1	1	1	0	0	1	1
MR42 Seq3	1	0	1	1	1	0	1	1
MR42 Seq4	0	0	1	1	1	0	1	1

### 7.8.16.2 PPR Fail Row Address Repair

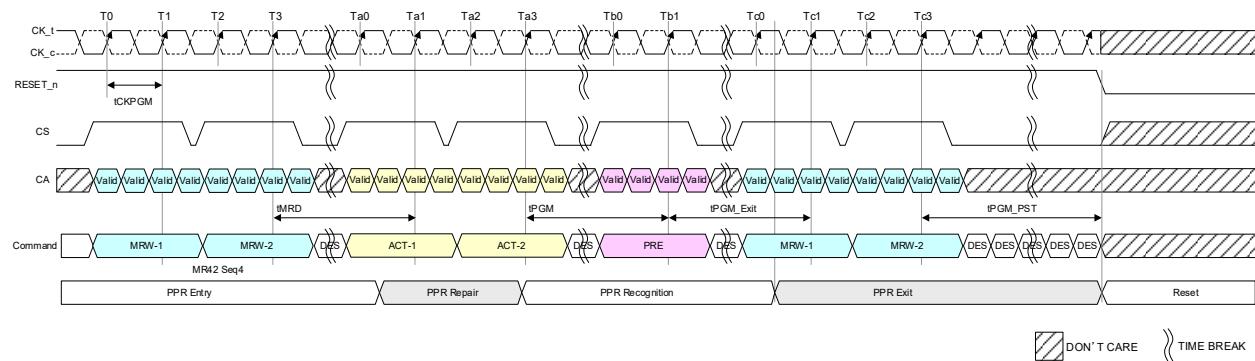
Once PPR mode is entered by setting MR41 OP[4]=1<sub>B</sub> (enable) and issuing the guard key sequence, the ACT command is used to transmit the bank and row address of the row to be repaired in SDRAM. The specific steps of PPR are as follows.

The following is procedure of PPR.

1. Before entering PPR mode, all banks must be Precharged and in an idle state, and WCK Sync. must be expired. If not, WCK Sync. must be turned off intentionally.
2. During PPR mode, non-target PPR sub-channel must be idle state and kept idle state.
3. Enable PPR using MR41 OP[4]=1<sub>B</sub> and wait tMRD.
4. Issue the guard key as four consecutive MR42 OP[7:0] MRW commands each with a unique address field OP[7:0]. Each MRW command should be spaced by tMRD.
5. Issue an ACT command with the Bank Group, Bank and Row fail address.
6. Wait tPGM to allow the SDRAM to repair target Row Address internally then issue PRE.
7. Wait tPGM\_Exit after PRE which allows the SDRAM to recognize repaired Row address RAn.
8. Exit PPR by setting MR41 OP[4]=0<sub>B</sub> and wait tPGMPST.
9. Assert Reset\_n, and then do the reset and initialization procedure.
10. In more than one fail address repair case, Repeat Steps 2 to 8.

After entering PPR mode, do not deviate from the above-mentioned procedure. It is prohibited to insert any other command except DES between step 3 and step 8. The PPR procedure is required to be performed at a clock frequency of 800 MHz or less, the frequency for PPR mode is defined as tCKPGM.

Once PPR mode is exited, the controller can verify that the target row was repaired by writing data into the target row and reading it back after reset and initialization procedure.



NOTE 1 With one PPR command, only one row can be repaired at one time per die.

NOTE 2 RESET is required at the end of every PPR procedure.

NOTE 3 During PPR, memory contents are not refreshed and may be lost.

NOTE 4 Assert Reset\_n: Refer to Power up and Initialization section for details on reset, power-up, initialization and power-off procedures.

Figure 187 – PPR Timing

Table 349 — PPR Timing Parameters

Parameter	Symbol	Min	Max	Unit	Notes
PPR Programming Clock	tCKPGM	1.25	50	ns	
PPR Programming Time	tPGM	2000	-	ms	
PPR Exit Time	tPGM_Exit	15	-	ns	
New Address Setting time	tPGMPST	500	-	μs	

### 7.8.17 Soft Post Package Repair(sPPR)

LPDDR6 supports Fail Row address repair, PPR which allows a simple and easy repair method in a system. Three methods are provided. Hard Post Package Repair (hPPR) and mBIST PPR (mPPR) for a permanent Row repair, Soft Post Package Repair (sPPR) for a temporary Row repair. sPPR is LPDDR6 optional feature which indicated by MR2 OP[3]

The DRAM will retain the sPPR information inside the DRAM as long as DRAM powers remain within the operating region. If DRAM power is removed or the DRAM is Reset the sPPR will revert to the un-repaired state. With sPPR, LPDDR6 can repair one row address per bank. sPPR resources are shared with hPPR. However, MBIST-mPPR resources are separated from hPPR resources. The use of sPPR will not decrease the availability of hPPR resources, so the host must track the resources used. If the resources for the bank that is targeted for sPPR are used up, the bank will have no more available resources for soft PPR. If a soft repair sequence is issued to a Bank with no repair resources available, the DRAM will ignore the programming sequence. sPPR must have been disabled, cleared and unlocked prior to entering hPPR, MBIST or mPPR modes.

Entry into hPPR, sPPR, MBIST and mPPR is protected through a sequential MRW guard key to prevent unintentional PPR programming. The sequential MRW guard key is the same for hPPR, sPPR, MBIST and mPPR.

The following is the procedure of sPPR with PRE command. Note that during the soft repair sequence, no refresh is allowed.

- 1) User should back up the data of the target row address for sPPR in the bank before sPPR execution. The backup data should be one row per bank. After sPPR has been completed, user restores the data in the repaired array.
- 2) sPPR resources are shared with hPPR. The hPPR resource designation registers (MR43, MR44) should be checked prior to sPPR. If the MRR of hPPR resource designation (MR43, MR44) shows that hPPR resources in the bank that is targeted for sPPR repair is not available, the host controller should not issue sPPR mode.
- 3) Before entering 'sPPR' mode, all banks shall be in a precharged and idle state.
- 4) Enable sPPR using MR26 OP[5:4]=01<sub>B</sub> and wait tMRD.
- 5) Issue Guard Key as four consecutive MRW commands(MR42) each with a unique address field OP[7:0] Each MRW command shall be separated by tMRD. The Guard Key sequence is the same as hPPR in Table 348.
- 6) Issue ACT command Bank Group, Bank and Row Fail address. For static efficiency mode devices, the SC bits should identify Sub-Channel information, and non-static efficiency mode devices, should be disabled dynamic efficiency mode for 'sPPR' mode.
- 7) Wait tPGM\_sPPR(min) for the internal repair register to be written and then issue PRE to the Bank.
- 8) Wait tRP after PRE command to allow the DRAM to recognize repaired Row address.
- 9) Exit sPPR with setting MR26 OP[5:4]=00<sub>B</sub> and wait tMRD.
- 10) sPPR can be performed without affecting the hPPR previously performed provided a row is available in that repair region. When more than one sPPR request is made to the same repair region, the most recently issued sPPR address would replace the early issued one associated with given bank and row addresses. In the case of conducting soft repair address in a different repair region, repeat steps 4 to 9. During a soft repair, refresh command is not allowed between sPPR MRS entry and exit.

### 7.8.17 Soft Post Package Repair(sPPR) (cont'd)

**Table 350 – sPPR Timings**

Max	Operand	Min	Unit	Notes
PPR Programming Time	tPGM_sPPR	tRAS	ns	2
PPR Exit Time	tPGM_EXT	tRP	ns	2
New Address Setting Time	tPGMPST_sPPR	tMRD	ns	

#### 7.8.17.1 sPPR Undo

sPPR Undo is a method of setting the sPPR resource back to its unused state, as it was following Reset. It follows the exact same protocol as the sPPR sequence, but with MR26 OP[5:4] set to 10<sub>B</sub>. The host controller must send the same BG bits, Bank bits, and row address in the Activate command as it did for the most recent sPPR for this resource. The DRAM may ignore row address bits if it so chooses, as BG and BK bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For static efficiency mode devices, the SC bits should identify Sub-Channel information, and non-static efficiency mode devices should issue exact address information to each Sub-Channel. If the row address does NOT match that of the most recent sPPR to this resource, the DRAM may or may not perform the undo. Any required copying of data is the host controller's responsibility.

Following an sPPR Undo, a later sPPR may be done to assign the resource to a new or the same location. Data is retained in the sPPR resource, but it need not be refreshed by the DRAM. If the host controller requires the data to remain valid, it must send enough ACT commands to the row while it is mapped in to guarantee the data.

#### 7.8.17.2 sPPR Lock

sPPR Lock allows an sPPR resource to be locked in place. Locks are done to sPPR resources individually. Following an sPPR Lock, any sPPR or sPPR undo is blocked to that spare resource. A hardware reset or power cycle must be done to undo the lock. The hardware reset or power cycle must also be done before any hPPR operation can be done if any sPPR resources are locked.

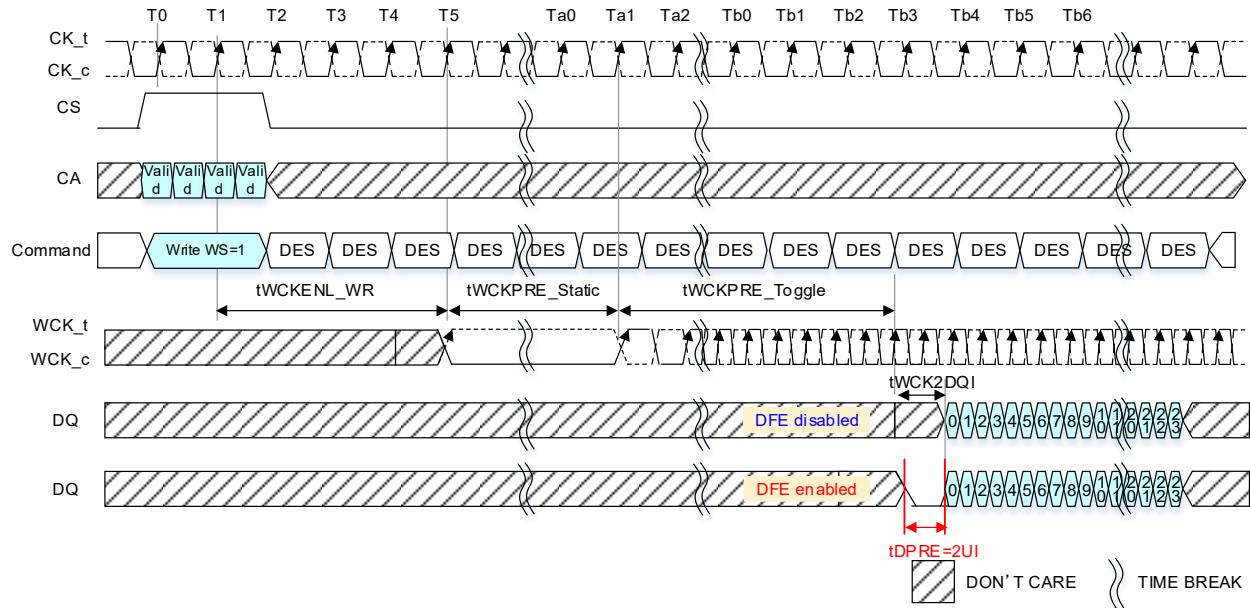
The sPPR Lock uses the same protocol as the sPPR function except that MR26 OP[5:4] is set to 11<sub>B</sub>. The Activate command must contain BG bits, bank bits and row address of the most recent for that resource. The DRAM may ignore the row address bits if it so chooses, as the BG and BK bits may be enough to uniquely identify the sPPR resource depending on number of repair elements. For static efficiency mode devices, the SC bits should identify Sub-Channel information, and non-static efficiency mode devices should issue exact address information to each Sub-Channel. If the row address does NOT match that of the most recent sPPR to this resource, the DRAM may or may not perform the lock.

### 7.8.18 Per-pin Controlled Decision Feedback Equalization (Pin-pin DFE)

LPDDR6 supports very high data rate over 9600bps. To compensate channel characteristics and enhanced signal integrity, equalization technique helps Rx margin. LPDDR6 provides advanced per-pin controlled Decision Feedback Equalization (DFE) for DQ Rx. Per-pin DFE is set by MR41 OP[0] and MR70 to MR75 are offset DFE quantity setting fields for each DQ and all Offset DFE Quantity for Per-pin DFE have negative feedback quantities for preventing inappropriate feedback direction setting. All Per-pin DFE quantity controller is allowed by FSP procedure.

If Per Pin DFE is enabled, tMRW\_L (stretched MODE Register Write command period) and tMRD\_L (stretched Mode Register set command delay) are required after issuing MRW command for MR41 and MR70~MR75.

To optimize per-pin variation and distortion of equalization effect, system can set each per-pin DFE quantity with MR70~MR75. Refer to Table 182 ~ Table 192 for detailed MR setting for Per-pin controlled DFE.



NOTE 1 tWCK2CK is in this instance.

NOTE 2 The end of both WL and tWCKPRE\_Toggle\_WR are the same timing in this instance.

**Figure 188 – Per-pin DFE Pre-Drive Requirement**

### 7.8.19 Single-ended Mode for Clock, Write Clock, and RDQS

LPDDR6 SDRAM supports the function of single-ended mode for Clock, Write Clock and Strobe independently to reduce power consumption during low frequency operation. The data rate is required to be equal or less than TBDMbps and ODT and NT ODT states for CK, CA, WCK, RDQS, and DQ are required to be unterminated during Single-ended mode for Clock, Write Clock and/or RDQS.

Entering and exiting single-ended mode for Clock, Write Clock and RDQS is controlled by the following MR setting.

MR1 OP[3]: CK mode

MR20 OP[1:0]: RDQS (Read DQS)

MR20 OP[3:2] : WCK mode

Single-ended mode for RDQS affects the following commands.

Read

Mode Register Read

Read DQ Training

Read FIFO

RDQS toggle mode

Enhanced RDQS training mode

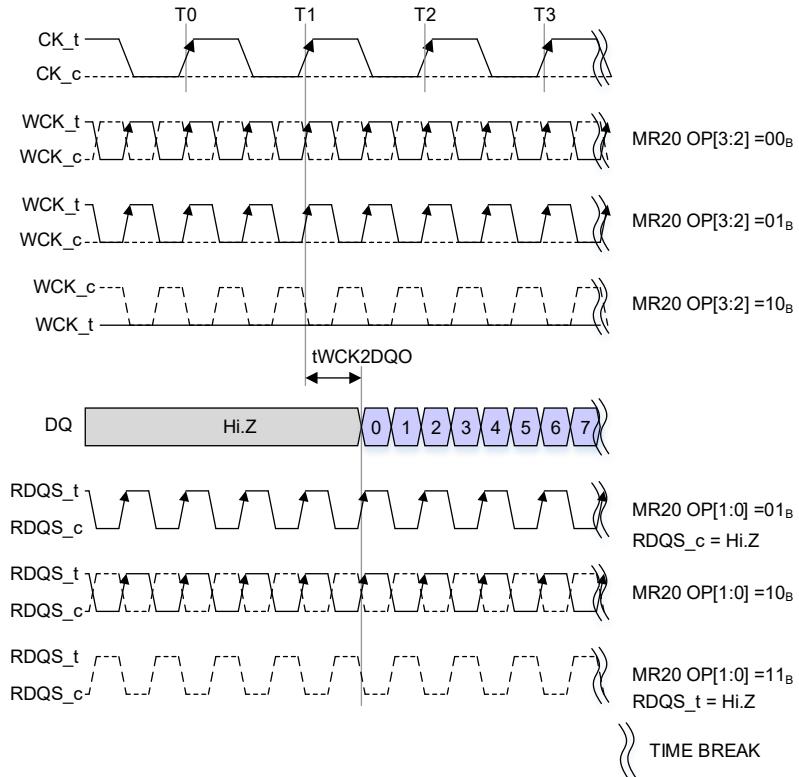
The allowable combinations for CK\_t/c, WCK\_t/c and RDQS\_t/c are shown in Table 351. The remaining combinations are inhibited.

**Table 351 – Allowable Combination among CK\_t/c, WCK\_t/c, and RDQS\_t/c**

CK_t	CK_c	WCK_t	WCK_c	RDQS_t	RDQS_c
Enable	Enable	Enable	Enable	Enable	Enable
Enable	Disable	Enable	Enable	Enable	Enable
		Enable	Disable	Enable	Disable
		Disable	Enable	Disable	Enable
		Enable	Disable	Disable	Disable

### 7.8.19.1 Relationship among CK, WCK, and RDQS during Single-ended Mode

The timing of WCK\_t/c and RDQS\_t/c is defined as shown in Figure 189



NOTE 1 tWCK2CK is 0 ps in this instance.

NOTE 2 tDQSQ is 0 ps in this instance.

NOTE 3 WCK clocking generates RDQS\_t and RDQS\_c.

NOTE 4 When MR20 OP[3:2]=01<sub>B</sub>, WCK\_t is used as WCK timing, and WCK\_c should be maintained at a valid logic level.

NOTE 5 When MR20 OP[3:2]=10<sub>B</sub>, WCK\_c is used as WCK timing, and WCK\_t should be maintained at a valid logic level.

NOTE 6 When MR20 OP[1:0]=01<sub>B</sub>, RDQS\_t is used as RDQS timing, and RDQS\_c should be Hi-Z state.

NOTE 7 When MR20 OP[1:0]=11<sub>B</sub>, RDQS\_c is used as RDQS timing, and RDQS\_t should be Hi-Z state.

NOTE 8 When MR20 OP[3:2]=01<sub>B</sub>, WCK\_t polarity is the same as WCK\_t in MR20 OP[3:2]=00<sub>B</sub>, and when MR20 OP[3:2]=10<sub>B</sub>, WCK\_c polarity is the same as WCK\_c in MR20 OP[3:2]=00<sub>B</sub>.

NOTE 9 When MR20 OP[1:0]=01<sub>B</sub>, RDQS\_t polarity is the same as RDQS\_t in MR20 OP[1:0]=10<sub>B</sub>, and when MR20 OP[1:0]=11<sub>B</sub>, RDQS\_c polarity is the same as RDQS\_c in MR20 OP[1:0]=10<sub>B</sub>.

**Figure 189 – Timing Relationship among CK, WCK, and RDQS**

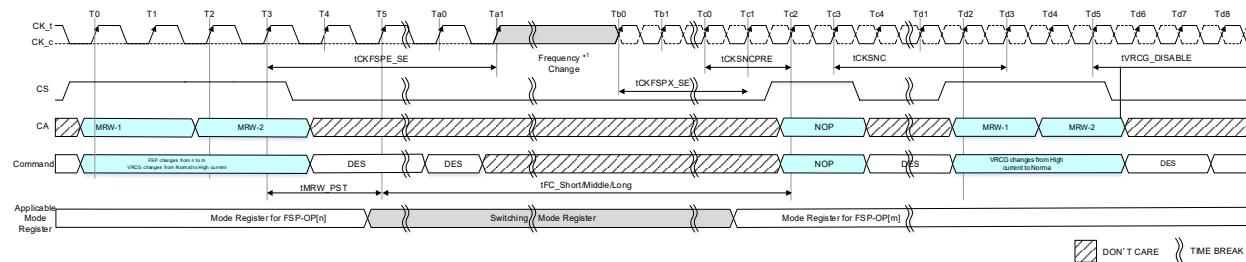
### 7.8.19.2 Switching Sequence between Single-ended and Differential

The mode switching for WCK and RDQS can be made by both an MR setting by MRW command and Frequency Set Point (FSP) procedure.

Switching the CK mode from differential to single ended and vice versa is done only via FSP procedure. The frequency set point update timing for Differential from/to Single-ended mode switching is shown in Figure 190.

When changing the frequency set point MR16 OP[3:2], the VRCG setting: MR16 OP[6] is required to be changed into VREF Fast Response (high current) mode at the same time. After frequency change time ( $t_{FC}$ ) is satisfied, VRCG can be changed into normal operation mode via MR16 OP[6].

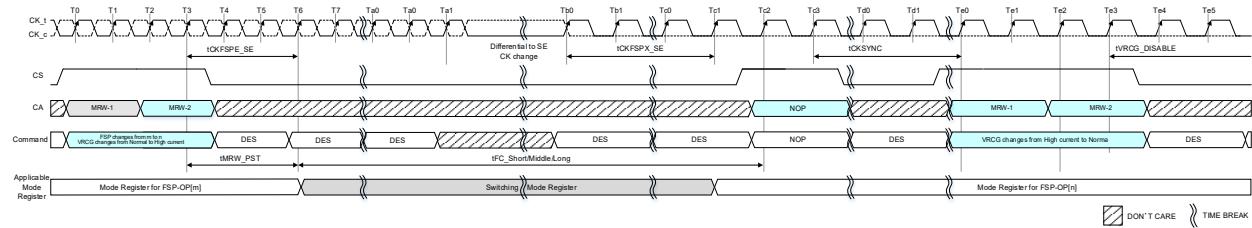
When CK mode switches via FSP procedure, additional timing period is needed after MRW command.



- NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to Input Clock Stop and Frequency Change.
- NOTE 2 CK\_c input level before Ta1 is an example. A stable high clock input is also allowed.
- NOTE 3 Mode Register Setting FSP-OP=n: MR1 OP[3]=1<sub>B</sub>: Single-Ended CK, Mode Register Setting FSP-OP=m: MR1 OP[3]=0<sub>B</sub>: Differential CK.
- NOTE 4 The CS input is required to be LOW from the rising edge of CK\_t (at cycle T3) until the rising edge of CK\_t at the end of tCKFSPX\_SE timing (Tc1).

**Figure 190 – SE to Differential CK and RDQS -FSP Switching Timing**

### 7.8.19.2 Switching Sequence between Single-ended and Differential (cont'd)

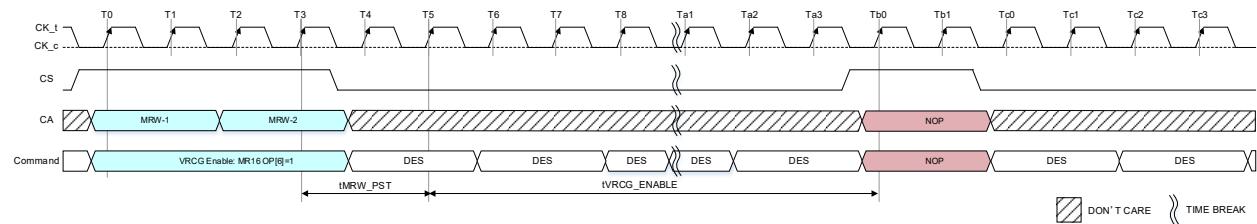


- NOTE 1 The Clock frequency change definition should follow the frequency change operation. For more information, refer to 7.8.6.
- NOTE 2 Clock input level after Tb0 is an example. A stable high clock input is also allowed.
- NOTE 3 Mode Register Setting FSP-OP=m: MR1 OP[3]=0<sub>B</sub>: Differential CK Mode Register Setting FSP-OP=m: MR1 OP[3]=1<sub>B</sub>: Single-Ended CK.
- NOTE 4 The CS input is required to be LOW from the rising edge of CK\_t (at cycle T2) until the rising edge of CK\_t at the end of tCKFSPX\_SE timing (Tc1).

**Figure 191 – Differential to SE CK and RDQS -FSP Switching Timing**

### 7.8.19.3 VRCG Enable Timing

The VRCG Enable timing is postponed 2 clocks after MRW command to remove the effect of VREF(CA) variation by VRCG mode change when MR1 OP[3]: Single ended Clock has been set 1<sub>B</sub> (Enable) at least one physical register is shown in Figure 192 and yyy.



**Figure 192 – VRCG Status Change to High Current Mode: Single-ended Clock Case**

### 7.8.19.3 VRCG Enable Timing (cont'd)

The AC timing, as shown in Table 352, is applied under conditions of Single ended mode.

**Table 352 – SE From/To Differential FSP and Additional Period for MRW AC Timing**

Parameter	Symbol	Min/ Max	Data Rate		Unit	Note	
			Equal to or less than TBD Mbps				
Frequency Set Point Parameters for Switching Single-ended from/to Differential Clock							
Valid Clock Requirement after entering FSP when changing between SE/Differential modes	tCKFSPE_SE	Min	Max(15ns, 8nCK)	-			
Valid Clock Requirement before first valid command after an FSP change between SE/Differential modes	tCKFSPX_SE	Min	Max(15ns, 8nCK)	-			
Additional period for after MRW command							
Post Clock for MRW	tMRW_PST	Min	4	nCK			

**Table 353 – Delta CK and DQS Specification**

Item	Min/ Max	Equal to or less than TBD Mbps	Unit	Note
Vref for single ended CK	-	VDDQ/2	-	
Vref for single ended WCK	-	VDDQ/2	-	
tClVWW_total	Min	0.35	UI	UI= 0.5tCK
tDlVWW_total	Min	0.35	UI	UI=0.5tWCK
tQSH	Min	tWCKH-0.10	tWCK(avg)	
tQLS	Min	tWCKL-0.10	tWCK(avg)	
tWCK2CK	Min	Max(-0.25*tWCK -100ps, TBDps)	ps	
	Max	Max(0.25*tWCK +100ps,TBDps)	ps	

### 7.8.20 LPDDR6 Temperature Sensor Read Out

LPDDR6 provides temperature sensor readout information as reference. Temperature is not located in the same area as memory array. Only limited position temperature is measured.

LPDDR temperature sensor cannot provide accurate enough temperature due to circuits and placement. SOC can use this information as temperature gradient information. Temperature accuracy is not guaranteed by design values.

Mode Register 109 is assigned for temperature sensor report. Please refer MR109 definition for more detailed information.

Mode register read out shows on-die temperature sensor value.

### 7.8.21 Selectable Link ECC/EDC

Selectable Link ECC/EDC is required to be supported by LPDDR6 SDRAM. Selectable Link ECC/EDC is not required to be supported or used by the Host; the Host may choose to support only Link ECC mode, only EDC Mode, or the Host may choose to not support any form of Selectable Link ECC/EDC Mode altogether.

The LPDDR6 SDRAM Link ECC/EDC Mode default state is not enabled; the Host must enable use of Selectable Link ECC/EDC when operation is desired. The Host may enable either Link ECC Mode or Link EDC Mode when the LPDDR6 DRAM is in Idle state and DQs are not driving data. The Host may switch the LPDDR6 DRAM between both modes disabled, Link ECC Mode enabled, and Link EDC Mode enabled when the LPDDR6 DRAM is in Idle state and DQs are not driving data. The time required to enable Link ECC/EDC mode or switch between the three states (Disabled, Link ECC enabled, or Link EDC enabled) shall be TBD.

The sixteen parity-bits required for Selectable Link ECC/EDC are generated using the same H-matrix whether operating in the Link ECC mode or Link EDC mode. The sixteen parity-bits are defined by a specific H-matrix (detailed in H-matrix section) and are allocated for Link ECC/EDC sequence as determined by the LPDDR6 data burst definition. The coverage for Selectable Link ECC/EDC Mode shall encompass 256-bits of transmitted data {payload data} and 16-bits of meta-data from System-Meta for a total of 272-bits covered by Link ECC or Link EDC error checking with the sixteen parity-bits.

The LPDDR6 DRAM shall implement control allowing the Host to be able to select between Write Link ECC and Write Link EDC mode for writes to the LPDDR6 DRAM. The LPDDR6 DRAM shall drive required parity bits during Read Selectable Link ECC/EDC.

If the Host elects to support Selectable Link ECC/EDC, the Host shall implement control to enable/disable and select between Link ECC mode and Link EDC mode during reads from the LPDDR6 DRAM. The Host shall drive required sixteen parity-bits during Write Selectable Link ECC/EDC if enabled.

When both Link ECC/EDC is enabled and System Meta {Carve Out} Mode is enabled, the 16-bits allocated for System Meta Mode data must be populated with known values. If the System Meta Mode function is not enabled, the 16-bits allocated for meta-data shall be zeros. If 16-bits allocated for System Meta Mode are not zeros (or valid meta-data), then Link ECC/EDC operation is uncertain and results are undefined.

#### 7.8.21.1 ECC Correction Mode

Selectable Link ECC/EDC when in the ECC Mode (MR23 OP[1:0] 01), shall correct SBE (Single Bit Error). The SBE and detected error correction attempts, i.e., aliased errors, shall be registered for Host notification as SBE correction. The remaining MBE (Multi-Bit Error) shall be registered for Host notification. The Link ECC H-matrix shall provide  $\geq 99.5\%$  MBE DC (Diagnostic Coverage).

Link ECC Mode Diagnostic Coverage:

SBE Correction	DBE Detection	MBE Detection
100%	100%	$\geq 99.5\%$

#### 7.8.21.2 EDC Detection Mode

Selectable Link ECC/EDC when in the EDC Mode (MR23 OP[1:0] 10), shall detect SBE (Single Bit Error) and MBE (Multi-Bit Error) and shall be registered for Host notification. The Link ECC H-matrix when in the EDC mode shall provide  $\geq 99.998\%$  SBE/MBE DC.

Link EDC Mode Diagnostic Coverage:

SBE Detection	DBE Detection	MBE Detection
100%	100%	$\geq 99.998\%$

#### 7.8.21.3 Selectable Link ECC/EDC H-Matrix

The H-matrix for Selectable Link ECC/EDC is 272+16 SEC ECC (sometimes referenced as 288,272) where 256-bits are allocated for payload data and 16-bits allocated for System-Meta data, while there are 16-parity bits for ECC/EDC H-matrix coding.

The Link ECC/EDC H-Matrix is shown in Appendix A (Table) and Appendix B (Algebraic) where D0 through D255 refers to payload data-bits defined in the Data-Packet, and M0 through M15 refers to meta-data for the System Carveout option defined by the Data-Packet; CB0 through CB15 are the parity check bits, sometimes referred to as check bits.

The EDC fault detection is generated by detecting any non-zero syndrome using the same H-matrix. The H-matrix meets or exceeds the Diagnostic Coverage limits stated in sections 2 and 3.

#### 7.8.21.4 Write ECC Fault Reporting

When Selectable Link ECC/EDC is in the Write Link ECC Mode, the DRAM shall register first occurrence of corrected SBE in MR97 OP[2] and subsequent occurrences shall be ignored unless MR97 OP[2] has been reset. The DRAM shall register first occurrence of uncorrected MBE in MR97 OP[1] and subsequent occurrences shall be ignored unless MR97 OP[1] has been reset. The Host may monitor MR97 OP[2:1] for fault status or Host may enable Faut Alert Control for notification of either or both faults real-time. When Write Link ECC/EDC is disable, the bit defined by MR97 OP[1] and MR97 OP[2] shall remain in the default state.

#### 7.8.21.5 Write EDC Fault Reporting

When Selectable Link ECC/EDC is in the Write Link EDC Mode, the DRAM shall register first occurrence of any detected error (all SBE and all MBE) in MR97 OP[1] and subsequent occurrences shall be ignored unless MR97 OP[1] has been reset

The Host may monitor MR97 OP[1] for fault status or Host may enable Faut Alert Control for notification of fault real-time. When Write Link ECC/EDC is disable, the bit defined by MR97 OP[1] shall remain in the default state.

### 7.8.21.6 Selectable Link ECC/EDC Operation

To be defined; pending completion of Data-burst sequence and feature multi-function allowance.

**Table 354 – MR23 Mode Register Definition**

Function	Register Type	Operand	Data	Notes
Write Link ECC Mode	Write	OP[0]	0 <sub>B</sub> : Not Enabled {default} 1 <sub>B</sub> : Enabled	1, 2
Write Link EDC Mode	Write	OP[1]	0 <sub>B</sub> : Not Enabled {default} 1 <sub>B</sub> : Enabled	1, 2
Read Link ECC/EDC Mode	Write	OP[2]	0 <sub>B</sub> : Not Enabled {default} 1 <sub>B</sub> : Enabled	1
TBD	RFU	OP[3]	0 <sub>B</sub> : RFU 1 <sub>B</sub> : RFU	
CS ODT PD (CS ODT behavior option on Power Down)	Write	OP[4]	0 <sub>B</sub> : CS ODT is disabled on Power Down (default) 1 <sub>B</sub> : CS ODT follows on MR setting (MR17 OP[5:3]) even though Power Down	
TBD	RFU	OP[5]	0 <sub>B</sub> : RFU 1 <sub>B</sub> : RFU	
TBD	RFU	OP[6]	0 <sub>B</sub> : RFU 1 <sub>B</sub> : RFU	
TBD	RFU	OP[7]	0 <sub>B</sub> : RFU 1 <sub>B</sub> : RFU	
NOTE 1 Write Link ECC/EDC process shall precede a valid Read Link ECC/EDC process; the write and read Link ECC/EDC shall be to the same DRAM address.				
NOTE 2 Write Link ECC and Write Link EDC shall not be enabled at the same time.				

### 7.8.21.7 Error Definitions

**SBE** = Single Bit Error: one single bit error per ECC code word; sometimes referred to as payload or mission data.

**DBE** = Double Bit Error: two single bit errors per ECC code word; sometimes referred to as payload or mission data.

**MBE** = Multi-Bit Error: two or more single bit errors per ECC code word; sometimes referred to as payload or mission data.

### 7.8.21.7 Error Definitions (cont'd)

#### Appendix A

DQ	BL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	D0			1				1	1								
1	D1				1			1	1								
2	D2					1		1	1								
3	D3						1	1	1								
4	D48					1	1			1							
5	D49					1	1			1							
6	D50					1	1				1						
7	D51					1	1				1						
8	D96	1						1	1								
9	D97	1						1	1								
10	D98		1					1	1								
11	D99		1					1	1								
12	D128			1				1	1								
13	D129			1				1	1								
14	D130				1			1	1								
15	D131					1		1	1								
16	D176					1	1	1	1								
17	D177					1	1	1	1								
18	D178					1	1	1	1								
19	D179					1	1	1	1								
20	D224	1						1	1								
21	D225	1						1	1								
22	D226		1					1	1								
23	D227		1					1	1								
0	D4			1				1	1								
1	D5			1				1	1								
2	D6				1			1	1								
3	D7				1			1	1								
4	D52					1		1	1								
5	D53					1		1	1								
6	D54					1		1	1		1						
7	D55					1		1	1			1					
8	D100	1				1		1	1								
9	D101	1				1		1	1								
10	D102		1			1		1	1								
11	D103		1			1		1	1								
12	D132			1				1	1								
13	D133				1			1	1								
14	D134					1		1	1								
15	D135						1	1	1								
16	D180						1	1	1								
17	D181						1	1	1								
18	D182						1	1	1								
19	D183						1	1	1								
20	D228	1						1	1								
21	D229	1						1	1								
22	D230		1					1	1								
23	D231		1					1	1								
0	D8			1				1	1								
1	D9				1			1	1								
2	D10				1			1	1								
3	D11					1		1	1								
4	D56					1		1	1								
5	D57					1		1	1								
6	D58					1		1	1								
7	D59					1		1	1								
8	D104	1						1	1								
9	D105	1						1	1								
10	D106		1					1	1								
11	D107		1					1	1								
12	D136			1				1	1								
13	D137				1			1	1								
14	D138					1		1	1								
15	D139						1	1	1								
16	D184						1	1	1								
17	D185						1	1	1								
18	D186						1	1	1								
19	D187						1	1	1								
20	D232	1						1	1								
21	D233	1						1	1								
22	D234		1					1	1								
23	D235		1					1	1								
0	D12	1	1					1	1								
1	D13	1	1					1	1								
2	D14	1	1					1	1								
3	D15	1	1						1								
4	D60	1	1							1							
5	D61	1	1								1						
6	D62	1	1									1					
7	D63	1	1										1				
8	D108	1	1						1								
9	D109	1	1							1							
10	D110	1	1								1						
11	D111	1	1									1					
12	D140		1	1													
13	D141		1	1													
14	D142		1	1													
15	D143		1	1													
16	D188		1														
17	D189		1														
18	D190		1														
19	D191		1														
20	D236		1														
21	D237		1														
22	D238		1														
23	D239		1														
0	D16	1						1	1								
1	D17	1							1								
2	D18	1								1							
3	D19	1									1						
4	D64	1										1					
5	D65	1											1				
6	D66	1												1			
7	D67	1													1		
8	M0	1														1	
9	M1	1															1
10	M2	1															1
11	M3	1															1
12	D144	1															1
13	D145	1															1
14	D146	1															1
15	D147	1															1
16	D192	1															1
17	D193	1															1
18	D194	1															1
19	D195	1															

### 7.8.21.7 Error Definitions (cont'd)

#### Appendix B

**CB0**=D96^D224^D100^D228^D104^D232^D12^D13^D14^D15^D60^D61^D62^D63^D108^D109^D110^D111^D16^D17^D18^D19^D64^D65^D66^D67^M0^M1^M2^M3^D148^D149^D150^D151^D196^D197^D198^D199^D24^D152^D28^D156^D32^D160^D36^D164^D40^D168^D44^D172

**CB1**=D97^D225^D101^D229^D105^D233^D12^D13^D14^D15^D60^D61^D62^D63^D108^D109^D110^D111^D144^D145^D146^D147^D192^D193^D194^D195^D20^D21^D22^D23^D68^D69^D70^D71^M4^M5^M6^M7^D25^D153^D29^D157^D33^D161^D37^D165^D41^D169^D45^D173

**CB2**=D98^D226^D102^D230^D106^D234^D140^D141^D142^D143^D188^D189^D190^D191^D236^D237^D238^D239^D144^D145^D146^D147^D192^D193^D194^D195^D148^D149^D150^D151^D196^D197^D198^D199^D26^D154^D30^D158^D34^D162^D38^D166^D42^D170^D46^D174

**CB3**=D99^D227^D103^D231^D107^D235^D140^D141^D142^D143^D188^D189^D190^D191^D236^D237^D238^D239^D16^D17^D18^D19^D64^D65^D66^D67^M0^M1^M2^M3^D20^D21^D22^D23^D68^D69^D70^D71^M4^M5^M6^M7^D27^D155^D31^D159^D35^D163^D39^D167^D43^D171^D47^D175

**CB4**=D0^D128^D4^D132^D8^D136^D12^D140^D16^D144^M4^D24^D25^D26^D27^D72^D73^D74^D75^D112^D113^D114^D115^D28^D29^D30^D31^D76^D77^D78^D79^D116^D117^D118^D119^D160^D161^D162^D163^D208^D209^D210^D211^D248^D249^D250^D251^D84^D212^D88^D216^D92^D220

**CB5**=D1^D129^D5^D133^D9^D137^D13^D141^D17^D145^M5^D24^D25^D26^D27^D72^D73^D74^D75^D112^D113^D114^D115^D156^D157^D158^D159^D204^D205^D206^D207^D244^D245^D246^D247^D32^D33^D34^D35^D80^D81^D82^D83^D120^D121^D122^D123^D85^D213^D89^D217^D93^D221

**CB6**=D2^D130^D6^D134^D10^D138^D14^D142^D18^D146^M6^D152^D153^D154^D155^D200^D201^D202^D203^D240^D241^D242^D243^D156^D157^D158^D159^D204^D205^D206^D207^D244^D245^D246^D247^D160^D161^D162^D163^D208^D209^D210^D211^D248^D249^D250^D251^D86^D214^D90^D218^D94^D222

**CB7**=D3^D131^D7^D135^D11^D139^D15^D143^D19^D147^M7^D152^D153^D154^D155^D200^D201^D202^D203^D240^D241^D242^D243^D28^D29^D30^D31^D76^D77^D78^D79^D116^D117^D118^D119^D32^D33^D34^D35^D80^D81^D82^D83^D120^D121^D122^D123^D87^D215^D91^D219^D95^D223

**CB8**=D0^D1^D2^D3^D48^D49^D50^D51^D96^D97^D98^D99^D4^D5^D6^D7^D52^D53^D54^D55^D100^D101^D102^D103^D136^D137^D138^D139^D184^D185^D186^D187^D232^D233^D234^D235^D108^D236^M0^D20^D148^D112^D240^D116^D244^D120^D248^D124^D252^M8^M12

**CB9**=D0^D1^D2^D3^D48^D49^D50^D51^D96^D97^D98^D99^D132^D133^D134^D135^D180^D181^D182^D183^D228^D229^D230^D231^D8^D9^D10^D11^D56^D57^D58^D59^D104^D105^D106^D107^D109^D237^M1^D21^D149^D113^D241^D117^D245^D121^D249^D125^D253^M9^M13

**CB10**=D128^D129^D130^D131^D176^D177^D178^D179^D224^D225^D226^D227^D132^D133^D134^D135^D180^D181^D182^D183^D228^D229^D230^D231^D136^D137^D138^D139^D184^D185^D186^D187^D232^D233^D234^D235^D110^D238^M2^D22^D150^D114^D242^D118^D246^D122^D250^D126^D254^M10^M14

### 7.8.21.7 Error Definitions (cont'd)

**CB11**=D128^D129^D130^D131^D176^D177^D178^D179^D224^D225^D226^D227^D4^D5^D6^D7^D52^D53^D54^D55^D100^D101^D102^D103^D8^D9^D10^D11^D56^D57^D58^D59^D104^D105^D106^D107^D111^D239^M3^D23^D151^D115^D243^D119^D247^D123^D251^D127^D255^M11^M15

**CB12**=D48^D176^D52^D180^D56^D184^D60^D188^D64^D192^D68^D196^D72^D200^D76^D204^D80^D208^D36^D37^D38^D39^D84^D85^D86^D87^D124^D125^D126^D127^D40^D41^D42^D43^D88^D89^D90^D91^M8^M9^M10^M11^D172^D173^D174^D175^D220^D221^D222^D223

**CB13**=D49^D177^D53^D181^D57^D185^D61^D189^D65^D193^D69^D197^D73^D201^D77^D205^D81^D209^D36^D37^D38^D39^D84^D85^D86^D87^D124^D125^D126^D127^D168^D169^D170^D171^D216^D217^D218^D219^D44^D45^D46^D47^D92^D93^D94^D95^M12^M13^M14^M15

**CB14**=D50^D178^D54^D182^D58^D186^D62^D190^D66^D194^D70^D198^D74^D202^D78^D206^D82^D210^D164^D165^D166^D167^D212^D213^D214^D215^D252^D253^D254^D255^D168^D169^D170^D171^D216^D217^D218^D219^D172^D173^D174^D175^D220^D221^D222^D223

**CB15**=D51^D179^D55^D183^D59^D187^D63^D191^D67^D195^D71^D199^D75^D203^D79^D207^D83^D211^D164^D165^D166^D167^D212^D213^D214^D215^D252^D253^D254^D255^D40^D41^D42^D43^D88^D89^D90^D91^M8^M9^M10^M11^D44^D45^D46^D47^D92^D93^D94^D95^M12^M13^M14^M15

### 7.8.22 Pre-Emphasis for DQ Output

LPDDR6 SDRAM supports beyond 6400 Mbps. At this kind of high data rate operation, we need to compensate for transmission loss during read operation.

LPDDR6 SDRAM features Pre-Emphasis for DQ to compensate transmission loss and the pre-emphasis applies above 6400 Mbps ( $> 6400$  Mbps). The Pre-Emphasis can be enabled by MR78~MR84.

The drive strength is boosted every time the bit transitions. And LPDDR6 SDRAM adopts 1-Tap and 1-Post-cursor Pre-Emphasis.

The Pre-Emphasis function applies to RDQS\_t/c too, if RDQS\_t/c output is enabled.

#### 7.8.22.1 Driver Strength of Pre-Emphasis

If Pre-emphasis is enabled, the driver strength looks like to have additional parallel driver. PDDS (Pull-Down Drive Strength) || Pre-PDDS (Pre-Emphasis Pull-Down Drive Strength) for example.

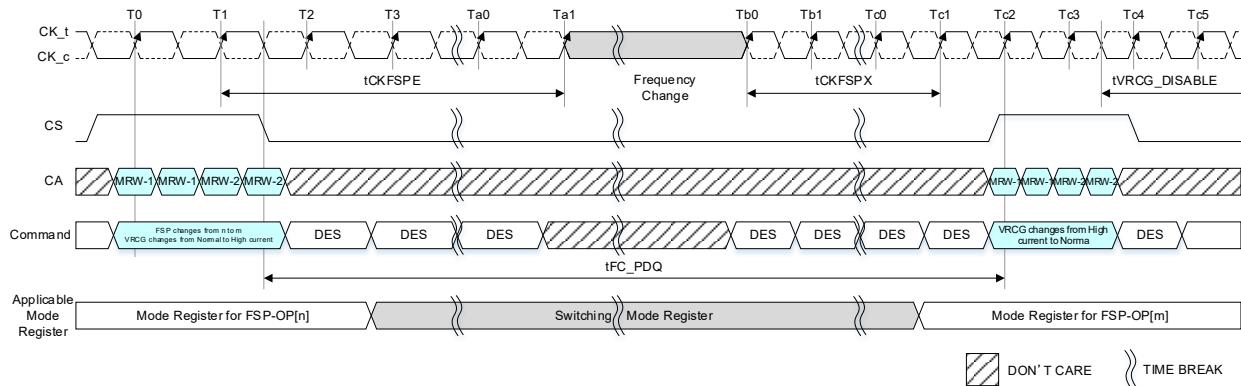
Additionally, Pull-Up/Down driver for Pre-Emphasis cannot train using ZQ calibration procedure.

#### 7.8.22.2 Mode Register Change Procedure

Following Mode Register change is only allowed FSP.

- MR[n+6:n]: Pre-Emphasis Pull-up/down Drive Strength for DQ[11:0] and RDQS\_t/c

And an Exclusive Frequency Set Point Switching Time (tFC\_PDQ) applies if including above-mentioned Mode Register change at FSP procedure.



**Figure 193 – Frequency Set Point Switching Timing for Per DQ Pre-Emphasis Change**

**Table 355 – Frequency Set Point AC Timing Table for Per DQ Pre-Emphasis Change**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			All Operating Frequency		
Frequency Set Point Switching Time for per DQ setting	tFC_PDQ	Min	TBD	ns	

### 7.8.23 LPDDR6 On-Die ECC

The LPDDR6 SDRAM shall support on-die ECC covering the array bits. The on-die ECC may be whatever type of ECC the DRAM manufacturer determines is to best support its design objectives. However, the MBE (multi-bit error) diagnostic coverage (DC) shall be available to Host.

#### 7.8.23.1 Error Definitions

**SBE** = Single Bit Error: one single bit error per ECC code word; sometimes referred to as payload or mission data.

**MBE** = Multi-Bit Error: two or more single bit errors per ECC code word; sometimes referred to as payload or mission data.

#### 7.8.23.2 ECC Diagnostic Coverage

The on-die ECC shall correct one bit error (SBE) detected in the ECC code word while more than one bit error detected in the ECC code word shall be classified as an uncorrectable MBE.

The LPDDR6 DRAM shall have on-die ECC with the ability to meet or exceed the following Diagnostics:

- 100% SBE correction
  - On-die ECC shall correct one bit error (SBE) detected in the ECC code word
- $\geq 95\%$  MBE detection
  - On-die ECC shall classify more than one bit error detected in the ECC code word as an uncorrectable MBE and the detected MBE shall be registered.

**Table 356 – On-Die ECC Diagnostic Coverage**

SBE Correction	MBE Detection
100%	$\geq 95\%$

#### 7.8.23.3 MBE Registration

The on-die ECC MBE detection shall be registered in MR97 OP[3].

## 7.8.24 Alert Output

### 7.8.24.1 Alert Signal

Alert is an output pin which signals fault status defined and controlled by MR97 {FMR1}, MR98 {FMR2}, MR99 {FMR3}, and MR100{FMR4} as determined in the Fault Register section.

### 7.8.24.2 Alert Output

The Alert output shall be inactive when the DRAM has not detected a fault condition. The Alert output will be Hi-Z when inactive and the Host shall provide termination to VSS.

The Alert output shall be active when the DRAM has detected a covered fault condition. The Alert output will drive high, to VDDQ, when active and the Host shall provide termination to VSS.

The DRAM pull-up driver strength is fixed at RZQ/6. The Host shall set the pull-down impedance(s), i.e., External Pulldown, to derive the desired VOH Level for both DVFSQ disabled and DVFSQ enabled states.

### 7.8.24.3 Alert Pull Up Driver Characteristics

Alert output pin driver characteristics are defined by the following tables.

**Table 357 – Alert Output Leakage Current**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output Leakage Current	OZ	-20	20	µA	1

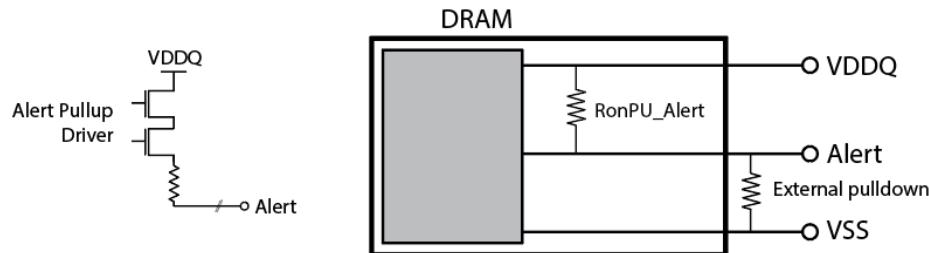
NOTE 1 Output status is disabled: High Impedance and ODT Off.

**Table 358 – Alert Output Driver Pullup Impedance – RonPU\_Alert**

RonPU_Alert	Vout	Min	Nom	Max
40 Ohm	0.5 * VDDQ	0.2	1	1.3

NOTE 1 All values are without ZQ calibration. {Fixed ZQcode applied to avoid hazard on Alert pin.}  
 NOTE 2 RonPU\_Alert impedance range is applicable whether DVFSQ is disabled or enabled.  
 NOTE 3 Vout assumes nominal VDDQ=0.5 V and VDD2C = 1.0 V; external pulldown with matching impedance.  
 NOTE 4 VOH level is dependent on Host on pull-down resistance, i.e., External Pulldown. The Signal integrity of the channel between the DRAM and the DRAM Host should be confirmed during simulation and design effort.

### 7.8.24.4 DRAM Alert Output Driver with Alert Equivalent Circuit



### 7.8.24.5 VOH calculations

Alert VOH at Host can be determined by:

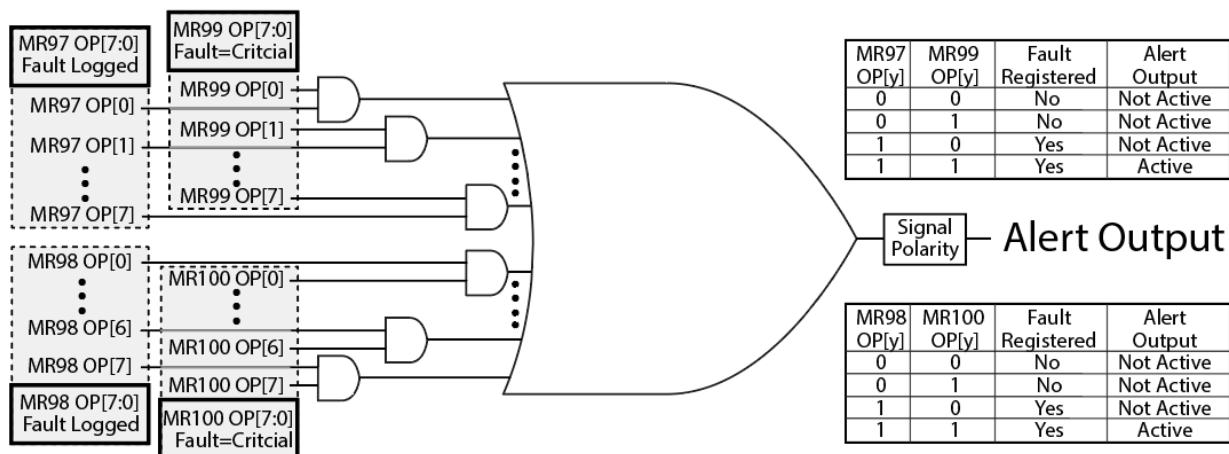
$$VOH = (VDDQ * \text{External Pulldown}) / (\text{RonPU}_\text{Alert} + \text{External Pulldown})$$

## 7.8.25 Fault Registers

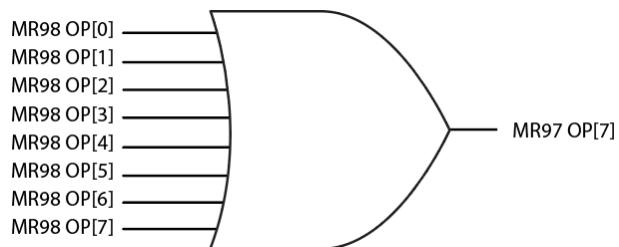
### 7.8.25.1 Fault Registers

Two Fault Registers, MR97 and MR98 register up to 15 functions when fault(s) is detected by covered function. Fault Registers MR97 and MR98 shall be default low and remain low unless a covered function has a detected fault and sets associated register bit high. The affected Fault Registers' bit(s) retain their fault status until either (1) affected register is read from, (2) RESET command applied, or (3) power is removed.

The supported functions, when enabled via MR99 and MR100, control the Alert Output when a fault occurs. FMR3 and FMR4 may be written to when the DRAM is in idle state and no data is driven. The Alert Output is driven active, asynchronously, upon fault occurrence and remains active until either (1) affected MR97 and/or MR98 is read from, with one exception; MR97 OP[0] clearing is controlled by PRAC operation and will clear as defined by PRAC Alert Back-Off protocol (ABO), (2) RESET command applied, or (3) power is removed. The logical diagram below depicts the functionality.



Fault Register MR97 OP[7] is derived by OR'ing MR98 OP[7:0], logical diagram below depicts this functionality. When Host interrogates MR97 and if MR97 OP[7] is low then Host does not need to read MR98.



### 7.8.25.2 Fault Register Definitions

Fault Registers MR97 and MR98 define which functions register fault occurrence. These Functions are not required to be supported by LPDDR6 DRAM; however, if a Function is supported, it shall use the defined register bit. MR97 and MR98 are default low and remain low unless a covered function has a detected fault and sets associated register bit high. The affected Fault Registers' bit(s) retain their fault status until either (1) register is read from (MR97 OP[7] is not required to be reset by MRR command, MR97 OP[7] may be cleared by clearing of MR98), (2) RESET command applied, or (3) power is removed.

### 7.8.25.2 Fault Register Definitions (cont'd)

**Table 359 – MR97 {FMR1} Mode Register Definition**

Function	Register Type	Operand	Data	Notes
PRAC limit exceeded	Read	OP[0]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Write Link ECC MBE Fault / Write Link EDC SBE/MBE Fault	Read	OP[1]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Write Link ECC SBE Correction Attempted	Read	OP[2]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
On-die ECC MBE Fault	Read	OP[3]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
TBD	Read	OP[4]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
CA Parity Fault	Read	OP[5]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
TBD	Read	OP[6]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
Sum of MR98 OP[7:0]	Read	OP[7]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	1
NOTE 1 FMR1 OP[7] is sum of FMR2 OP[7:0]				

**Table 360 – MR98 {FMR2} Mode Register Definition**

Function	Register Type	Operand	Data	Notes
RFU	Read	OP[0]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[1]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[2]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[3]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[4]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[5]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[6]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	
RFU	Read	OP[7]	0 <sub>B</sub> : Fault not detected 1 <sub>B</sub> : Fault detected	

### 7.8.25.3 Fault Alert Control

The two registers, MR99 and MR100, control which functions with registered faults affect the Alert Output status. MR99 and MR100 are default low and remain low until written to; these two MR registers may be written to when the DRAM is in idle state and no data is driven. These two registers retain set values until either (1) rewritten to different state (2) RESET command applied, or (3) power is removed.

**Table 361 – MR99 {FMR3} Mode Register Definition**

Function	Register Type	Operand	Data	Notes
PRAC limit exceeded	Write	OP[0]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
Write Link ECC MBE Fault/ Write Link EDC SBE/MBE Fault	Write	OP[1]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
Write Link ECC SBE Correction Attempted	Write	OP[2]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
On-die ECC MBE Fault	Write	OP[3]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
TBD	Write	OP[4]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
CA Parity Fault	Write	OP[5]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
TBD	Write	OP[6]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	
Sum of FMR2 OP[7:0]	Write	OP[7]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	

NOTE 1 MR99 OP[0] Controls if PRAC ABO Protocol drives ALERT active.

**Table 362 – MR100 {FMR4} Mode Register Definition**

Function	Register Type	Operand	Data	Notes
RFU	Write	OP[0]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[1]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[2]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[3]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[4]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[5]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[6]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1
RFU	Write	OP[7]	0 <sub>B</sub> : Fault does not affect Alert Output 1 <sub>B</sub> : Fault affects Alert Output	1

NOTE 1 MR99 OP[7] set to 0B overrides MR100 OP[7:0] and prevents MR100 OP[7:0] from affecting Alert Output.

#### 7.8.25.4 Fault to Alert Timing

The timing for fault occurrence to detection and notification is defined in Table 363.

**Table 363 — Fault Timing**

Function	Operand	Detection to valid MRR	Valid MRR to Alert Output	Notes
PRAC limit exceeded	MR97 OP[0]	$t \leq \text{Max (85nCK or 10nCK+500ns)}$		1
Write Link ECC MBE Fault	MR97 OP[1]	$\leq WL + BL/n + 2nCK + RU(13ns/tCK)$	$\leq 9ns/tCK$	2
Write Link EDC SBE/MBE Fault	MR97 OP[1]	$\leq WL + BL/n + 2nCK + RU(13ns/tCK)$	$\leq 9ns/tCK$	2
Write Link ECC SBE Correction Attempted	MR97 OP[2]	$\leq WL + BL/n + 2nCK + RU(13ns/tCK)$	$\leq 9ns/tCK$	2
On-die ECC MBE Fault	MR97 OP[3]	$\leq RL + RU(4ns/tCK)$	$\leq 9ns/tCK$	2
TBD	MR97 OP[4]	tbd	tbd	
CA Parity Fault	MR97 OP[5]	$\leq \text{Max (2nCK or 8ns/tCK)}$	$\leq 9ns/tCK$	2
TBD	MR97 OP[6]	tbd	tbd	
Sum of FMR2 MR98 OP[7:0]	MR97 OP[7]	na	$\leq 9ns/tCK$	
RFU	MR98 OP[0]	tbd	na	
RFU	MR98 OP[1]	tbd	na	
RFU	MR98 OP[2]	tbd	na	
RFU	MR98 OP[3]	tbd	na	
RFU	MR98 OP[4]	tbd	na	
RFU	MR98 OP[5]	tbd	na	
RFU	MR98 OP[6]	tbd	na	
RFU	MR98 OP[7]	tbd	na	
NOTE 1 Triggering: Several events can trigger PRAC limit exceeded, large variation required since relationship is asynchronous.				
NOTE 2 The 2nd CK rising edge is timing reference; that is, CK rising (R2) of error command.				

The time for clearing fault from Alert Output shall be

- If MR97 OP[7] is 0 then time required for TBD
- If MR97 OP[7] is 1 then time required for TBD

#### 7.8.25.5 Error Definitions

**SBE:** Single Bit Error: one single bit error per ECC code word; sometimes referred to as payload or mission data.

**DBE:** Double Bit Error: two single bit errors per ECC code word; sometimes referred to as payload or mission data.

**MBE:** Multi-Bit Error: two or more single bit errors per ECC code word; sometimes referred to as payload or mission data.

## 7.8.26 CA Parity Check Mode

### 7.8.26.1 Overview

CA Parity Check Mode, aka CA parity, is an optional LPDDR6 DRAM feature. If CA parity is supported, CA Parity may either be disabled {default} or enabled by the Host. WCK Always ON mode must be set active when CA parity is enabled. When CA Parity is enabled, the Host generates an even bit parity based on the 1st and 2nd rising and falling edges of CA[3:0] signals, excluding the CA Parity bit. Host issues the CA Parity state to the DRAM on the 1st rising edge of CA3 except for CAS command which uses the 2nd rising edge of CA3.

When CA Parity is enabled, DRAM computes parity state on the same captured CA[3:0] signals the Host generated its parity state from and compares the two CA Parity states. If the two CA Parity states do not match, then a fault state, "1" is sent to CA Parity Fault Register, MR97 OP[5]. Once MR97 OP[5] is set to a '1', it shall remain a "1" until cleared as defined by the MR97 specifications: MR97 OP[5] retains its fault status until either.

- 1) Register is read from (MRR MR97), or
- 2) RESET command applied, or
- 3) Power is removed.

Additionally, when CA Parity mode is enabled, "X" defined by the command truth table shall be replaced to "V" (Valid) except DES command. Since Valid (high or low) level command input is required to compute the parity state.

When the parity error condition occurs, DRAM will log received CA bus data in MR125 OP[7:0] and MR126 OP[7:0]. Only the 1st error is logged, and subsequent error logging is ignored until the CA burst error logs are read from. The DRAM will allow update to MR125 and MR126 for subsequent error when MR126 is read via MRR.

The CA Parity operation requires MR99 OP[5] set to a "1" when CA Parity is enabled if the DRAM is required to have a CA Parity fault drive the Alert signal active. The Alert signal will go active by the time tPAR\_ALERT\_ON occurs after the DRAM captured the CA parity bit identifying the fault. The Alert signal shall remain active until MR97 OP[7:0], MR98 OP[7:0] if applicable, are cleared.

### 7.8.26.1 Overview (cont'd)

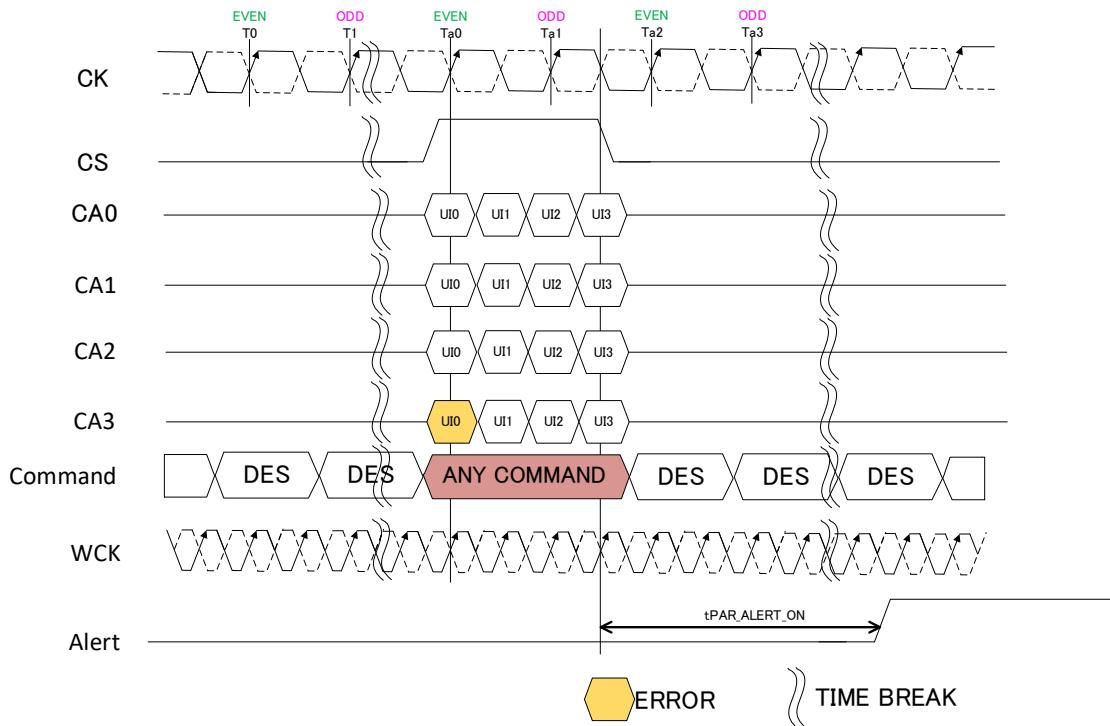


Figure 194 – CA Parity Alert Signal Active Timing

### 7.8.26.2 Specification

- Host shall read MR2 OP[0] to confirm CA Parity mode is supported
- DRAM must be in idle state when CA Parity mode is enabled or disabled
- CA Parity mode cannot be switched on-the-fly
- CA Parity mode is enabled/disabled with MR26 OP[2]
  - WCK Always-ON mode must be enabled prior to enabling CA Parity mode
- CA Parity fault driving Alert flag is enabled/disabled with MR99 OP[5]
- Host sends even bit parity for CA[3:0], 1st rising, 1st falling, 2nd rising and 2nd falling edges, excluding the CA Parity bit, on CA3 2nd rising edge.
- DRAM will compute the parity on the same captured CA[3:0] and compare the two
  - If two parity states do not match, then log "1" to CA Parity MR97 OP[5]
  - If two parity states do not match and this is the 1st instance of a parity error (i.e., MR97 OP[5] is 0), the received CA bus data is logged in MR125 and MR126.
- Host may poll MR97 OP[5] periodically or the Host may have the Alert go active to signal the CA parity error via an MRR to MR97 OP[5]
- Host should take appropriate action to resolve CA Parity Fault

Table 364 – CA Parity Error and Alert Toggle Timing

Parameter	Description	Value (ns)		Notes
tPAR_Alert_ON	Timing delay between CA Parity error and Alert toggle	Min	Max	
		TBD	TBD	

## 7.8.27 Per Row Activation Counting (PRAC)

### 7.8.27.1 Introduction

LPDDR6 SDRAM provides Per Row Activation Counting (PRAC) for data integrity. This feature detects row activity that may adversely affect the data stored in cells on physically adjacent rows within the DRAM.

The intended implementation for PRAC is to add Activation Counter bits to every row in the DRAM. These bits store a count associated with the number of received activations for a row since the last time it was refreshed. Activations to a row include the ACT command and may include REF and RFM commands.

### 7.8.27.2 Activation Counter Initialization (ACI)

Upon power-up or any time that DRAM refresh requirements are violated, the Activation Counter bits may be in an unknown state, requiring an initialization to put the bits into a known state.

Prior to use of Activation Counter bits, a full array Activation Counter Initialization (ACI) must be performed. The DRAM will not track activation counts, nor issue an Alert Back-Off (ABO), until the Activation Counter bits are initialized.

To initialize the Activation Counter bits, the host sets MR85 OP[2]=1<sub>B</sub> to indicate to the DRAM that a full array refresh will take place. Only REF and MRR commands are permitted during initialization. Upon completion of a full refresh cycle, the DRAM indicates completion by setting MR85 OP[3]=1<sub>B</sub>, which the host then follows by setting MR85 OP[2]=0<sub>B</sub>. The DRAM starts counting activations from that point forward and issues the ABO as necessary.

During ACI, the DRAM does not need to refresh the main array, and any data previously written may be corrupted. If the host reenters ACI by setting MR85 OP[2]=1<sub>B</sub>, the DRAM will reset MR85 OP[3]=0<sub>B</sub> before the initialization has been completed.

Like normal DRAM cells, the Activation Counter bits require refresh to maintain the stored values. Any time refresh is violated during ACI or after ACI, the ACI shall be performed again by the host to set the Activation Counter bits to a known state. Since array data is also corrupted by refresh violations, previous Activation Counter values become irrelevant.

### 7.8.27.3 Per Row Activation Counting Core Timing Parameters

PRAC requires additional counter cells per row in the DRAM to store Activation (ACT) command counts. Updating the activation counter cells requires a read-modify-write to the activation counter cells, known as Activation Counter Update (ACU), resulting in a change in some of the core timing parameters.

Examples of the timings affected by the updating of the activation counter bits are shown below. The “i” references DRAM internal commands, not external commands issued by the Host.

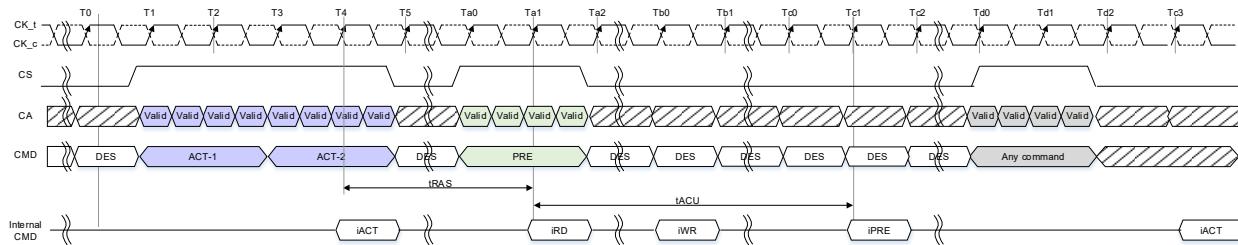


Figure 195 – Example ACT-PRE with ACU

### 7.8.27.3.1 Precharge Timing

Unlike the traditional Precharge (PRE) command, the PRAC PRE initiates an internal read (iRD) followed by an internal write (iWR) to increment the Activation Counting bits for all open rows affected by the PRE command.

### 7.8.27.4 Per Row Activation Counting Response

Since the DRAM is counting ACT commands on a per row basis, back-off action may shall be required upon one or more rows reaching a counter threshold level or levels, or when registers holding row addresses for targeted refreshing reaches or passes a critical level. This back-off action is a request by the DRAM for the host to pause normal activity for a recovery period so that refresh management (RFM) commands or other functions shall be performed. The back-off protocol is described in the next clause.

The counter and/or register threshold level(s) may be changed (reduced) by setting the Adaptive Per Row Activation Counting level in MR86 OP[3:2] to something other than the default MR86 OP[3:2]=00<sub>B</sub>. These alternate levels are based on the default starting value. The threshold level(s) reductions are approximately Level A = default - 10%, Level B = default - 20%, and Level C = default - 30%. Changing levels requires an ACI or full array refresh to set/reset all counters to a known state below critical threshold levels and to empty the registers.

In addition to the back-off which is required to keep activation counts from exceeding the threshold level, the DRAM should proactively perform targeted refreshes during Refresh Management (RFM) and/or Refresh (REF) commands to reduce and/or prevent the occurrence of the Alert Back-Off being triggered.

The host should track the level of activity that occurs on a per-bank basis.

When the Bank Activation Threshold (BAT) is reached (shown in Table 365), the RFMpb or RFMab command is issued. For bank activation, counting is done for every ACT, and additional count is also added by dividing the activation time by tRC to account for long tRAS. The duration of the RFM command (tRFM) is sufficient for the Row Refresh Span of +/-1 and +/-2 physically adjacent rows and the target row to be refreshed. Each Row Refresh Span is determined as tRRFab and tRRFpb.

**Table 365 – Bank Activation Threshold (BAT)**

Parameter	Symbol	Value	Unit	Notes
Bank Activation Threshold	BAT	TBD	Activations	

**Table 366 – Per Row Refresh Timing**

Parameter	Symbol	Value	Unit	Notes
All bank Per Row Refresh	tRRFab(min)	80	ns	
Per bank Per Row Refresh	tRRFpb(min)	70	ns	

**Table 367 – Refresh Management Command Timing**

Parameter	Symbol	Value	Unit	Notes
All bank RFM(RFMab)	tRFMab(min)	(4+1) * tRRFab	ns	
Per bank RFM(RFMpb)	tRFMpb(min)	(4+1) * tRRFpb	ns	

#### 7.8.27.4 Per Row Activation Counting Response (cont'd)

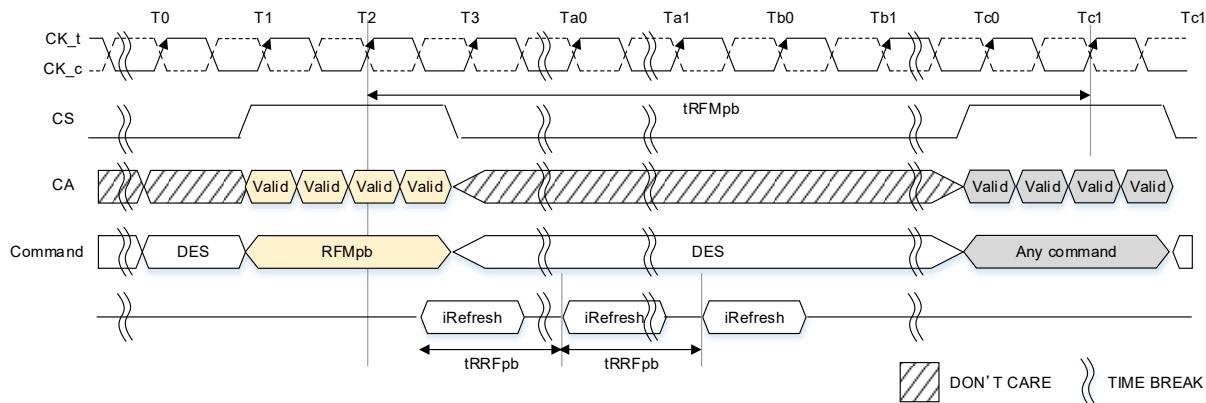


Figure 196 – tRRF Timing Definition

#### 7.8.27.5 Back-Off Protocol

LPDDR6 devices support PRAC for monitoring per row activity to ensure all rows are refreshed as needed to maintain data integrity. To facilitate the refresh activity, the DRAM requests the host to pause normal activity for a maintenance period where refresh management (RFM) commands or other functions may be performed. This is called a “back-off”.

##### 7.8.27.5.1 Alert Back-Off Protocol

The LPDDR6 back-off protocol uses the ALERT signal and mode register settings to provide a handshake between the DRAM and the host. This is the Alert Back-Off (ABO).

###### 7.8.27.5.1.1 PRAC Triggered Alert Back-Off

ABO protocol is enabled, upon reaching critical threshold levels by one or more rows, or when registers holding addresses for targeted refreshing reaches or passes a critical level, the DRAM asserts ALERT and sets the ABO Flag at MR85 OP[5]=1<sub>B</sub>, indicating that ALERT was asserted due to additional refresh management (RFM) being required. All commands received by the DRAM are executed while ALERT is asserted to maintain synchronization between sub-channels in a channel.

Commands that may trigger the ABO include PREab/PREPb, REFab/REFdb and RFMab/RFMpb. ALERT will be asserted between issuing the trigger command and before the max (5ns, 10nCK) following the completion of the respective command duration (PREab/PREPb=tRP, REFab/REFdb=tRFC, RFMab/RFMpb=tRFM).

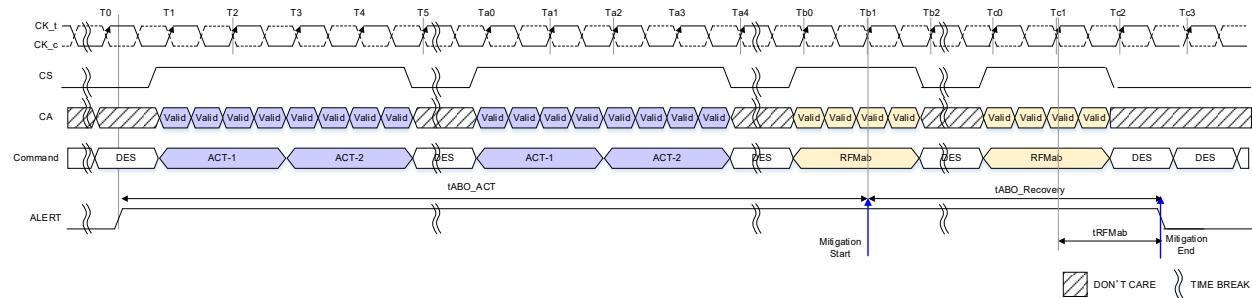
###### 7.8.27.5.1.2 Alert Back-off

To instantiate the ABO, ALERT\_n is asserted by the DRAM with a fixed duration of clock cycles as defined by tABO\_PW.

Table 368 – Alert Back-off Timing

Symbol	Symbol	Max/Min /Typ	Value	Unit	Notes
tABO_PW	Alert Back-off pulse width	Typ	tABO_ACT + tABO_Recovery	ns	
tABO_ACT	Normal traffic to the DRAM Allowed	Max	180	ns	

### 7.8.27.5.1.2 Alert Back-off (cont'd)



**Figure 197 – ABO: MRFMaACT=2 Case(MR86 OP[1:0]=01b)**

After the ALERT is asserted, a bounded number of Activate (ACT) commands are permitted before the host starts the RFM-based recovery period. Issuing ACT commands along with normal traffic is allowed within the tABO\_ACT window.

At the end of the tABO\_ACT window, the host begins issuing Refresh Management (RFM) commands. The only RFM command allowed during the tABO\_Recovery period is RFMab. The duration of the RFMab command is described in the previous clause (Per Row Activation Counting Response). The number of RFMab commands required to be issued per ABO maintenance period is defined by mode register ABO\_RFMs bits, MR86 OP[1:0]. Systems that have stricter requirements for isochronous bandwidth may limit the number of RFMab commands by setting MR86 OP[1:0] to a lower value.

The recovery period begins when the host issues the first RFMab command in response to ALERT. The DRAM self-clears the ABO flag by setting MR85 OP[5]=0<sub>B</sub> by the end of the tABO\_Recovery period, which ends tRFMab after the last RFMab command.

If additional RFM commands are needed, the ABO protocol is restarted following the ABO delay, as described below.

During the ABO\_Recovery period, a host can issue only RFMab, REFab/REFdb, PDE, PDX, SRE, PREab and MRR commands.

Refresh commands issued are to ensure that DRAM refresh requirements are not violated. The Refresh commands do not perform any of the refresh management required.

Power Down Entry and Exit (PDE, PDX) and Self Refresh Entry and Exit (SRE, SRX) are allowed during recovery period.

In Self Refresh, the DRAM de-asserts ALERT. Upon exiting Self Refresh, the DRAM will reevaluate and issue a new ALERT if ABO is still needed. In Power Down, the DRAM still keeps the current ALERT state.

### 7.8.27.5.1.3 Alert Back-off Delays

ABO\_Delay defines an interval in which DRAM shall service a minimum number of Activate commands before it can reassert ALERT for another ABO.

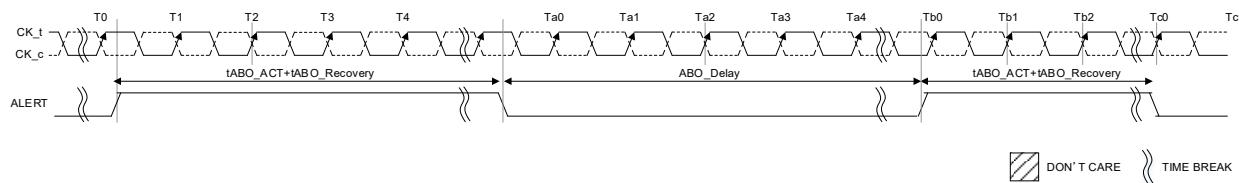
ABO\_Delay is specified by the number of Activate commands in MR86 OP[1:0].

Following ABO\_Delay, any of the commands included in section 7.8.27.5.1.1 may trigger the ABO, as well as an ACT command.

ALERT Pin is shared between sub-channels in a channel, but parameters associated with ABO (tABO\_ACT, tABO\_PW, tABO\_Recovery, ABO\_Delay) are independent per sub-channel.

**Table 369 – Alert Back-Off Delay Parameter**

Parameter	Symbol	Value	Unit	Notes
ABO_Delay	Minimum number of Activation Commands allowed per bank prior to reassert ALERT	MR86 OP[1:0]	Activations	



**Figure 198 – Bank to Back Alert Back-Off Delay**

### 7.8.27.6 Activation Counter Errors

The DRAM has the capability to detect errors that occur within the counter bits, and the following protocol defines how the DRAM will report the associated failing row address to the host.

If a counter bit error is detected, the DRAM sets the Counter Error Flag, MR85 OP[0]=1<sub>B</sub>.

While the Counter Error Flag is set, the counter function for the specific row with the error is disabled. The DRAM will not assert the ABO to request RFM commands for errors associated with that row. All other rows without counter errors continue to count activity and assert ALERT, if necessary.

A counter RAS error that occurs during the ECS triggers the Counter Error Flag, set the Counter Address Report Flag and report the failing row address.

The host clears the Counter Error Flag and Counter Address Report Flag, once the necessary information about the failing row has been collected and mitigative actions has been taken.

### 7.8.27.7 Per Row Activation Counting Testing

An optional test mode for PRAC may be included to check the ability of the DRAM to reach a threshold per row or fill the row address registers and issue the ABO. Test mode support is indicated by MR86 OP[4]=1<sub>B</sub>.

PRAC Testing is activated by setting MR86 OP[5]=1<sub>B</sub>. Once enabled, the counter for a target row to be tested is initialized by the host setting MR86 OP[6]=1<sub>B</sub>, followed by an ACT/PRE to the target row. The host then sets MR86 OP[6]=0<sub>B</sub> and issues 32 Activations or fewer to the target row or rows to trigger the ABO (multiple increments to the counter bits may occur depending on tRAS duration, mimicking normal operation). ABO is required as described previously before testing subsequent rows.

Depending on counter bit starting values, all DRAMs on a Package may not trigger the ABO at the same time (detected by MR85 OP[5]), however all DRAMs will trigger within 32 Activations. After PRAC Testing has been completed, the test mode is cleared by setting MR86 OP[5]=0<sub>B</sub>. Since the counter cells will be in an unknown state following testing, a full ACI is required before resuming normal operations. Data in normal cells are not maintained during PRAC Testing.

### 7.8.27.8 Alert Verification

Support for an optional mode to verify ALERT is indicated by MR85 OP[6]=1<sub>B</sub>. ALERT Verification is triggered by setting MR85 OP[7]=1<sub>B</sub>. The DRAM asserts ALERT and sets the ABO Flag at MR85 OP[5]=1<sub>B</sub> within tMRD after the MRW and will keep ALERT asserted for tABO\_PW. The host shall follow all normal ABO procedures for clearing the ALERT. MR85 OP[7] and MR85 OP[5] will be self-cleared by the DRAM prior to the end of the tABO\_Recovery period. Data in normal cells are maintained during ALERT Verification, as long as refresh is maintained. No per row counter values nor thresholds are altered during this mode.

### 7.8.28 Error Check and Scrub (ECS)

LPDDR6 Error Check and Scrub (ECS) feature as optional feature which can indicated by MR111 OP[0] for Auto ECS and MR111 OP[5] for Manual ECS. LPDDR6 support two different ECS mode which are auto ECS and manual ECS. Two different ECS mode only can be exclusively enabled and its mode should be changed after device RESET or ECS Reset. ECS shall be programmed during DRAM initialization and shall not be changed once the first ECS operation occurs unless followed by an ECS reset, otherwise an unknown operation could result during subsequent ECS operations.

ECS allows the DRAM to internally read, detect errors, correct errors, and write back corrected data bits to the array (scrub errors). Any errors corrected by on-die ECC during ECS must be logged in the transparency registers according to the rules described in this section.

During ECS, the internal Read-Modify-Write cycle will:

- 1) Read the entire code-word(s) from the DRAM array.
- 2) If the ECC engine detects a correctable error, the error will be corrected, and code-word(s) will be written back to DRAM.
- 3) If an error is detected in the code-word(s) and is uncorrectable, the bits in the code-word(s) will not be modified. The code-word(s) must not be written back to DRAM.
- 4) If the ECC engine detects no error, the DRAM may choose to write the resultant code-word(s) back to DRAM or not.

The DRAM can only guarantee valid ECS operations if array bits are written to prior to enabling ECS operations, thus enabling DRAM to calculate the proper initial parity bits

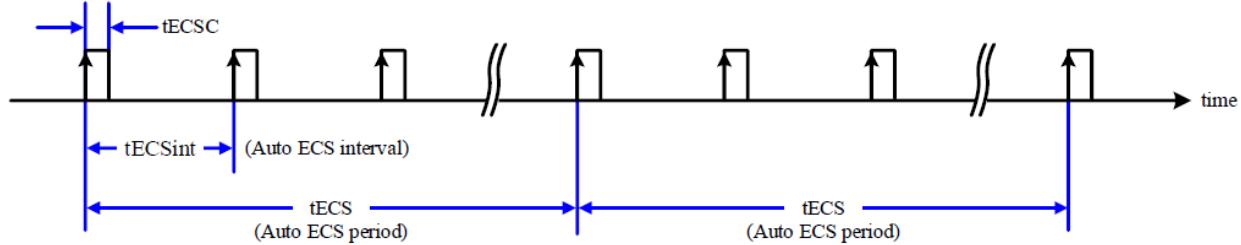
**Table 370 – MR111 Definition for ECS**

Function	Register Type	Operand	Data	Notes
Auto ECS On	Write-Only	OP[0]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Enabled	1
ECS Reset		OP[1]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Reset (bit is self-clearing)	2
ECS Flag Reset		OP[2]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Reset (bit is self-clearing)	2
ECS Log Rules		OP[3]	0 <sub>B</sub> : Maintain 1 <sub>B</sub> : Overwrite	
Auto ECS State Entry		OP[4]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Enabled	3
Manual ECS On		OP[5]	0 <sub>B</sub> : Disabled (default) 1 <sub>B</sub> : Enabled	1
RFU	N/A	OP[7:6]	RFU	
NOTE 1 Auto ECS On (MR111 OP[0]) and Manual ECS On(MR111 OP[5]) are mutually exclusive. NOTE 2 The bit is self-clearing in Table 370 means that it returns to the value 0B after the reset has been issued. NOTE 3 When Auto ECS On (MR111 OP[0]=1 <sub>B</sub> ) is enabled, the host needs to use Auto ECS State Entry (MR111 OP[4]=1 <sub>B</sub> ) for Auto ECS operation. If Auto ECS State Entry is not enabled (0 <sub>B</sub> ), the host can issue CAS CMD in LPDDR6 state diagram.				

### 7.8.28.1 Auto ECS

Auto ECS will operate in the background during Self Refresh with ECS 'H' (Auto ECS State Entry = 'H'), Self-Refresh with Power down and All bank Refresh with ECS 'H' (Auto ECS State Entry = 'H') period in which CAS command cannot issue when Auto ECS is enabled by MR111 OP[4].

The Auto ECS operation timing is shown in Figure 199.



**Figure 199 – Example of ECS Operation Timing**

- tECSC: Maximum time for LPDDR6 to complete an ECS operation (tECSC must be less than or equal to tRFCab)
- tECSint: Average periodic interval of ECS events to cover all codewords in a specified period of tECS (e.g., TBD hours)
- tECS: Period of time to complete ECS on all codewords.

In order to complete a full Error Check and Scrub within the recommended tECS (e.g., TBD 24 hours) which is affected by RM(Refresh Multiplier), the average periodic interval of ECS operations (tECSint) should be defined by tECS and tREFi = 3.9  $\mu$ s (MR4 x1). The total number of ECS operations is density and configuration dependent, as listed in Table 371.

**Table 371 – Example of tECSint per Subchannel**

Gb per subchannel	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
272b codewords per subchannel	$2^{24}$	$2^{24} \times 1.5$	$2^{25}$	$2^{25} \times 1.5$	$2^{26}$	$2^{26} \times 1.5$	$2^{27}$
tECSint [ms] per subchannel(TBD)	5.15	3.43	2.57	1.72	1.29	0.86	0.64

Even if the efficiency mode enabled, it is adequate to execute the Auto ECS for each sub-channel separately since it is dependent on refresh operation. And the host can access the MR using MRR with subchannel information.

### 7.8.28.1 Auto ECS (cont'd)

#### Expiration of tECS period:

For each Auto ECS operation, ECS Address Counters increment the column address after each internal ECS WR command such that the next code word and check bits are selected. Once the column counter wraps (all code words and check bits on the row have been accessed), the row counter will increment until all code words on each of the rows within a bank are accessed. When the row counter wraps (all rows within the bank have been accessed), the bank counter will increment, and the next bank will repeat the process of accessing each code word. After all the code words within the DRAM are read, corrected, and written once, the bank counter will wrap, and the process begins again with the next Auto ECS operation.

### 7.8.28.2 Manual ECS

Manual ECS LPDDR6 supports manual ECS option for better system ECS usage, which is enabled by MR111 OP[5]. Manual ECS can issue by MPC (TBD 10000111) during only DRAM IDLE but other MPC can be accepted in MPC allowable state in Figure 200 when manual ECS enabled.

### 7.8.28.3 ECS Error Type and Log

LPDDR6 ECS supports two ECS error types as outlined in the Table 372. The ECS Error Logs consist of several MR (Mode Register) that are read out using MRR command. ECS Error Logs consist of ECS Error Flags and Address Logs. See the MR section for details. Two ECS Error Flags default to 1'b0 and change to a 1'b1 in case of an error. The logs remain unchanged when read out, however the two ECS Error Flags are reset to 1'b0 when the host reads out MR112 OP[7:6].

**Table 372 – ECS Error Types**

ECS Error Type	ECS Error Flag	ECS Error Registers	Notes
<b>Uncorrected Error Address Logging (UEAL)</b>	ECS UE FLAG	1. UE Address Bank (MR113 OP[3:0] 2. UE Address Row (MR116 OP[7:0] and MR117 OP[7:0]))	
<b>Corrected Errors per row Address Logging (CEAL)</b>	ECS CE FLAG	1. Max CE per ROW Address Bank (MR113 OP[7:4]) 2. Max CE per ROW Address Row (MR114 OP[7:0] and MR115 OP[7:0])	

#### Uncorrected Error Address Logging (UEAL)

- 1) When the on-die ECC detects an Uncorrected Error (UE), the device first determines if the log can be updated based on the rules programmed in the ECS\_LOG\_RULES mode register (MR111 OP[3]).
  - a. For UE errors, if the ECS\_LOG\_RULES register is set to maintain (0B) the DRAM will not update the log if the ECS UE FLAG = 1'b1, otherwise the log will be updated.
  - b. If the MR is set to overwrite (1B) the log will always be updated.
- 2) If the log can be updated, the DRAM address of the error is logged in the form of Bank Address in MR113 OP[3:0] and Row Address in MR116 OP[7:0] and MR117 OP[7:0].
- 3) The ECS UE FLAG in MR112 OP[6] is updated to 1'b1.
- 4) The ECS FLAG is updated to 1'b1 per the ECS FLAG equation.
- 5) The error is logged within tECS.

### 7.8.28.3 ECS Error Type and Log (cont'd)

#### Corrected Errors per Row Address Logging (CEAL)

- 1) During ECS operation the on-die ECC will scrub a row by reading every column address in the row under scrub.
- 2) The device will track the number of corrected errors in the row.
- 3) Once the full row has been scrubbed the device first determines if the log can be updated.
  - a. If the ECS\_LOG\_RULES mode register is set to maintain ( $0_B$ ), the log can only be updated if the number of errors in the row is greater than TBD(8) errors in the individual row and the number of errors is greater than the previous errors logged.
  - b. If the ECS\_LOG\_RULES mode register is set to overwrite ( $1_B$ ), the log can be updated if the number of errors in the row is greater than TBD(8) errors.
- 4) If the log can be updated:
  - a. the DRAM address of the error is logged in the form of Bank Address in MR113 OP[7:4] and Row Address in MR114 OP[7:0] and MR115 OP[7:0]).
  - b. The ECS CE FLAG in MR112 OP[7] is updated to 1'b1.
  - c. The ECS FLAG is updated to 1b'1 per the ECS FLAG equation.
  - d. The error is logged after the column counter wraps

(All code words and check bits on the row have been accessed)

#### Reset of ECS Error Flags:

There are four independent methods for clearing the ECS Error Flags:

- 1) The host reads MR112 OP[7:6]
- 2) The host may issue an ECS Flag reset using MR111 OP[2]
- 3) The host may issue an ECS reset according to MR111 OP[1]
- 4) The host may issue device RESET

#### Reset of ECS Function:

The host may issue an ECS reset using MR111 OP[1] to reset all aspects of the ECS function including but not limited to the current scrub address counter in the DRAM, internal running the ECS Error Flags.

#### Reading of Auto ECS Error Logs:

LPDDR6 DRAMs avoid situations where the host is reading out the logs while the DRAM is in the process of updating the logs by not allowing both operations in a state. Figure 200 illustrates the states and their associated commands for the ECS operation as well as that states and their associated commands that the host can use to read the ECS Error Logs.

### 7.8.28.3 ECS Error Type and Log (cont'd)

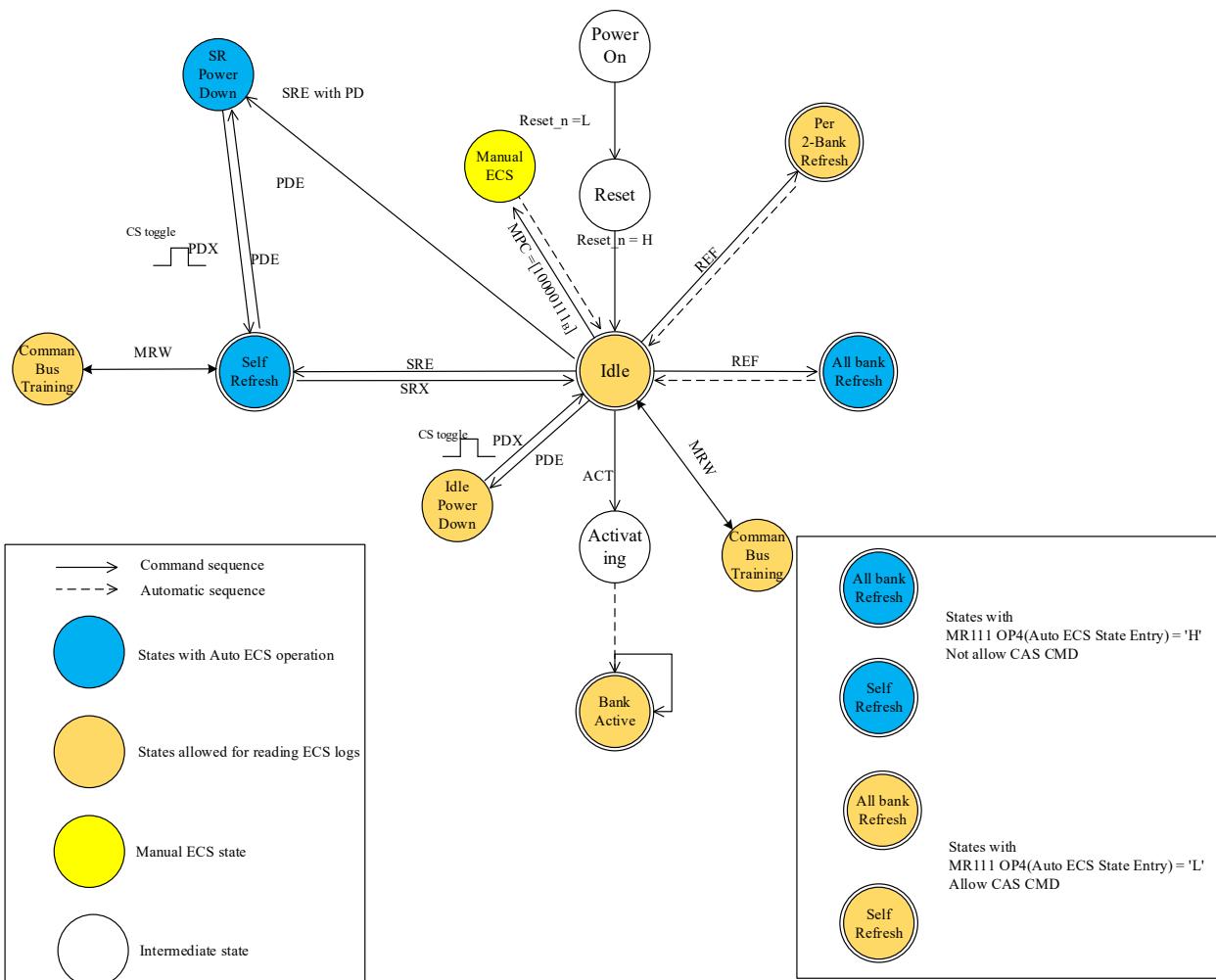


Figure 200 – Auto ECS State Diagram

When Auto ECS operation is enabled, and the host enters Self Refresh with ECS 'H', the ECS operation will continue until the Self Refresh Exit command is received by the DRAM. The ECS logs will not be guaranteed to be updated until  $t_{XSR\_ECSLOG\_UP} = t_{XP} + t_{REFab}$  has expired. Reading the log before  $t_{XSR\_ECSLOG\_UP}$  may result in existing or invalid data being read out. It means that when ECS operation is enabled,  $t_{XSR\_ECSLOG\_UP}$  is minimum requirement to avoid conflict between ECS and any command.

### 7.8.28.3 ECS Error Type and Log (cont'd)

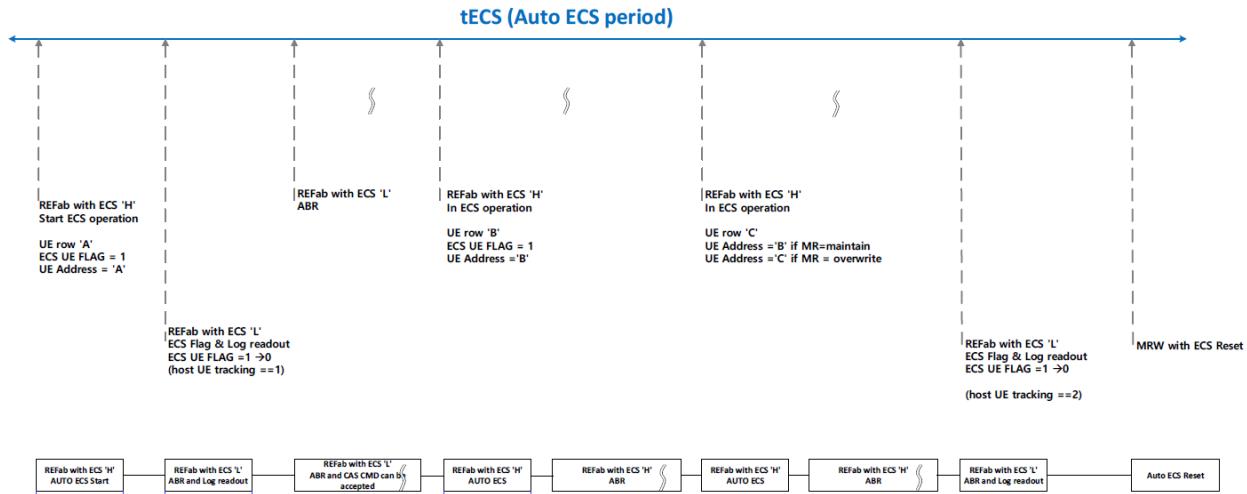


Figure 201 – Example Auto ECS Operation

## 7.8.29 Efficiency Mode

### 7.8.29.1 Features

LPDDR6 SDRAMs support an Efficiency (EFF) mode for normal operations. In case Dynamic Efficiency (DEFF) mode is enabled ( $MR1\ OP[6]=1_B$ ) by a host, a primary sub-channel keeps in active to execute write/read operations for both 16banks whereas a secondary sub-channel enters into standby and/or deep sleep to reduce LPDDR6 die's power consumption. A host must maintain refresh timing and RFM requirement for each sub-channel 16 banks separately regardless of the Dynamic Efficiency mode enable/disable. The  $MR0\ OP[3]$  (Read only) is a bit that indicates whether a specific sub-channel is the primary ( $MR0\ OP[3]=0_B$ ) or the secondary sub-channel ( $MR0\ OP[3]=1_B$ ).

The Efficiency mode has two exclusive applications. One can dynamically switch between Normal and Efficiency modes on demand (Dynamic Efficiency mode), while the other stays in Efficiency mode permanently to configure the device as a single sub-channel x12 DQ device (Static Efficiency mode).

- $MR0\ OP[2]=0_B$ : Device is switchable between Normal and Dynamic Efficiency (DEFF) mode.
- $MR0\ OP[2]=1_B$ : Device supports Static Efficiency (SEFF) mode only.

LPDDR6 SDRAM devices that can support Dynamic Efficiency mode manage Normal mode and Efficiency mode switching by  $MR1\ OP[6]$ :Efficiency mode Control.

- $MR1\ OP[6]=0_B$ : Normal mode
- $MR1\ OP[6]=1_B$ : Dynamic Efficiency mode

Figure 202 and Figure 203 illustrate the Normal Mode and the Dynamic Efficiency (DEFF) Mode LPDDR6 configuration examples. The Dynamic Efficiency mode entry by  $MR1\ OP[6]=1_B$  is allowed when LPDDR6 SDRAM is in a standby idle or active idle state.

### 7.8.29.1 Features (cont'd)

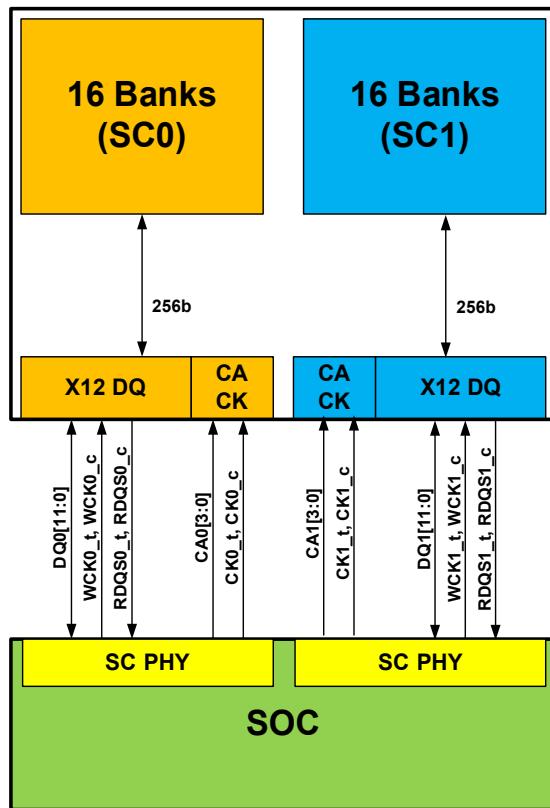


Figure 202 – LPDDR6 Normal Mode Configuration Example

### 7.8.29.1 Features (cont'd)

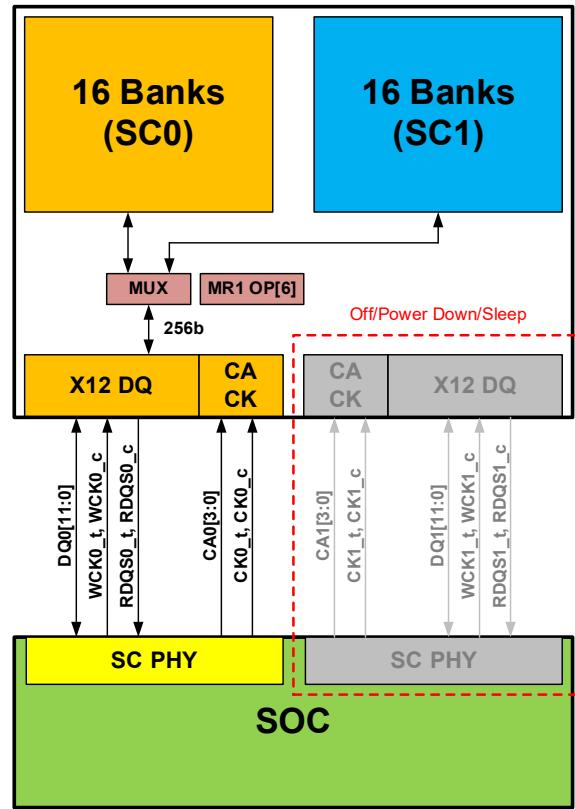


Figure 203 – LPDDR6 Dynamic Efficiency Mode Configuration Example

### 7.8.29.2 Efficiency Mode Commands

LPDDR6 SDRAM features the efficiency mode that accesses each sub-channel 16 banks separately by using commands including a sub-channel selection operand (SC). Precharge All (AB="H") or Refresh All (AB = "H") command is applied to the target sub-channel 16 banks (SC= 0 or 1) only. The following commands support a "SC" operand when the efficiency mode is enabled.

- Bank Activate (ACT-1)
- Precharge (PRE)
- Refresh (REF)
- Write (WR-S, WR-L)
- Read (RD-S, RD-L)
- Mode Register Read (MRR)

When DEFF mode is enabled, the "BC" operand (CA3-F1) of the MRW-1 command becomes effective. As the default behavior in DEFF mode, an MRW command containing the address and data for the target MR, which MRW-1 initiates with BC=0<sub>B</sub>, is executed in the primary sub-channel (the currently active one), and the MR data will be updated. In contrast, the MR contents in the secondary sub-channel remain as is. In the case of an MRW command initiated by MRW-1 with BC=1<sub>B</sub>, a broadcast MRW function is internally executed, and the MRW function in both primary and secondary sub-channels simultaneously is performed. As a result, the contents of the target MR in both primary and secondary sub-channels will be updated.

### 7.8.29.3 Dynamic Efficiency Mode

In case LPDDR6 SDRAM configures both primary and secondary sub-channel interface for write/read operations, a host may apply a dynamic efficiency mode to improve LPDDR6 SDRAM power at the expense of a half of LPDDR6 data bandwidth depending on system performance vs. power trade-off. At given clock frequency condition, the LPDDR6 SDRAM device can enter into the efficiency mode while accessing both sub-channel 16banks throughout the primary interface and returns to the normal mode by disabling the efficiency mode dynamically with a MRW command. The following constraints are applied to the dynamic efficiency mode usage.

- LPDDR6 clock frequency change and FSP procedure are prohibited when the Dynamic Efficiency (DEFF) mode is enabled.
- When enabling/disabling ZQ Stop, the Dynamic Efficiency mode must be disabled.
- A host must make the settings of specified MRs list in primary and secondary sub-channels to be identical before DEFF mode entry.
- When the Dynamic Efficiency (DEFF) mode is enabled, only specified MR list is allowed for MRW operation.
- ECS, mBIST, and PPR operations are not allowed during DFEE mode enable.

### 7.8.29.3 Dynamic Efficiency Mode (cont'd)

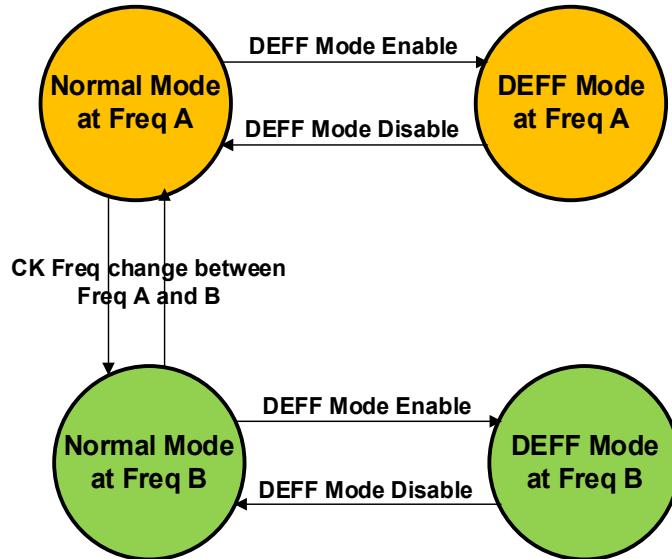


Figure 204 – Normal vs. Dynamic Efficiency Mode State Diagram

Table 373 – Dynamic Efficiency Mode Functional Behavior

Function	DEFF Mode Behavior	Note
DEFF Mode Entry	DEFF Mode Entry by MRW- MR1 OP[6]=1 <sub>B</sub> at primary SC	1
DEFF Mode Exit	DEFF Mode Exit by MRW- MR1 OP[6]=0 <sub>B</sub> at primary SC	1
Power Down	Power Down Entry & Exit is allowed	2
Self Refresh (PASR)	Self Refresh is prohibited	
PARC	PARC is applied during DEFF Mode if PARC is enabled	3
MRR	MRR operation with a “SC” operand	4
MRW	MRW operation to allowed MRs	
NOTE 1 MR1 OP[6] status in the secondary sub-channel is Don't Care.		
NOTE 2 The same CK frequency shall be maintained with or without CK stop. Power Down is prohibited in case CK frequency changes during DEFF Mode enable.		
NOTE 3 MR25 OP[6]=1 <sub>B</sub> (PARC enable).		
NOTE 4 An “SC” operand of MRR is invalid during Normal mode.		

### **7.8.29.3 Dynamic Efficiency Mode (cont'd)**

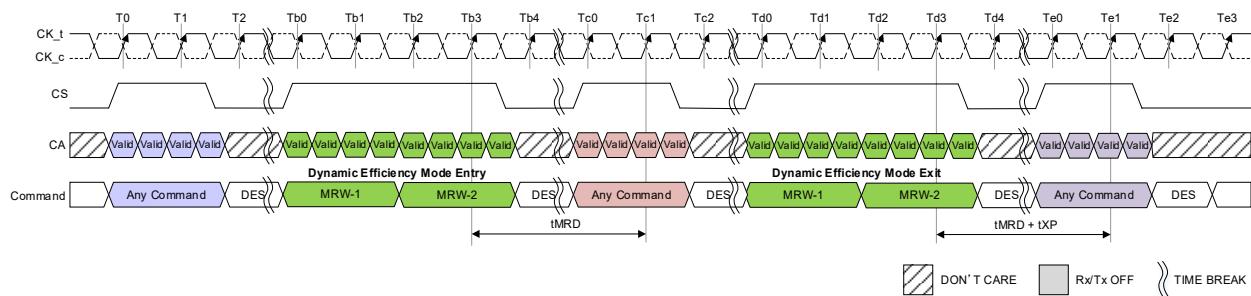
**Table 374 – Identical Mode Register List before DEFF Mode Entry**

### 7.8.29.3 Dynamic Efficiency Mode (cont'd)

**Table 375 – Allowed Mode Register List for MRW during DEFF Mode Enable**

### 7.8.29.3 Dynamic Efficiency Mode (cont'd)

Dynamic Efficiency Mode entry and exit are executed throughout a primary sub-channel interface by a MRW command. Refer to Figure 205 on Dynamic Efficiency Mode Entry and Exit timing example. After the Dynamic Efficiency Mode entry, the secondary Sub-Channel interface enters into a low power state which does not accept any commands from a host. Both 16banks memory arrays can be accessed and maintained only by the primary sub-channel interface during the Dynamic Efficiency mode enable. If an MRW command to exit Dynamic Efficiency Mode is issued to the primary sub-channel, the secondary sub-channel interface wakes up and normal valid operations can resume after CK SYNC procedure is finished. CK SYNC NOP command in the secondary sub-channel should wait for "tMRD + tXP" at least from a MRW command with Dynamic Efficiency Mode Exit. Any valid command can be issued after "tCKSYNC" from the CK SYNC NOP command.



**Figure 205 – Dynamic Efficiency Mode Entry/Exit Timing Example in Primary Sub-Channel**

#### 7.8.29.4 Static Efficiency Mode

LPDDR6 SDRAM efficiency mode can be used to double up total memory density. Two X12 sub-channel LPDDR6 devices can be logically combined into X24 LPDDR6 as shown in Figure 206. The primary sub-channel operates always to access both 16banks and the secondary sub-channel interface shuts down permanently.

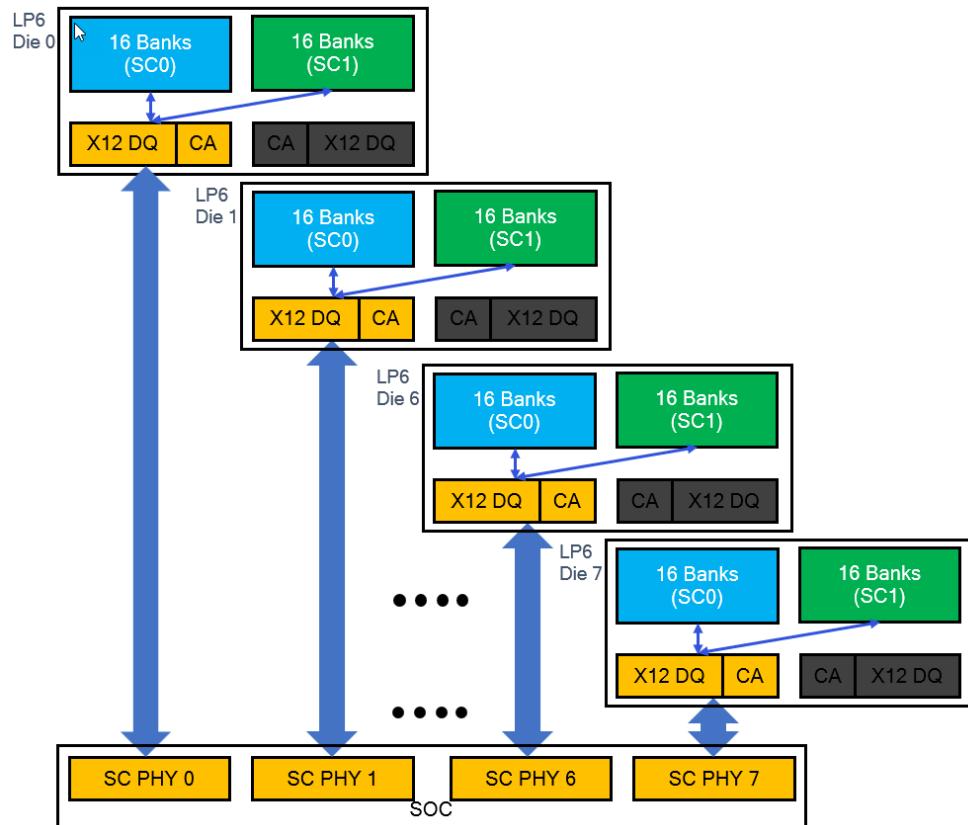


Figure 206 – Static Efficiency (SEFF) Mode based High-Capacity Configuration Example

### 7.8.30 Mode Register Write Control for Efficiency Mode

The MRW command is valid in Static Efficiency (SEFF) and Dynamic Efficiency (DEFF) modes. DEFF mode allows switching between normal mode and DEFF mode, and special MR content management considering primary and secondary sub-channel coherence is required. SEFF mode is permanently enabled, and its writable mode register (MR) settings between primary and secondary sub-channels in a die are assumed to be identical even if only CA bus in primary sub-channel is active.

Clause 7.8.29 Efficiency Mode describes the identical mode register list before DEFF mode entry and the list of MRW allowable mode registers in DEFF mode, and the mode registers are managed according to them.

### 7.8.30.1 Mode Register Write Command Behavior in SEFF Mode

In SEFF mode, an MRW command containing the address and the data for the target MR is executed the same as in normal mode, and the data is written to the writable mode register. The executed MRW is effective in primary and secondary sub-channels; hence, the target MR contents of primary and secondary sub-channels become identical automatically.

### 7.8.30.2 Mode Register Write Command Behavior in DEFF Mode

When DEFF mode is enabled, the command truth table of the MRW-1 command is changed, and the "BCST" operand (CA3-F1) becomes effective as shown in Table 376. As the default behavior in DEFF mode, an MRW command containing the address and data for the target MR, which MRW-1 initiates with BCST=0<sub>B</sub>, is executed in the primary sub-channel (the currently active one), and the MR data will be updated. In contrast, the MR contents in the secondary sub-channel remain as is.

In the case of an MRW command initiated by MRW-1 with BCST=1<sub>B</sub>, a broadcast MRW function is internally executed, and the MRW function in both primary and secondary sub-channels simultaneously is performed. As a result, the contents of the target MR in both primary and secondary sub-channels will be updated.

**Table 376 – MRW-1 Command Definition in DEFF Mode**

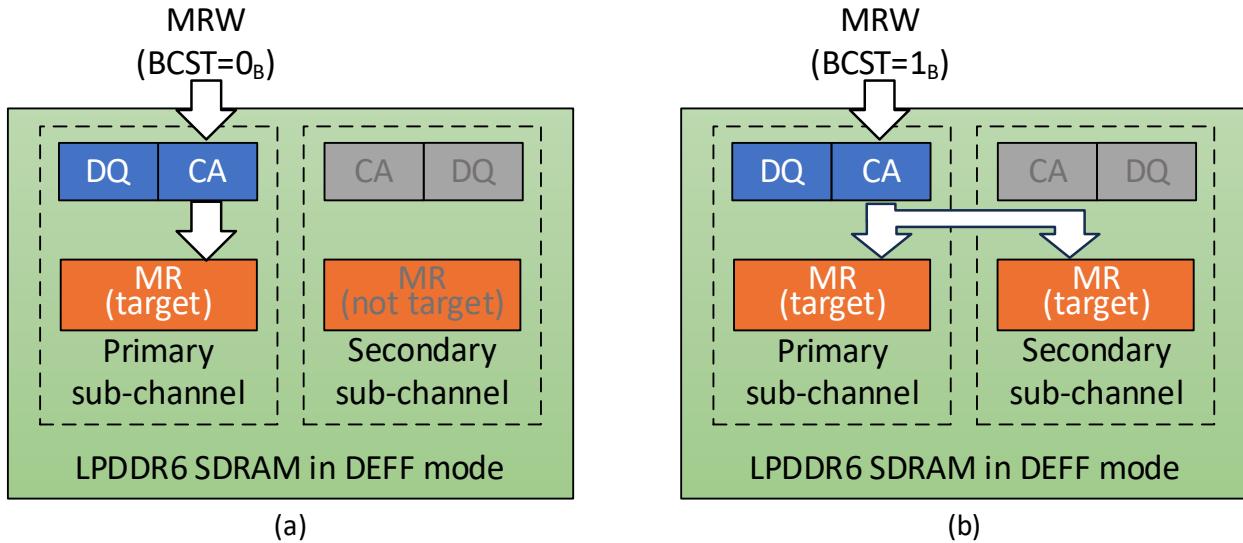
SDRAM COMMAND	CS	DDR COMMAND PIN				CK_t Edge
		CA0	CA1	CA2	CA3	
MODE REGISTER WRITE-1 (MRW-1)	H	H	L	L	V/PAR	R1
	X	L	L	H	BCST	F1
	H	MA4	MA5	MA6	MA7	R2
	X	MA0	MA1	MA2	MA3	F2

NOTE 1 The "BCST" operand is valid when DEFF mode is enabled.

NOTE 2 When the MRW-1 command with "BCST" operand = 0<sub>B</sub> is issued, MRW executes a MRW function in primary sub-channel.

NOTE 3 When the MRW-1 command with "BCST" operand = 1<sub>B</sub> is issued, MRW executes a broadcast MRW function and the contents specified in the OP7 through OP0 fields of the associated MRW-2 are written to the target mode registers specified in the MA7 through MA0 fields in the MRW-1 in both primary and secondary sub-channels simultaneously.

### 7.8.30.2 Mode Register Write Command Behavior in DEFF Mode (cont'd)



**Figure 207 – MRW Command Behavior when (a) BCST Operand = 0<sub>B</sub> in MRW-1 Command, and (b) BCST Operand = 1<sub>B</sub> in MRW-1 Command**

#### 7.8.30.2.1 Mode Registers requiring a Broadcast Mode-Register-Write

When DEFF mode is enabled, the mode registers listed in both "the identical mode register list before DEFF mode entry" and "the list of MRW allowable mode registers in DEFF mode" require a broadcast MRW operation by MRW-1 with BCST=1<sub>B</sub> when a host wants to modify their contents.

## 7.8.31 MBIST/mPPR

### 7.8.31.1 LPDDR6 MBIST Overview

The LPDDR6 Memory Built-In Self-Test (MBIST) primary charter is to mitigate array faults, single-bit errors (SBE), and latent multi-bit errors (MBE) that might occur after leaving the manufacturer's factory and be observed by the user's post-assembly board testing. The MBIST operation takes a significant amount of time to perform and is destructive to existing array data; thus, it is targeted to be part of the final post-assembly board test process.

The MBIST operation is not affected by the DRAM input clock rate, as the timing is controlled by an internal oscillator. The MBIST test and repair flow is bifurcated into two operations: 1) **MBIST-Test** where the DRAM uses internal patterns to self-test the entire memory array to detect suspect row(s) with faults and 2) **MBIST-mPPR** where the DRAM will self-repair suspect row(s) identified during the MBIST-Test process, provided resources are available. LPDDR6 MBIST repair resources are not pulled from sPPR/hPPR resources.

The MBIST operation may only be entered while in All Banks Idle state and may be initiated after the device has been properly initialized and prior to when payload data is written to the array. Once payload data is written to the array, use of the MBIST operation will overwrite payload data, and it should only be used when powering down or back-up of array data is available to reload the array after completion.

MBIST-Test and MBIST-mPPR are only supported in Normal Mode and Static Efficiency Mode. MBIST is not supported in Dynamic Efficiency Mode. To save DRAM die area and power, some devices might have a single MBIST controller in one sub-channel that controls test and repair in both sub-channels. In Normal Mode, hosts should initiate MBIST Test and mPPR in both sub-channels simultaneously by writing to MR41 OP[3:2] in both sub-channels. In Static Efficiency Mode, hosts control MBIST Test and mPPR by writing to MR41 OP[3:2] in the primary sub-channel. In either mode, separate results are available on a per-sub-channel basis, by reading MR41 OP[6:5] in each sub-channel.

#### 7.8.31.1.1 MBIST-Test

The Host shall issue an MRW with MR41 OP[3:2]=10<sub>B</sub> to enable an MBIST-Test. During MBIST-Test, the DRAM uses internal patterns to test the entire memory and identify suspect row(s) with faults. The MBIST-Test procedure may be aborted at any time via RESET. Should the MBIST-Test operation be aborted, then the Host should restart the MBIST-Test from the beginning.

After completion of the MBIST-Test, the Host shall issue an MRR to MR41 OP[6:5] to determine the results of the MBIST-Test operation, which are one of four possible outcomes: (1) no error detected, (2) error detected and resources are available to repair, (3) error detected but no repair resources remain, and (4) unresolved operation and abort. In the second outcome (error detected and resources are available to repair), the suspect row can be permanently repaired by enabling MBIST-mPPR. If either sub-channel indicates error detected and resources are available to repair, the host should execute MBIST-mPPR by writing to MR41 OP[3:2] in both sub-channels (Normal Mode), or the primary sub-channel (Static Efficiency Mode).

The MBIST-Test should be repeated after each MBIST-mPPR until either outcome 1 (no error detected) is obtained or outcome 3 (error detected but no repair resources remain) is obtained. Testing should be halted, and the memory device replaced if outcome 4 is ever obtained (unresolved operation and abort).

### 7.8.31.1.2 MBIST-mPPR

After completion of an MBIST-Test, if the Host issues an MRR to MR41 OP[6:5] and obtains outcome 2 (error detected and resources are available to repair) then MBIST-mPPR should be performed by issuing an MRW with MR41 OP[3:2]=11<sub>B</sub>.

The MBIST-mPPR procedure will fuse-blow a spare row in place of the suspect row identified as having a fault. Once the MBIST-mPPR command is registered, the DRAM must not be interrupted; any interruption makes operation uncertain thereafter. The MBIST-mPPR procedure should only be done following a valid MBIST-Test; MBIST-mPPR procedure used at any other time can place the DRAM in an unknown state.

### 7.8.31.1.3 MBIST Times

The LPDDR6 MBIST operating time is not affected by the input clock rate, timing is controlled by an internal oscillator. The MBIST-Test time will vary with die density while the MBIST-mPPR time doesn't vary with die density.

The time to complete the MBIST-Test process is tSELF\_TEST, and the time to complete the MBIST-mPPR process is tSELF\_REPAIR.

**Table 377 – MBIST Timing Parameters Test Times (2 Sub-channels per Die)**

Parameter	Density (per 2 sub-channel)								Min/ Max	Units	Notes
	4Gb	8Gb	12Gb	16Gb	24Gb	32Gb	48Gb	64Gb			
tSELF_TEST	5.4	8.7	12.0	15.4	22	28.7	42	55.4	Max	s	1
tSELF_REPAIR					5.6				Max	s	2
NOTE 1 Time to complete one full MBIST-Test loop.											
NOTE 2 Time to complete MBIST-mPPR process.											

### 7.8.31.2 LPDDR6 MBIST Operation

The following general guidelines apply when using MBIST:

- a) The DRAM shall be powered-up and initialized according to "Power-up Initialization Sequence".
- b) The DRAM shall be in All Banks Idle state.
- c) The MBIST sequence is performed on both sub-channels at the same time.
- d) DVFS shall be disabled.
- e) ODT guidance is as follows:
  - a. Command/Address Bus ODT state should be maintained.
  - b. Entering MBIST-Test or MBIST-mPPR should not affect the Command/Address Bus ODT state.
  - c. ODT for WCK\_t/c should not be affected while in MBIST-Test or MBIST-mPPR state.
  - d. ODT for CS should not be affected while in MBIST-Test or MBIST-mPPR state.
  - e. While LPDRAM is under MBIST operation, the state of ODT should not be changed.
- f) MBIST-Test can be performed with any clock rate between tCKmin = 1.25 ns and tCKmax = 5.0 ns.
  - a. External clock rate doesn't affect MBIST operation.
- g) The Host shall read MR41 OP[1] and detect a "1" to confirm LPDDR6 MBIST is supported.
- h) Prior to initiating at least one MBIST-Test operation, MR41 OP[6:5] defaults to 00, but MBIST Status is only valid after at least one MBIST-Test has been completed.

### 7.8.31.2.1 MBIST-Test Procedure:

#### 7.8.31.2.1.1 Initiate MBIST-Test (Refer to Figure 208)

- a) After tMRD of ALL Banks Idle, the Host shall write MR41 OP[3:2] to enable MBIST-Test.
  - a. MR41 OP[3:2] 10 = Enable MBIST-Test
- b) After tMRD, the Host shall issue the LP6 guard key as defined by MR42.
  - a. MBIST-Test is entered at completion of the guard key sequence.
    - i. Alert pin will drive high and remain high until the completion of MBIST-Test.
    - ii. While Alert is high, the DRAM shall have only continuous DES clocked to the DRAM.
    - iii. MBIST-Test may be interrupted via a RESET command while Alert is high.
- c) Once the MBIST-Test is completed, Alert will no longer be driven high and will go low with appropriate pull-down by the Host.
  - a. The DRAM shall set MR41 OP[6:5] to the correct setting prior to Alert no longer being driven high.
    - i. OP[6:5] 00 = No error detected
    - ii. OP[6:5] 01 = Error detected; repair resources available
    - iii. OP[6:5] 10 = Error detected; repair resources expired
    - iv. OP[6:5] 11 = Unresolved operation, abort required
- d) Host shall write "00" to MR41 OP[3:2] to disable MBIST.
  - a. After tMRD, issue PDE, then after tCSPD issue PDX, then wait tCSH+tXP+tMRRI.
    - i. DRAM is now in standard operating mode when both Alert is high-z and tMRD+tCSPD+tCSH+tXP+tMRRI delay from MRW to MR41 OP[3:2] 00 are satisfied.
- e) Once MR41 OP[3:2] disables MBIST and the delay above is satisfied, Host may issue MRR to MR41 OP[6:5] and after tMRD read MR41 OP[6:5] to determine results of the MBIST-Test:
  - a. If MR41 OP[6:5]=00<sub>B</sub> then additional MBIST testing not required.
  - b. If MR41 OP[6:5]=11<sub>B</sub> then issue RESET to the DRAM, power down, and replace DRAM.
  - c. If MR41 OP[6:5]=10<sub>B</sub> then no further MBIST testing should be performed since no available resources exist.
  - d. If MR41 OP[6:5]=01<sub>B</sub> then MBIST-mPPR should be performed.

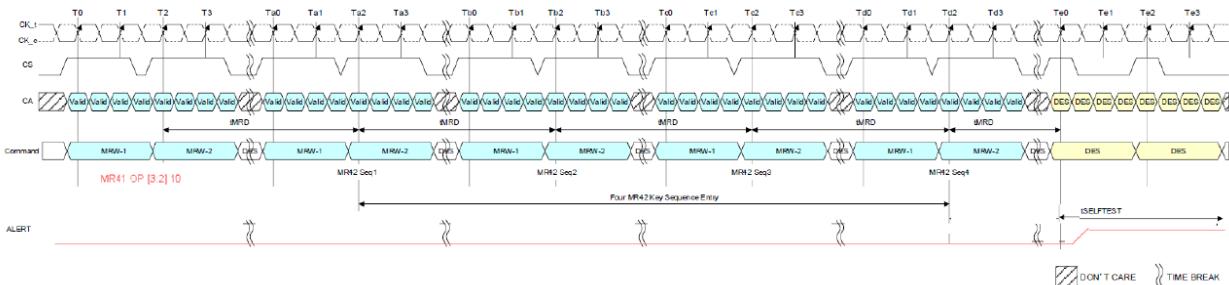


Figure 208 – MBIST-Test Entry

### 7.8.31.2.1.2 MBIST-mPPR Procedure

- a) Immediately after performing MBIST-Test, the Host shall write MR41 OP[3:2] to initiate MBIST-mPPR to repair row with detected error, refer to Figure 209. Once the MBIST-mPPR is initiated, the repair process must not be interrupted.
  - a. MR41 OP[3:2] 11 = Enable MBIST-mPPR
- b) After tMRD, the Host shall issue the LP6 guard key as defined by MR42.
  - a. MBIST-mPPR is entered at completion of the guard key sequence.
    - i. Alert pin will drive high and remain high until MBIST-mPPR completes.
    - ii. While Alert is high, the DRAM shall have only continuous DES clocked to the DRAM.
    - iii. MBIST-mPPR must never be interrupted while Alert is high.
- c) Once the MBIST-mPPR is completed, Alert will no longer be driven high and will go low with appropriate pull-down by the Host.
  - a. The DRAM shall set MR41 OP[6:5] to the correct setting prior to Alert no longer being driven high.
- d) Host shall write "00" to MR41 OP[3:2] to disable MBIST.
  - a. After tMRD, issue PDE, then after tCSPD issue PDX, then wait tCSH+tXP+tMRRI.
    - i. DRAM is now in standard operating mode when both Alert is high-z and tMRD+tCSPD+tCSH+tXP+tMRRI delay from MRW to MR41 OP[3:2] 00 are satisfied.
- e) Once MR41 OP[3:2] disables MBIST and delay above is satisfied, Host may issue MRR to MR41 OP[6:5] and after tMRD read MR41 OP[6:5] to determine results of the MBIST-mPPR:
  - a. If MR41 OP[6:5]=00<sub>B</sub> then additional MBIST-Test not required.
  - b. If MR41 OP[6:5]=11<sub>B</sub> then issue RESET to the DRAM, power down, and replace DRAM.
  - c. If MR41 OP[6:5]=10<sub>B</sub> then no further MBIST testing should be performed since no available resources exist.
  - d. If MR41 OP[6:5]=01<sub>B</sub> then another MBIST-Test should be performed.

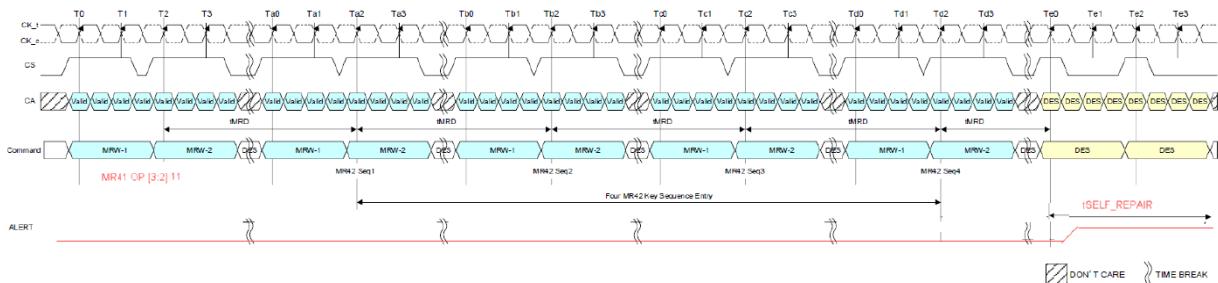
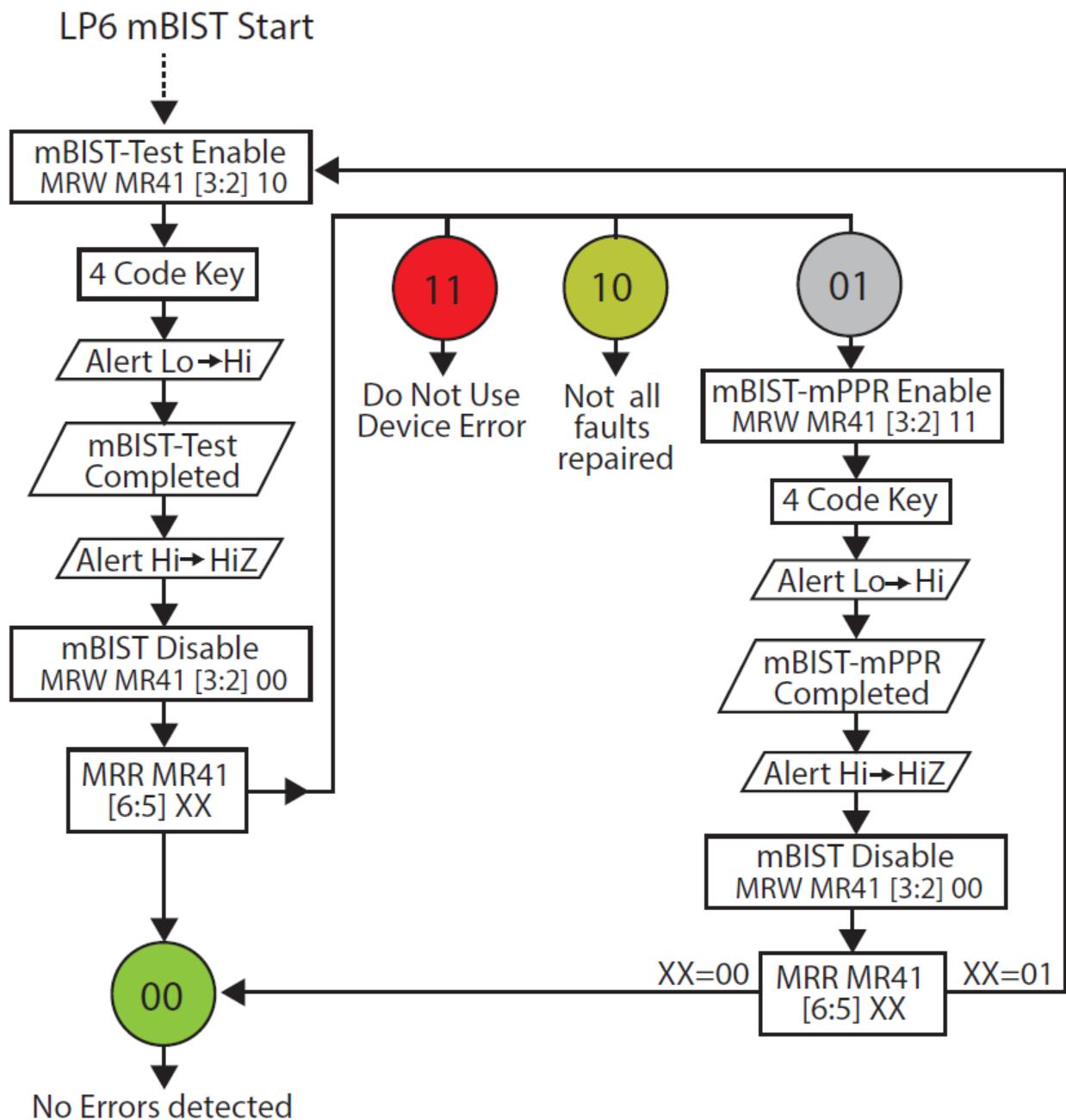


Figure 209 – MBIST-mPPR Entry

### 7.8.31.2.2 MBIST Flow Diagram



### 7.8.32 Loopback Mode

With Loopback, LPDDR6 SDRAM can feed a received signal or data back out to an external receiver for multiple purposes. Loopback allows the host (memory controller or test instrument) to monitor data that was just sent to the DRAM without having to store the data in the DRAM or use READ operations to retrieve data sent to the DRAM. Loopback in LPDDR6 SDRAM requires that the data be sent to the Loopback path before sending it to the core so no READ/WRITE commands are required for Loopback to be operational. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis. At BER=1E-16, for example, (1) there is not enough memory depth in the DRAM to store all the 1E+16 data; (2) the amount of time to perform multiple WRITE/READ commands to/from the memory is prohibitively long; (3) since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention; and (4) limited pattern depth means limited Inter Symbol Interference (ISI) and limited Random Jitter (Rj), and, therefore, limited errors at the receiver. Use of the Loopback feature is a necessity for characterizing the receiver without the limitations and complexities of other traditional validation methods.

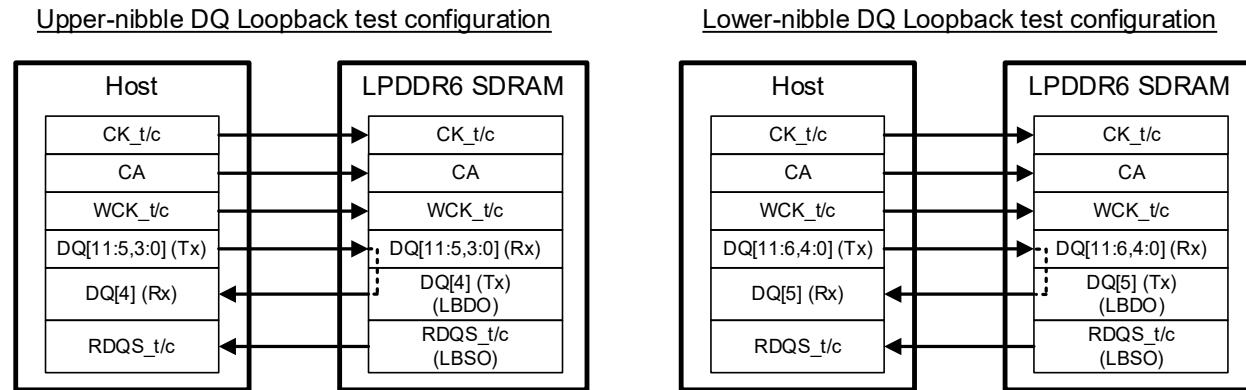


Figure 210 – Overview of Loopback Test

#### 7.8.32.1 Loopback Output Definition

For the loopback function, one single-ended Loopback data output (LBDO) pin and one single-ended or differential Loopback strobe output (LBSO) pin/pair are required per sub-channel. In LPDDR6 SDRAM, these two output pins reuse either DQ4, DQ5 pin, which is automatically selected by MR92 OP[3:0], for the LBDO, and RDQS\_t/c for the LBSO.

The RTT settings for LBDO and LBSO follow the ODT and NT-ODT settings of DQ&RDQS that should be appropriately configured for an environment.

Selecting any valid Loopback Output value via MR92 OP[3:0] other than the default Loopback Disabled (MR92 OP[3:0] = 0000<sub>B</sub>) will result in the LBDO and LBSO pins transitioning from the normal operation mode to Loopback mode, and to a DRAM Drive State.

Before changing the LBDO Select from DQ4 to DQ5 or vice versa, host shall set Loopback Output Select to MR92 OP[3:0]=0000<sub>B</sub> to disable Loopback mode.

The LBSO will transition with the differential input crossing point of WCK\_t/WCK\_c plus latency.

The LBDO output will transition with the receiver data state of the DQ pin selected by MR92 OP[3:0]. If an RFU output is selected, or if an invalid output for device configuration is selected, the LBDO output will remain in a DRAM Drive State.

### 7.8.32.1 Loopback Output Definition (cont'd)

Table 378 – Loopback Output Definition and Target DQ Setting

Condition	MR92 OP[3:0]	Loopback target DQ	LBDO	LBSO	DQs other than LBDO	Notes
Loopback Disabled	0000 <sub>B</sub>	Not selected	Both DQ4,DQ5 are not in Loopback mode	Both RDQS_t/c pins are not in Loopback mode	Not in Loopback mode	
Loopback Enabled	0001 <sub>B</sub>	DQ0 is selected	DQ5 is selected as LBDO	RDQS_t/c pins are in Loopback mode	Receivers turned on	1
Loopback Enabled	0010 <sub>B</sub>	DQ1 is selected				1
Loopback Enabled	0011 <sub>B</sub>	DQ2 is selected				1
Loopback Enabled	0100 <sub>B</sub>	DQ3 is selected				1
Loopback Enabled	0101 <sub>B</sub>	DQ4 is selected				1
Loopback Enabled	1001 <sub>B</sub>	DQ5 is selected				1
Loopback Enabled	1010 <sub>B</sub>	DQ6 is selected				1
Loopback Enabled	1011 <sub>B</sub>	DQ7 is selected				1
Loopback Enabled	1100 <sub>B</sub>	DQ8 is selected				1
Loopback Enabled	1101 <sub>B</sub>	DQ9 is selected				1
Loopback Enabled	1110 <sub>B</sub>	DQ10 is selected				1
Loopback Enabled	1111 <sub>B</sub>	DQ11 is selected				1
NOTE 1 Selection of an unsupported DQ for the device configuration will result in undefined LBDO output.						

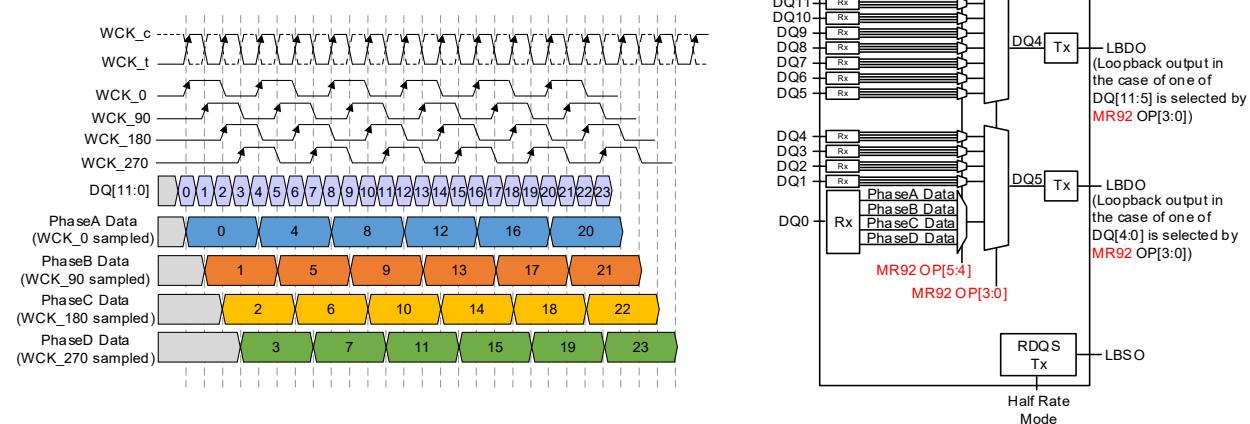


Figure 211 – Overview of 4-way Interleave Loopback Mode Timing Chart and Circuit

### 7.8.32.2 Loopback Phase

Due to the high data rates of the LPDDR6 SDRAM, Loopback is implemented 4-way interleaved outputs. With a 4-way implementation, the WCK and DQ will be sampled and output every 2 WCK or 4 UI.

To be able to sample all bits with a 4-way interleave implementation, the Loopback Select Phase programmed in MR92 OP[5:4] allows selection of the WCK and DQ phase to be output; Phase A, Phase B, Phase C and Phase D, are valid options. Figure 211 shows an example of a Loopback implementation for 4-way interleave. This example requires a divided clock to produce WCK\_0, WCK\_90, WCK\_180 and WCK\_270. Phase A through D refers to the 4-bit naturally aligned bits in a data stream. The output of the DQ slicer runs at 1/4 the speed as received data. In a 4-way interleave design, the data is received at full speed, but internally the data is latched only at quarter speed. For example, if the input bit stream consists of A, B, C, D, then the multiplexer input "A" receives data bit A and strobe WCK\_0; multiplexer input "B" receives data bit B and strobe WCK\_90; multiplexer input "C" receives data bit C and strobe WCK\_180; and multiplexer input "D" receives data bit D and WCK\_270.

**Table 379 – Loopback Phase Selection Setting**

Condition	MR92 OP[5:4]	Loopback target Phase	Notes
PhaseA	00 <sub>B</sub>	PhaseA is selected	1
PhaseB	01 <sub>B</sub>	PhaseB is selected	1
PhaseC	10 <sub>B</sub>	PhaseC is selected	1
PhaseD	11 <sub>B</sub>	PhaseD is selected	1

NOTE 1 Loopback Phase selection is applied to any DQ selected by Loopback DQ selected by MR92 OP[3:0].

### 7.8.32.3 Loopback Normal Output Mode

In Normal Output Mode, the selected DQ state is captured with every WCK\_t/WCK\_c toggle for the selected Loopback Phase and output on LBDO. The LBDO output will be delayed by tLBDLY from the selected WCK\_t/WCK\_c Loopback Phase. The LBSO behaves same as the RDQS\_t/c with half-rate mode. LBSO uses RDQS\_t/c circuits. The LBSO output delay timing will be tLBDLY as well. With these LBDO and LBSO implementations, LBDO and LBSO will be in-phase state; the Loopback Select Phase setting is applied to LBSO as well. Since no Write commands are required in Normal Output Mode, MR settings pertaining to WL are ignored by the Loopback function.

Additional requirements for Normal Output Mode:

- WCK\_t/WCK\_c must be driven differentially low (WCK\_t low, WCK\_c high) prior to entry into Normal Output Mode.
- WCK\_t/WCK\_c must be continuously driven during Loopback operation. (HiZ state not allowed.)
- Only DSEL and MRW commands applied at command pins during Normal Output Mode.
- RESET is required to exit Loopback Normal Output Mode.

LPDDR6 SDRAM array data is not guaranteed after entering Normal Output Mode.

### 7.8.32.4 Loopback Normal Output Mode Timing Diagrams

The Loopback Normal Output Mode entry and output example timing diagrams are shown below. To initiate loopback mode operation correctly, it is highly recommended that a host use WCK always-on mode. Therefore, a host should send the CAS command with the WS=1 setting and after that, the host sends the mode register write command to enable Loopback Normal Output Mode.

#### 7.8.32.4 Loopback Normal Output Mode Timing Diagrams (cont'd)

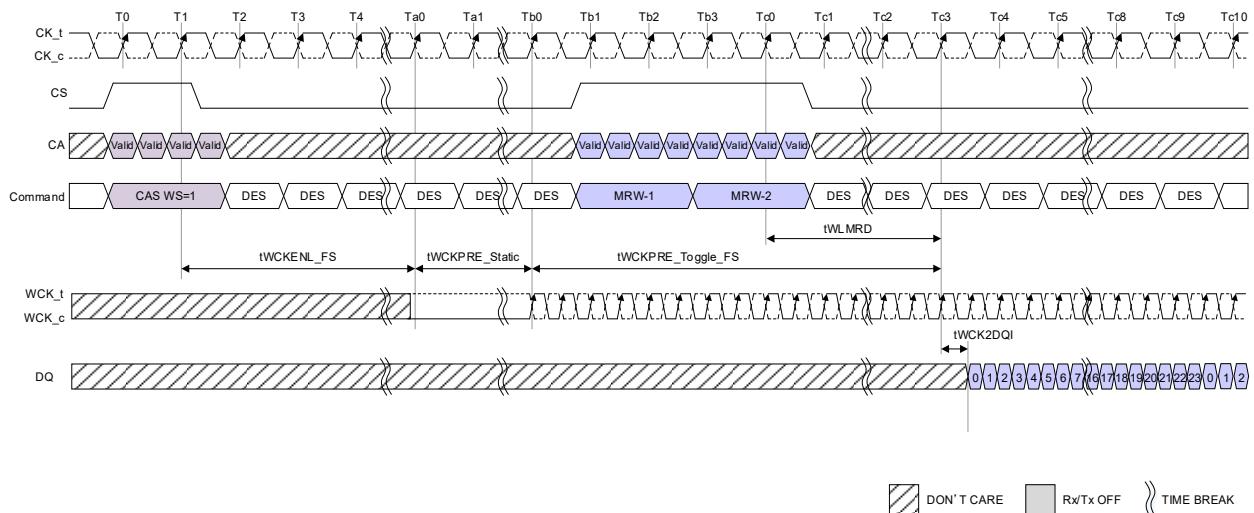
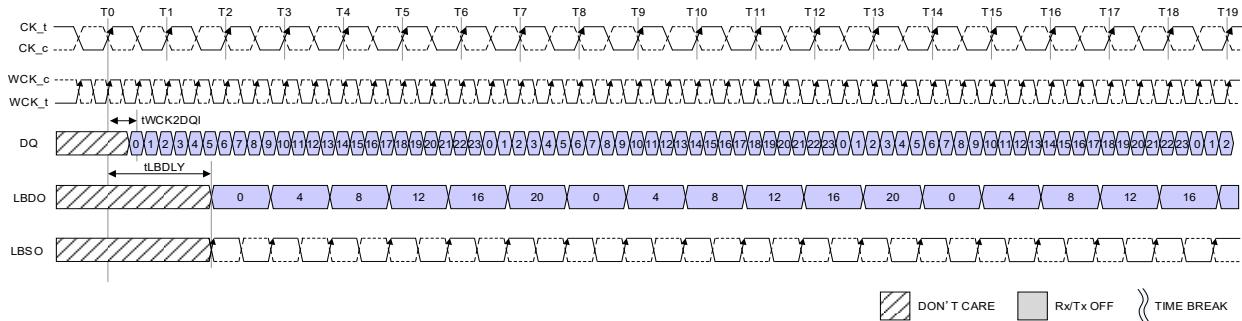


Figure 212 – Loopback Normal Output Mode Entry

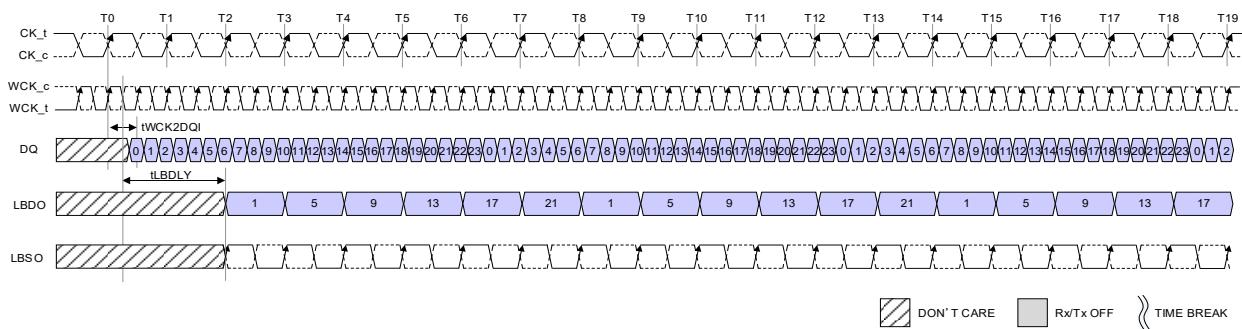
The Loopback Normal Output Mode Entry timing parameter is defined below.

Parameter	Symbol	Min/Max	Value	Unit	Notes
Delay time from MRW entry to valid DQ loopback input delay	tWLMDR	Max	TBD	ns	

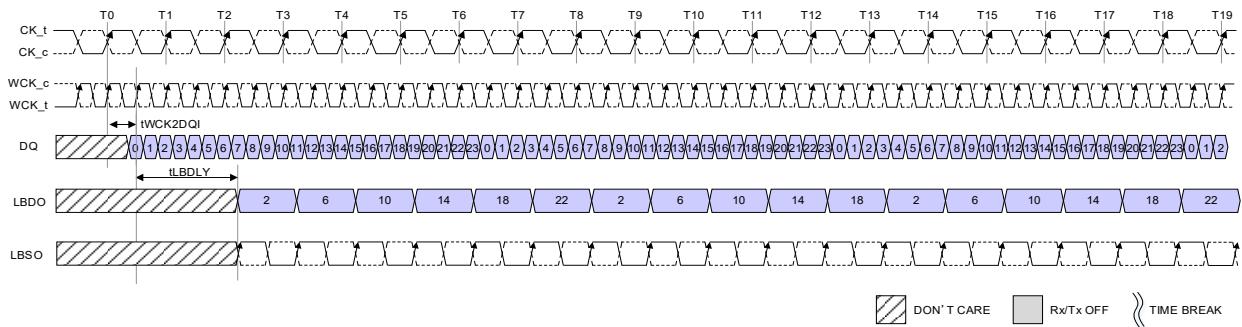
#### 7.8.32.4 Loopback Normal Output Mode Timing Diagrams (cont'd)



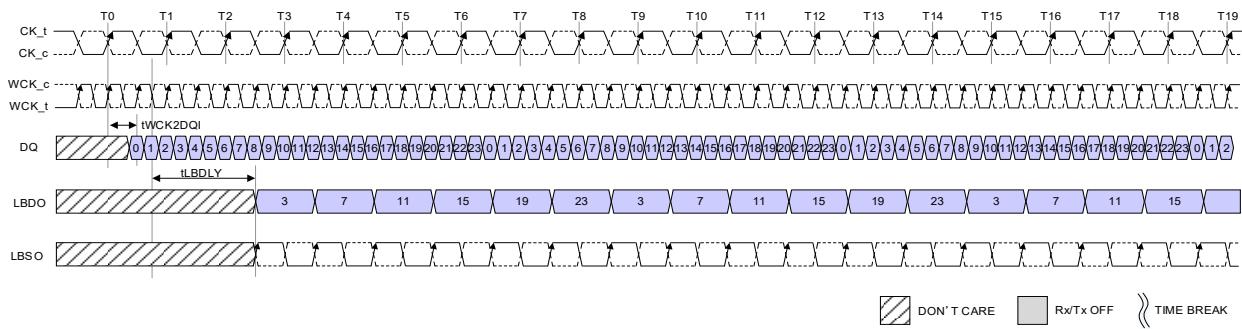
**Figure 213 – Loopback Normal Output Mode PhaseA Example**



**Figure 214 – Loopback Normal Output Mode PhaseB Example**



**Figure 215 – Loopback Normal Output Mode PhaseC Example**



**Figure 216 – Loopback Normal Output Mode PhaseD Example**

#### 7.8.32.5 Loopback Timing and Levels

The LBDO and LBSO output will be delayed from the selected WCK\_t/WCK\_c Loopback Phase. The timing parameter, tLBDLY, is shown in Table 380.

**Table 380 – Loopback LBDO and LBSO Output Timing Parameter**

Parameter	Symbol	Min/Max	Value	Unit	Notes
LBDO and LBSO Delay from selected WCK Loopback Phase	tLBDLY	Max	10	ns	

The interaction between LBDO and LBSO is described in clause 7.8.32.3. ODT for Loopback is described in clause 7.8.32.1. Output driver electrical characteristics of LBDO and LBSO follows “Pull Up/Pull Down Driver Characteristics and Calibration” in clause 15.9.

## 8 Command Constraint and AC Timing

### 8.1 Effective Burst Length (BL/n) Definition

**Table 381 – Effective Burst Length (BL/n) Definition**

WCK frequency	Bank to Bank Constraints	BL24			BL48			Unit
		BL/n	BL/n_min	BL/n_max	BL/n	BL/n_min	BL/n_max	
$\leq 3200 \text{ MHz}$	Same BG	6			12			nCK
	Different BG							
$> 3200 \text{ MHz}$	Same BG	Max[6, RU(tCCD_L/tCK)]	6	12	12 + RU(tCCD_L/tCK)		18	24
	Different BG	6			6			

## 8.2 tCCD

**Table 382 – Same BG tCCD Timing Definition**

Data Rate [Mbps]		CK Frequency [MHz]		BL/n (Same BG)	
Lower Limit (>)	Upper Limit (≤)	Lower Limit (>)	Upper Limit (≤)	BL24 [nCK]	BL48 [nCK]
80	1067	20	267	6	12
1067	1600	267	400	6	12
1600	2133	400	533	6	12
2133	2750	533	688	6	12
2750	3200	688	800	6	12
3200	3750	800	938	6	12
3750	4267	938	1067	6	12
4267	4800	1067	1200	6	12
4800	5500	1200	1375	6	12
5500	6400	1375	1600	6	12
6400	7500	1600	1875	8	20
7500	8533	1875	2133	8	20
8533	9600	2133	2400	10	22
9600	10667	2400	2667	10	22
10667	11733	2667	2933	12	24
11733	12800	2933	3200	12	24

NOTE 1 BL/n is minimum column to column cycle time, tCCD(min).

## 8.3 Command Timing Constraints

**Table 383 – Command Timing Constraints for Same Banks in Same Bank Group  
(DQ ODT is Disabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
ACTIVE	Illegal	RU(tRCDr/tCK)	RU(tRCDw/tCK)	RU(tRAS/tCK)
READ (BL24 or BL48)	Illegal	BL/n	tRTW <sup>1)</sup>	nRTP
WRITE (BL24 or BL48)	Illegal	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	WL + BL/n_max + nWTP
PRECHARGE	RU(tRP/tCK)	Illegal	Illegal	4

NOTE 1 Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.

NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.

### 8.3 Command Timing Constraints (cont'd)

**Table 384 – Command Timing Constraints for Different Banks in Same Bank Group  
(DQ ODT is Disabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	2	2	2
READ (BL24 or BL48)	2	BL/n	tRTW <sup>1)</sup>	2
WRITE (BL24 or BL48)	2	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	2
PRECHARGE	2	2	2	4

NOTE 1 Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.

NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.

**Table 385 – Command Timing Constraints for Different Banks in Different Bank Group  
(DQ ODT is Disabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
ACTIVE	RU(tRRD/tCK)	2	2	2
READ (BL24 or BL48)	2	BL/n	tRTW <sup>1)</sup>	2
WRITE (BL24 or BL48)	2	WL + BL/n_min + RU(tWTR_S/tCK)	BL/n	2
PRECHARGE	2	2	2	4

NOTE 1 Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.

NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol

### 8.3 Command Timing Constraints (cont'd)

**Table 386 – Command Timing Constraints for Same Banks in Same Bank Group  
(DQ ODT is Enabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
READ (BL24 or BL48)	Illegal	BL/n	tRTW <sup>1)</sup>	nRTP
NOTE 1	Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.			
NOTE 2	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

**Table 387 – Command Timing Constraints for Different Banks in Same Bank Group  
(DQ ODT is Enabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
READ (BL24 or BL48)	2	BL/n	tRTW <sup>1)</sup>	2
NOTE 1	Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.			
NOTE 2	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

**Table 388 – Command Timing Constraints for Different Banks in Different Bank Group  
(DQ ODT is Enabled)**

Current CMD	Next CMD			
	ACTIVE	READ	WRITE	PRECHARGE
READ (BL24 or BL48)	2	BL/n	tRTW <sup>1)</sup>	2
NOTE 1	Read to Write Timing (tRTW) varies depending on DQ Bus Receiver On-Die-Termination, Non-Target DQ Bus Receiver On-Die-Termination, Read DQS and TBD. Refer to the Read to Write Timing (tRTW) clause in 8.3.1.			
NOTE 2	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

### 8.3.1 READ to WRITE Command Timing Constraints (tRTW)

The following tables show the command constraint from Read to Write timing when LPDDR6 SDRAM can be controlled NT-ODT turn on/off timing for DQ and RDQS separately.

**Table 389 – Same/Different Banks in Same Bank Group**

NT-ODT MRaa OP[7:5]:	ODT MRbb OP[2:0]:	tRTW	Unit	Note
Disable	Disable	RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL	nCK	1,2,3
Enable	Disable	RL+BL/n_max+RU(tWCK2DQO(max)/tCK)-WL	nCK	1,2,3
Disable	Enable	RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)- ODTLon-RD(tODTon(min)/tCK)+1	nCK	1
Enable	Enable	RL+BL/n_max+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)- ODTLon-RD(tODTon(min)/tCK)+1	nCK	1
NOTE 1		tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MR11 OP[6]: WCK Frequency Mode setting. MR11 OP[6]=0 <sub>B</sub> : tWCK2DQO_LF(max), MR11 OP[6]=1 <sub>B</sub> : tWCK2DQO_HF(max)		
NOTE 2		Need to add 1nCK to tRTW in case of not "MRdd OP[2:0]=000 <sub>B</sub> and MRdd OP[6:4]=000 <sub>B</sub> " (In case of DFEQ is enabled).		
NOTE 3		Need to add 1nCK to tRTW in case of Per-pin DFE Control:MR41 OP[0]=1 <sub>B</sub> : (In case of Per Pin DFE is enabled).		
NOTE 4		Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.		

**Table 390 – Different Banks in Different Bank Group**

NT-ODT MRaa OP[7:5]:	ODT MRbb OP[2:0]:	tRTW	Unit	Note
Disable	Disable	RL+BL/n_min+RU(tWCK2DQO(max)/tCK)-WL	nCK	1,2,3
Enable	Disable	RL+BL/n_min+RU(tWCK2DQO(max)/tCK)-WL	nCK	1,2,3
Disable	Enable	RL+BL/n_min+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)- ODTLon-RD(tODTon(min)/tCK)+1	nCK	1
Enable	Enable	RL+BL/n_min+RU(tWCK2DQO(max)/tCK)+RD(tRPST/tCK)- ODTLon-RD(tODTon(min)/tCK)+1	nCK	1
NOTE 1		tWCK2DQO(max) is applied tWCK2DQO_LF(max) or tWCK2DQO_HF(max) depending on MRcc OP[3]: WCK Frequency Mode setting. MRcc OP[3]=0 <sub>B</sub> : tWCK2DQO_LF(max), MRcc OP[3]=1 <sub>B</sub> : tWCK2DQO_HF(max)		
NOTE 2		Need to add 1nCK to tRTW in case of not "MRdd OP[2:0]=000 <sub>B</sub> and MRdd OP[6:4]=000 <sub>B</sub> " (In case of DFEQ is enabled).		
NOTE 3		Need to add 1nCK to tRTW in case of Per-pin DFE Control:MRee OP[0]=1 <sub>B</sub> : (In case of Per Pin DFE is enabled).		
NOTE 4		Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.		

#### 8.4 Auto Precharge Command Timing Constraints

**Table 391 – Auto Precharge Command Timing Constraints for Same Banks in Same Bank Group**

Current CMD	Next CMD						
	ACTIVE	READ or READ with AP	READ Meta or READ Meta with AP	WRITE or WRITE with AP	WRITE Meta or WRITE Meta with AP	PRECHARGE	PRECHARGE ALL
READ with AP (BL24 or BL48)	nRTP <sup>1)</sup> + RU(tRPpb/tCK)	illegal	illegal	illegal	illegal	illegal	nRTP <sup>1)</sup>
WRITE with AP (BL24 or BL48)	WL + BL/n_max + nWTP <sup>3)</sup> + RU(tRPpb/tCK)	illegal	illegal	illegal	illegal	illegal	WL + BL/n_max + nWTP <sup>3)</sup>

**Table 392 – Command Timing Constraints for Different Banks in Same Bank Group**

Current CMD	Next CMD						
	ACTIVE	READ or READ with AP	READ Meta or READ Meta with AP	WRITE or WRITE with AP	WRITE Meta or WRITE Meta with AP	PRECHARGE	PRECHARGE ALL
READ with AP (BL24 or BL48)	2	BL/n	BL/n	tRTW <sup>2)</sup>	RL + BL/n_max -WL	2	nRTP <sup>4)</sup>
WRITE with AP (BL24 or BL48)	2	WL + BL/n_max + RU(tWTR_L/tCK)	WL + BL/n_max + RU(tWTR_L/tCK)	BL/n	BL/n	2	WL + BL/n_max + nWTP <sup>4)</sup>

#### 8.4 Auto Precharge Command Timing Constraints (cont'd)

**Table 393 – Command Timing Constraints for Different Banks in Different Bank Group**

Current CMD	Next CMD						
	ACTIVE	READ or READ with AP	READ Meta or READ Meta with AP	WRITE or WRITE with AP	WRITE Meta or WRITE Meta with AP	PRECHARGE	PRECHARGE ALL
READ with AP (BL24 or BL48)	2	BL/n	BL/n	tRTW <sup>2</sup>	RL + BL/n_min -WL	2	nRTP <sup>4</sup>
WRITE with AP (BL24 or BL48)	2	WL + BL/n_min + RU(tWTR_S/tCK)	WL + BL/n_min + RU(tWTR_S/tCK)	BL/n	BL/n	2	WL+ BL/n_max + nWTP <sup>4</sup>

## 8.5 CAS Command Timing Constraints

**Table 394 – CAS(WS\_AON) Command Timing Constraints**

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS=1, WS OFF=0)	POWER DOWN ENTRY (PDE)	tCMDPD	-	4
	ACTIVATE-1 (ACT-1)	2	-	4
	ACTIVATE-2 (ACT-2)	2	-	2, 4
	PRECHARGE (PRE) (Per Bank, All Banks)	2	-	4
	REFRESH (REF) (Per-2-Bank, All Banks)	2	-	4
	WRITE (WR_S/WR_L)	2	-	1, 3, 4
	READ (RD_S/RD_L)	2	-	1, 3, 4
	CAS (WS=1, WS_OFF=0)	illegal	illegal	1
	CAS (WS=0, WS_OFF=1)	Max(TBD, "tWCKENL_CAS + tWCKPRE_Static")	-	4
	MULTI PURPOSE COMMAND (MPC)	2	-	4
	SELF REFRESH ENTRY (SRE)	2	-	4
	SELF REFRESH EXIT (SRX)	2	-	4
	MODE REGISTER WRITE-1 (MRW-1)	2	-	4
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	2	-	1, 3, 4
	WRITE FIFO (WFF)			1, 3, 4
	READ FIFO (RFF)			1, 3, 4
	READ DQ CALIBRATION (RDC)			1, 3, 4
NOTE 1	Duplicated WCK2CK SYNC initiation is illegal with the next command (WS=1).			
NOTE 2	It is illegal unless an ACT-1 command is issued before the current command (CAS(WS=1)).			
NOTE 3	Valid WCK input is required until next command is issued. If WCK2CK SYNC status is off, new WCK2CK SYNC initiation is required.			
NOTE 4	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

## 8.5 CAS Command Timing Constraints (cont'd)

**Table 395 – CAS(WS\_OFF) Command Timing Constraints**

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
CAS (WS=0, WS_OFF=1)	POWER DOWN ENTRY (PDE)	tCMDPD	-	2
	ACTIVATE-1 (ACT-1)	2	-	2
	ACTIVATE-2 (ACT-2)	2	-	2
	PRECHARGE (PRE) (Per Bank, All Banks)	2	-	2
	REFRESH (REF) (Per-2-Bank, All Banks)	2	-	2
	WRITE (WR_S/WR_L)	TBD	-	1
	READ (RD_S/RD_L)	TBD	-	1
	CAS (WS=1, WS_OFF=0)	TBD		2
	CAS (WS=0, WS_OFF=1)	illegal	-	
	MULTI PURPOSE COMMAND (MPC)	2	-	2
	SELF REFRESH ENTRY (SRE)	2	-	2
	SELF REFRESH EXIT (SRX)	2	-	2
	MODE REGISTER WRITE-1 (MRW-1)	2	-	2
	MODE REGISTER WRITE-2 (MRW-2)	illegal	illegal	
	MODE REGISTER READ (MRR)	TBD	-	1
NOTE 1 New WCK2CK SYNC (WS=-1) should be initiated together. If not, it is illegal.				
NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.				

## 8.5 CAS Command Timing Constraints (cont'd)

**Table 396 – CAS(WS/WS\_OFF) Command Timing Constraints**

Current Command	Next Command	Timing Constraints (nCK)		Note
		Min	Max	
POWER DOWN ENTRY (PDE)	CAS(WS=1, WS_OFF=0) or CAS(WS=0, WS_OFF=1)	illegal	illegal	
ACTIVATE-1 (ACT-1)		2	-	6
ACTIVATE-2 (ACT-2)		2	-	6
PRECHARGE (PRE) (Per Bank, All Banks)		2	-	6
REFRESH (REF) (Per-2-Bank, All Banks)		2	-	6
WRITE (WR_S/WR_L)		WL + BL/n_min + RD(tWCKPST/tCK) +1	-	1, 6
READ (RD_S/RD_L)		RL + BL/n_min + RD(tWCKPST/tCK) +1	-	1, 6
MULTI PURPOSE COMMAND (MPC)		2	-	6
SELF REFRESH ENTRY (SRE)		2	-	6
SELF REFRESH EXIT (SRX)		tXSR	-	6
MODE REGISTER WRITE-1 (MRW-1)		illegal	illegal	
MODE REGISTER WRITE-2 (MRW-2)		tMRD	-	6
MODE REGISTER READ (MRR)		RL + BL/n_min + RD(tWCKPST/tCK) +1	-	1, 6
WRITE FIFO (WFF)		WL + BL/n_min + RD(tWCKPST/tCK) +1	-	1, 2, 4, 6
READ FIFO (RFF)		Max[(tRTRRD-1), (RL + BL/n_min + RD(tWCKPST/tCK) + 1)] or Max[(tRTW-1),(RL + BL/n_min + RD(tWCKPST/tCK) + 1)]	-	1, 3, 4, 5, 6
READ DQ CALIBRATION (RDC)		Max[(tRTRRD-1), (RL + BL/n_min + RD(tWCKPST/tCK) + 1)]	-	1, 3, 4, 6
NOTE 1	WCK2CK SYNC automatic off timing delay from a current command (RD, WR, MRR, WFF, RFF, RDC) is "WL (or RL) + BL/n_min + RD(tWCKPST/tCK)".			
NOTE 2	For CAS(WS_OFF=1), the min timing should be "WL + BL/n_min + RD(tWCKPST/tCK) + 1".			
NOTE 3	For CAS(WS_OFF=1), the min timing should be "RL + BL/n_min + RD(tWCKPST/tCK) + 1".			
NOTE 4	Refer to Timing Constraints for Training Commands.			
NOTE 5	"tRTRRD-1" timing (min) is applied to "CAS(WS) + RD/MRR/RDC" or "CAS(WS) + WR/MWR". "tRTW-1" timing(min) is applied in case of "CAS(WS) + WFF".			
NOTE 6	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

## 8.6 LPDDR6 MPC CK Sync Off Timing Constraints

MPC CK Sync off command can be issued in the following states.

- Idle
- Bank Active
- Dual Bank Refresh
- All Bank Refresh
- Self Refresh

Not to mention, LPDDR6 SDRAM doesn't accept any command except NOP that starts CK Sync after MPC CK Sync off command.

Even though WCK2CK sync state, MPC CK Sync off command can be issued. However, WCK2CK Sync state will be stopped.

**Table 397 – MPC CK Sync Off Timing Constraints**

Previous Command	Next Command	Min Delay	Unit	Note
SELF REFRESH ENTRY (SRE)	MPC CK SYNC Off	2	nCK	
SELF REFRESH EXIT (SRX)		tXSR	ns	
PRECHARGE ALL (PREab)		tRPab	-	
PRECHARGE Per Bank (PREpb)		tRPpb	-	
REFRESH (REF) (Dual Bank, All Banks)		2	nCK	
ACTIVATE-2 (ACT-2)		tRCDw	-	
WRITE (BL24/48/META)		WL + BL/n_min + RD(tWCKPST/tCK) +1	nCK	
WRITE w/ AP (BL24/48/META)		WL + BL/n_max + nWTP + RU(tRPpb/tCK)	nCK	
READ (BL24/48/META)		RL + BL/n_min + RD(tWCKPST/tCK) +1	nCK	
READ w/ AP (BL24/48/META)		max(RL+BL/n_min+RD(tWCKPST/tCK)+1, nRTP+RU(tRPpb/tCK))	nCK	
CAS (WS=1)		tWCKENL_FS + tWCKPRE_Static	nCK	
CAS(WS_OFF=1)		2	nCK	
MODE REGISTER READ (MRR)		RL + BL/n_max + RD(tWCKPST/tCK) +1	nCK	
MODE REGISTER WRITE-2 (MRW-2)		tMRD	ns	
WRITE FIFO (WFF)		WL + BL/n_min + RD(tWCKPST/tCK) +1	nCK	
READ FIFO (RFF)		RL + BL/n_min + RD(tWCKPST/tCK) +1	nCK	
READ DQ CALIBRATION (RDC)		RL + BL/n_min + RD(tWCKPST/tCK) +1	nCK	

**Table 397 — MPC CK Sync off Timing Constraints (cont'd)**

Previous Command	Next Command	Min Delay	Unit	Note
MPC Start WCK2DQI Interval Oscillator	MPC CK SYNC off	MR37 OP[7:0] WCK2DQI interval timer run time setting + tOSCODQI	ns	2
MPC Stop WCK2DQI Interval Oscillator		tOSCODQI	ns	
MPC Start WCK2DQO Interval Oscillator		MR40 OP[7:0] WCK2DQO interval timer run time setting + tOSCODQO	ns	3
MPC Stop WCK2DQO Interval Oscillator		tOSCODQO	ns	
MPC ZQ CAL Latch		tZQLAT	ns	
MPC CK SYNC off		illegal	-	
NOTE 1 Refer to Every other cycle command input clause 7.2 for delay time from NOP that CK Sync start to MPC CK SYNC Off command.				
NOTE 2 In case of WCK2DQI interval timer run time: MR37 OP[7:0]≠00000000 <sub>B</sub> .				
NOTE 3 In case of WCK2DQO interval timer run time: MR40 OP [7:0]≠00000000 <sub>B</sub> .				

## 8.7 Training-related Timing Constraints

LPDDR6 SDRAM can enter the Read or Write training state by issuing such as WRITE FIFO, READ FIFO and READ DQ Calibration. For those training commands that Read or Write the SDRAM, read latency (RL) and write latency (WL) are counted from the rising CK edge of each training command with the same timing relationship as any normal Read or Write command. Also, WCK synchronization should be applied in the same manner as normal Read or Write operation. WRITE FIFO, READ FIFO and READ DQ Calibration have a burst length of 24.

**Table 398 – Training-Related Timing Constraints**

Previous Command	Next Command	Min Delay	Unit	Note
WRITE (WR_S/WR_L)	WRITE FIFO	tWRWTR	nCK	1
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	WL+BL/n_max +RU(tWTR/tCK)	nCK	
READ (RD_S/RD_L)/MRR	WRITE FIFO	tRTRRD	nCK	3
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	tRTRRD	nCK	3
WRITE FIFO	WRITE (WR_S/WR_L)	Not Allowed	-	2
	WRITE FIFO	6	nCK	
	READ (RD_S/RD_L)/MRR	Not Allowed	-	2
	READ FIFO	Max(6nCK, WL+BL/n_max-RL +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT disabled (MR11 OP[3]=0 <sub>B</sub> )  Max(6nCK, WL+BL/n_max-RL+RU[tODToff(max)/tCK] +Max[RU(10ns/tCK), 4nCK]) @ NT-ODT enabled (MR11 OP[3]=1 <sub>B</sub> )	nCK	
	READ DQ Calibration	Not Allowed	-	2
	WRITE (WR_S/WR_L)	tRTRRD	nCK	3
READ FIFO	WRITE FIFO	tRTW	nCK	4, 5
	READ (RD_S/RD_L)/MRR	tRTRRD	nCK	3
	READ FIFO	6	nCK	
	READ DQ Calibration	tRTRRD	nCK	3
	WRITE (WR_S/WR_L)	tRTRRD	nCK	3
READ DQ Calibration	WRITE FIFO	tRTRRD	nCK	3
	READ (RD_S/RD_L)/MRR	tRTRRD	nCK	3
	READ FIFO	Not Allowed	-	2
	READ DQ Calibration	6	nCK	
	NOTE 1 tWRWTR = WL + BL/n_max + MAX[RU(7.5ns/tCK), 6nCK]			
NOTE 2 No commands are allowed between Write FIFO and Read FIFO except DES, NOP, REF, and MRW commands related to training parameters.				
NOTE 3 tRTRRD = RL + BL/n_max + MAX[RU(7.5ns/tCK), 6nCK]				
NOTE 4 tRTW is TBD and has a different value based on ODT state.				
NOTE 5 The value of tRTW that is applied for different banks in different bank groups should be used for this constraint.				

## 8.8 MRR/MRW Timing Constraints

**Table 399 – MRR/MRW Timing Constraints**

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Note	
MRR	MRR	tMRR			
	RD/RDA	RL +BL/n_max + RD(tWCKPST/tCK) + 1			
	WR/WRA	tRTW + 2	nCK	1,2	
	MRW	RL +BL/n_max+ Max[RU(tWCK2DQO(max)/tCK), RD(tWCKPST(max)/tCK)] + 2	nCK	1,4	
RD	MRR	RL +BL/n_max + RD(tWCKPST/tCK) + 1	nCK	1	
RDA		RL + nRTP + nACU + Max(RU(7.5ns/tCK), 6nCK)			
WR		WL+BL/n_max +RU(tWTR_L/tCK)	nCK	1,3	
WRA		WL+BL/n_max +RU(tWTR_L/tCK)+nACU+2	nCK	1,3	
MRW		tMRD			
PDX		tXP + tMRRI			
MRW	RD/RDA	tMRD			
	WR/WRA	tMRD			
	MRW	tMRW			
RD/RD FIFO/ RD DQ CAL	MRW	RL+RU(tWCK2DQO(max)/tCK)+BL/n_max+ Max(7.5ns,6nCK)	nCK	1	
RDA		RL+ RU(tWCK2DQO(max)/tCK)+BL/n_max +Max(7.5ns,6nCK)+ nRTP-6	nCK	1	
WR/WR FIFO		WL+BL/n_max +Max[RU(7.5ns/tCK), 6nCK]	nCK	1	
WRA		WL+BL/n_max +Max[RU(7.5ns/tCK), 6nCK]+ nWTP+nACU+2	nCK	1	
PRE/PREA		nACU+2	nCK		
<p>NOTE 1 The timing variable “BL/n” and “BL/n_max” are defined by the previous command and shown in the effective burst length table.</p>					
<p>NOTE 2 The Mode Register Read to Write Timing varies depending on DQ Bus Receiver On-Die-Termination (MR19 OP[2:0]), Non-Target DQ Bus Receiver On-Die-Termination (MR20 OP[2:0]), Read DQS (MR22 OP[1:0]), and Write link ECC Control (MR23 OP[1:0]). Refer to 8.3.1 for information about the Read to Write Timing (tRTW).</p>					
<p>NOTE 3 Refer to the core timing tables about tWTR in section 9.</p>					
<p>NOTE 4 If the ensuing MRW changes the settings of a Mode Register which affects data output condition and/or timing, the delay time from MRR to MRW must be as follows when NT-ODT is enabled (MR20 OP[2:0]≠000<sub>B</sub>) (Refer to Table 400 for the list of such Mode Registers.) RL+BL/n_max+Max[RU(tWCK2DQO(max)/tCK),RD(tWCKPST(max)/tCK)]+RU(ODT_RDon(max))+3</p>					

## 8.8 MRR/MRW Timing Constraints (cont'd)

**Table 400 – Mode Register which Affects Data Output Condition and/or Timing**

Function	MR# and Operand
RL/WL/nWTP/nRTP/nACU	MR1 OP[4:0]
PDDS	MR3 OP[7:5]
DBI-RD	MR3 OP[0]
EDBI-WR	MR3 OP[1]
RDQS PST Mode	MR10 OP[5]
WCK PST	MR22 OP[7:6]
RDQS PRE	MR10 OP[4:2]
RDQS PST Length	MR10 OP[7:6]
RDQS PS	MR10 OP[0]
SoC ODT	MR17 OP[2:0]
WCK ODT	MR19 OP[5:3]
WCK FM	MR11 OP[6]
WCK ON	MR22 OP[5]
RDQS	MR22 OP[1:0]
WCK Mode	MR22 OP[3:2]
WECC	MR23 OP[0]
WEDC	MR23 OP[1]
RECC/REDC	MR23 OP[2]
DQ NT-ODT	MR20 OP[2:0]

## 8.9 Rank to Rank Command Timing Constraints

**Table 401 – Command Timing Constraints in Case of Different Ranks, “DQ ODT ON and NT-ODT OFF” Setting for Both Ranks, WCK AON Mode ON**

Current CMD	Next CMD	
	READ (RD_S/RD_L) or RFF or MRR or RDC	WRITE (WR_S/WR_L) or WFF
READ (RD_S/RD_L) or RFF or MRR or RDC	BL/n_min + RU(tWCK2DQO_rank2rank(max)/tCK) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)	RL + BL/n_min + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1
WRITE (WR_S/WR_L) Or WFF	ODTLoff + RU(tODToff(max)/tCK) - RL	ODTLoff + RU(tODToff(max)/tCK) - ODTLon
NOTE 1 Next command is issued to a different rank. NOTE 2 The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies. NOTE 3 RD(tWCK2DQO(min)/tCK) = 0. NOTE 4 In case of RDQS disabled (MR22 OP[1:0]=00 <sub>B</sub> ), tRPRE and tRPST delay should be 0. NOTE 5 Rank to Rank command timing constraints in Table 401 is for LPDDR6 users design and consideration only. NOTE 6 Each rank CA should comply with LPDDR6 every other nCK command protocol.		

**Table 402 – Command Timing Constraints in Case of Different Ranks, “DQ ODT ON and NT-ODT ON” Setting for Both Ranks, WCK AON Mode ON**

Current CMD	Next CMD	
	READ (RD_S/RD_L) or RFF or MRR or RDC	WRITE (WR_S/WR_L) or WFF
READ (RD_S/RD_L) or RFF or MRR or RDC	ODTLon_RD - ODTLoff_RD	RL + BL/n_min + RU(tWCK2DQO(max)/tCK) - ODTLon - RD(tODTon(min)/tCK) + 1
WRITE (WR_S/WR_L) Or WFF	ODTLoff + RU(tODToff(max)/tCK) - RL	ODTLoff + RU(tODToff(max)/tCK) - ODTLon
NOTE 1 Next command is issued to a different rank. NOTE 2 RD(tWCK2DQO(min)/tCK) = 0. NOTE 3 Rank to Rank command timing constraints in Table 402 is for LPDDR6 users design and consideration only. NOTE 4 Each rank CA should comply with LPDDR6 every other nCK command protocol.		

## 8.9 Rank to Rank Command Timing Constraints (cont'd)

**Table 403 – Command Timing Constraints in Case of Different Ranks, “DQ ODT OFF and NT-ODT OFF” Setting for Both Ranks, WCK AON Mode ON**

Current CMD	Next CMD	
	READ (RD_S/RD_L) or RFF or MRR or RDC	WRITE (WR_S/WR_L) or WFF
READ (RD_S/RD_L) or RFF or MRR or RDC	BL/n_min + RU(tWCK2DQO_rank2rank(max)/tCK) + RU((tRPST+tRPRE - 0.5*tWCK)/tCK)	RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL
WRITE (WR_S/WR_L) Or WFF	WL + BL/n_min + 1 <sup>3)</sup> - RL	BL/n_min + 1 <sup>4)</sup>
NOTE 1 Next command is issued to a different rank. NOTE 2 The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies. NOTE 3 RU(tWCK2DQI(max)/tCK) = 1. NOTE 4 RU(tWCK2DQI_rank2rank(max)/tCK) = 1. The same voltage and temperature are applied to multi ranks DQ bytes per channel within a package consisting of the same design dies. If LPDDR6 DFE feature is enabled, an additional timing delay may be required like RU[(tWCK2DQI(max) + tDPRE)/tCK]. NOTE 5 In case of RDQS disabled (MR20 OP[1:0]=00B), tRPRE and tRPST delay should be 0. NOTE 6 Rank to Rank command timing constraints in Table 403 is for LPDDR6 users design and consideration only. NOTE 7 Each rank CA should comply with LPDDR6 every other nCK command protocol.		

**Table 404 – Command Timing Constraints in Case of Different Ranks, “DQ ODT ON and NT-ODT OFF” or “DQ ODT ON and NT-ODT ON” Setting for Both Ranks, WCK AON Mode OFF**

Current CMD	Next CMD	
	WRITE (WR_S/WR_L) or WFF	READ (RD_S/RD_L) or RFF or MRR or RDC
WRITE (WR_S/WR_L) Or WFF	WL + BL/n_min + max[RU(tODToff(max)/tCK), RU((tWCKPST -0.5*tWCK)/tCK)] - tWCKENL_WR	WL + BL/n_min + max[RU(tODToff(max)/tCK), RU((tWCKPST -0.5*tWCK)/tCK)] - tWCKENL_RD
READ (RD_S/RD_L) or RFF or MRR or RDC	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - min[(ODTLon + RD(tODTon(min)/tCK)), tWCKENL_WR]	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD
NOTE 1 Next command is issued to a different rank. NOTE 2 Rank to Rank command timing constraints in Table 404 is for LPDDR6 users design and consideration only. NOTE 3 Each rank CA should comply with LPDDR6 every other nCK command protocol.		

## 8.9 Rank to Rank Command Timing Constraints (cont'd)

**Table 405 – Command Timing Constraints in Case of Different Ranks, “DQ ODT OFF and NT-ODT OFF” Setting for Both Ranks, WCK AON Mode OFF**

Current CMD	Next CMD	
	WRITE (WR_S/WR_L) or WFF	READ (RD_S/RD_L) or RFF or MRR or RDC
WRITE (WR_S/WR_L) Or WFF	WL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR	WL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD
READ (RD_S/RD_L) or RFF or MRR or RDC	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_WR	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) - tWCKENL_RD
NOTE 1 Next command is issued to a different rank. NOTE 2 Rank to Rank command timing constraints in Table 405 is for LPDDR6 users design and consideration only. NOTE 3 Each rank CA should comply with LPDDR6 every other nCK command protocol.		

## 8.10 Meta Mode Command Timing Constraints

### 8.10.1 Meta Command Timing Constraints in Same Ranks

**Table 406 – LPDDR6 Meta Command Timing Constraints in Same Rank, Same BG**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	BL/n	WL+BL/n_max + RU(tWTR_L/tCK)	BL/n	WL+BL/n_max + RU(tWTR_L/tCK)
Read (RD-S, RD-L)	tRTW	BL/n	RL + BL/n_max -WL	BL/n
Meta Write (WR-M)	BL/n	WL+BL/n_max + RU(tWTR_L/tCK)	BL/n	WL+BL/n_max + RU(tWTR_L/tCK)
Meta Read (RD-M)	RL + BL/n_max -WL	BL/n	RL + BL/n_max -WL	BL/n

NOTE 1 WCK AON mode ON or OFF, “DQ ODT ON and NT ODT OFF” or “DQ ODT ON and NT-ODT ON” or “DQ ODT OFF and NT ODT OFF”.

NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.

**Table 407 – LPDDR6 Meta Command Timing Constraints in Same Rank, Different BG**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	BL/n	WL+BL/n_min + RU(tWTR_S/tCK)	BL/n	WL+BL/n_min + RU(tWTR_S/tCK)
Read (RD-S, RD-L)	tRTW	BL/n	RL + BL/n_min -WL	BL/n
Meta Write (WR-M)	BL/n	WL+BL/n_min + RU(tWTR_S/tCK)	BL/n	WL+BL/n_min + RU(tWTR_S/tCK)
Meta Read (RD-M)	RL + BL/n_min -WL	BL/n	RL + BL/n_min -WL	BL/n

NOTE 1 WCK AON mode ON or OFF, “DQ ODT ON and NT ODT OFF” or “DQ ODT ON and NT-ODT ON” or “DQ ODT OFF and NT ODT OFF”.

NOTE 2 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.

### 8.10.2 Meta Command Timing Constraints in Different Ranks

**Table 408 – LPDDR6 Meta Command Timing Constraints in Different Ranks  
(WCK AON Mode OFF, “DQ ODT ON and NT ODT OFF” or “DQ ODT ON and NT-ODT ON”)**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	WL + BL/n_min + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] – tWCKEN_WR	WL + BL/n_min + max[RU(tODToff(max)/tCK), RU((tWCKPST - 0.5*tWCK)/tCK)] – tWCKEN_RD	2nCK <sup>2)</sup> Or 4nCK <sup>3)</sup>	2nCK
Read (RD-S, RD-L)	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) – min[(ODTOn + RD(tODTon(min)/tCK)), tWCKENL_WR]	RL + BL/n_min + RU((tWCKPST – 0.5*tWCK)/tCK) – tWCKENL_RD	2nCK	2nCK
Meta Write (WR-M)	2nCK <sup>2)</sup> Or 4nCK <sup>3)</sup>	2nCK	2nCK	2nCK
Meta Read (RD-M)	2nCK	2nCK	2nCK	2nCK
NOTE 1 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol. NOTE 2 Write NT-ODT is disabled. NOTE 3 Write NT-ODT is enabled.				

**Table 409 — LPDDR6 Meta Command Timing Constraints in Different Ranks  
(WCK AON Mode OFF, “DQ ODT OFF and NT ODT OFF”)**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	WL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) – tWCKEN_WR	WL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) – tWCKEN_RD	2nCK	2nCK
Read (RD-S, RD-L)	RL + BL/n_min + RU((tWCKPST - 0.5*tWCK)/tCK) – tWCKENL_WR	RL + BL/n_min + RU((tWCKPST – 0.5*tWCK)/tCK) – tWCKENL_RD	2nCK	2nCK
Meta Write (WR-M)	2nCK	2nCK	2nCK	2nCK
Meta Read RD-M)	2nCK	2nCK	2nCK	2nCK
NOTE 1 Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.				

### 8.10.2 Meta Command Timing Constraints in Different Ranks (cont'd)

**Table 410 – LPDDR6 Meta Command Timing Constraints in Different Ranks  
(WCK AON Mode ON, “DQ ODT ON and NT ODT OFF” or “DQ ODT ON and NT-ODT ON”)**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	ODTloff + RU(tODT(max)/tCK) - ODTlon	ODTloff + RU(tODT(max)/tCK) - RL	2nCK <sup>2</sup> Or 4nCK <sup>3</sup>	2nCK
Read (RD-S, RD-L)	RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - ODTlon - RD(tODTon(min)/tCK) + 1	BL/n_min + RU(tWCK2DQO_rank2rank(max)/tCK) + RU((tRPST + tRPRE - 0.5*tWCK)/tCK) <sup>4</sup> Or ODTlon_RD - ODTloff_RD <sup>5</sup>	2nCK	2nCK
Meta Write (WR-M)	2nCK <sup>2</sup> Or 4nCK <sup>3</sup>	2nCK	2nCK	2nCK
Meta Read (RD-M)	2nCK	2nCK	2nCK	2nCK
NOTE 1	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			
NOTE 2	Write NT-ODT is disabled.			
NOTE 3	Write NT-ODT is enabled.			
NOTE 4	DQ ODT ON and NT-ODT OFF			
NOTE 5	DQ ODT ON and NT-ODT ON			

**Table 411 – LPDDR6 Meta Command Timing Constraints in Different Ranks  
(WCK AON Mode ON, “DQ ODT OFF and NT ODT OFF”)**

Current CMD	Next CMD			
	Write (WR-S, WR-L)	Read (RD-S, RD-L)	Meta Write (WR-M)	Meta Read (RD-M)
Write (WR-S, WR-L)	BL/n_min + 1	WL + BL/n_min + 1 - RL	2nCK	2nCK
Read (RD-S, RD-L)	RL + BL/n_min + RU(tWCK2DQO(max)/tCK) + RU((tRPST - 0.5*tWCK)/tCK) - WL	BL/n_min + RU(tWCK2DQO_rank2rank(max)/tCK) + RU((tRPST + tRPRE - 0.5*tWCK)/tCK)	2nCK	2nCK
Meta Write (WR-M)	2nCK	2nCK	2nCK	2nCK
Meta Read (RD-M)	2nCK	2nCK	2nCK	2nCK
NOTE 1	Even nCK command gap is required to comply with LPDDR6 every other nCK command protocol.			

## 8.11 Efficiency AND Meta Modes Command Timing Constraints

### 8.11.1 Efficiency and Meta Modes Command Timing Constraints between Same Die Sub-Channels

**Table 412 – LPDDR6 Efficiency Meta Mode Command Timing Constraints between Same Die Sub-Channels**

Current CMD	Next CMD					
	ACTIVE	WRITE (WR-S, WR-L)	READ (RD-S, RD-L)	META WRITE (WR-M)	META READ (RD-M)	PRECHARGE
ACTIVE	4	2	2	2	2	2
WRITE (WR-S, WR-L)	2	BL/n	WL+BL/n_min + RU(tWTR_S/tCK)	4	2	2
READ (RD-S, RD-L)	2	tRTW	BL/n	2	4	2
META WRITE (WR-M)	2	4	2	4	2	2
META READ (RD-M)	2	2	4	2	4	2
PRECHARGE	2	2	2	2	2	4

## 9 AC Timing

### 9.1 Core AC Timing Parameters for LPDDR6

The tables' summary in this section is shown below.

**Table 413 – Core AC Timing Tables Summary**

#	DVFSL	Link-ECC/EDC	Static/Dynamic Efficiency mode
Table 414	Disabled	Disabled	Disabled
Table 416	Disabled	Disabled	Enabled
Table 417	Disabled	Enabled	Disabled
Table 418	Disabled	Enabled	Enabled
Table 419	Enabled	Disabled	Disabled
Table 421	Enabled	Disabled	Enabled
Table 422	Enabled	Enabled	Disabled
Table 423	Enabled	Enabled	Enabled

**Table 414 – Core AC Timing: DVFSL is Disabled, Link Protection is Disabled and Static/Dynamic Efficiency Mode is Disabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
ACTIVATE to ACTIVATE Command period (same bank)	tRC	Min	tRAS+tRPab with all-bank precharge tRAS+tRPpb with per-bank precharge	-	
RAS to CAS delay for Write	tRCDw	Min	Max (8ns, 2nCK)	-	
RAS to CAS delay for Read	tRCDr	Min	Max (18ns, 2nCK)	-	
Activation Counter Update time	tACU	Min	22	ns	
Row pre-charge time (all Banks)	tRPab	Min	nACU + Max(21ns, 4nCK)	-	1
Row pre-charge time (single Banks)	tRPpb	Min	nACU + Max(18ns, 4nCK)	-	1
Row Active time	tRAS	Min	Max(20ns, 4nCK)	-	2
		Max	Min ((9 * tREFI * Refresh Multiplier) - tACU, 70.2us - tACU)	-	
Write to PRECHARGE delay	tWTP	Min	Max(12ns, 6nCK)	-	
Active bank-A to active bank-B	tRRD	Min	Max (3.75ns, 4nCK)	-	
Four-bank ACTIVATE window	tFAW	Min	4*tRRD	-	
Read to PRECHARGE delay	tRTP	Min	BL/n + 1.25ns	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(6.25ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(12ns, 6nCK)	-	
PRECHARGE to PRECHARGE delay	tPPD	Min	4	nCK	
NOTE 1 nACU value (Clock Counts) is unique for each speed grade. Refer to concrete value for Table 415.					
NOTE 2 Minimum analog delay time from ACT command to "Precharge All/Per bank" command is "42ns - tACU (22 ns)".					

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 415 – nACU: DVFSL is Disabled**

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nACU [nCK]	Notes
80	1067	20	267	6	
1067	1600	267	400	9	
1600	2133	400	533	12	
2133	2750	533	688	16	
2750	3200	688	800	18	
3200	3750	800	938	21	
3750	4267	938	1067	24	
4267	4800	1067	1200	27	
4800	5500	1200	1375	31	
5500	6400	1375	1600	36	
6400	7500	1600	1875	42	
7500	8533	1875	2133	47	
8533	9600	2133	2400	53	
9600	10667	2400	2667	59	
10667	11733	2667	2933	TBD	
11733	12800	2933	3200	TBD	
12800	14400	3200	3600	TBD	

NOTE 1 nACU value is calculated as follows: Round-Up(tACU/tCK @ Value at minimum clock period at corresponding speed grade.

For example, @upper Clock Frequency Limit = 400 MHz (tCK=2.5 ns), nACU=RU(22/2.5)=9.

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 416 – Core AC Timing: DVFSL is Disabled, Link protection is Disabled and Static/Dynamic Efficiency Mode is Enabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
Write to PRECHARGE delay	tWTP	Min	Max(14ns, 6nCK)	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(8.25ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(14ns, 6nCK)	-	

NOTE 1 The rest of the Core AC timing is the same as Core AC Timing (Basic): See Table 414

**Table 417 – Core AC Timing: DVFSL is Disabled, Link Protection is Enabled and Static/Dynamic Efficiency Mode is Disabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
Write to PRECHARGE delay	tWTP	Min	Max(16ns, 6nCK)	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(10.25ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(16ns, 6nCK)	-	

NOTE 1 The rest of the Core AC timing is the same as Core AC Timing (Basic): See Table 414

**Table 418 – Core AC Timing: DVFSL is Disabled, Link Protection is Enabled and Static/Dynamic Efficiency Mode is Enabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
Write to PRECHARGE delay	tWTP	Min	Max(18ns, 6nCK)	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(12.25ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(18ns, 6nCK)	-	

NOTE 1 The rest of the Core AC timing is the same as Core AC Timing (Basic): See Table 414

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 419 – Core AC Timing: DVFSL is Enabled, Link Protection is Disabled and Static/Dynamic Efficiency Mode is Disabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
ACTIVATE to ACTIVATE Command period (same bank)	tRC	Min	tRAS+tRPab with all-bank precharge tRAS+tRPpb with per-bank precharge	-	
RAS to CAS delay for Write	tRCDw	Min	Max (9.2ns, 2nCK)	-	
RAS to CAS delay for Read	tRCDr	Min	Max (20.7ns, 2nCK)	-	
Activation Counter Update time	tACU	Min	25.3	ns	
Row pre-charge time (all Banks)	tRPab	Min	nACU + Max(24.2ns, 4nCK)	-	1
Row pre-charge time (single Banks)	tRPpb	Min	nACU + Max(20.7ns, 4nCK)	-	1
Row Active time	tRAS	Min	Max(20ns, 4nCK)	-	2
		Max	Min ((9 * tREFI * Refresh Multiplier) - tACU, 70.2us - tACU)	-	
Write to PRECHARGE delay	tWTP	Min	Max(13.8ns, 6nCK)	-	
Active bank-A to active bank-B	tRRD	Min	Max (3.75ns, 4nCK)	-	
Four-bank ACTIVATE window	tFAW	Min	4*tRRD	-	
Read to PRECHARGE delay	tRTP	Min	BL/n + 1.5ns	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(7.2ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(13.8ns, 6nCK)	-	
PRECHARGE to PRECHARGE delay	tPPD	Min	4	nCK	
NOTE 1 nACU value (Clock Counts) is unique for each speed grade. Refer to concrete value for Table 420.					
NOTE 2 Minimum analog delay time from ACT command to "Precharge All/Per bank" command is "42ns - tACU (25.3ns)".					

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 420 — nACU: DVFSL is Enabled**

Data Rate Lower Limit (Mbps)	Data Rate Upper Limit (Mbps)	Lower Clock Frequency Limit (>) (MHz)	Upper Clock Frequency Limit (<=) (MHz)	nACU [nCK]	Notes
80	1067	20	267	7	
1067	1600	267	400	11	
1600	2133	400	533	14	
2133	2750	533	688	18	
2750	3200	688	800	21	
3200	3750	800	938	24	
3750	4267	938	1067	27	
4267	4800	1067	1200	31	
4800	5500	1200	1375	35	
5500	6400	1375	1600	41	
6400	7500	1600	1875	48	
7500	8533	1875	2133	54	
8533	9600	2133	2400	61	
9600	10667	2400	2667	68	
10667	11733	2667	2933	TBD	
11733	12800	2933	3200	TBD	
12800	14400	3200	3600	TBD	
NOTE 1 nACU value is calculated as follows: Round-Up(tACU/tCK @ Value at minimum clock period at corresponding speed grade.					
For example, @upper Clock Frequency Limit = 400 MHz (tCK=2.5 ns), nACU=RU(25.3/2.5)=11.					

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 421 — Core AC Timing: DVFSL is Enabled, Link Protection is Disabled and Static/Dynamic Efficiency Mode is Enabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
ACTIVATE to ACTIVATE Command period (same bank)	tRC	Min	tRAS+tRPab with all-bank precharge tRAS+tRPpb with per-bank precharge	-	
RAS to CAS delay for Write	tRCDw	Min	Max (9.2ns, 2nCK)	-	
RAS to CAS delay for Read	tRCDr	Min	Max (20.7ns, 2nCK)	-	
Activation Counter Update time	tACU	Min	25.3	ns	
Row pre-charge time (all Banks)	tRPab	Min	nACU + Max(24.2ns, 4nCK)	-	1
Row pre-charge time (single Banks)	tRPpb	Min	nACU + Max(20.7ns, 4nCK)	-	1
		Min	Max(20ns, 4nCK)	-	2
Row Active time	tRAS	Max	Min ((9 * tREFI * Refresh Multiplier) - tACU, 70.2us - tACU)	-	
Write to PRECHARGE delay	tWTP	Min	Max(16.1ns, 6nCK)	-	
Active bank-A to active bank-B	tRRD	Min	Max (3.75ns, 4nCK)	-	
Four-bank ACTIVATE window	tFAW	Min	4*tRRD	-	
Read to PRECHARGE delay	tRTP	Min	BL/n + 1.5ns	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(9.5ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(16.1ns, 6nCK)	-	
PRECHARGE to PRECHARGE delay	tPPD	Min	4	nCK	
NOTE 1 nACU value (Clock Counts) is unique for each speed grade. Refer to concrete value for Table 420.					
NOTE 2 Minimum analog delay time from ACT command to "Precharge All/Per bank" command is "42ns - tACU (25.3ns)".					

**Table 422 — Core AC Timing: DVFSL is Enabled, Link Protection is Enabled and Static/Dynamic Efficiency Mode is Disabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
ACTIVATE to ACTIVATE Command period (same bank)	tRC	Min	tRAS+tRPab with all-bank precharge tRAS+tRPpb with per-bank precharge	-	
RAS to CAS delay for Write	tRCDw	Min	Max (9.2ns, 2nCK)	-	
RAS to CAS delay for Read	tRCDr	Min	Max (20.7ns, 2nCK)	-	
Activation Counter Update time	tACU	Min	25.3	ns	
Row pre-charge time (all Banks)	tRPab	Min	nACU + Max(24.2ns, 4nCK)	-	1
Row pre-charge time (single Banks)	tRPpb	Min	nACU + Max(20.7ns, 4nCK)	-	1
		Min	Max(20ns, 4nCK)	-	2
Row Active time	tRAS	Max	Min ((9 * tREFI * Refresh Multiplier) - tACU, 70.2us - tACU)	-	
Write to PRECHARGE delay	tWTP	Min	Max(18.4ns, 6nCK)	-	
Active bank-A to active bank-B	tRRD	Min	Max (3.75ns, 4nCK)	-	
Four-bank ACTIVATE window	tFAW	Min	4*tRRD	-	
Read to PRECHARGE delay	tRTP	Min	BL/n + 1.5ns	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(11.8ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(18.4ns, 6nCK)	-	
PRECHARGE to PRECHARGE delay	tPPD	Min	4	nCK	
NOTE 1 nACU value (Clock Counts) is unique for each speed grade. Refer to concrete value for Table 420.					
NOTE 2 Minimum analog delay time from ACT command to "Precharge All/Per bank" command is "42ns - tACU (25.3ns)".					

## 9.1 Core AC Timing Parameters for LPDDR6 (cont'd)

**Table 423 — Core AC Timing: DVFSL is Enabled, Link Protection is Enabled and Static/Dynamic Efficiency Mode is Enabled**

Item	Symbol	Min/Max	CK Frequency (MHz)	Unit	Notes
			Up to 2667		
ACTIVATE to ACTIVATE Command period (same bank)	tRC	Min	tRAS+tRPab with all-bank precharge tRAS+tRPpb with per-bank precharge	-	
RAS to CAS delay for Write	tRCDw	Min	Max (9.2ns, 2nCK)	-	
RAS to CAS delay for Read	tRCDr	Min	Max (20.7ns, 2nCK)	-	
Activation Counter Update time	tACU	Min	25.3	ns	
Row pre-charge time (all Banks)	tRPab	Min	nACU + Max(24.2ns, 4nCK)	-	1
Row pre-charge time (single Banks)	tRPpb	Min	nACU + Max(20.7ns, 4nCK)	-	1
Row Active time	tRAS	Min	Max(20ns, 4nCK)	-	2
		Max	Min ((9 * tREFI * Refresh Multiplier) - tACU, 70.2us - tACU)	-	
Write to PRECHARGE delay	tWTP	Min	Max(20.7ns, 6nCK)	-	
Active bank-A to active bank-B	tRRD	Min	Max (3.75ns, 4nCK)	-	
Four-bank ACTIVATE window	tFAW	Min	4*tRRD	-	
Read to PRECHARGE delay	tRTP	Min	BL/n + 1.5ns	-	
WRITE to READ delay (Different BG)	tWTR_S	Min	Max(14.1ns, 6nCK)	-	
WRITE to READ delay (Same BG)	tWTR_L	Min	Max(20.7ns, 6nCK)	-	
PRECHARGE to PRECHARGE delay	tPPD	Min	4	nCK	
NOTE 1 nACU value (Clock Counts) is unique for each speed grade. Refer to concrete value for Table 420.					
NOTE 2 Minimum analog delay time from ACT command to "Precharge All/Per bank" command is "42ns - tACU (25.3ns)".					

## 9.2 Core AC Temperature Derating for AC Timing

**Table 424 – Temperature Derating AC Timing**

Item	Symbol	Min/ Max	CK Frequency (MHz)		Unit	Notes
			Up to 10667 Mbps ≤ 10667 Mbps	Beyond 10667 Mbps > 10667 Mbps		
Temperature Derating						
DQ to WCK input offset	tWCK2DQI_HF	Max	TBD	TBD	ps	
	tWCK2DQI_LF	Max	TBD	TBD	ps	
	tWCK2DQI_LF_L	Max	TBD	TBD	ps	
WCK to DQ output offset	tWCK2DQO_HF	Max	TBD	TBD	ps	
	tWCK2DQO_LF	Max	TBD	TBD	ps	
	tWCK2DQO_LF_L	Max	TBD	TBD	ps	
RAS-to-CAS delay	tRCD	Min	TBD	TBD	ns	
ACTIVATE-to- ACTIVATE command period (same bank)	tRC	Min	TBD	TBD	ns	
Row active time	tRAS	Min	TBD	TBD	ns	
Row precharge time (all banks)	tRPab	Min	TBD	TBD	ns	
Row precharge time (single bank)	tRPpb	Min	TBD	TBD	ns	
NOTE 1 Timing derating applies for operation between greater than 85 °C (>85 °C) to 105 °C (≤105 °C).						
NOTE 2 Consult the memory vendor when using at greater than 105 °C.						
NOTE 3 The derated values are required only when MR4 OP[4:0] are 01101 <sub>B</sub> or 01111 <sub>B</sub> .						

## 9.3 Rank to Rank AC Parameter

TBD

## 10 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this standard is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 425 — Absolute Maximum DC Ratings**

Parameter	Symbol	Min	Max	Unit	Note
VDD1 Supply Voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2C Supply Voltage relative to VSS	VDD2C	-0.4	1.2	V	1
VDD2D Supply Voltage relative to VSS	VDD2D	-0.4	1.2	V	1
VDDQ Supply Voltage relative to VSS	VDDQ	-0.4	1.2	V	1
Voltage on Any Ball Except VDD1 relative to VSS	VIN, VOUT	-0.4	1.2	V	
Storage Temperature	TSTG	-55	125	°C	2

NOTE 1 See 4.1 relationships between power supplies.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the LPDDR6 device. For the measurement conditions, please refer to JESD51-2A.

## 11 AC and DC Operating Condition

## **11.1 Recommended DC Operating Conditions**

**Table 426 – Recommended Voltage Operating Conditions**

**Table 426 — Recommended Voltage Operating Conditions (cont'd)**

- NOTE 1 VDD1 uses significantly less current than VDD2C and VDD2D.
- NOTE 2 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW. Refer to Figure 217.
- NOTE 3 The Step-up range of VDD2C is defined for supporting high data rate DRAM operations. Its necessity is indicated in the read only mode register MR21 OP[1:0].
- NOTE 4 Allowable Range is valid only when Step-up range is supported, and it is valid when DVFSH is enabled. 115 mV tolerance (-30 mV/+85 mV) is applied to VDD2C allowable range during transition. Refer to Figure 218. For further detail procedure of DVFSH, please refer the clause 11.2.
- NOTE 5 The Step-down range of VDD2D is defined for assisting low-power DRAM operations. Its supportability or applicable WCK frequency range are indicated in the read only mode register MR21 OP[5:4]. The Step-down range requires the core AC parameters relaxations as well. Please refer to the clause 11.3 for further detail of DVFSL.
- NOTE 6 Allowable Range is valid only when Step-down range is supported, and it is valid when DVFSL is enabled. 115 mV tolerance (-30 mV/+85 mV) is applied to VDD2D allowable range during transition. Refer to Figure 219. For further detail procedure of DVFSL, please refer the clause 11.3.
- NOTE 7 The Range-1 is intended for IO operation with both ODT enabled and disabled.
- NOTE 8 The Range-2 is intended for IO operation with ODT disabled.
- NOTE 9 IO operation at VDDQ levels between outside SPEC Range-1 or SPEC Range-2 is allowed with ODT disabled.
- NOTE 10 Allowable range is valid only when DVFSQ enabled.
- NOTE 11 100mV tolerance (-30 mV/+70 mV) is applied to VDDQ allowable ranges during transition. Refer to Figure 220.
- NOTE 12 ZQ calibration is optimized at VDDQ = 0.5 V.
- NOTE 13 Z(f) is defined for all pins per voltage domain per sub-channel. Z(f) does not include the DRAM package and silicon die. Z(f) is the impedance of an effective equivalent PDN network as if it were connected only to this sub-channel, not shared with other sub-channels.
- NOTE 14 Consult the memory vendor for further voltage scaling.
- NOTE 15 The Step-up range of VDD2D is defined for supporting high data rate DRAM operations. Its necessity is indicated in the read only mode register MR21 OP[3:2].
- NOTE 16 Allowable Range is valid only when Step-up range is supported, and it is valid when DVFSB is enabled. 115 mV tolerance (-30 mV/+85 mV) is applied to VDD2D allowable range during transition. Refer to Figure 221. For further detail procedure of DVFSB, please refer to clause 11.4.

## 11.1 Recommended DC Operating Conditions (cont'd)

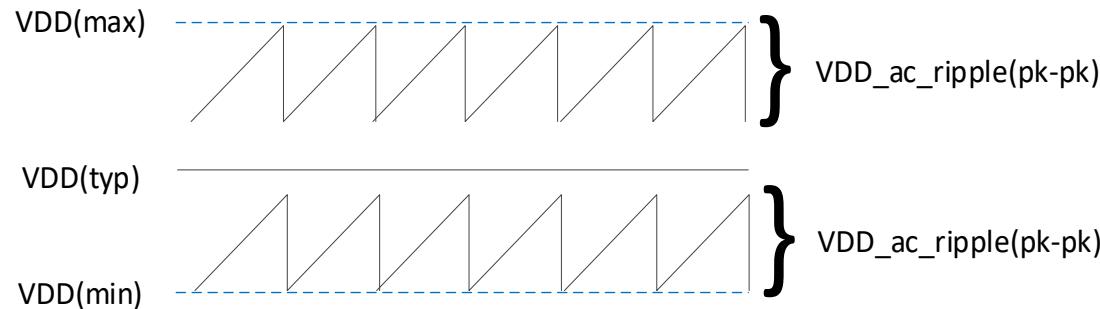


Figure 217 — DC Voltage Range

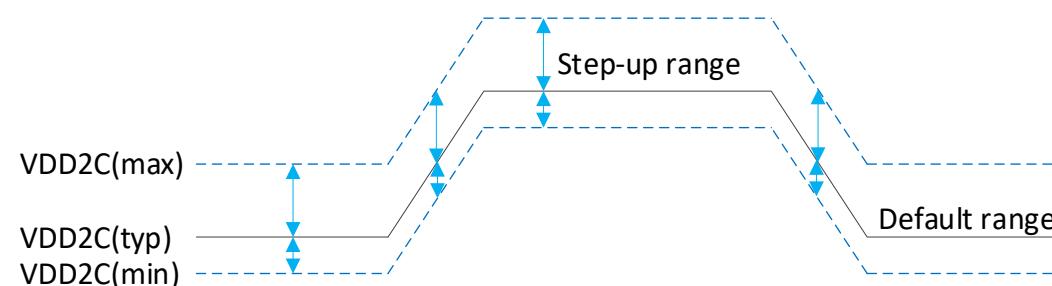


Figure 218 — VDD2C Tolerance Definition in Allowable Range

### 11.1 Recommended DC Operating Conditions (cont'd)

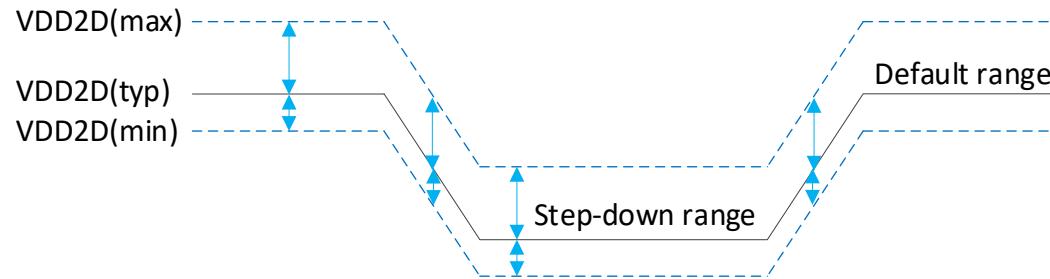


Figure 219 – VDD2D Tolerance Definition in Allowable Range for DVFSL

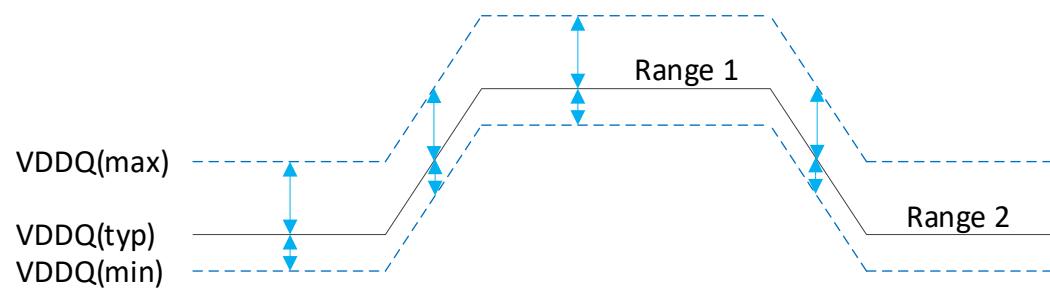


Figure 220 – VDDQ Tolerance Definition in Allowable Range

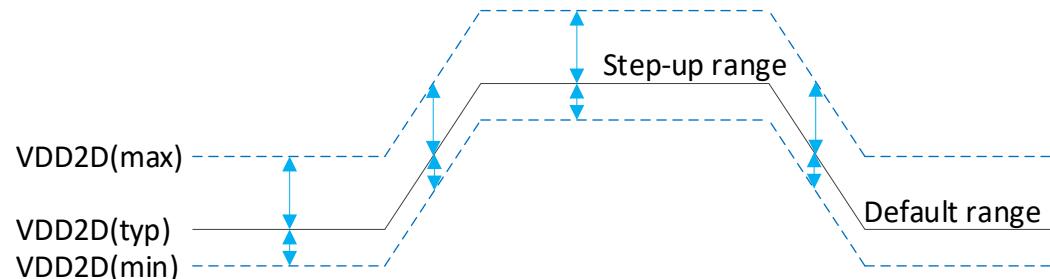


Figure 221 – VDD2D Tolerance Definition in Allowable Range for DVFSB

### 11.1 Recommended DC Operating Conditions (cont'd)

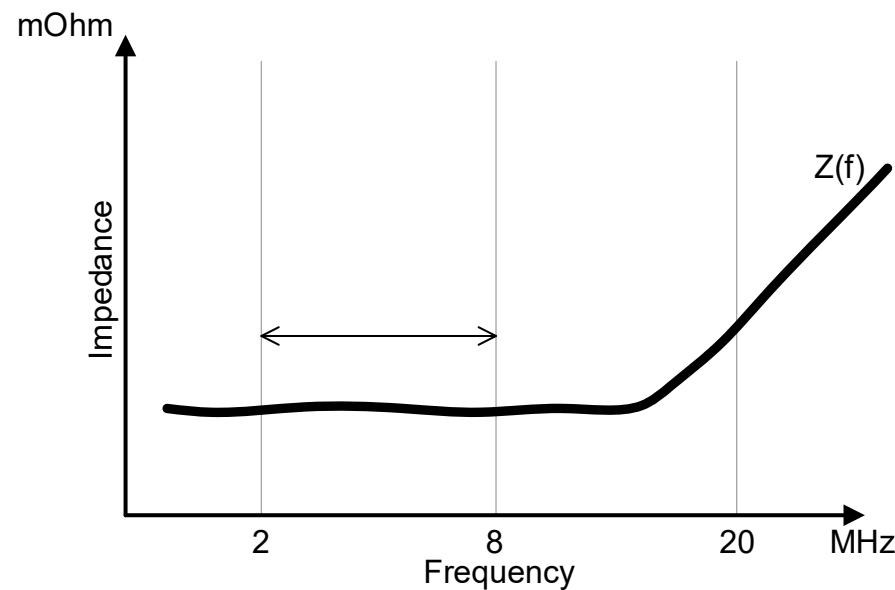


Figure 222 – Zprofile  $Z(f)$  of the System at the DRAM Package Solder Ball (without the DRAM Component)

## 11.2 DVFSH (Dynamic Voltage Frequency Scaling on High Voltage Rail) Mode

LPDDR6 devices can allow the VDD2C to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Actual DRAM command sequence can be optimized depending on system, as long as DRAM timing parameters and DVFSH requirements are satisfied. Some guidelines are:

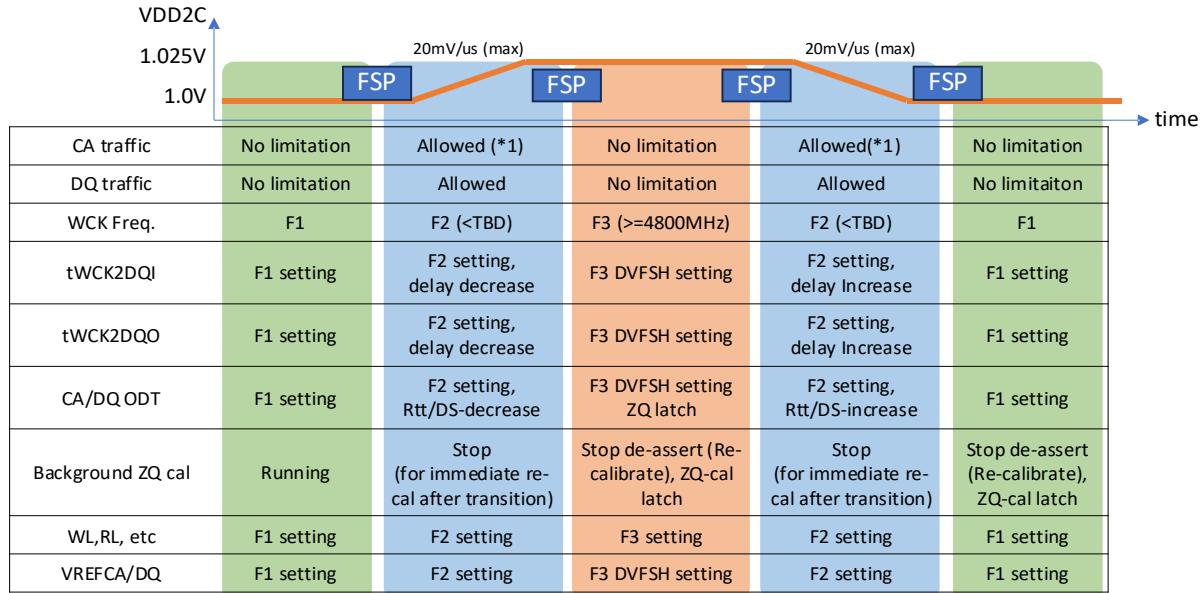
If operation of the LPDDR6 SDRAM will be halted during the VDD2C voltage ramp

- 1) MR11 OP[2] must be set to 1 to enable DVFSH and to ramp VDD2C to the step-up range.  
Switching MR11 OP[2] is allowed only through the FSP procedure.
- 2) The device must be placed in power-down mode or CS held low until the voltage ramp is complete
- 3) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-up range
- 4) FSP change to appropriate new settings should occur before operation at the new level

If operation of the LPDDR6 SDRAM during the VDD2C voltage ramp is intended

- 1) MR11 OP[2] must be set to 1 to enable DVFSH and to ramp VDD2C to the step-up range.  
Switching MR11 OP[2] is allowed only through the FSP procedure.
- 2) The device should be operated at settings and speeds suitable for the ramping VDD2C level
- 3) The VDD2C voltage ramp should always be equal or slower than the specified limits
- 4) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-up range
- 5) FSP change to appropriate new settings should occur before operation at the new level
- 6) Any commands listed below cannot be issued during voltage transition

Overview of the DVFSH mode requirements and sequence are shown in Figure 223.



NOTE 1 Any commands listed as TBD are not allowed.

**Figure 223 – DVFSH Requirements and Sequence Overview**

### 11.2.1 DVFSH Low-to-High Transition

An example of a recommended DVFSH low-to-high transition sequence is:

- 1) Operating at WCK freq.=F1 with VDD2C in the default range
- 2) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 3) FSP switch from WCK freq.=F1 to WCK freq.=F2 suitable for VDD2C ramping up transition, MR11 OP[2]=1 to indicate DVFSH enabled
- 4) Wait tFC (stall traffic)
- 5) Issue MRW MR13 to set VRCG = 0
- 6) Wait tVRCG\_DISABLE (stall traffic)
- 7) Issue MRW MR28 to set ZQ Stop=1 to disable background calibration
- 8) Wait tZQSTOP
- 9) Start ramping up VDD2C to the step-up range
- 10) Continue operation at WCK freq.=F2 with VDD2C in the allowable range
- 11) Complete VDD2C ramping up and VDD2C within the step-up range
- 12) Issue MRW MR28 to set ZQ Stop=0 to enable and initiate background calibration with new voltage level
- 13) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 14) FSP switch from WCK freq.=F2 to DVFSH enabled target WCK freq.=F3
- 15) Wait tFC (stall traffic)
- 16) Issue MRW MR13 to set VRCG = 0 to disable VRCG
- 17) Wait tVRCG\_DISABLE (stall traffic)
- 18) Issue ZQ latch once tZQCALx expired from the last ZQ Stop reset command
- 19) Wait tZQLATCH
- 20) Continue operation with VDD2C in the step-up range

### 11.2.2 DVFSH High-to-Low Transition

An example of a recommended DVFSH low-to-high transition sequence is:

- 1) Operating at WCK frequency=F3 with VDD2C in the step-up range and DVFSH enabled
- 2) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 3) FSP switch from WCK frequency=F3 to WCK frequency=F2 suitable for VDD2C ramping transition
- 4) Wait tFC (stall traffic)
- 5) Issue MRW MR13 to set VRCG = 0
- 6) Wait tVRCG\_DISABLE (stall traffic)
- 7) Issue MRW MR28 to set ZQ Stop=1 to disable background calibration
- 8) Wait tZQSTOP
- 9) Start ramping VDD2C to the step-down range
- 10) Continue operation at WCK freq.=F2 with VDD2C in the allowable range
- 11) Complete VDD2C ramping and VDD2C within the default range
- 12) Issue MRW MR28 to set ZQ Stop=0 to enable and initiate background calibration with new voltage level
- 13) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 14) FSP switch from WCK freq.=F2 to DVFSH disabled target WCK freq.=F1, MR11 OP[2]=0 to indicate DVFSH disabled
- 15) Wait tFC (stall traffic)
- 16) Issue MRW MR13 to set VRCG = 0 to disable VRCG
- 17) Wait tVRCG\_DISABLE (stall traffic)
- 18) Issue ZQ latch once tZQCALx expired from the last ZQ Stop reset command
- 19) Wait tZQLATCH
- 20) Issue MRW MR11 OP[2] to disable DVFSH
- 21) Continue operation with VDD2C in the default range

### 11.2.3 DVFSH VDD2C Voltage Transition Slew Rate

In DVFSH Mode, the VDD2C voltage ramp must conform to the limits in Table 427.

**Table 427 — VDD2C Voltage Transition Slew Rate**

Parameter	Symbol	Max/Min	Value	Units
VDD2C Slew Rate	VDD2CSR1	Max	20	mV/ $\mu$ s

## 11.3 DVFSL (Dynamic Voltage Frequency Scaling on Low Voltage Rail) Mode

LPDDR6 devices can allow the VDD2D to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Actual DRAM command sequence can be optimized depending on system as long as DRAM timing parameters and DVFSL requirements are satisfied. Some guidelines are:

If operation of the LPDDR6 SDRAM will be halted during the VDD2D voltage ramp

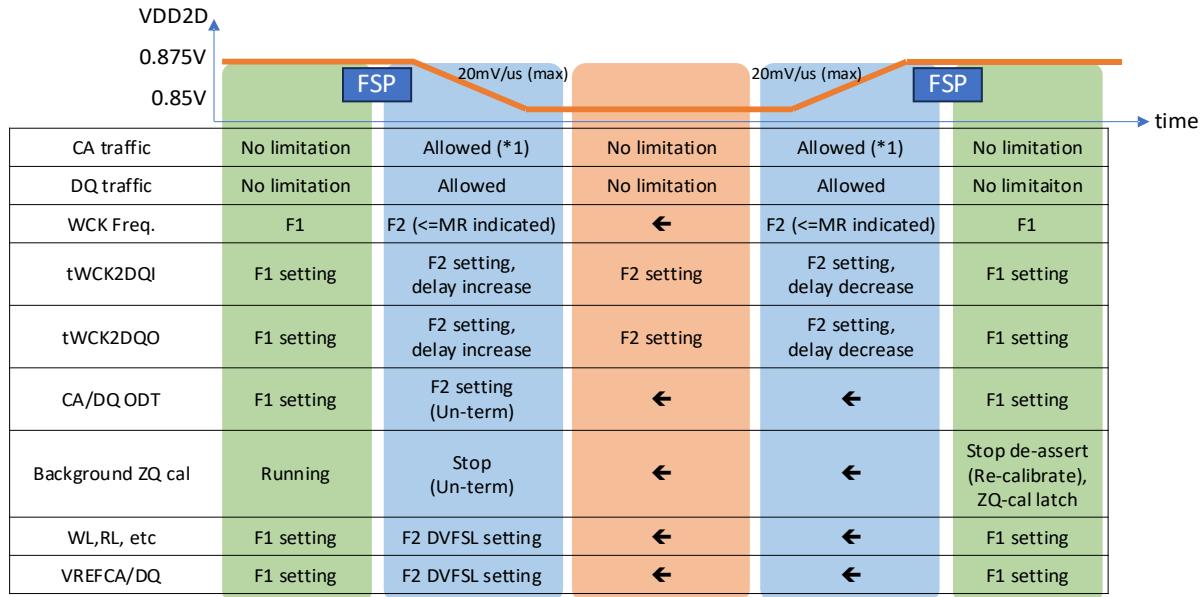
- 1) MR11 OP[4] must be set to 1 to enable DVFSL and VDD2D ramp to the step-down range.  
Switching MR11 OP[4] is allowed only through the FSP procedure.
- 2) The device must be placed in power-down mode or CS held low until the voltage ramp is complete
- 3) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-down range
- 4) FSP change to appropriate new settings should occur before operation at the new level
- 5) DVFSQ must be enabled before the DVFSL is applied
- 6) CA and DQ must be un-terminated configuration

If operation of the LPDDR6 SDRAM during the VDD2D voltage ramp is intended

- 1) MR11 OP[4] must be set to 1 to enable DVFSL and ramp VDD2D to the step-down range.  
Switching MR11 OP[4] is allowed only through the FSP procedure.
- 2) The device should be operated at settings and speeds suitable for the ramping VDD2D level
- 3) The VDD2D voltage ramp should always be equal or slower than the specified limits
- 4) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-down range
- 5) FSP change to appropriate new settings should occur before operation at the new level
- 6) DVFSQ must be enabled before the DVFSL is applied
- 7) CA and DQ must be un-terminated configuration
- 8) Any commands listed below cannot be issued during voltage transition  
TBD

Overview of the DVFSL mode requirements and sequence are shown in Figure 224.

### 11.3 DVFSL (Dynamic Voltage Frequency Scaling on Low Voltage Rail) Mode (cont'd)



NOTE 1 Any commands listed as TBD are not allowed.

**Figure 224 – DVFSL Requirements and Sequence Overview**

#### 11.3.1 DVFSL High-to-Low Transition

An example of a recommended DVFSL high-to-low transition sequence is:

- 1) Operating at WCK freq.=F1 with VDD2D in the default range
- 2) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 3) FSP switch from WCK freq.=F1 to DVFSL target WCK freq.=F2 for VDD2D ramping, MR11 OP[4]=1 to indicate DVFSL enabled
- 4) Wait tFC (stall traffic)
- 5) Issue MRW MR13 to set VRCG = 0
- 6) Wait tVRG\_DISABLE (stall traffic)
- 7) Issue MRW MR28 to set ZQ Stop=1 to disable background calibration
- 8) Wait tZQSTOP
- 9) Start ramping VDD2D to the step-down range
- 10) Continue operation at WCK freq.=F2 with VDD2D in the allowable range
- 11) Complete VDD2D ramping and VDD2D within the step-down range
- 12) Continue operation with VDD2D in the step-down range

### 11.3.2 DVFSL Low-to-High Transition

An example of a recommended DVFSL low-to-high transition sequence is:

- 1) Operating at WCK freq.=F2 with VDD2D in the step-down range and DVFSL enabled
- 2) Issue MRW MR13 to set VR<sub>CG</sub> = 1 to enable VR<sub>CG</sub>
- 3) Start ramping VDD2D to the step-down range
- 4) Continue operation at WCK freq.=F2 with VDD2D in the allowable range
- 5) Complete VDD2D ramping and VDD2D within the default range
- 6) Issue MRW MR28 to set ZQ Stop=0 to enable and initiate background calibration with new voltage level
- 7) FSP switch from WCK freq.=F2 to WCK freq.=F1 for VDD2D disabled operation, MR11 OP[4]=0 to indicate DVFSL disabled
- 8) Wait t<sub>FC</sub> (stall traffic)
- 9) Issue MRW MR13 to set VR<sub>CG</sub> = 0
- 10) Wait t<sub>VRCG\_DISABLE</sub> (stall traffic)
- 22) Issue ZQ latch once t<sub>ZQCALx</sub> expired from the last ZQ Stop reset command
- 11) Wait t<sub>ZQLATCH</sub>
- 12) Continue operation with VDD2D in the default range

## 11.4 DVFSB (Dynamic Voltage Frequency Scaling on VDD2D Power Rail) Mode

LPDDR6 devices can allow the VDD2D to be ramped during operation including Read/Write transactions. Exact speeds and levels are to be determined by the system builder according to the limits specified in this standard, their own system limitations, and at their own risk. Actual DRAM command sequence can be optimized depending on system as long as DRAM timing parameters and DVFSB requirements are satisfied. Some guidelines are:

If operation of the LPDDR6 SDRAM will be halted during the VDD2D voltage ramp

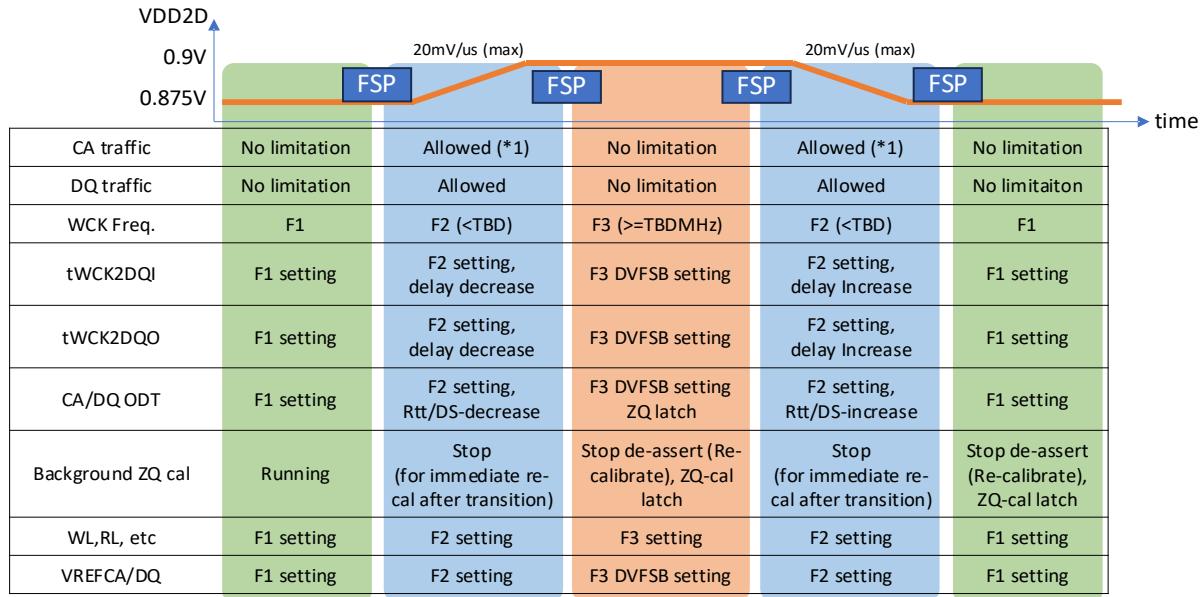
- 1) MR11 OP[3] must be set to 1 to enable DVFSB and to ramp VDD2D to the step-up range. Switching MR11 OP[3] is allowed only through the FSP procedure.
- 2) The device must be placed in power-down mode or CS held low until the voltage ramp is complete
- 3) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-up range
- 4) FSP change to appropriate new settings should occur before operation at the new level

If operation of the LPDDR6 SDRAM during the VDD2D voltage ramp is intended

- 1) MR11 OP[3] must be set to 1 to enable DVFSB and to ramp VDD2D to the step-up range. Switching MR11 OP[3] is allowed only through the FSP procedure.
- 2) The device should be operated at settings and speeds suitable for the ramping VDD2D level
- 3) The VDD2D voltage ramp should always be equal or slower than the specified limits
- 4) Re-calibration is recommended after a voltage ramp is completed and before operations at the nominal level of the default range or the step-up range
- 5) FSP change to appropriate new settings should occur before operation at the new level
- 6) Any commands listed below cannot be issued during voltage transition

Overview of the DVFSB mode requirements and sequence are shown in Figure 225.

## 11.4 DVFSB (Dynamic Voltage Frequency Scaling on VDD2D Power Rail) Mode (cont'd)



NOTE 1 Any commands listed as TBD are not allowed.

**Figure 225 – DVFSB Requirements and Sequence Overview**

### 11.4.1 DVFSB Low-to-High Transition

An example of a recommended DVFSB low-to-high transition sequence is:

- 1) Operating at WCK freq.=F1 with VDD2D in the default range
- 2) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 3) FSP switch from WCK freq.=F1 to WCK freq.=F2 suitable for VDD2D ramping up transition, MR11 OP[3]=1 to indicate DVFSB enabled
- 4) Wait tFC (stall traffic)
- 5) Issue MRW MR13 to set VRCG = 0
- 6) Wait tVRCG\_DISABLE (stall traffic)
- 7) Issue MRW MR28 to set ZQ Stop=1 to disable background calibration
- 8) Wait tZQSTOP
- 9) Start ramping up VDD2D to the step-up range
- 10) Continue operation at WCK freq.=F2 with VDD2D in the allowable range
- 11) Complete VDD2D ramping up and VDD2D within the step-up range
- 12) Issue MRW MR28 to set ZQ Stop=0 to enable and initiate background calibration with new voltage level
- 13) Issue MRW MR13 to set VRCG = 1 to enable VRCG
- 14) FSP switch from WCK freq.=F2 to DVFSB enabled target WCK freq.=F3
- 15) Wait tFC (stall traffic)
- 16) Issue MRW MR13 to set VRCG = 0 to disable VRCG
- 17) Wait tVRCG\_DISABLE (stall traffic)
- 18) Issue ZQ latch once tZQCALx expired from the last ZQ Stop reset command
- 19) Wait tZQLATCH
- 20) Continue operation with VDD2D in the step-up range

### 11.4.2 DVFSB High-to-Low Transition

An example of a recommended DVFSB low-to-high transition sequence is:

- 1) Operating at WCK freq.=F3 with VDD2D in the step-up range and DVFSB enabled
- 2) Issue MRW MR13 to set VR<sub>CG</sub> = 1 to enable VR<sub>CG</sub>
- 3) FSP switch from WCK freq.=F3 to WCK freq.=F2 suitable for VDD2D ramping transition
- 4) Wait t<sub>FC</sub> (stall traffic)
- 5) Issue MRW MR13 to set VR<sub>CG</sub> = 0
- 6) Wait t<sub>VRCG\_DISABLE</sub> (stall traffic)
- 7) Issue MRW MR28 to set ZQ Stop=1 to disable background calibration
- 8) Wait t<sub>ZQSTOP</sub>
- 9) Start ramping VDD2D to the default range
- 10) Continue operation at WCK freq.=F2 with VDD2D in the allowable range
- 11) Complete VDD2D ramping and VDD2D within the default range
- 12) Issue MRW MR28 to set ZQ Stop=0 to enable and initiate background calibration with new voltage level
- 13) Issue MRW MR13 to set VR<sub>CG</sub> = 1 to enable VR<sub>CG</sub>
- 14) FSP switch from WCK freq.=F2 to DVFSB disabled target WCK freq.=F1, MR11 OP[4]=0 to indicate DVFSB disabled
- 15) Wait t<sub>FC</sub> (stall traffic)
- 16) Issue MRW MR13 to set VR<sub>CG</sub> = 0 to disable VR<sub>CG</sub>
- 17) Wait t<sub>VRCG\_DISABLE</sub> (stall traffic)
- 18) Issue ZQ latch once t<sub>ZQCALx</sub> expired from the last ZQ Stop reset command
- 19) Wait t<sub>ZQLATCH</sub>
- 20) Continue operation with VDD2D in the default range

### 11.4.3 VDD2D Voltage Transition Slew Rate in DVFSL and DVFSB

In DVFSL and DVFSB, the VDD2D voltage ramp must conform to the limits in Table 428.

**Table 428 – VDD2D Voltage Transition Slew Rate**

Parameter	Symbol	Max/Min	Value	Units
VDD2D Slew Rate	VDD2DSR1	Max	20	mV/ $\mu$ s

## 11.5 Input Leakage Current

**Table 429 – Input Leakage Current**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage Current	IL	-18	18	µA	1,2,3
CS Leakage Current	ILCS	TBD	TBD	µA	1,2,4,5
NOTE 1 For CK_t, CK_c, WCK_t, WCK_c, and CA. Any input $0V \leq VIN \leq VDDQ$ (All other pins not under test = 0V).					
NOTE 2 For CS and RESET_n. Any input $0V \leq VIN \leq VDD2C$ (All other pins not under test = 0V).					
NOTE 3 CA ODT is disabled for CA, CK ODT is disabled for CK_t and CK_c, and WCK ODT is disabled for WCK_t and WCK_c.					
NOTE 4 CS ODT is disabled for CS if optional CS ODT is supported.					
NOTE 5 ILCS is applied when CS ODT is supported. If CS ODT is not supported, the input leakage current for CS shall meet IL.					

## 11.6 Input Leakage Current

**Table 430 – Input/Output Leakage Current**

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage Current	IOZ	-20	20	µA	1,2
NOTE 1 For DQ, RDQS_t, and RDQS_c. Any I/O $0V \leq VOUT \leq VDDQ$ .					
NOTE 2 I/Os status are disabled: High Impedance and ODT Off.					

## 11.7 Operating Temperature Range

**Table 431 – Operating Temperature Range**

Parameter / Condition	Symbol	Min	Max	Unit	Notes
Standard	$T_{oper\_standard}$	-25	85	°C	1,2,3
Elevated	$T_{oper\_elevated}$	-25	105	°C	1,2,3
NOTE 1	Operating Temperature is the case surface temperature on the center-top side of the LPDDR6 device. For the measurement conditions, please refer to JESD51-2A.				
NOTE 2	Some applications require operation of LPDDR6 in the maximum temperature conditions in the Elevated Temperature Range between 85 °C and 105 °C case temperature. For LPDDR6 devices, de-rating may be necessary to operate in this range.				
NOTE 3	Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or Elevated Temperature Ranges. For example, TCASE may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.				

### 11.7.1 Operating Temperature Range (Automotive Spec Addendum only)

**Table 432 — Operating Temperature Range**

Parameter / Condition	Symbol	Min	Max	Unit	Notes
Standard	$T_{oper\_standard}$	-25	85	°C	1
Automotive Grade1	$T_{oper\_auto\_grade1}$	-40	125	°C	1,2,3,4
Automotive Grade 2	$T_{oper\_auto\_grade2}$	-40	105	°C	1,2,3,4
Automotive Grade 3	$T_{oper\_auto\_grade3}$	-40	85	°C	1,2,3,4
NOTE 1	Operating Temperature is the case surface temperature on the center-top side of the LPDDR6 device. For the measurement conditions, please refer to JESD51-2A.				
NOTE 2	Automotive: Some applications require operation of LPDDR6 in the maximum temperature conditions over 85°C. For LPDDR6 devices, de-rating may be necessary to operate in this range (over 85 °C).				
NOTE 3	Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating, and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard or automotive grades Temperature Ranges. For example, TCASE may be above 85 °C when the temperature sensor indicates a temperature of less than 85 °C.				
NOTE 4	Automotive temperature condition is only allowed at the limited part which specifies the guarantee in the datasheet.				

## 11.8 Electrostatic Discharge Sensitivity Characteristics

**Table 433 – Electrostatic Discharge Sensitivity Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD <sub>HBM</sub>	1000		V	1
Charged-device model (CDM)	ESD <sub>CDM</sub>	250		V	2
NOTE 1 Refer to ESDA/JEDEC Joint Standard JS-001 for measurement procedures.					
NOTE 2 Refer to JS-002 for measurement procedures.					

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## 12 AC and DC Input/Output Measurement Levels

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### 12.1 High Speed LVC MOS

#### 12.1.1 Standard Specifications

All voltages are referenced to ground except where noted.

#### 12.1.2 Input Level for Reset\_n

LPDDR6 uses CMOS with VDD2C Reset\_n signaling to ensure stable LPDDR6 reset operation.

**Table 434 – Reset Input Level Specification**

Item	Symbol	Min/Max		Unit	Note
Reset_n ViH	ViH_RS	Min	0.8xVDD2C	V	
		Max	VDD2C+0.2	V	
Reset_n ViL	ViL_RS	Min	-0.2	V	
		Max	0.2xVDD2C	V	

### 12.1.3 AC Overshoot / Undershoot

#### 12.1.3.1 AC Overshoot / Undershoot for LVC MOS

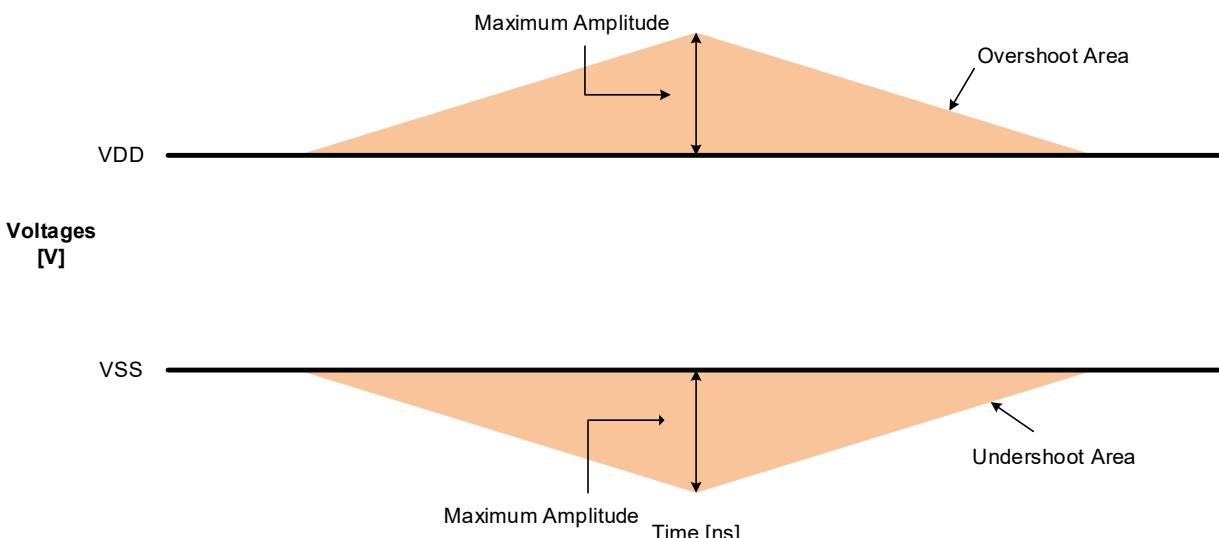
Table 435 – AC Overshoot / Undershoot for LVC MOS

Parameter	Specification
Maximum Peak Amplitude allowed for overshoot area	0.35 V
Maximum Peak Amplitude allowed for undershoot area	0.35 V
Maximum overshoot area above VDD2C/VDDQ	0.8 V·ns
Maximum undershoot area above VSS	0.8 V·ns

#### 12.1.3.2 AC Overshoot / Undershoot for LVSTL

Table 436 – LPDDR6 AC Overshoot / Undershoot for LVSTL

Parameter	Min/ Max	Data Rate					Units
		3200	6400	9600	11733	14400	
Maximum Peak Amplitude allowed for overshoot area	Max	0.3	0.3	0.3	0.3	0.3	V
Maximum Peak Amplitude allowed for undershoot area	Max	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area above VDD2C/VDDQ	Max	0.1	0.1	0.1	0.1	0.1	V·ns
Maximum undershoot area above VSS	Max	0.1	0.1	0.1	0.1	0.1	V·ns



NOTE 1 Reference VDD should use following definitions. VDD is VDD2C for CS and RESET\_n. VDD is VDDQ for CA[3:0], CK\_t/c, DQ, WCK\_t/c, RDQS\_t\_c and Alert.

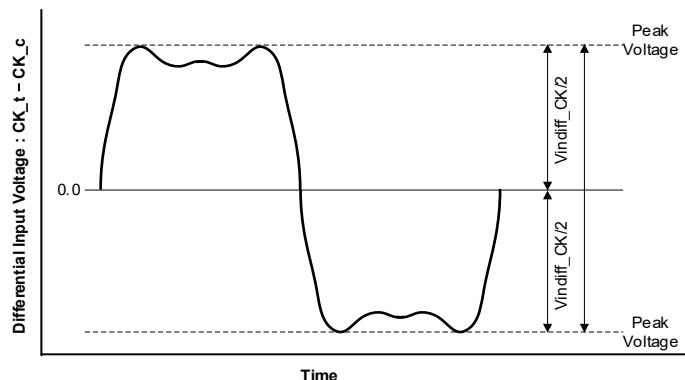
NOTE 2 Maximum peak amplitude values are referenced from actual VDD and VSS values.

NOTE 3 Maximum area values are referenced from maximum operating VDD and VSS values.

## 12.2 Differential Input Voltage

### 12.2.1 Differential Input Voltage for CK

The minimum input voltage needs to satisfy both Vindiff\_CK and Vindiff\_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff\_CK is the peak to peak voltage centered on 0 volts differential and Vindiff\_ CK /2 is max and min peak voltage from 0 V.



**Figure 226 – CK Differential Input Voltage**

**Table 437 – CK Differential Input Voltage**

Parameter	Symbol	Clock Rate										Unit	Note		
		533 MHz		800 MHz		1600 MHz		2400 MHz		3600 MHz					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
CK Differential Input Voltage	Vindiff_CK	350	-	350	-	300	-	280	-	TBD	-	mV	1,2		

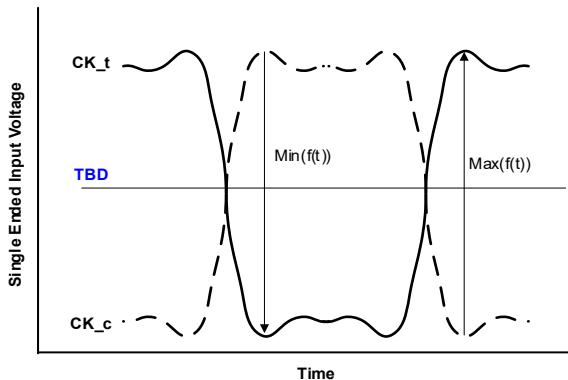
### 12.2.1.1 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals is calculated in the following equations.

$$\text{VIH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$\text{VIL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VCK_t - VCK_c$$

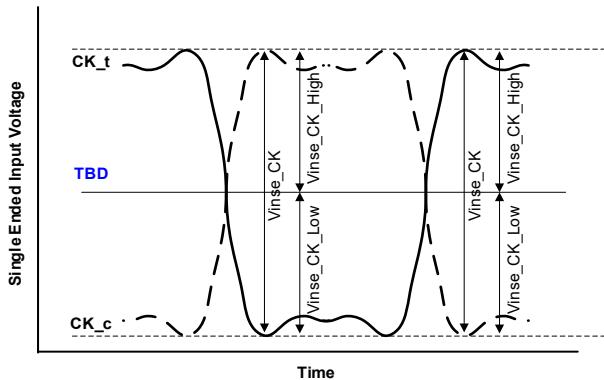


NOTE 1 TBD is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 227 – Definition of Differential Clock Peak Voltage**

### 12.2.1.2 Single Ended Input Voltage for CK

The minimum input voltage needs to satisfy both Vinse\_CK, Vinse\_CK\_High/Low specification at input receiver.



NOTE 1 TBD is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 228 – Clock Single-ended Input Voltage**

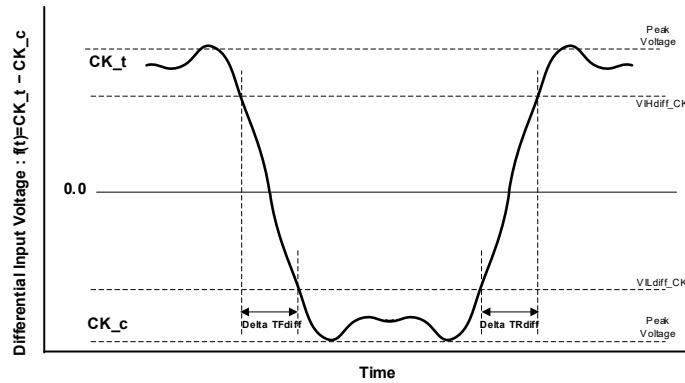
### 12.2.1.2 Single Ended Input Voltage for CK (cont'd)

**Table 438 – Clock Single-ended Input Voltage**

Parameter	Symbol	Clock Rate										Unit	Note		
		533 MHz		800 MHz		1600 MHz		2400 MHz		3600 MHz					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Clock Single-ended input Voltage	Vinse_CK	175	-	175	-	175	-	175	-	175	-	mV			
Clock Single-ended input Voltage High from TBD	Vinse_CK_High	87.5	-	87.5	-	87.5	-	87.5	-	87.5	-	mV			
Clock Single-ended input Voltage Low from TBD	Vinse_CK_Low	87.5	-	87.5	-	87.5	-	87.5	-	87.5	-	mV			

### 12.2.1.3 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals ( $CK_t$ ,  $CK_c$ ) are defined and measured as shown in Figure 229 and the following tables.



- NOTE 1 Differential signal rising edge from  $VIL_{diff\_CK}$  to  $VIH_{diff\_CK}$  must be monotonic slope.  
NOTE 2 Differential signal falling edge from  $VIH_{diff\_CK}$  to  $VIL_{diff\_CK}$  must be monotonic slope.

**Figure 229 – Differential Input Slew Rate Definition for CK<sub>t</sub>, CK<sub>c</sub>**

### 12.2.1.3 Differential Input Slew Rate Definition for CK (cont'd)

**Table 439 – Differential Input Slew Rate Definition for CK\_t, CK\_c**

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	$ VILdiff\_CK - VIHdiff\_CK /\Delta TRdiff$
Differential input slew rate for falling edge (CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	$ VILdiff\_CK - VIHdiff\_CK /\Delta TFdiff$

**Table 440 – Differential Input Level for CK\_t, CK\_c**

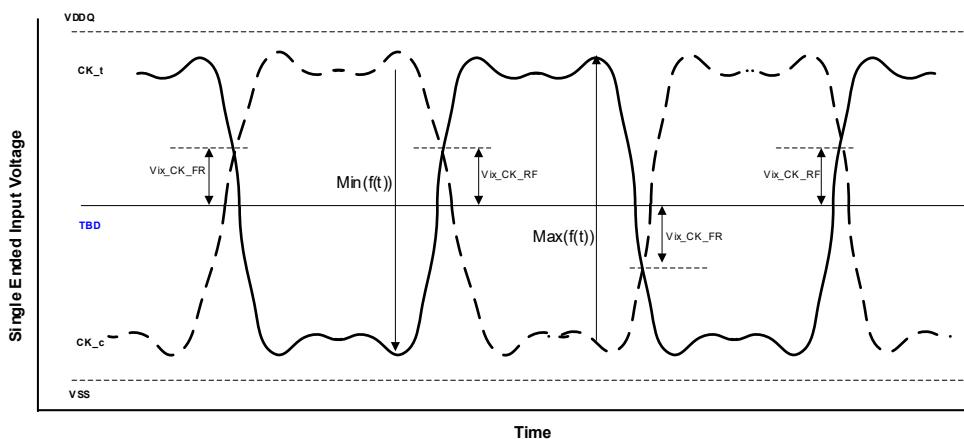
Parameter	Symbol	Clock Rate										Unit	Note		
		533 MHz		800 MHz		1600 MHz		2400 MHz		3600 MHz					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input High	VIHdiff_CK	145	-	145	-	145	-	145	-	145	-	mV			
Differential Input Low	VILdiff_CK	-	145	-	145	-	145	-	145	-	145	mV			

**Table 441 – Differential Input Slew Rate for CK\_t, CK\_c**

Parameter	Symbol	Clock Rate										Unit	Note		
		533 MHz		800 MHz		1600 MHz		2400 MHz		3600 MHz					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns			

### 12.2.1.4 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK\_t, CK\_c) must meet the requirements in Figure 230. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix\_CK\_FR/RF is TBD that is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 230 – Differential Input Slew Rate Definition for CK\_t, CK\_c**

#### 12.2.1.4 Differential Input Slew Rate Definition for CK (cont'd)

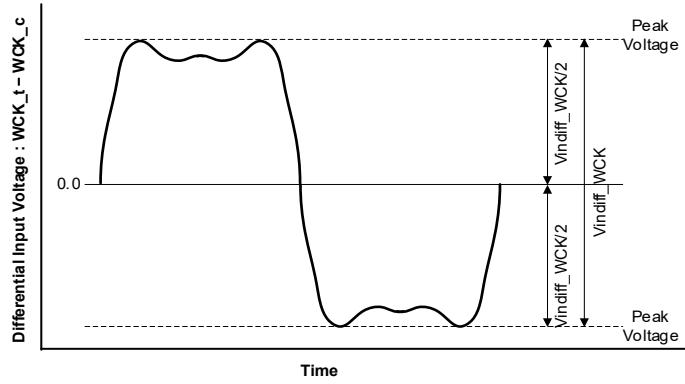
**Table 442 – Cross Point Voltage for Differential Input Signals (Clock)**

Parameter	Symbol	Clock Rate										Unit	Note		
		533 MHz		800 MHz		1600 MHz		2400 MHz		3600 MHz					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Clock Differential input crosspoint voltage ratio	Vix_CK_ratio	-	25	-	25	-	25	-	25	-	25	%	1,2		

NOTE 1 Vix\_CK\_Ratio is defined by this equation:  $Vix\_CK\_Ratio = Vix\_CK\_FR / |Min(f(t))|$   
 NOTE 2 Vix\_CK\_Ratio is defined by this equation:  $Vix\_CK\_Ratio = Vix\_CK\_RF / Max(f(t))$

#### 12.2.2 Differential Input Voltage for WCK

The minimum input voltage needs to satisfy both Vindiff\_WCK and Vindiff\_WCK /2 specification at input receiver and their measurement period is 1tWCK. Vindiff\_WCK is the peak to peak voltage centered on 0 volts differential and Vindiff\_WCK /2 is max and min peak voltage from 0V.



**Figure 231 – WCK Differential Input Voltage**

### 12.2.2 Differential Input Voltage for WCK (cont'd)

**Table 443 – WCK Differential Input Voltage**

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		533		800		1067		1375		1600		1875					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential Input Voltage	Vindiff_WCK	300	-	300	-	300	-	300	-	300	-	280	-	mV	1,2		
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		2134		2400		2750		3200		3750		4267					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential Input Voltage	Vindiff_WCK	280	-	280	-	280	-	280	-	TBD	-	TBD	-	mV	1,2		
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		4800		5334		5867		6400		7200		-					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	-	-				
WCK Differential Input Voltage	Vindiff_WCK	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	-	mV	1,2		

NOTE 1 Refer to the latency table to match the WCK rate to data rate.

NOTE 2 The peak voltage of Differential WCK signals is calculated in the following equations.

$$\text{Vindiff\_WCK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VWCK}_t - \text{VWCK}_c$$

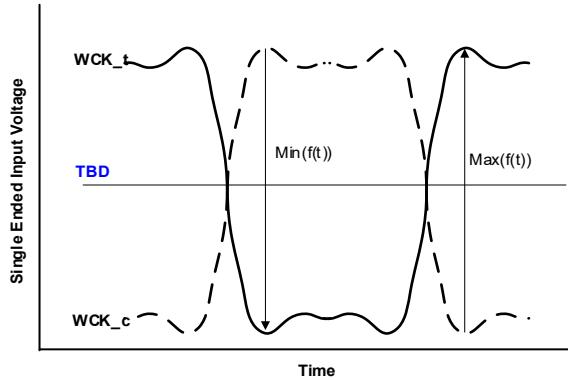
### 12.2.2.1 Peak Voltage Calculation Method

The peak voltage of Differential WCK signals is calculated in the following equations.

$$\text{VIH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$\text{VIL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{WCK}_t - \text{WCK}_c$$

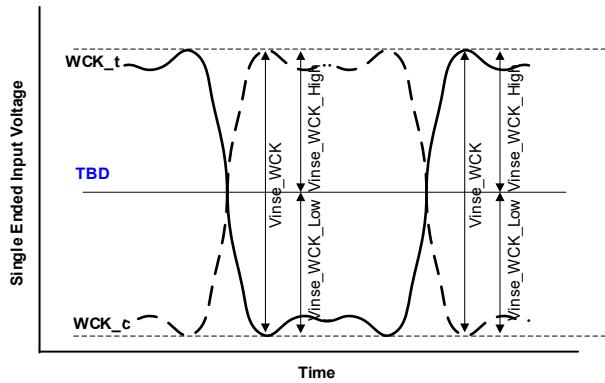


NOTE 1 TBD is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 232 – Definition of Differential WCK Peak Voltage**

### 12.2.2.2 Single Ended Input Voltage for WCK

The minimum input voltage needs to satisfy both  $\text{Vinse\_WCK}$  and  $\text{Vinse\_WCK\_High/Low}$  specifications at input receiver.



NOTE 1 TBD is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 233 – WCK Single-ended Input Voltage**

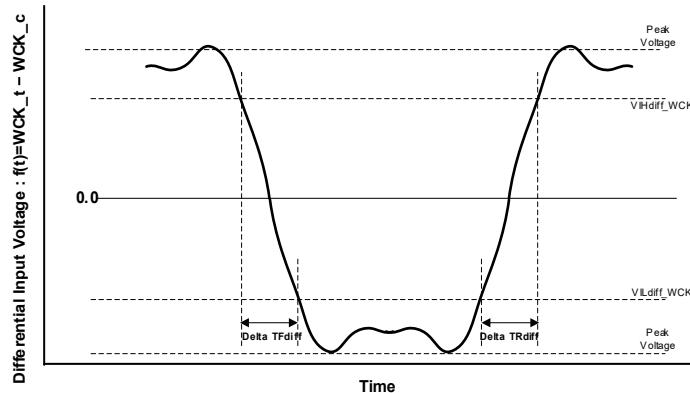
### 12.2.2.2 Single Ended Input Voltage for WCK (cont'd)

Table 444 — WCK Single-ended Input Voltage

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		533		800		1067		1375		1600		1875					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Single-ended input Voltage	Vinse_WCK	150	-	150	-	150	-	150	-	150	-	140	-	mV			
WCK Single-ended input Voltage High from TBD	Vinse_WCK_High	75	-	75	-	75	-	75	-	75	-	70	-	mV			
WCK Single-ended input Voltage Low from TBD	Vinse_WCK_Low	75	-	75	-	75	-	75	-	75	-	70	-	mV			
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		2134		2400		2750		3200		3750		4267					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Single-ended input Voltage	Vinse_WCK	140	-	140	-	140	-	140	-	TBD	-	TBD	-	mV			
WCK Single-ended input Voltage High from TBD	Vinse_WCK_High	70	-	70	-	70	-	70	-	TBD	-	TBD	-	mV			
WCK Single-ended input Voltage Low from TBD	Vinse_WCK_Low	70	-	70	-	70	-	70	-	TBD	-	TBD	-	mV			
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		4800		5334		5867		6400		7200		-					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Single-ended input Voltage	Vinse_WCK	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	-	mV			
WCK Single-ended input Voltage High from TBD	Vinse_WCK_High	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	-	mV			
WCK Single-ended input Voltage Low from TBD	Vinse_WCK_Low	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	-	mV			

### 12.2.2.3 Differential Input Slew Rate Definition for WCK

Input slew rate for differential signals (WCK\_t, WCK\_c) are defined and measured as shown in Figure 234 and the following tables.



NOTE 1 Differential signal rising edge from VILdiff\_WCK to VIHdiff\_WCK must be monotonic slope.

NOTE 2 Differential signal falling edge from VIHdiff\_WCK to VILdiff\_WCK must be monotonic slope.

**Figure 234 – Differential Input Slew Rate Definition for WCK\_t, WCK\_c**

**Table 445 – Differential Input Slew Rate Definition for WCK\_t, WCK\_c**

Description	From	To	Defined by
Differential input slew rate for rising edge (WCK_t - WCK_c)	VILdiff_WCK	VIHdiff_WCK	$ VILdiff_WCK - VIHdiff_WCK /\Delta TRdiff$
Differential input slew rate for falling edge (WCK_t - WCK_c)	VIHdiff_WCK	VILdiff_WCK	$ VILdiff_WCK - VIHdiff_WCK /\Delta TFdiff$

### 12.2.2.3 Differential Input Slew Rate Definition for WCK (cont'd)

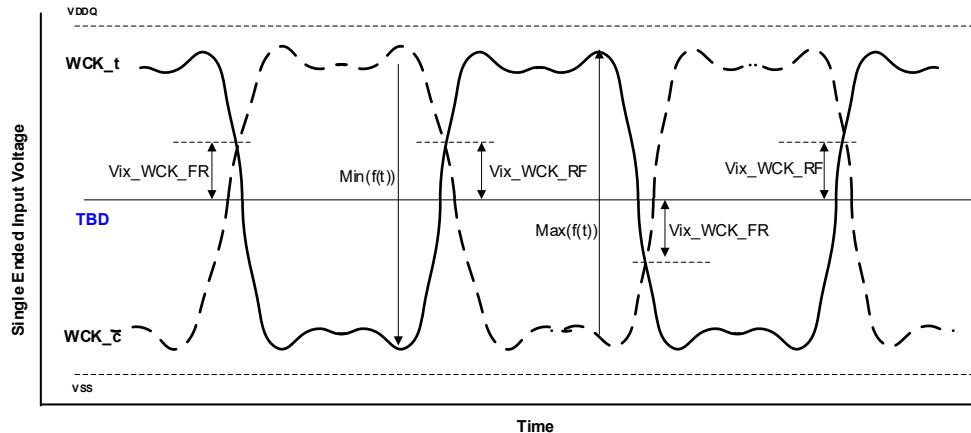
**Table 446 — Differential Input Level for WCK\_t, WCK\_c**

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		533		800		1067		1375		1600		1875					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input High	VIHdiff_WCK	120	-	120	-	120	-	100	-	100	-	100	-	mV			
Differential Input Low	VILdiff_WCK	-	120	-	120	-	120	-	100	-	100	-	100	mV			
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		2134		2400		2750		3200		3750		4267					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input High	VIHdiff_WCK	100	-	100	-	100	-	100	-	100	-	TBD	-	mV			
Differential Input Low	VILdiff_WCK	-	100	-	100	-	100	-	100	-	100	-	TBD	mV			
Parameter	Parameter	WCK Rate [MHz]												Unit	Note		
		4800		5334		5867		6400		7200		-					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
Differential Input High	VIHdiff_WCK	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	-	mV			
Differential Input Low	VILdiff_WCK	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	-	mV			

**Table 447 — Differential Input Slew Rate for WCK\_t, WCK\_c**

#### 12.2.2.4 Differential Input Cross Point Voltage for WCK

The cross point voltage of differential input signals (WCK\_t, WCK\_c) must meet the requirements in Table 448. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid-level that is TBD.



NOTE 1 The base level of Vix\_WCK\_RF/RF is TBD that is LPDDR6 SDRAM internal setting value by Vref training.

**Figure 235 – Vix Definition (WCK)**

#### 12.2.2.4 Differential Input Cross Point Voltage for WCK (cont'd)

**Table 448 — Cross Point Voltage for Differential Input Signals (WCK)**

Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		533		800		1067		1375		1600		1875					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential input crosspoint voltage ratio	Vix_WCK_ratio	-	20	-	20	-	20	-	20	-	20	-	20	%	1,2		
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		2134		2400		2750		3200		3750		4267					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential input crosspoint voltage ratio	Vix_WCK_ratio	-	20	-	20	-	20	-	20	-	20	-	TBD	%	1,2		
Parameter	Symbol	WCK Rate [MHz]												Unit	Note		
		4800		5334		5867		6400		7200		-					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
WCK Differential input crosspoint voltage ratio	Vix_WCK_ratio	-	TBD	-	TBD	-	TND	-	20	-	20	-	-	%	1,2		

NOTE 1 Vix\_WCK\_Ratio is defined by this equation: Vix\_WCK\_Ratio = Vix\_WCK\_RF/|Min(f(t))|

NOTE 2 Vix\_WCK\_Ratio is defined by this equation: Vix\_WCK\_Ratio = Vix\_WCK\_RF/Max(f(t))

## 12.3 Single-ended Mode CK

### 12.3.1 Single-ended Mode CK Input Definitions

The minimum input voltage needs to satisfy both  $V_{inse\_CK\_SE\_High}$  and  $V_{inse\_CK\_SE\_Low}$  specification at input receiver and their measurement period is  $1tCK$ .  $V_{inse\_CK\_SE}$  is the peak to peak voltage centered on  $VDDQ/2$  and  $V_{inse\_CK\_SE\_High}$  and  $V_{inse\_CK\_SE\_Low}$  is max and min peak voltage from  $VDDQ/2$ .

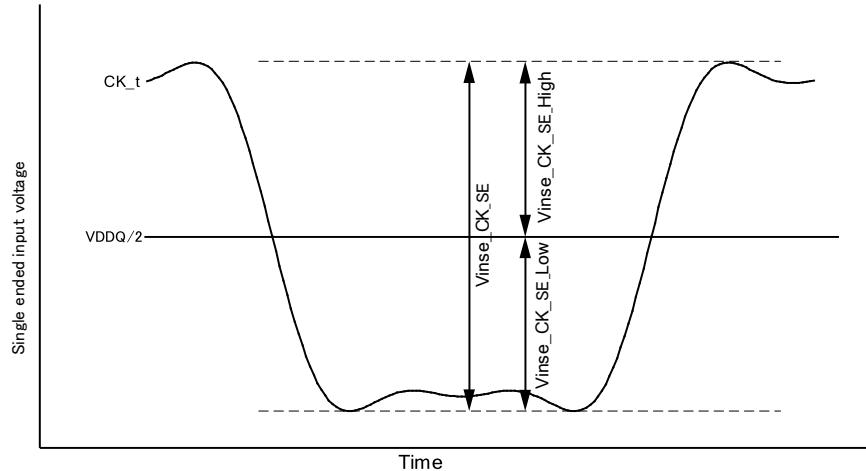


Figure 236 – Single-ended Mode CK Input Voltage

#### 12.3.1.1 Single Ended Mode CK Pulse Definitions

Single Ended Mode CK pulse definitions are defined as shown in Table 449.

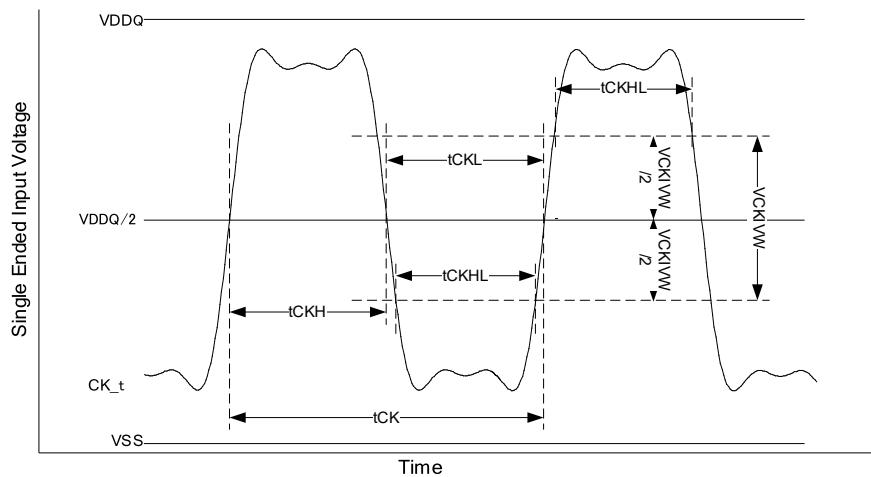


Figure 237 – Single-ended Mode CK Pulse

### 12.3.1.1 Single Ended Mode CK Pulse Definitions (cont'd)

**Table 449 — Single-ended CK Parameters**

Parameter	Symbol	Min/Max	CK Frequency	Unit	Note
			TBD MHz		
CK Single ended input voltage	Vinse_CK_SE	Min	220	mV	
CK Single Ended Input Voltage High	Vinse_CK_SE_High	Min	110	mV	
CK Single Ended Input Voltage Low	Vinse_CK_SE_low	Min	110	mV	
CK single ended timing window	VCKIVW	min	190	mV	
Clock Single Ended CK Pulse	tCKHL	Min	0.26	tCK(avg)	
CK single ended Slew Rate	SRICKSE	Min	1	V/ns	1
		Max	7		
NOTE 1 Single ended slew rate is measured at VDDQ/2 - VCKIVW/2 and VDDQ/2 + VCKIVW/2.					

### 12.3.2 Single Ended Mode WCK

#### 12.3.2.1 Single Ended WCK Input Definitions

The minimum input voltage needs to satisfy both  $V_{inse\_WCK\_SE\_High}$  and  $V_{inse\_WCK\_SE\_Low}$  specification at input receiver and their measurement period is  $1t_{WCK}$ .  $V_{inse\_WCK\_SE}$  is the peak to peak voltage centered on  $VDDQ/2$  and  $V_{inse\_WCK\_SE\_High}$  and  $V_{inse\_WCK\_SE\_Low}$  is max and min peak voltage from  $VDDQ/2$ .

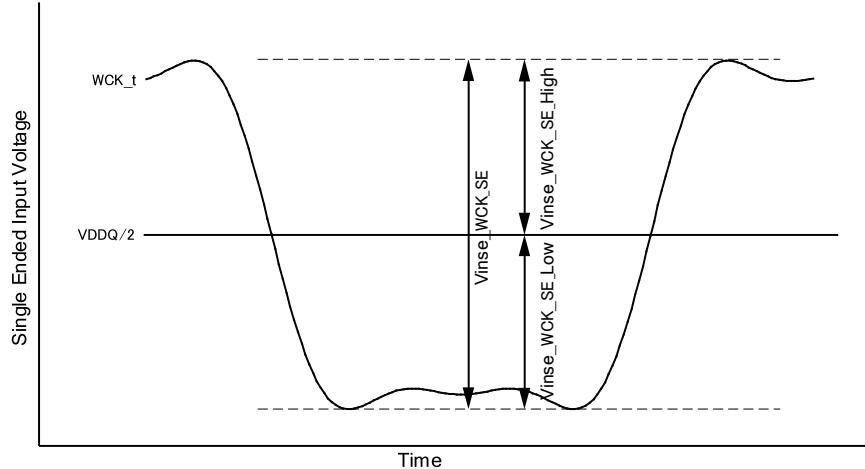


Figure 238 – Single Ended Mode WCK Input Voltage

#### 12.3.2.2 Single Ended Mode WCK Pulse Definitions

Single ended Mode WCK pulse definitions are shown in Figure 239.

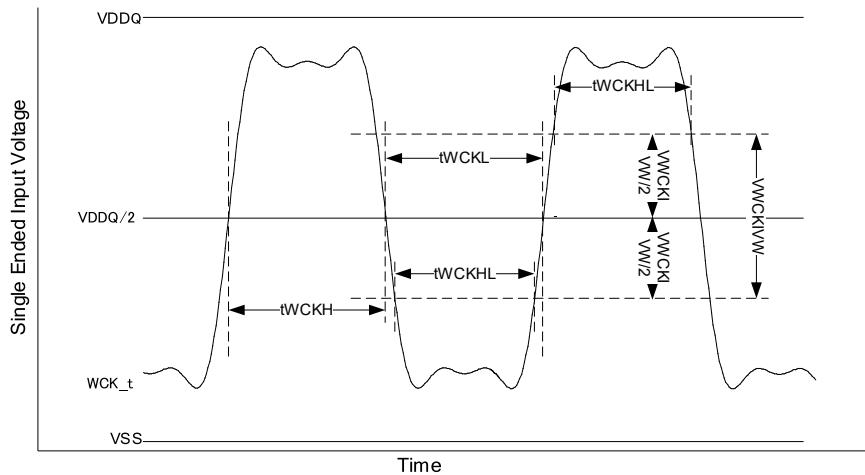


Figure 239 – Single Ended Mode WCK Pulse

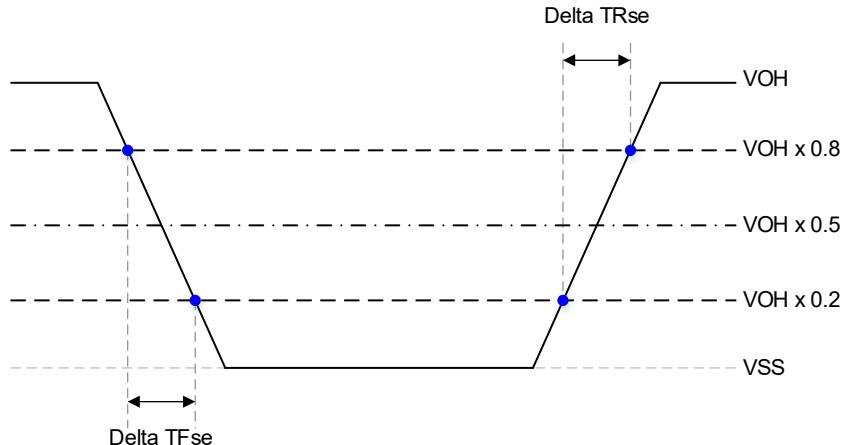
### 12.3.2.2 Single Ended Mode WCK Pulse Definitions (cont'd)

**Table 450 — Single-ended WCK Parameters**

Parameter	Symbol	Min/Max	WCK Frequency	Unit	Note
			TBD MHz		
WCK Single ended input voltage	Vinse_WCK_SE	Min	220	mV	
WCK Single Ended Input Voltage High	Vinse_WCK_SE_High	Min	110	mV	
WCK Single Ended Input Voltage Low	Vinse_WCK_SE_low	Min	110	mV	
WCK single ended timing window	VWCKIVW	Min	180	mV	
Clock Single Ended WCK Pulse	tWCKHL	Min	0.23	tWCK (avg)	
WCK single ended Slew Rate	SRIWCKSE	Min	1	V/ns	1
		Max	7		
NOTE 1 Single ended slew rate is measured at VDDQ/2 - VWCKIVW/2 and VDDQ/2 + VWCKIVW/2					

## 12.4 Output Slew Rate

### 12.4.1 Single Ended Output Slew Rate



**Figure 240 – Single Ended Output Slew Rate Definition**

**Table 451 — Output Slew Rate (Single-Ended)**

Parameter	Symbol	Value		Units
		Min	Max	
Single-ended Output Slew Rate	SRQse	TBD	-	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	TBD	TBD	-

Description:

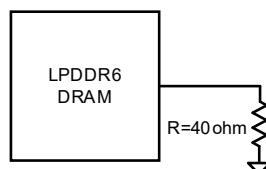
SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

NOTE 1 These values are guaranteed by design.

Assumption: Pull up/down driver=40 ohm, Reference load=40 ohm.



NOTE 2 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.

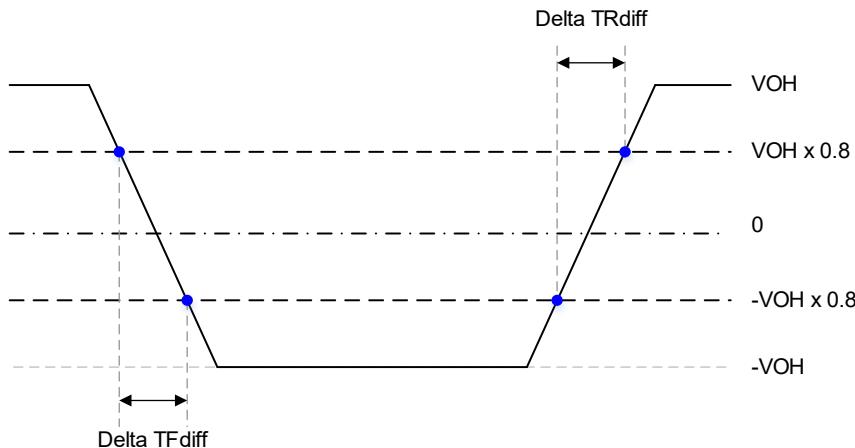
The equation is  $(\text{Rise slew Rate}) / (\text{Fall Slew Rate}) \times 100$ .

NOTE 3 The output slew rate for falling and rising edges is defined and measured between  $\text{VOH} \times 0.2$  and  $\text{VOH} \times 0.8$ .

NOTE 4 Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces  $\text{Voh}(\text{ac})$  at high frequency close to  $F_{\text{max}}$ , the signal using PRBS data pattern may not achieve a full swing at such conditions.

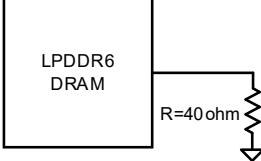
NOTE 5 The parameters about Single-ended applies to RDQS\_t and RDQS\_c when either RDQS\_t or RDQS\_c is disabled.

### 12.4.2 Differential Output Slew Rate



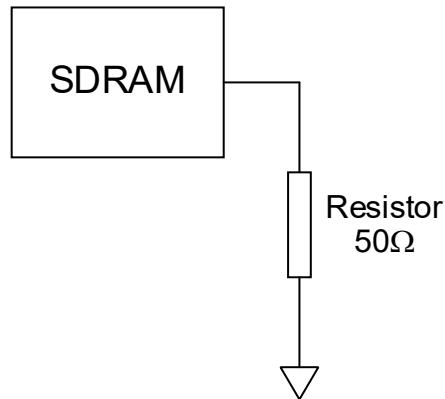
**Figure 241 – Differential Output Slew Rate Definition**

**Table 452 – Differential Output Slew Rate**

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate	SRQdiff	TBD	-	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals				
NOTE 1 These values are guaranteed by design. Assumption: Pull up/down driver=40 ohm, Reference load=40 ohm.				
				
NOTE 2 The output slew rate for falling and rising edges is defined and measured between -VOH x 0.8 and VOH x 0.8. NOTE 3 Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces Voh(ac) at high frequency close to Fmax, the signal using PRBS data pattern may not achieve a full swing at such conditions.				

## 12.5 Output Reference Load

These “Timing Reference Loads” are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



**Figure 242 – Driver Output Reference Load for Timing**

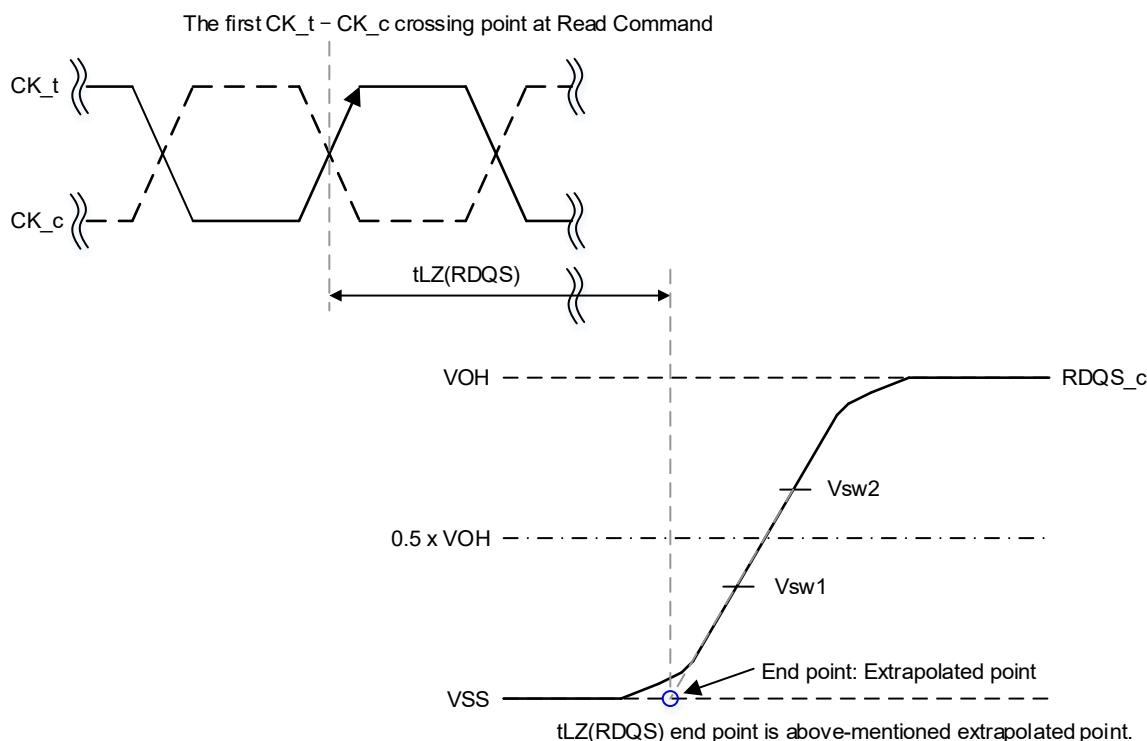
## 12.6 Read Timing tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

### 12.6.1 tLZ(RDQS) tLZ(DQ) tHZ(RDQS) tHZ(DQ)

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to voltage levels that indicate when the device output is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ).

This section includes a method to calculate the point when the device is no longer driving tHZ(RDQS) and tHZ(DQ), or begins driving tLZ(RDQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(RDQS), tLZ(DQ), tHZ(RDQS), and tHZ(DQ) are defined as single ended.

#### 12.6.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE (Automatic Test Equipment)



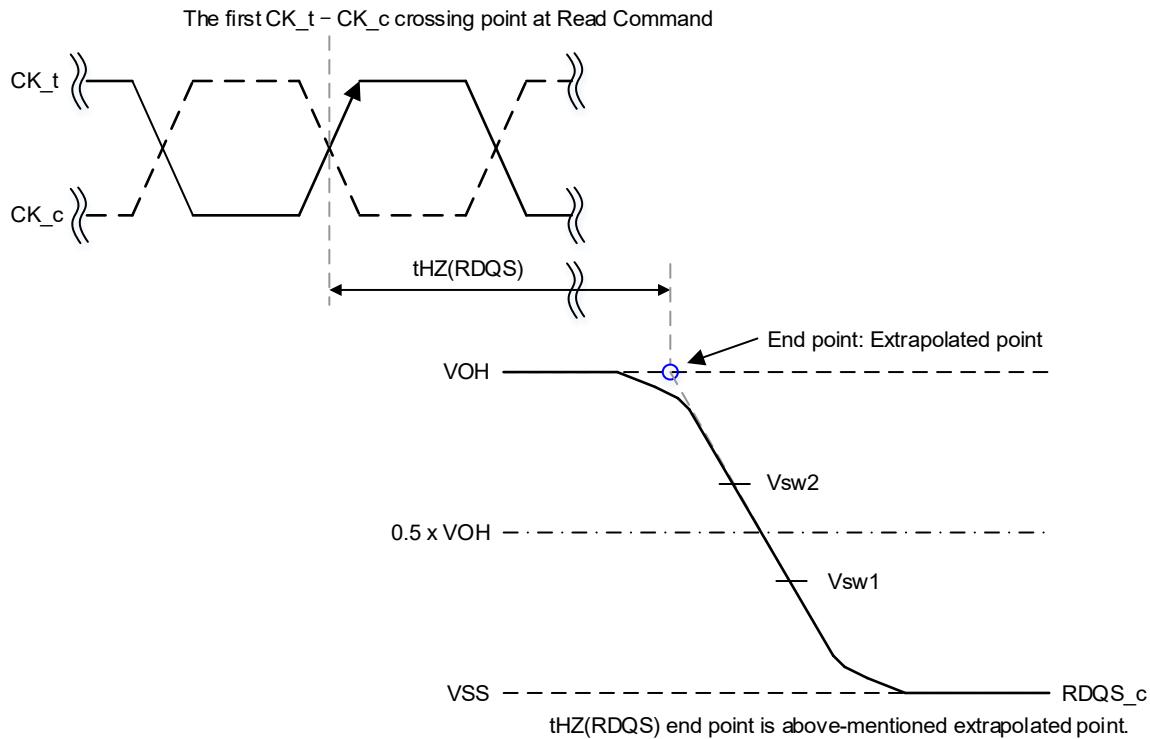
NOTE 1 Conditions for Calibration: VDDQ = TBD V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for RDQS\_t and RDQS\_c = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 243 – tLZ(RDQS) Method for Calculating Transitions and End Point**

### 12.6.1.1 tLZ(RDQS) and tHZ(RDQS) Calculation for ATE (Automatic Test Equipment) (cont'd)



NOTE 1 Conditions for Calibration: VDDQ = TBD V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for RDQS<sub>t</sub> and RDQS<sub>c</sub> = 50ohm to VSS.

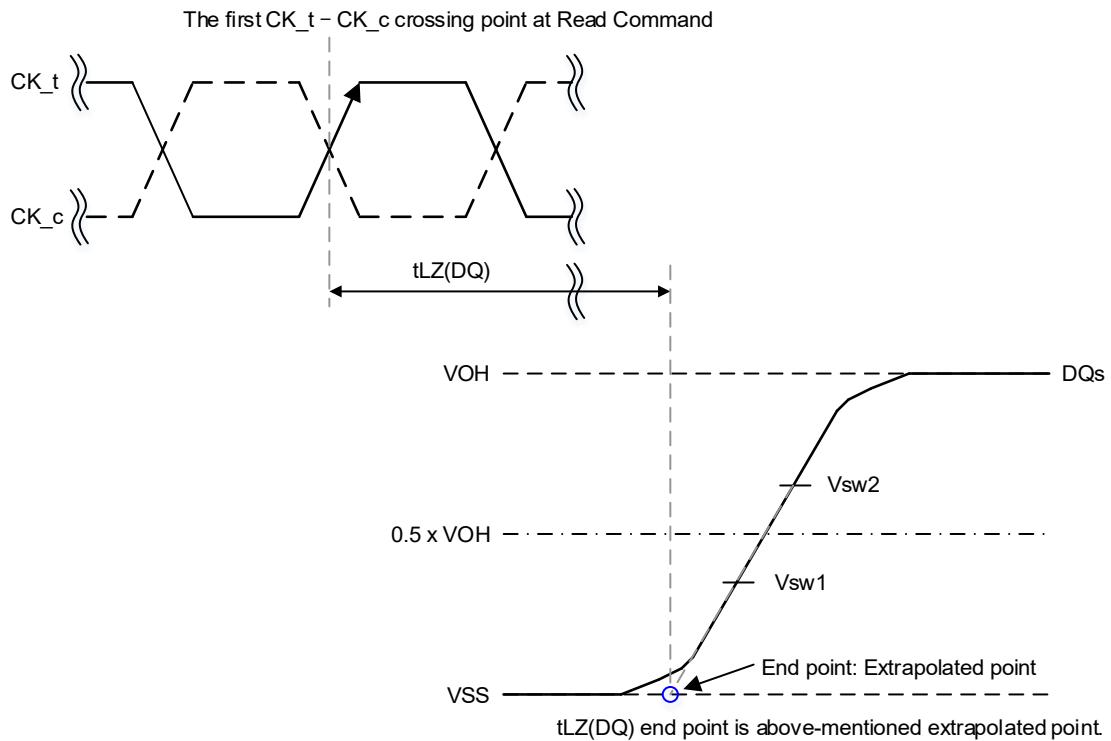
NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 244 – tHZ(RDQS) Method for Calculating Transitions and End Point**

**Table 453 – Reference Voltage for tLZ(RDQS), tHZ(RDQS) Timing Measurements**

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Notes
RDQS <sub>c</sub> low-impedance time from CK <sub>t</sub> , CK <sub>c</sub>	tLZ(RDQS)	0.4 x VOH	0.6 x VOH	
RDQS <sub>c</sub> high impedance time from CK <sub>t</sub> , CK <sub>c</sub>	tHZ(RDQS)	0.4 x VOH	0.6 x VOH	

### 12.6.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)



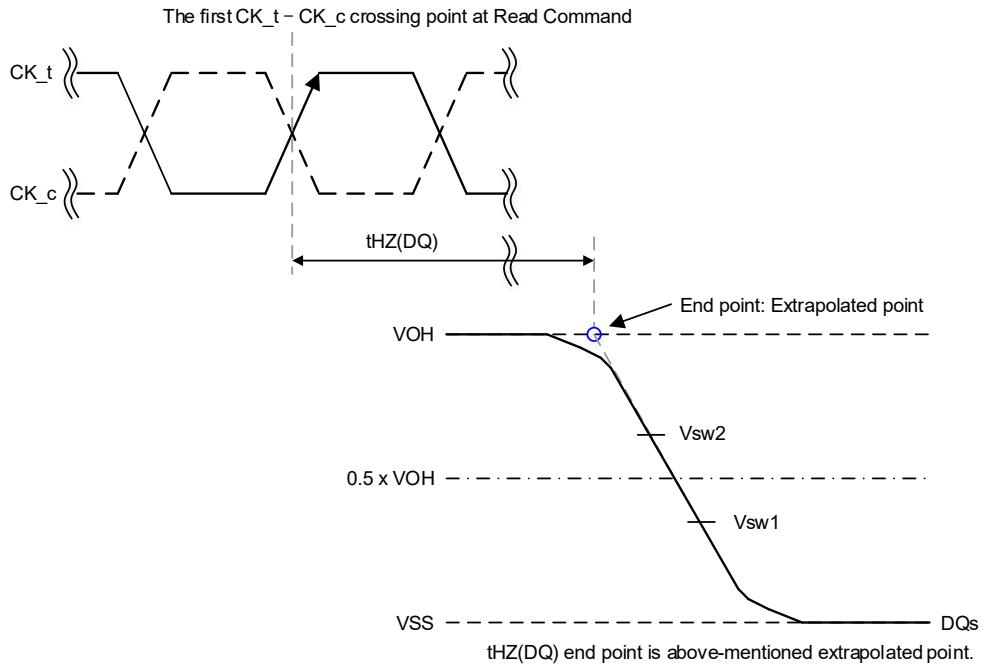
NOTE 1 Conditions for Calibration: VDDQ = TBD V, Pull Down Driver Ron = 40 ohm, VOH = VDDQ/2

NOTE 2 Termination condition for DQs = 50 ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 245 – tLZ(DQ) Method for Calculating Transitions and End Point**

### 12.6.1.2 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) (cont'd)



NOTE 1 Conditions for Calibration: VDDQ = TBD V, Pull Down Driver Ron = 40ohm, VOH = VDDQ/2

NOTE 2 Termination condition for DQs = 50ohm to VSS.

NOTE 3 Use the actual VOH value for tHZ and tLZ measurements.

**Figure 246 – tHZ(DQ) Method for Calculating Transitions and End Point**

**Table 454 – Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements**

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Notes
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	0.4 x VOH	0.6 x VOH	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	0.4 x VOH	0.6 x VOH	

**Table 455 – Read AC Timing**

Parameter	Symbol	Min/Max	Data Rate	Unit	Notes
			Up to 10667 MHz		
READ preamble	tRPRE	Min	TBD	tCK(avg)	
READ postamble	tRPST	Min	TBD	tCK(avg)	
RDQS_c low-impedance time from CK_t, CK_c	tLZ(RDQS)	Min	(RL x tCK) + tWCK2CK(Min) + tWCK2DQO(Min) - (tRPRE(Max) x tCK) - TBDps	ps	
RDQS_c high impedance time from CK_t, CK_c	tHZ(RDQS)	Max	(RL x tCK) + tWCK2CK(Max) + BL/n_min + (RPST(Max) x tCK) - TBDps	ps	
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL x tCK + tWCK2CK(Min) + tDQSQ(Min) - TBDps	ps	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL x tCK) + tWCK2CK(Max) + tWCK2DQO(Max) + BLn_min - TBDps	ps	

## 13 Input / Output Capacitance

**Table 456 — Input / Output Capacitance**

## 14 IDD Specification Parameters and Test Conditions

### 14.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW:  $V_{IN} \leq V_{IL(DC)} \text{ MAX}$

HIGH:  $V_{IN} \geq V_{IH(DC)} \text{ MIN}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 457.

**Table 457 – Definition of Switching for CA Input Signals**

CK_t edge	R1	F1	R2	F2	R3	F3	R4	F4	R5	F5	R6	F6	R7	F7	R8	F8
<b>CS</b>	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
<b>CA0</b>	H	L	L	L	H	H	H	H	L	L	L	L	L	H	H	H
<b>CA1</b>	H	H	H	L	L	L	H	H	H	H	L	L	L	L	L	H
<b>CA2</b>	H	L	L	L	L	H	H	H	L	L	L	L	L	H	H	H
<b>CA3</b>	H	H	H	L	L	L	H	H	H	H	L	L	L	L	L	H

NOTE 1 CS must always be driven LOW.  
 NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.  
 NOTE 3 The pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

**Table 458 – CA Pattern for IDD4R**

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	Note
<b>R0</b>	H	Read	H	H	L	L	1
<b>F0</b>	X		L	L	L	L	
<b>R1</b>	H		L	L	L	L	
<b>F1</b>	X		L	H	H	L	
<b>R3</b>	L	DES	L	L	L	L	
<b>F3</b>	X		L	L	L	L	
<b>R4</b>	L	DES	L	L	L	L	
<b>F4</b>	X		L	L	L	L	
<b>R5</b>	L	DES	L	L	L	L	
<b>F5</b>	X		L	L	L	L	
<b>R6</b>	L	DES	L	L	L	L	
<b>F6</b>	X		L	L	L	L	
<b>R7</b>	H	Read	H	H	L	H	2
<b>F7</b>	X		L	L	L	L	
<b>R8</b>	H		L	L	L	L	
<b>F8</b>	X		L	L	L	L	
<b>R9</b>	Low	DES	L	L	L	L	
<b>F9</b>	Low		L	L	L	L	
<b>R10</b>	L	DES	L	L	L	L	
<b>F10</b>	X		L	L	L	L	
<b>R11</b>	L	DES	L	L	L	L	
<b>F11</b>	X		L	L	L	L	

**Table 458 — CA Pattern for IDD4R (cont'd)**

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	Note
R12	L	DES	L	L	L	L	
F12	X		L	L	L	L	
R13	H	Read	H	H	L	L	3
F13	X		L	L	L	L	
R14	H		L	L	L	L	
F14	X		L	H	H	L	
R15	L	DES	L	L	L	L	
F15	X		L	L	L	L	
R16	L	DES	L	L	L	L	
F16	X		L	L	L	L	
R17	L	DES	L	L	L	L	
F17	X		L	L	L	L	
R18	L	DES	L	L	L	L	
F18	X		L	L	L	L	
R19	H	Read	H	H	L	H	4
F19	X		L	L	L	L	
R20	H		L	L	L	L	
F20	X		L	L	L	L	
R21	Low	DES	L	L	L	L	
F21	Low		L	L	L	L	
R22	L	DES	L	L	L	L	
F22	X		L	L	L	L	
R23	L	DES	L	L	L	L	
F23	X		L	L	L	L	
R24	L	DES	L	L	L	L	
F24	X		L	L	L	L	

**Table 459 – CA Pattern for IDD4W**

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	Note
R0	H	Write	H	L	H	L	1
F0	X		L	L	L	L	
R1	H		L	L	L	L	
F1	X		L	H	L	H	
R3	L	DES	L	L	L	L	
F3	X		L	L	L	L	
R4	L	DES	L	L	L	L	
F4	X		L	L	L	L	
R5	L	DES	L	L	L	L	
F5	X		L	L	L	L	
R6	L	DES	L	L	L	L	
F6	X		L	L	L	L	

**Table 459 — CA Pattern for IDD4W (cont'd)**

Clock Cycle #	CS	Command	CA0	CA1	CA2	CA3	Note
R7	H	Write	H	L	H	L	2
F7	X		L	L	L	L	
R8	H		L	L	L	L	
F8	X		L	H	L	H	
R9	Low	DES	L	L	L	L	
F9	Low		L	L	L	L	
R10	L	DES	L	L	L	L	
F10	X		L	L	L	L	
R11	L	DES	L	L	L	L	
F11	X		L	L	L	L	
R12	L	DES	L	L	L	L	
F12	X		L	L	L	L	
R13	H	Write	H	L	H	L	3
F13	X		L	L	L	L	
R14	H		L	L	L	L	
F14	X		L	H	L	H	
R15	L	DES	L	L	L	L	
F15	X		L	L	L	L	
R16	L	DES	L	L	L	L	
F16	X		L	L	L	L	
R17	L	DES	L	L	L	L	
F17	X		L	L	L	L	
R18	L	DES	L	L	L	L	
F18	X		L	L	L	L	
R19	H	Write	H	L	H	L	4
F19	X		L	L	L	L	
R20	H		L	L	L	L	
F20	X		L	H	L	H	
R21	Low	DES	L	L	L	L	
F21	Low		L	L	L	L	
R22	L	DES	L	L	L	L	
F22	X		L	L	L	L	
R23	L	DES	L	L	L	L	
F23	X		L	L	L	L	
R24	L	DES	L	L	L	L	
F24	X		L	L	L	L	

### **14.1 IDD Measurement Conditions (cont'd)**

**Table 460 – Data Pattern for IDD4R @ DBI Off**

**Table 460 — Data Pattern for IDD4R @ DBI Off (cont'd)**

**Table 460 — Data Pattern for IDD4R @ DBI Off (cont'd)**

**Table 460 — Data Pattern for IDD4R @ DBI Off (cont'd)**

### **14.1 IDD Measurement Conditions (cont'd)**

**Table 461 – Data Pattern for IDD4R @ DBI On**

**Table 461 — Data Pattern for IDD4R @ DBI On (cont'd)**

**Table 461 — Data Pattern for IDD4R @ DBI On (cont'd)**

**Table 461 — Data Pattern for IDD4R @ DBI On (cont'd)**

#### **14.1 IDD Measurement Conditions (cont'd)**

**Table 462 – Data Pattern for IDD4W @ DBI Off**

**Table 462 — Data Pattern for IDD4W @ DBI Off (cont'd)**

**Table 462 — Data Pattern for IDD4W @ DBI Off (cont'd)**

**Table 462 — Data Pattern for IDD4W @ DBI Off (cont'd)**

### **14.1 IDD Measurement Conditions (cont'd)**

**Table 463 – Data Pattern for IDD4W @ DBI On**

**Table 463 — Data Pattern for IDD4W @ DBI On (cont'd)**

**Table 463 — Data Pattern for IDD4W @ DBI On (cont'd)**

**Table 463 — Data Pattern for IDD4W @ DBI On (cont'd)**

## 14.2 IDD Specifications

**Table 464 – LPDDR6 IDD Specification Parameters and Operating Conditions**

Parameter / Condition	Symbol	Power Supply	Note
<b>Operating one bank active-Precharge current:</b> tCK = tCKmin; tRC = tRCmin; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled WCK inputs are stable	IDD0 <sub>1</sub>	VDD1	
	IDD0 <sub>2C</sub>	VDD2C	
	IDD0 <sub>2D</sub>	VDD2D	
	IDD0 <sub>Q</sub>	VDDQ	3
<b>Idle power-down standby current:</b> tCK = tCKmin; Power-down entry command is issued CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT disabled WCK inputs are stable	IDD2P <sub>1</sub>	VDD1	
	IDD2P <sub>2C</sub>	VDD2C	
	IDD2P <sub>2D</sub>	VDD2D	
	IDD2P <sub>Q</sub>	VDDQ	3
	IDD2PS <sub>1</sub>	VDD1	
<b>Idle power-down standby current with clock stop:</b> CK_t =LOW, CK_c =HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled WCK inputs are stable	IDD2PS <sub>2C</sub>	VDD2C	
	IDD2PS <sub>2D</sub>	VDD2D	
	IDD2PS <sub>Q</sub>	VDDQ	3
	IDD2N <sub>1</sub>	VDD1	
<b>Idle non power-down standby current:</b> tCK = tCKmin; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled WCK inputs are stable	IDD2N <sub>2C</sub>	VDD2C	
	IDD2N <sub>2D</sub>	VDD2D	
	IDD2N <sub>Q</sub>	VDDQ	3
	IDD2NS <sub>1</sub>	VDD1	
<b>Idle non power-down standby current with clock stopped:</b> CK_t=LOW; CK_c=HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled WCK inputs are stable	IDD2NS <sub>2C</sub>	VDD2C	
	IDD2NS <sub>2D</sub>	VDD2D	
	IDD2NS <sub>Q</sub>	VDDQ	3
	IDD3P <sub>1</sub>	VDD1	
<b>Active power-down standby current:</b> tCK = tCKmin; CS is LOW; One bank is active; Power-down entry command is issued CA bus inputs are switching; Data bus inputs are stable ODT disabled WCK inputs are stable	IDD3P <sub>2C</sub>	VDD2C	
	IDD3P <sub>2D</sub>	VDD2D	
	IDD3P <sub>Q</sub>	VDDQ	3

**Table 464 — LPDDR6 IDD Specification Parameters and Operating Conditions (cont'd)**

Parameter / Condition	Symbol	Power Supply	Note
<b>Active power-down standby current with clock stop:</b> Power-down entry command is issued CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled WCK inputs are stable and static	IDD3PS <sub>1</sub> IDD3PS <sub>2C</sub> IDD3PS <sub>2D</sub> IDD3PS <sub>Q</sub>	VDD1 VDD2C VDD2D VDDQ	
<b>Active non-power-down standby current:</b> tCK = tCKmin; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled WCK inputs are stable and static	IDD3N <sub>1</sub> IDD3N <sub>2C</sub> IDD3N <sub>2D</sub> IDD3N <sub>Q</sub>	VDD1 VDD2C VDD2D VDDQ	
<b>Operating burst READ current</b> tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; <b>One bank in each bank group 1 and 2 is active;</b> BL = 24 or 48 ; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4R <sub>1</sub> IDD4R <sub>2C</sub> IDD4R <sub>2D</sub> IDD4R <sub>Q</sub>	VDD1 VDD2C VDD2D VDDQ	
<b>Operating burst READ current with DVFSH or DVFSB</b> tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; <b>One bank is active;</b> BL = 24 or 48; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled <b>DVFSH or DVFSB mode is enabled</b>	IDD4R <sub>DVFS1</sub> IDD4R <sub>DVFS2C</sub> IDD4R <sub>DVFS2D</sub> IDD4R <sub>DVFSQ</sub>	VDD1 VDD2C VDD2D VDDQ	8, 9
<b>Operating burst WRITE current</b> tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; <b>One bank in each bank group 1 and 2 is active;</b> BL = 24 or 48 ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	IDD4W <sub>1</sub> IDD4W <sub>2C</sub> IDD4W <sub>2D</sub> IDD4W <sub>Q</sub>	VDD1 VDD2C VDD2D VDDQ	
<b>Operating burst WRITE current with DVFSH or DVFSB</b> tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; <b>One bank is active;</b> BL = 24 or 48; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled <b>DVFSH or DVFSB mode is enabled</b>	IDD4W <sub>DVFS1</sub> IDD4W <sub>DVFS2C</sub> IDD4W <sub>DVFS2D</sub> IDD4W <sub>DVFSQ</sub>	VDD1 VDD2C VDD2D VDDQ	8, 9

**Table 464 — LPDDR6 IDD Specification Parameters and Operating Conditions (cont'd)**

Parameter / Condition	Symbol	Power Supply	Note
<b>All-bank REFRESH Burst current:</b> tCK = tCKmin; CS is LOW between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled WCK inputs are stable and static	IDD5 <sub>1</sub>	VDD1	
	IDD5 <sub>2C</sub>	VDD2C	
	IDD5 <sub>2D</sub>	VDD2D	
	IDD5 <sub>Q</sub>	VDDQ	4
<b>All-bank REFRESH Average current:</b> tCK = tCKmin; CS is LOW between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT disabled WCK inputs are stable and static	IDD5AB <sub>1</sub>	VDD1	
	IDD5AB <sub>2C</sub>	VDD2C	
	IDD5AB <sub>2D</sub>	VDD2D	
	IDD5AB <sub>Q</sub>	VDDQ	4
<b>Per-2-bank REFRESH Average current:</b> tCK = tCKmin; CS is LOW between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT disabled WCK inputs are stable and static	IDD5PDB <sub>1</sub>	VDD1	
	IDD5PDB <sub>2C</sub>	VDD2C	
	IDD5PDB <sub>2D</sub>	VDD2D	
	IDD5PDB <sub>Q</sub>	VDDQ	4
<b>Power down Self refresh current:</b> CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ( $\leq 85^{\circ}\text{C}$ ) Maximum TBDx Self-Refresh Rate; ( $> 85^{\circ}\text{C}$ ) ODT disabled WCK inputs are stable and static	IDD6 <sub>1</sub>	VDD1	6,7
	IDD6 <sub>2C</sub>	VDD2C	6,7
	IDD6 <sub>2D</sub>	VDD2D	6,7
	IDD6 <sub>Q</sub>	VDDQ	4,6,7
NOTE 1 Published IDD values are the maximum of the distribution of the arithmetic mean.			
NOTE 2 DQ ODT disabled. MR19 OP[2:0]=000 <sub>B</sub> .			
NOTE 3 IDD current specifications are tested after the device is properly initialized.			
NOTE 4 Measured currents are the summation of VDDQ and VDD2C / VDD2D.			
NOTE 5 Guaranteed by design with output load = 5 pF and RON = 40 ohm.			
NOTE 6 The 1x Self-Refresh Rate is the rate at which the LPDDR6 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.			
NOTE 7 This is the general definition that applies to full array Self Refresh.			
NOTE 8 When DVFSH or DVFSB is enabled, the minimum tCK shall be set by following DVFSH or DVFSB operating frequency.			
NOTE 9 IDD values can be different according to the DVFSH or DVFSB set by MR11 OP[3:2].			

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## 15 Electrical Characteristics and AC Timing

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### 15.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR6 device.

#### 15.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200-cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(\text{avg}) = \left( \sum_{j=1}^N tCKj \right) / N$$

where  $N = 200$

Unit "tCK(avg)" represents the actual clock average tCK(avg) of the input clock under operation. Unit "nCK" represents one clock cycle of the input clock, counting the actual clock edges. tCK(avg) may change by up to +/-1% within a 100-clock cycle window, provided that all jitter and timing specs are met.

#### 15.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

#### 15.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(\text{avg}) = \left( \sum_{j=1}^N tCHj \right) / (N \times tCK(\text{avg}))$$

where  $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(\text{avg}) = \left( \sum_{j=1}^N tCLj \right) / (N \times tCK(\text{avg}))$$

where  $N = 200$

#### 15.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

#### 15.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCK*i* - tCK(avg) where *i* = 1 to 200}.

tJIT(per),act is the actual clock jitter for a given system.

tJIT(per),allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

#### 15.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of |{tCK(*i*+1) - tCK(*i*)}|.

tJIT(cc) defines the cycle-to-cycle jitter.

tJIT(cc) is not subject to production test.

#### 15.1.7 Clock Timing

**Table 465 — Clock AC Timings for 20/267/400 MHz**

Parameter	Symbol	20 MHz		267 MHz		400 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	50	50	3.75	50	2.5	50	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-2800	2800	-210	210	-140	140	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	5600	-	420	-	280	ps	

### 15.1.7 Clock Timing (cont'd)

**Table 466 – Clock AC Timings for 533/688/800 MHz**

Parameter	Symbol	533 MHz		688 MHz		800 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	1.875	50	1.453	50	1.25	50	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-110	110	-85	85	-70	70	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	220	-	170	-	140	ps	

**Table 467 – Clock AC Timings for 937.5/1066.5/1200 MHz**

Parameter	Symbol	937.5 (938) MHz		1066.5 (1067) MHz		1200 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	1066.7ps	50ns	937.6ps	50ns	833ps	50ns	-	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-60	60	-55	55	-50	50	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	120	-	110	-	100	ps	

**Table 468 – Clock AC Timings for 1375/1600/1875 MHz**

Parameter	Symbol	1375 MHz		1600 MHz		1875 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Average clock period	tCK(avg)	727ps	50ns	625ps	50ns	533ps	50ns	-	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-46	46	-40	40	-34	34	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	92	-	80	-	68	ps	

### 15.1.7 Clock Timing (cont'd)

**Table 469 – Clock AC Timings for 2133/2400 MHz**

Parameter	Symbol	2133 MHz		2400 MHz		Units	Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	469ps	50ns	417ps	50ns	-	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-30	30	-28	28	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	60	-	56	ps	

**Table 470 – Clock AC Timings for 2667/2933 MHz**

Parameter	Symbol	2667 MHz		2933 MHz		Units	Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	375ps	50ns	341ps	50ns	-	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	TBD	TBD	TBD	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	TBD	-	TBD	ps	

**Table 471 – Clock AC Timings for 3200/3600 MHz**

Parameter	Symbol	3200 MHz		3600 MHz		Units	Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	313ps	50ns	278ps	50ns	-	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	TBD	TBD	TBD	TBD	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	TBD	-	TBD	ps	

## 15.2 Write Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input write clocks violating the min/max values may result in malfunction of the LPDDR6 device.

### 15.2.1 Definition for tWCK(avg) and nWCK

tWCK(avg) is calculated as the average write clock period across any consecutive 200-cycle window, where each write clock period is calculated from rising edge to rising edge.

$$tWCK(\text{avg}) = \left( \sum_{j=1}^N tWCKj \right) / N$$

where  $N = 200$

Unit "tWCK(avg)" represents the actual write clock average tWCK(avg) of the input write clock under operation. Unit "nWCK" represents one write clock cycle of the input write clock, counting the actual write clock edges. tWCK(avg) may change by up to +/-1% within a 100 write clock cycle window, provided that all jitter and timing specs are met.

### 15.2.2 Definition for tWCK(abs)

tWCK(abs) is defined as the absolute write clock period, as measured from one rising edge to the next consecutive rising edge.

tWCK(abs) is not subject to production test.

### 15.2.3 Definition for tWCKH(avg) and tWCKL(avg)

tWCKH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tWCKH(\text{avg}) = \left( \sum_{j=1}^N tWCKHj \right) / (N \times tWCK(\text{avg}))$$

where  $N = 200$

tWCKL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tWCKL(\text{avg}) = \left( \sum_{j=1}^N tWCKLj \right) / (N \times tWCK(\text{avg}))$$

where  $N = 200$

#### **15.2.4 Definition for tWCKH(abs) and tWCKL(abs)**

tWCKH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge.

tWCKL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge.

Both tWCKH(abs) and tWCKL(abs) are not subject to production test.

#### **15.2.5 Definition for tJIT(per)**

tJIT(per) is the single period jitter defined as the largest deviation of any signal tWCK from tWCK(avg).

$tJIT(\text{per}) = \text{Min/max of } \{tWCK_i - tWCK(\text{avg}) \text{ where } i = 1 \text{ to } 200\}.$

tJIT(per),act is the actual write clock jitter for a given system.

tJIT(per),allowed is the specified allowed write clock period jitter.

tJIT(per) is not subject to production test.

#### **15.2.6 Definition for tJIT(cc)**

tJIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles.

$tJIT(\text{cc}) = \text{Max of } |\{tWCK(i+1) - tWCK(i)\}|.$

tJIT(cc) defines the cycle-to-cycle jitter.

tJIT(cc) is not subject to production test.

### 15.2.7 Write Clock Timing

**Table 472 — Write Clock AC Timings for 40/533/800 MHz**

Parameter	Symbol	40 MHz		533 MHz		800 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write Clock Timing									
Average Write Clock period	tWCK(avg)	25	25	1.875	25	1.25	25	ns	
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns	
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-1400	1400	-110	110	-70	70	ps	
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	2800	-	220	-	140	ps	

**Table 473 — Write Clock AC Timings for 1067 (1066.5)/1375/1600 MHz**

Parameter	Symbol	1067 (1066.5) MHz		1375 MHz		1600 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write Clock Timing									
Average Write Clock period	tWCK(avg)	937.6ps	25ns	727ps	25ns	625ps	25ns	-	
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns	
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-55	55	-46	46	-40	40	ps	
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	110	-	92	-	80	ps	

### 15.2.7 Write Clock Timing (cont'd)

**Table 474 — Write Clock AC Timings for 1875/2133/2400 MHz**

Parameter	Symbol	1875 MHz		2133 MHz		2400 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
<b>Write Clock Timing</b>									
Average Write Clock period	tWCK(avg)	533ps	25ns	469ps	25ns	417ps	25ns	-	
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns	
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-34	34	-30	30	-28	28	ps	
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	68	-	60	-	56	ps	

**Table 475 — Write Clock AC Timings for 2750/3200/3750 MHz**

Parameter	Symbol	2750 MHz		3200 MHz		3750 MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
<b>Write Clock Timing</b>									
Average Write Clock period	tWCK(avg)	364ps	25ns	313ps	25ns	267ps	25ns	-	
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns	
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-25	25	-21	21	-18	18	ps	
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	50	-	42	-	36	ps	

### 15.2.7 Write Clock Timing (cont'd)

**Table 476 — Write Clock AC Timings for 4267 (4266.5)/4800/5334 (5333.5) MHz**

Parameter	Symbol	4267 (4266.5) MHz		4800 MHz		5334(5333.5) MHz		Units	Notes
		Min	Max	Min	Max	Min	Max		
<b>Write Clock Timing</b>									
Average Write Clock period	tWCK(avg)	235ps	25ns	209ps	25ns	188ps	25ns	-	
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tWCK(avg)	
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns	
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)	
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-16	16	-14	14	-13	13	ps	
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	32	-	28	-	26	ps	

### 15.3 tWCK2DQ AC Parameters

LPDDR6 supports two WCK frequency (WCK FM) modes. One is “Low frequency (LF) mode” and the other is “High frequency (HF) mode”.

WCK FM affects tWCK2DQI/O AC parameter values, and concrete parameters and their values defined in Table 477.

Switching LF mode and HF mode is controlled by MR11 OP[6]. And FSP procedure is required to change MR11 OP[6] setting from LF mode to HF mode and vice versa.

### 15.3 tWCK2DQ AC Parameters (cont'd)

Table 477 — tWCK2DQ AC Parameters

Parameter	Symbol	Data Rate				Min/Max	Units	Notes
		Up to 1600Mbps ≤ 1600Mbps	1600Mbps~4800Mbps > 1600Mbps ≤ 4800Mbps	4800Mbps~10667Mbps > 4800Mbps ≤ 10667Mbps	Beyond 10667Mbps > 10667Mbps			
DQ to WCK input offset	tWCK2DQI_HF	250/600	250/600	250/600	TBD	Min/Max	ps	
	tWCK2DQI_LF	300/900	300/900	N/A	N/A	Min/Max	ps	
	tWCK2DQI_LF_L	300/900	N/A	N/A	N/A	Min/Max	ps	
WCK to DQ input offset temperature variation (Write)	tWCK2DQI_temp_HF	0.6	0.6	0.5	TBD	Max	ps/°C	
	tWCK2DQI_temp_LF	0.7	0.7	N/A	N/A	Max	ps/°C	
	tWCK2DQI_temp_LF_L	0.7	N/A	N/A	N/A	Max	ps/°C	
WCK to DQ input offset voltage variation (Write)	tWCK2DQI_volt_HF	25	25	25	TBD	Max	ps/50mV	
	tWCK2DQI_volt_LF	50	50	N/A	N/A	Max	ps/50mV	
	tWCK2DQI_volt_LF_L	80	N/A	N/A	N/A	Max	ps/50mV	
DQ to WCK output offset	tWCK2DQO_HF	650/1600	650/1600	650/1600	TBD	Min/Max	ps	
	tWCK2DQO_LF	650/1900	650/1900	N/A	N/A	Min/Max	ps	
	tWCK2DQO_LF_L	650/1900	N/A	N/A	N/A	Min/Max	ps	
WCK to DQ output offset temperature variation (Read)	tWCK2DQO_temp_HF	1.5	1.5	1.4	TBD	Max	ps/°C	
	tWCK2DQO_temp_LF	1.8	1.8	N/A	N/A	Max	ps/°C	
	tWCK2DQO_temp_LF_L	1.8	N/A	N/A	N/A	Max	ps/°C	
WCK to DQ output offset voltage variation (Read)	tWCK2DQO_volt_HF	3.0	3.0	2.5	TBD	Max	ps/mV	
	tWCK2DQO_volt_LF	5.0	5.0	N/A	N/A	Max	ps/mV	
	tWCK2DQO_volt_LF_L	6.0	N/A	N/A	N/A	Max	ps/mV	

NOTE 1 Regarding Combination among WCKFM, DVFSL, DVFSH and DVFSB setting, and its application for HF, LF and LF\_L, refer to Table 478 for detail.

NOTE 2 Depending on the frequency of operation, the value may change within the specified range. Hence, the system should undergo re-training to align with the updated timing for proper operation following a frequency change.

NOTE 3 Depending on the frequency of operation and the transition of VDD2C/D level, the value exhibited by the SDRAM may change within the specified range (Informative).

### 15.3 tWCK2DQ AC Parameters (cont'd)

Relationship between WCK Frequency mode (WCK FM) setting and VDD2C/D setting is shown in Table 478.

**Table 478 – Relationship between WCK FM Setting and VDD2C/D Setting**

WCK FM: MR11 OP[6]	VDD2C/D Setting			
	Normal	DVFH	DVFSB	DVFSL
0 <sub>B</sub> : Low frequency mode	Allowed	Prohibited	Prohibited	Allowed
1 <sub>B</sub> : High frequency mode	Allowed	Allowed	Allowed	Prohibited

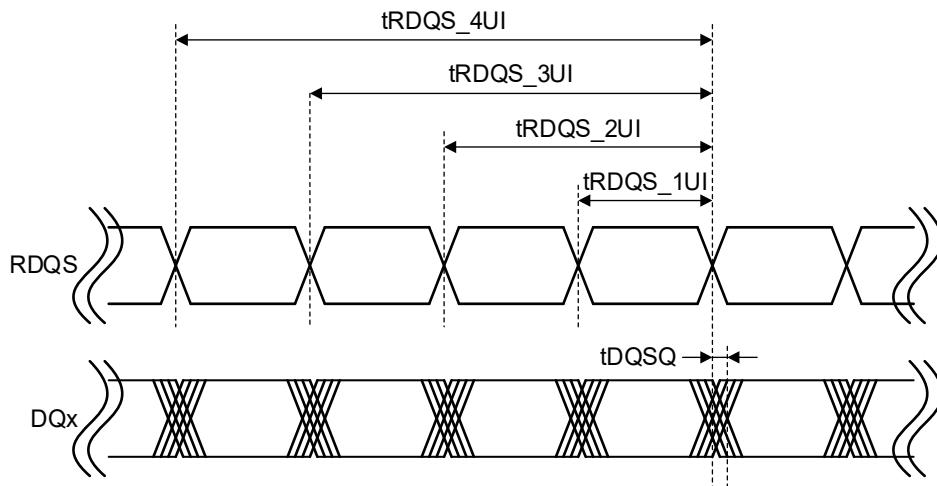
NOTE 1 VDD2C/D Setting for Mode Register is below.  
 Normal => DVFH: MR11 OP[2]=0<sub>B</sub>, DVFSB: MR11 OP[3]=0<sub>B</sub>, DVFSL: MR11 OP[4]=0<sub>B</sub>  
 DVFH => DVFH: MR11 OP[2]=1<sub>B</sub>, DVFSB: MR11 OP[3]= Don't Care,  
 DVFSL: MR11 OP[4]= 0<sub>B</sub>  
 DVFSB => DVFH: MR11 OP[2]=Don't Care, DVFSB: MR11 OP[3]=1<sub>B</sub>,  
 DVFSL: MR11 OP[4]=0<sub>B</sub>  
 DVFSL => DVFH: MR11 OP[2]=0<sub>B</sub>, DVFSB: MR11 OP[3]=0<sub>B</sub>,  
 DVFSL: MR11 OP[4]=1<sub>B</sub>

NOTE 2 "LF\_L" applies when DVFSL mode: DVFSL MR11 OP[4]=1<sub>B</sub>

### 15.4 DQ Tx Jitter Spec

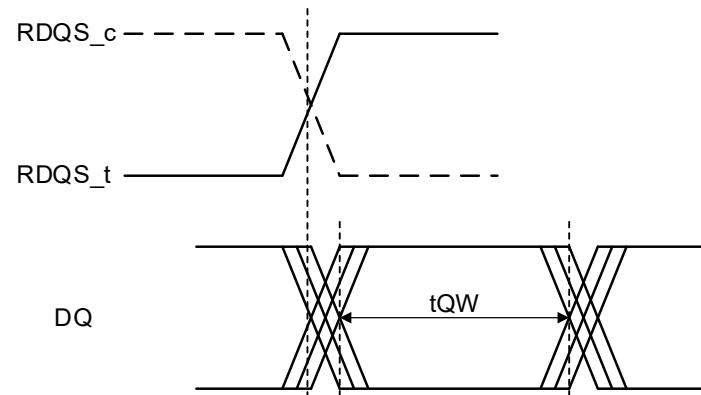
The DRAM DQ to RDQS differential jitter is defined to support both SOC matched and unmatched DQ-RDQS input receiver (Rx) types over NUI of mismatch. All output timings are referenced to RDQS for source synchronous timing relationship. The appropriate RDQS preamble mode must be selected in order to support the unmatched SOC Rx. It is the responsibility of the SOC and system to ensure the advanced RDQS preambles edges are robust for system operation.

The N-UI DQ to RDQS output timing is defined by tRDQS\_NUI in conjunction with tDQSQ where NUI defines the number of UI RDQS is shifted from the corresponding DQ as shown in the figures below.



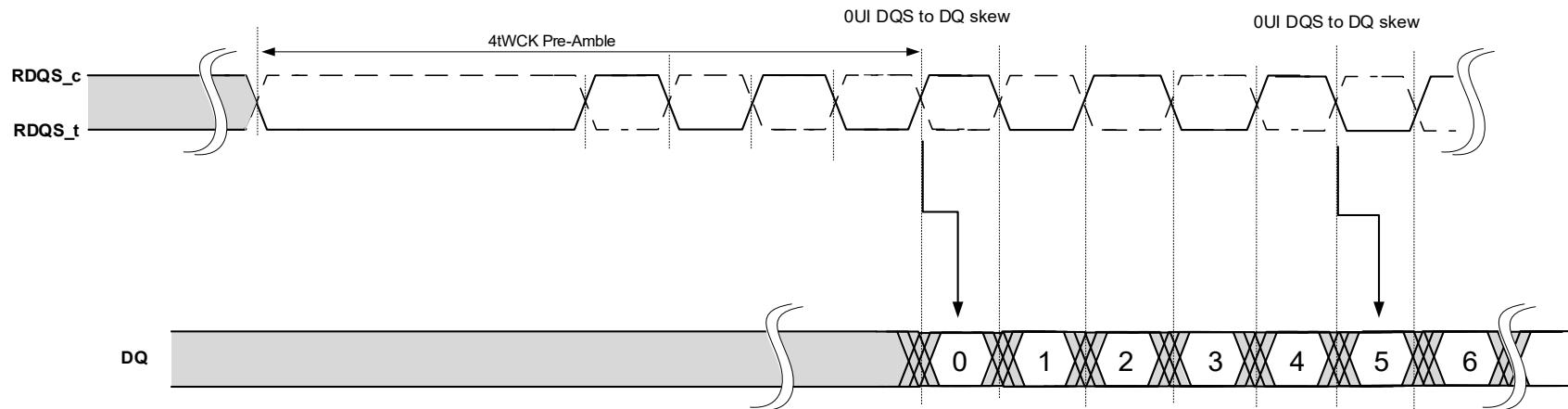
**Figure 247 – N-UI DQ to RDQS Output Timing Definitions**

#### 15.4.1 DQ Tx Jitter Spec (cont'd)



**Figure 248 – DQ Eye Width per Pin ( $tQW$ )**

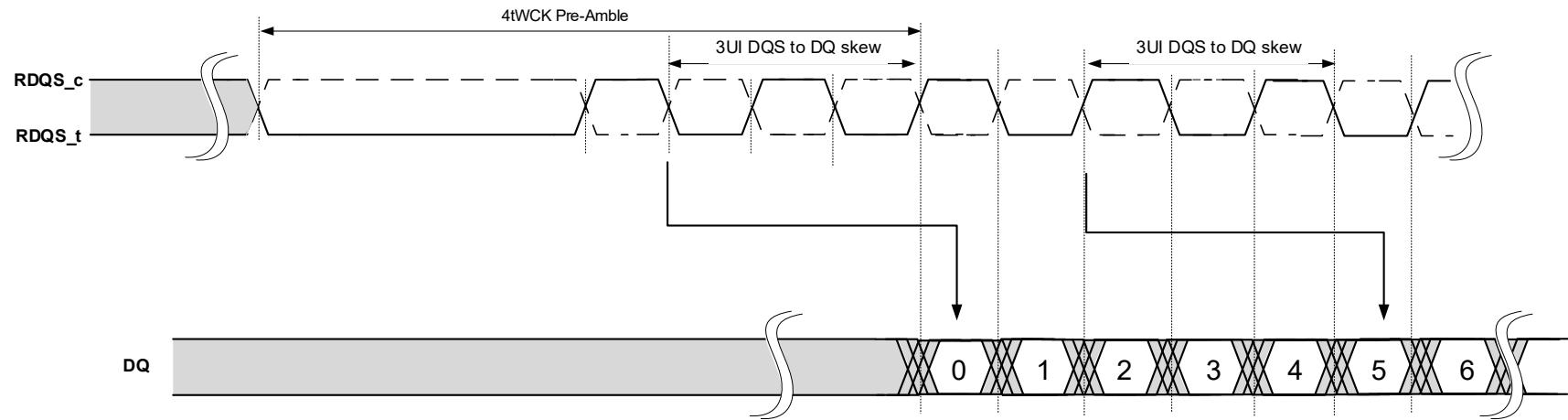
The figures below include examples of 0 and 3UI mismatch using the 4 twck RDQS read preamble of 2twck static + 2twck toggle.



NOTE 1 It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

**Figure 249 – Read Burst Example for Pin DQx Depicting Bits 0 and 5 Relative to the RDQS Edge for 0 UI Mismatch**

### 15.4.1 DQ Tx Jitter Spec (cont'd)



NOTE 1 It is the responsibility of the SOC and system to insure the advanced RDQS preambles edges are robust for system operation.

**Figure 250 – Read Burst Example for Pin DQx Depicting Bits 0 and 5 Relative to the RDQS Edge for 3 UI Mismatch**

### 15.4.1 DQ Tx Jitter Spec (cont'd)

**Table 479 – DRAM DQ, DQS Output Timing**

Symbol	Parameter	Data Rate [Mbps]								Units	Notes		
		$\leq 6400$		7500 / 8533/9600		10667		11733/12800/ 14400					
		Min	Max	Min	Max	Min	Max	Min	Max				
tDQSQ	RDQS_t, RDQS_c to DQ Skew per byte group	-	0.26	-	0.37	-	TBD	-	TBD	UI	1,2,3,4		
tQW	DQ eye width per pin	tWCKH/L(abs)MIN - 0.17	-	tWCKH/L(abs)MIN - 0.17	-	tWCKH/L(abs)MIN - 0.17	-	TBD	-	UI	1,2,5		
tjitRDQS_1UI(avg)	Average 1UI jitter of RDQS (Duty-Cycle jitter)	- 0.017	+ 0.017	- 0.017	+ 0.017	- 0.017	+ 0.017	TBD	TBD	UI			
tjitRDQS_1UI(abs)	Absolute 1UI jitter of RDQS	- 0.039	+ 0.039	- 0.039	+ 0.039	- 0.039	+ 0.039	TBD	TBD	UI	1,2,6		
tjitRDQS_2UI(abs)	Absolute 2UI jitter of RDQS	- 0.03	+ 0.03	- 0.03	+ 0.03	- 0.03	+ 0.03	TBD	TBD	UI	1,2,6		
tjitRDQS_3UI(abs)	Absolute 3UI jitter of RDQS	- 0.056	+ 0.056	- 0.056	+ 0.056	- 0.056	+ 0.056	TBD	TBD	UI	1,2,6		
tjitRDQS_4UI(abs)	Absolute 4UI jitter of RDQS	- 0.035	+ 0.035	- 0.035	+ 0.035	- 0.035	+ 0.035	TBD	TBD	UI	1,2,6		
tjitRDQS_5UI(abs)	Absolute 5UI jitter of RDQS	- 0.074	+ 0.074	- 0.074	+ 0.074	- 0.074	+ 0.074	TBD	TBD	UI	1,2,6		
tjitRDQS_6UI(abs)	Absolute 6UI jitter of RDQS	- 0.053	+ 0.053	- 0.053	+ 0.053	- 0.053	+ 0.053	TBD	TBD	UI	1,2,6		
tjitRDQS_1UI	Remainder of absolute 1UI jitter of RDQS with average 1UI jitter removed	- 0.022	+ 0.022	- 0.022	+ 0.022	- 0.022	+ 0.022	TBD	TBD	UI	1,2,6,7		
tjitRDQS_3UI	Remainder of absolute 3UI jitter of RDQS with average 1UI jitter removed	- 0.039	+ 0.039	- 0.039	+ 0.039	- 0.039	+ 0.039	TBD	TBD	UI	1,2,6,8		
tjitRDQS_5UI	Remainder of absolute 5UI jitter of RDQS with average 1UI jitter removed	- 0.057	+ 0.057	- 0.057	+ 0.057	- 0.057	+ 0.057	TBD	TBD	UI	1,2,6,9		

**Table 479 — DRAM DQ, DQS Output Timing (cont'd)**

NOTE 1	These parameters are defined over voltage and temperature.
NOTE 2	This parameter value is defined after duty cycle adjustment is applied. These parameter values before duty cycle adjustment can be varied depending on the amount of WCK input duty cycle distortion.
NOTE 3	These parameters are a function of WCK input clock jitter tWCKH and tWCKL. Note for tWCKL(abs)MIN of 0.43tWCK = 0.86 UI.
NOTE 4	These parameters are defined as min/max across all DQ pins per byte group. This includes the across pin variation within a byte group.
NOTE 5	Equation applies to tWCKH/L(abs) MIN = 0.43 ... 0.46tWCK. If tWCKH/L(abs) MIN >= 0.46tWCK then tQW = 0.75UI. Example1: If tWCKH/L(abs) MIN is 0.43tWCK then tQW MIN = tWCKH/L(abs) MIN - 0.17 UI = 0.86 UI - 0.17UI = 0.69UI. Example2: If tWCKH/L(abs) MIN is 0.46tWCK then tQW MIN = tWCKH/L(abs) MIN - 0.17 UI = 0.92 UI - 0.17UI = 0.75UI. Example3: If tWCKH/L(abs) MIN is 0.48tWCK then tQW MIN = 0.75UI.
NOTE 6	This parameter is defined as tjitRDQS_NUI = tRDQS_NUI - N*UI where N= 1,2,3,4 and UI is the unit interval. Example tjitRDQS_2UI= tRDQS_2UI - 2*UI.
NOTE 7	tjitRDQS_1UI MAX = tjitRDQS_1UI(abs) MAX - tjitRDQS_1UI(avg) MAX; tjitRDQS_1UI MIN = tjitRDQS_1UI(abs) MIN - tjitRDQS_1UI(avg) MIN.
NOTE 8	tjitRDQS_3UI MAX = tjitRDQS_3UI(abs) MAX - tjitRDQS_1UI(avg) MAX; tjitRDQS_3UI MIN = tjitRDQS_3UI(abs) MIN - tjitRDQS_1UI(avg) MIN.
NOTE 9	tjitRDQS_5UI MAX = tjitRDQS_5UI(abs) MAX - tjitRDQS_1UI(avg) MAX; tjitRDQS_5UI MIN = tjitRDQS_5UI(abs) MIN - tjitRDQS_1UI(avg) MIN.

## 15.5 Timing Reference Point

LPDDR6 timing reference point defined at PKG ball except following spec items. The items are listed here are defined at die pad.

**Table 480 – Spec items Defined at Die Pads**

Signal	Spec items	Note
CK	Vinse_CK, Vinse_CK_High, Vinse_CK_Low, VIHdiff_CK, VILdiff_CK, SRIdiff_CK, Vix_CK_ratio, Vinse_CK_SE, Vinse_CK_SE_High, Vinse_CK_SE_low, VCKIVW, tCKHL, SRICKSE	
WCK	Vindiff_WCK, Vinse_WCK, Vinse_WCK_High, Vinse_WCK_Low, VIHdiff_WCK, VILdiff_WCK, SRIdiff_WCK, Vix_WCK_ratio, Vinse_WCK_SE, Vinse_WCK_SE_High, Vinse_WCK_SE_low, VWCKIVW, tWCKHL, SRIWCKSE	
CS	tCSIVWI, vCSIVW, tCSIPW, vCSIHL_AC	
CA	tCIPW1, tCIPW2, tCIHL, vCIHP1, vCILP1, vCIHP2, vCILP2, tCIVW_total, tCIVWd, vCIVW_total, vCIVWd	
DQ	tDIPW1, tDIPW2, tDIHL, vDIHP1, vDILP1, vDIHP2, vDILP2, tDIVW_total, tDIVWd, vDIVW_total, vDIVWd	

## 15.6 LPDDR6 CS Rx Specification

Need to Update

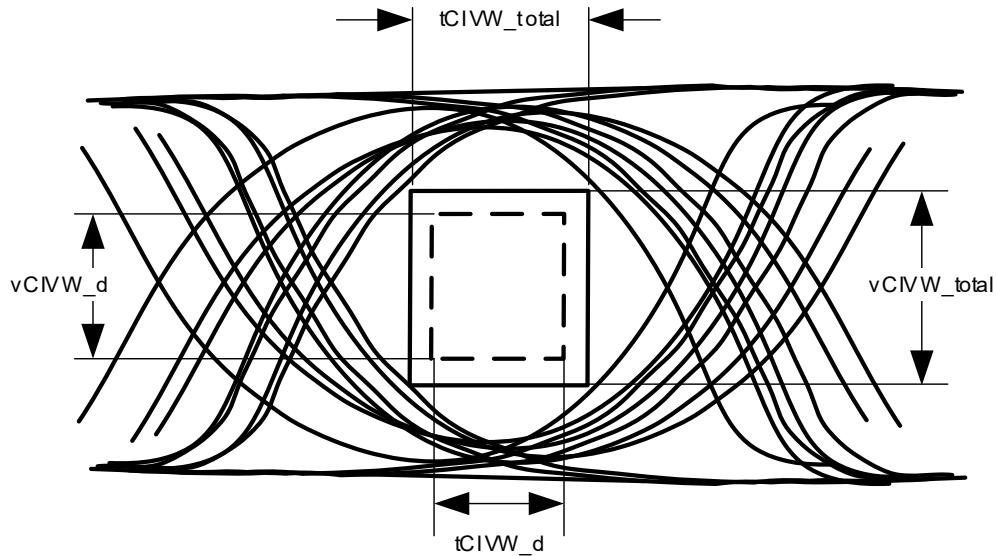
## 15.7 CA Rx Specification

### 15.7.1 CA Rx Mask and Single Pulse Definition

LPDDR6 CA Rx mask is defined as rectangle mask shape as shown in Figure 251. All CA signals apply the same compliance mask and operate in double data rate mode.

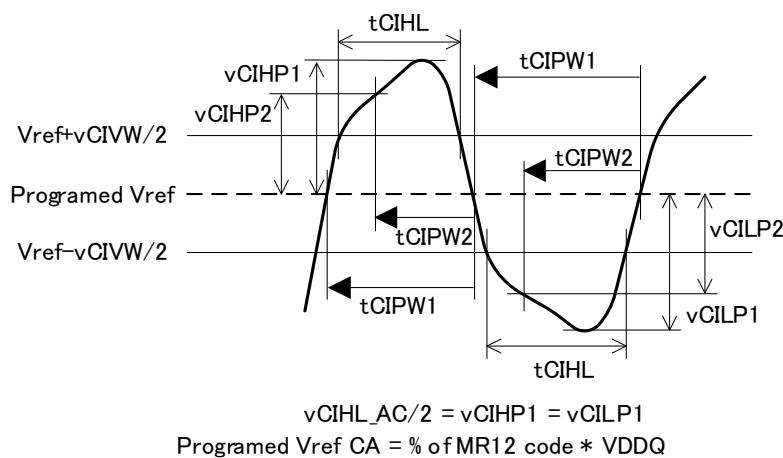
The input signal must not encroach the maximum area of the mask (Rx Mask) in order for the CA input receiver to successfully capture an input signal.

$t_{CIVW\_total}$  and  $v_{CIVW\_total}$  are defined at 1E-16 BER rate.  $t_{CIVWd}$  and  $v_{DIVWd}$  are defined as deterministic mask.



**Figure 251 – CA Rx Mask Definition**

LPDDR6 CA Rx single pulse definition is shown in Figure 252.

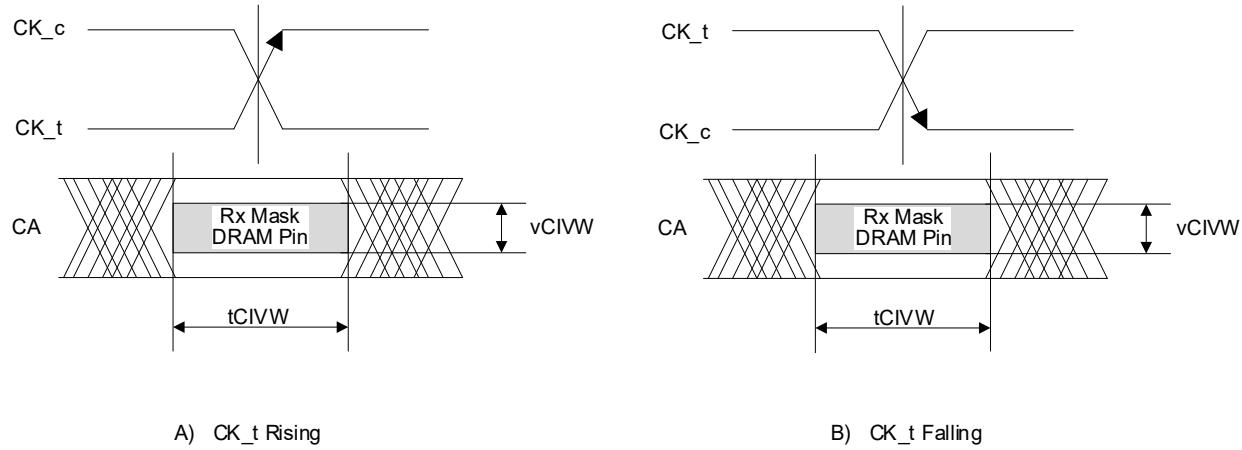


**Figure 252 – LPDDR6 CA Single Input Pulse Definition**

### 15.7.1.1 CA Rx Mask and Single Pulse Definition (cont'd)

**Table 481 – CA Single Input Pulse**

### 15.7.1.2 CA Rx Mask and Single Pulse Definition (cont'd)



**Figure 253 – CA Timings at the DRAM Pins**

Minimum CA Eye should be VrefCA aligned.

Differential CK mode definition.

All of the timing terms in Figure 253 are measured from CK<sub>t</sub>/CK<sub>c</sub> (differential mode) / CK (single ended mode) to the center (midpoint) of the tCIVW<sub>total</sub> and tCIVW<sub>d</sub> window taken at the midpoint and vCIVW voltage level. CA Rx mask window center is around CK<sub>t</sub>/CK<sub>c</sub> cross point (differential mode) / CK (single ended mode).

Single Ended CK mode definition

TBD

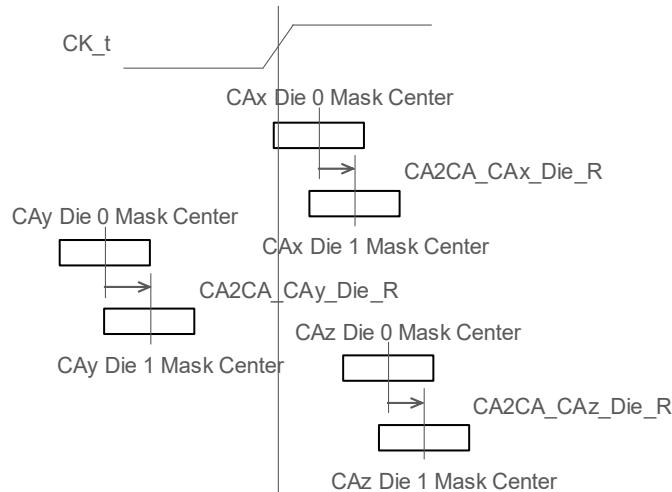
### 15.7.1.3 CA Rx Mask and Single Pulse Definition (cont'd)

**Table 482 — CA Rx**

#### 15.7.1.4 CA Rx Mask and Single Pulse Definition (cont'd)

tCA2CA\_share definition

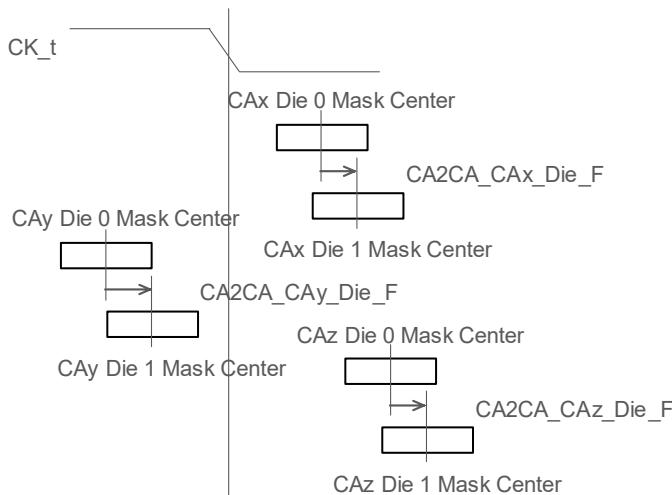
$$tCA2CA\_share = \max(CA2CA\_share\_R, CA2CA\_share\_F)$$



**Figure 254 – CK\_t Rising Edge CA Mask**

Definition of CA2CA\_share\_R

$$\begin{aligned} CA2CA\_share\_R &= \max(CA2CA\_CAi\_Die\_R) \text{ if } \min(CA2CA\_CAi\_Die\_R) \geq 0 \\ &\quad | \max(CA2CA\_CAi\_Die\_R) - \min(CA2CA\_CAi\_Die\_R) | \text{ if } \\ &\quad \max(CA2CA\_CAi\_Die\_R) \\ &\Rightarrow 0 \text{ and } \min(CA2CA\_CAi\_Die\_R) < 0 \\ &\quad | \min(CA2CA\_CAi\_Die\_R) | \text{ if } \max(CA2CA\_CAi\_Die\_R) < 0 \end{aligned}$$



**Figure 255 – CK\_t Falling Edge CA Mask**

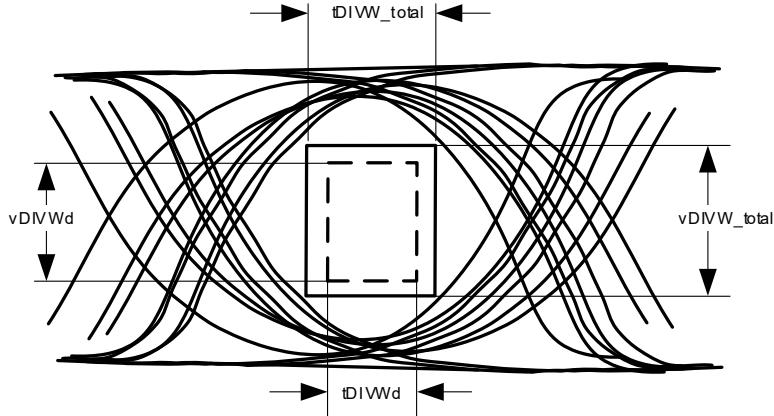
Definition of CA2CA\_share\_F

$$\begin{aligned} CA2CA\_share\_F &= \max(CA2CA\_CAi\_Die\_F) \text{ if } \min(CA2CA\_CAi\_Die\_F) \geq 0 \\ &\quad | \max(CA2CA\_CAi\_Die\_F) - \min(CA2CA\_CAi\_Die\_F) | \text{ if } \\ &\quad \max(CA2CA\_CAi\_Die\_F) \\ &\Rightarrow 0 \text{ and } \min(CA2CA\_CAi\_Die\_F) < 0 \\ &\quad | \min(CA2CA\_CAi\_Die\_F) | \text{ if } \max(CA2CA\_CAi\_Die\_F) < 0 \end{aligned}$$

## 15.8 DQ, Meta Data, and DBI Rx Specification

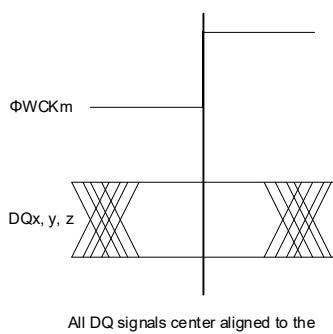
### 15.8.1 DQ, Meta Data, DBI Rx Mask, And Single Pulse Definition

LPDDR6 DQ, Meta Data, and DBI Rx mask are defined as rectangle mask as shown in Figure 256. The input signal must not encroach the maximum area of the mask( $vDIVWd$ ,  $vDIVW_{total}$ ,  $tDIVWd$ ,  $tDIVW_{total}$ ) in order for the DQ input receiver to successfully capture an input signal.



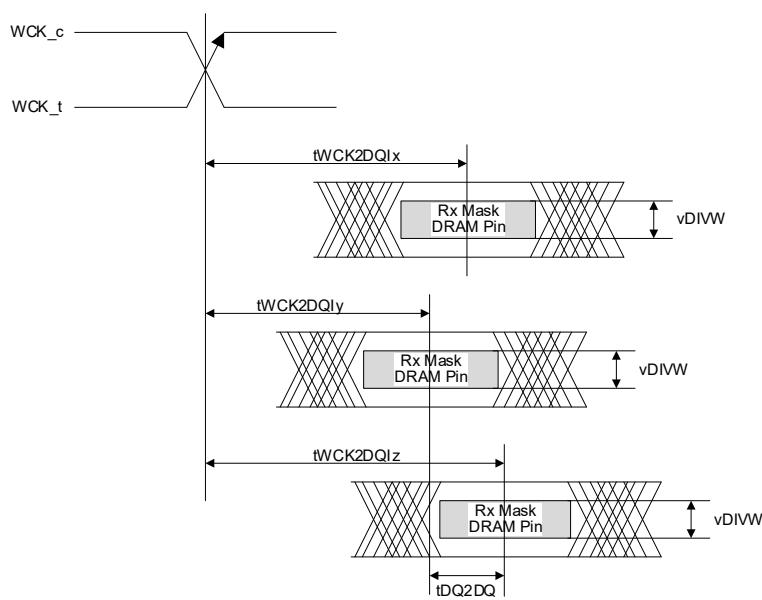
**Figure 256 – DQ, Meta Data, and DBI Rx Mask definition**

**DQ, internal WCK data-in at DRAM Latch**  
Internal composite Data-Eye Center aligned to Internal WCK



All DQ signals center aligned to the strobe at the DRAM internal latch

**DQ, WCK data-in at DRAM Pin**  
Non Minimum Data Eye / Maximum Rx Mask



NOTE 1 tWCK2DQI is measured at the center (midpoint) of the tDIVW window.

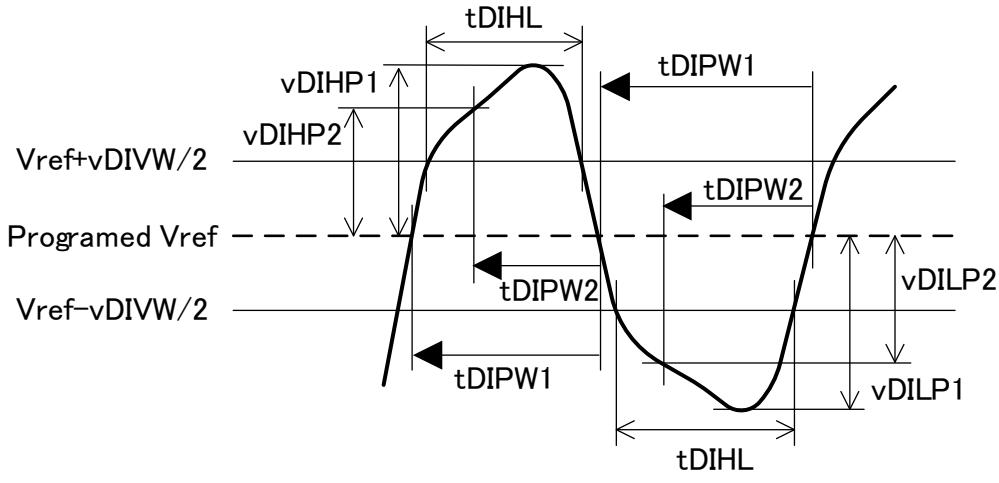
NOTE 2 DQz represents the max tWCK2DQI in this example.

NOTE 3 DQy represents the min tWCK2DQI in this example.

**Figure 257 – DQ to WCK tWCK2DQI and tDQ2DQ Timings at the DRAM Pins Referenced from the Internal Latch**

### 15.8.1 DQ, Meta Data, DBI Rx Mask, And Single Pulse Definition (cont'd)

LPDDR6 should follow the following single pulse definition.



$$vDIHL\_AC/2 = vDIHP1 = vDILP1$$

$$\text{Programmed Vref DQ} = \% \text{ of MR14/15 code} * VDDQ$$

**Figure 258 – LPDDR6 DQ Single Input Pulse Definition**

**Table 483 – DQ Single Input Pulse**

Item	Symbol	Min/ Max	Spec	Unit	Note
DQ Rx pulse width @ Vref DQ	tDIPW1	Min	0.45	UI	1
DQ Rx pulse reference	tDIPW2	Min	0.26	UI	1
DQ Rx pulse width @ Vref DQ +/- vDIVW/2	tDIHL	Min	0.21	UI	1
DQ Rx pulse amplitude from prog. Vref DQ	vDIHP1	Min	70	mV	
	vDILP1	Max	-70	mV	
DQ Rx early pulse amplitude from prog. Vref DQ	vDIHP2	Min	55	mV	
	vDILP2	Max	-55	mV	
NOTE 1 UI = tWCK/2, programed Vref is defined as % of MR14/15 code * VDDQ					

### **15.8.2 DQ, Meta Data, and DBI Rx Mask and Single Pulse Spec**

**Table 484 – DQ, Meta Data, and DBI Rx Specification**

## 15.9 Pull Up/Pull Down Driver Characteristics and Calibration

All output pins' (DQ, RDQS\_t and RDQS\_c) driver characteristics and calibration are defined as follows:

**Table 485 – Pull-down Driver Characteristics, with ZQ Calibration<sup>1,2</sup>**

$R_{ONPD,nom}$	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40PD}$	0.9	1	1.1	RZQ/6
48 Ohm	$R_{ON48PD}$	0.9	1	1.1	RZQ/5
60 Ohm	$R_{ON60PD}$	0.9	1	1.1	RZQ/4
80 Ohm	$R_{ON80PD}$	0.9	1	1.1	RZQ/3
120 Ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

NOTE 1 All values are after ZQ Calibration, see Table 487. Without ZQ Calibration  $R_{ONPD}$  values are  $\pm 30\%$ .  
 NOTE 2  $R_{ONPD}$  limits are defined at same voltage and temperature as at the time ZQ calibration was done.

**Table 486 – Pull-Up Characteristics, with ZQ Calibration<sup>1,2,3,4,5,6</sup>**

$VOH_{PU,nom}$	$VOH,nom$ (mV)	Min	Nom	Max	Unit
$V_{DDQ}^*0.5$	250	0.9	1	1.1	$VOH,nom$

NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration  $VOH(nom)$  values are  $\pm 30\%$ .  
 NOTE 2  $VOH,nom$  (mV) values are based on a nominal  $VDDQ = 0.5V$ ,  $VDD2C(TBD)=1.025 V$ .  
 NOTE 3  $VOH_{PU}$  limits are defined at same voltage and temperature as at the time ZQ calibration was done.  
 NOTE 4  $VOH_{PU}$  limits are defined for load termination matching the SOC ODT setting (in MR TBD) selected at the time ZQ calibration was done. If the selected SOC ODT setting MR TBD =000<sub>B</sub>, then the  $VOH_{PU}$  limits are not defined.  
 NOTE 5  $VOH_{PU}$  limits are defined as DC levels when all DQ drivers are driving high.  
 NOTE 6 Assumption of SOC ODT is typical for  $VOH_{PU,nom}$  definition.

**Table 487 – Valid Calibration Points<sup>1</sup>**

$VOH_{PU,nom}$	ODT Value					
	240	120	80	60	48	40
$V_{DDQ}^*0.5$	VALID	VALID	VALID	VALID	VALID	VALID

NOTE 1 Once the output is calibrated for a given  $VOH(nom)$  calibration point, the ODT value may be changed without recalibration.

**Table 488 – Unterminated Pull Up Characteristics**

$R_{ONUNPU,nom}^1$	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40UNPU}$	0.7	1	1.3	RZQ/6
48 Ohm	$R_{ON48UNPU}$	0.7	1	1.3	RZQ/5
60 Ohm	$R_{ON60UNPU}$	0.7	1	1.3	RZQ/4
80 Ohm	$R_{ON80UNPU}$	0.7	1	1.3	RZQ/3
120 Ohm	$R_{ON120UNPU}$	0.7	1	1.3	RZQ/2
240 Ohm	$R_{ON240UNPU}$	0.7	1	1.3	RZQ/1

NOTE 1  $R_{ONUNPU}$  is defined at  $VOH = VDDQ/2$ .

### 15.9.1 Output Driver and Termination Resistance Temperature and Voltage Sensitivity

If temperature and/or voltage condition is changed after calibration, the tolerance limits widen according to Table 489 and Table 490.

**Table 489 – Worst Case Output Driver and Termination Resistance**

Resistor	Definition Point	Min	Max	Unit	Notes
$R_{ONPD}$	$0.5 \times VDDQ$	$R_{ONPD}(\text{nom}) \times (0.90 - (dR_{OnD}dT(\text{max}) \times  \Delta T ) - (dR_{On}(\text{max})dV2 \times  \Delta V2 ) - (dR_{On}(\text{max})dVQ \times  \Delta VQ ))$	$R_{ONPD}(\text{nom}) \times (1.10 + (dR_{On}(\text{max})dT \times  \Delta T ) + (dR_{On}(\text{max})dV2 \times  \Delta V2 ) + (dR_{On}(\text{max})dVQ \times  \Delta VQ ))$	ohm	1,2,3
$R_{TT}$	$0.5 \times VDDQ$	$R_{TT}(\text{nom}) \times (0.90 - (dR_{On}(\text{max})dT \times  \Delta T ) - (dR_{On}(\text{max})dV2 \times  \Delta V2 ) - (dR_{On}(\text{max})dVQ \times  \Delta VQ ))$	$R_{TT}(\text{nom}) \times (1.10 + (dR_{On}(\text{max})dT \times  \Delta T ) + (dR_{On}(\text{max})dV2 \times  \Delta V2 ) + (dR_{On}(\text{max})dVQ \times  \Delta VQ ))$	ohm	1,2,3
$R_{ONUNPU}$	$0.5 \times VDDQ$	$R_{ONUNPU}(\text{nom}) \times (0.70 - (dR_{OnUN}dT(\text{max}) \times  \Delta T ) - (dR_{On}(\text{max})UNdV2 \times  \Delta V2 ) - (dR_{On}(\text{max})UNdVQ \times  \Delta VQ ))$	$R_{ONUNPU}(\text{nom}) \times (1.30 + (dR_{On}(\text{max})UNdT \times  \Delta T ) + (dR_{On}(\text{max})UNdV2 \times  \Delta V2 ) + (dR_{On}(\text{max})UNdVQ \times  \Delta VQ ))$	ohm	2,3
$R_{TTCS}$	$0.5 \times VDDQ$	$R_{TTCS}(\text{nom}) \times (0.90 - (dR_{On}(\text{max})dT \times  \Delta T ) - (dR_{On}(\text{max})dV2 \times  \Delta V2 ) - (dR_{On}(\text{max})dVQ \times  \Delta V2 ))$	$R_{TTCS}(\text{nom}) \times (1.10 + (dR_{On}(\text{max})dT \times  \Delta T ) + (dR_{On}(\text{max})dV2 \times  \Delta V2 ) + (dR_{On}(\text{max})dVQ \times  \Delta V2 ))$	ohm	1,2,3
NOTE 1 $\Delta T = T - T(@ \text{Calibration})$ , $\Delta V2 = VDD2C - VDD2C(@ \text{Calibration})$ , $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$					
NOTE 2 $dR_{OnD}dT$ , $dR_{OnD}V2$ , $dR_{OnD}VQ$ , $dR_{TTd}V2$ , $dR_{TTd}VQ$ , $dR_{TTd}T$ , $dR_{OnUN}dT$ , $dR_{OnUN}V2$ and $dR_{OnUN}VQ$ , $dR_{OnPDED}dT$ , $dR_{OnPDED}V2$ , $dR_{OnPDED}VQ$ , $dR_{OnUNED}dT$ , $dR_{OnUNED}V2$ and $dR_{OnUNED}VQ$ are not subject to production test but are verified by design and characterization.					
NOTE 3 VDD1, VDD2C, VDD2D, and VDDQ must be nominal during measurement.					

**Table 490 – Worst Case Output High Voltage**

Voltage	Min	Max	Unit	Notes	
$VOH_{PU}$	$VOH_{PU}(\text{nom}) \times (0.90 - (dVOH(\text{max})dT \times  \Delta T ) - (dVOH(\text{max})dV2 \times  \Delta V2 ) - (dVOH(\text{max})dVQ \times  \Delta VQ ))$	$VOH_{PU}(\text{nom}) \times (1.10 + (dVOH(\text{max})dT \times  \Delta T ) + (dVOH(\text{max})dV2 \times  \Delta V2 ) + (dVOH(\text{max})dVQ \times  \Delta VQ ))$	V	1,2,3,4	
NOTE 1 $\Delta T = T - T(@ \text{Calibration})$ , $\Delta V2 = VDD2C - VDD2C(@ \text{Calibration})$ , $\Delta VQ = VDDQ - VDDQ(@ \text{Calibration})$					
NOTE 2 $dVOHdT$ , $dVOHdV2$ and $dVOHdVQ$ are not subject to production test but are verified by design and characterization.					
NOTE 3 Refer to 15.9.					
NOTE 4 VDD1, VDD2C, and VDDQ must be nominal during measurement.					

### 15.9.1 Output Driver and Termination Resistance Temperature and Voltage Sensitivity (cont'd)

**Table 491 — Output Driver and Termination Resistance Temperature and Voltage Sensitivity**

Symbol	Parameter	Min	Max	Unit	Notes
$dR_{ON}dT$	$R_{ON}$ Temperature Sensitivity	0.00	0.75	%/°C	
$dR_{ON}dV2$	$R_{ON}$ VDD2C Voltage Sensitivity	0.00	0.50	%/mV	
$dR_{ON}dVQ$	$R_{ON}$ VDDQ Voltage Sensitivity	0.00	0.20	%/mV	
$dVOHdT$	VOH Temperature Sensitivity	0.00	0.75	%/°C	
$dVOHdV2$	VOH VDD2C Voltage Sensitivity	0.00	0.35	%/mV	
$dVOHdVQ$	VOH VDDQ Voltage Sensitivity	0.00	0.35	%/mV	
$dR_{TT}dT$	$R_{TT}$ Temperature Sensitivity	0.00	0.75	%/°C	
$dR_{TT}dV2$	$R_{TT}$ VDD2C Voltage Sensitivity	0.00	0.50	%/mV	
$dR_{TT}dVQ$	$R_{TT}$ VDDQ Voltage Sensitivity	0.00	0.20	%/mV	
$dRONUNDT$	Un-terminated RON Temperature Sensitivity	0.00	0.75	%/°C	
$dRONUNDV2$	Un-terminated RON VDD2C Voltage Sensitivity	0.00	0.75	%/mV	
$dRONUNDVQ$	Un-terminated RON VDDQ Voltage Sensitivity	0.00	0.75	%/mV	

## 16 Pad Order

Table 492 – LPDDR6 Pad Order

TOP		
Pad number	Sub-ch. Name	Pad Name
1	0	VDD2C
2	0	VDD1
3	0	VDD2D
4	0	VSS
5	0	DQ0[0]
6	0	VDDQ
7	0	DQ0[1]
8	0	VSS
9	0	DQ0[2]
10	0	VDD2D
11	0	VDD2C
12	0	VDDQ
13	0	DQ0[3]
14	0	VSS
15	0	DQ0[4]
16	0	VDDQ
17	0	VSS
18	0	RDQS0_t
19	0	RDQS0_c
20	0	VDD2C
21	0	VSS
22	0	WCK0_t
23	0	WCK0_c
24	0	VSS
25	0	VDD2D
26	0	DQ0[5]
27	0	VSS
28	0	DQ0[6]
29	0	VDDQ
30	0	DQ0[7]
31	0	VSS
32	0	DQ0[8]
33	0	VDDQ
34	0	VDD2C
35	0	VDD2D
36	0	DQ0[9]
37	0	VSS
38	0	DQ0[10]
39	0	VDDQ
40	0	DQ0[11]
41	0	VSS

Pad number	Sub-ch. Name	Pad Name
42	0	VDD2D
43	0	VDD2C
44	0	CA0[3]
45	0	VSS
46	0	CA0[2]
47	0	VDD2D
48	0	CA0[1]
49	0	VSS
50	0	CA0[0]
51	0	VDD2C
52	0	CS0
53	0	VSS
54	0	CK0_t
55	0	CK0_c
56	0	VSS
57	0/1	ZQ
58	0/1	VDDQ
59	0/1	ALERT
60	0/1	VDD2C
61	0/1	VDD2D
62	0/1	RESET_n
63	1	VSS
64	1	CK1_c
65	1	CK1_t
66	1	VSS
67	1	CS1
68	1	VDD2C
69	1	CA1[0]
70	1	VSS
71	1	CA1[1]
72	1	VDD2D
73	1	CA1[2]
74	1	VSS
75	1	CA1[3]
76	1	VDD2C
77	1	VDD2D

Pad number	Sub-ch. Name	Pad Name
78	1	VSS
79	1	DQ1[11]
80	1	VDDQ
81	1	DQ1[10]
82	1	VSS
83	1	DQ1[9]
84	1	VDD2D
85	1	VDD2C
86	1	VDDQ
87	1	DQ1[8]
88	1	VSS
89	1	DQ1[7]
90	1	VDDQ
91	1	DQ1[6]
92	1	VSS
93	1	DQ1[5]
94	1	VDD2D
95	1	VSS
96	1	WCK1_c
97	1	WCK1_t
98	1	VSS
99	1	VDD2C
100	1	RDQS1_c
101	1	RDQS1_t
102	1	VSS
103	1	VDDQ
104	1	DQ1[4]
105	1	VSS
106	1	DQ1[3]
107	1	VDDQ
108	1	VDD2C
109	1	VDD2D
110	1	DQ1[2]
111	1	VSS
112	1	DQ1[1]
113	1	VDDQ
114	1	DQ1[0]
115	1	VSS
116	1	VDD2D
117	1	VDD1
118	1	VDD2C

Bottom

**Table 492 — LPDDR6 Pad Order (cont'd)**

- NOTE 1 Additional pads are allowed for DRAM mfg-specific pads ("DNU"), or additional power pads as long as the extra pads are grouped with like-named pads.
- NOTE 2 Applications are recommended to follow DQ[11:0]/sub-channel assignments. DQ[11:0] or sub-channel swapping at the application level requires review of MR and calibration features assigned to specific DQ[11:0]/sub-channel.

## 16.1 Package Configuration

### 16.1.1 Package Considerations

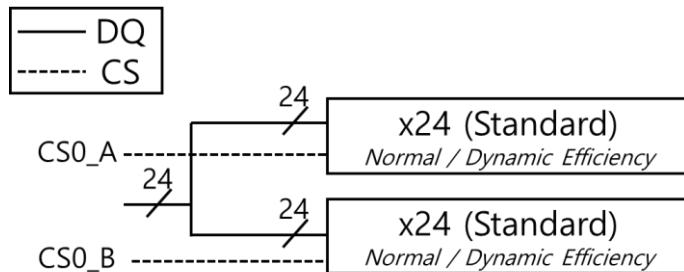
Two Static Efficiency mode LPDDR6 SDRAMs can be logically combined into a Standard LPDDR6 SDRAM. Static Efficiency mode devices use the same bank architecture with one Sub-Ch. indicator added. Two Static Efficiency mode dies of the same density can be combined to make an equivalent x24 device of twice the given density. The inputs are ganged and the DQ busses from the two devices are assigned individually to the 24-bit channels.

Packages for Standard and Static Efficiency mode devices share the same ball maps. This section describes internal wiring changes and system considerations when using packages containing Static Efficiency mode devices.

Three different die combinations are supported:

- 1) Standard - Packages configured with only Standard LPDDR6 die.
- 2) Static Efficiency mode - Packages configured with only Static Efficiency mode LPDDR6 die.
- 3) Mixed - Packages configured with both Standard and Static Efficiency mode LPDDR6 die.  
In this mixed configuration, some ranks contain only Standard die and other ranks contain only Static Efficiency mode die.

For mixed packages, standard devices shall be assigned to the lower numbered ranks and Static Efficiency mode devices shall be assigned to the higher numbered ranks.



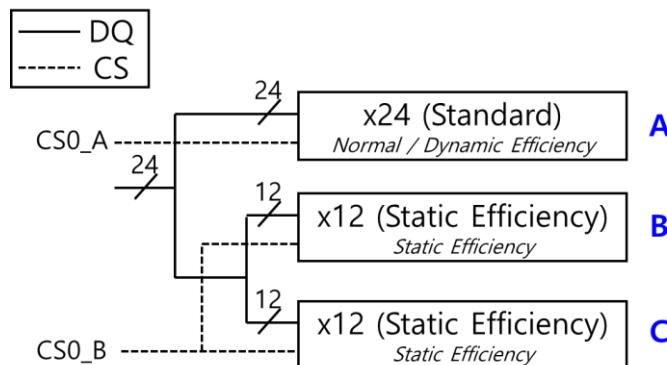
**Figure 259 – Example of Rank Assignment for Single-Channel Dual-Rank Package (Standard Packages)**

Packaged devices support only one set of latency parameters depending on the die combination:

- 1) Standard packages - configured with only x24 LPDDR6 dies - support x24 LPDDR6 latency parameters.
- 2) Static Efficiency mode packages - configured with only Static Efficiency mode LPDDR6 dies - support Efficiency mode latency parameters.
- 3) Mixed packages - configured with both x24 and Static Efficiency mode LPDDR6 dies - support Efficiency mode latency parameters.

### 16.1.1 Package Considerations (cont'd)

MR1 OP[7] for each die indicates the appropriate latency support. Dynamic efficiency mode cannot be allowed in Mixed packages.



**Figure 260 – Example of Mixed Packages with Both x24 and Static Efficiency Mode Dies**

**Table 493 – Efficiency Mode Related MR Setting for Mixed Packages**

Die	MR Setting			Notes
	MR0 OP[2] (Eff. Status)	MR1 OP[7] (Eff. Latency)	MR1 OP[6] (Eff. CNTL)	
A	0b (Switchable device)	1b (Eff. mode latency)	Allowable both 0b/1b (Normal/Dynamic Eff.)	1,2
B	1b (Static Eff. device)	1b (Eff. mode latency)	Ignored	1,2
C	1b (Static Eff. device)	1b (Eff. mode latency)	Ignored	1,2

NOTE 1 MR1 OP[7] should be automatically updated by MR1 OP[6] based on package configuration.  
NOTE 2 MR1 OP[6] should be same between multi-rank system.

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## **Standard Improvement Form**

JEDEC Standard No. **JESD209-6**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

Requirement, clause number \_\_\_\_\_

Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

Unclear    Too Rigid    In Error

Other \_\_\_\_\_

- ## 2. Recommendations for correction:

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- ### 3. Other suggestions for document improvement:

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Submitted by

Name:

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Date:

