

# **JEDEC STANDARD**

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**High Bandwidth Memory DRAM  
(HBM1, HBM2)**

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**JESD235D**  
**(Revision of JESD235C, January 2020)**

**FEBRUARY 2021**

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## HIGH BANDWIDTH MEMORY (HBM) DRAM

(From JEDEC Board Ballot JCB-20-10, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, under item number 1797.99L, Rev. 4.20).

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### 1 Scope

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The HBM DRAM is tightly coupled to the host compute die with a distributed interface. The interface is divided into independent channels. Each channel is completely independent of one another. Channels are not necessarily synchronous to each other. The HBM DRAM uses a wide-interface architecture to achieve high-speed, low power operation. Each channel interface maintains a 128 bit data bus operating at double data rate (DDR).

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### 2 Features

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- 256 bit prefetch per memory read and write access
- BL = 2 and 4
- 128 DQ width + optional ECC pin support/channel
- Legacy mode and Pseudo Channel (PC) mode operation; 64 DQ width for PC mode
- Differential clock inputs (CK\_t/CK\_c) for command/address
- Double data rate (DDR) command/address. Row Activate commands require two cycles, all other commands require one cycle
- Semi-independent row and column command interfaces allowing Activates/Precharges to be issued in parallel with Read/Writes.
- Data referenced to unidirectional differential data strobes RDQS\_t/RDQS\_c and WDQS\_t/WDQS\_c. One strobe pair each per DWORD
- Up to 8 channels / device
- Channel density of 1 Gb to 16 Gb
- 8, 16, 32 or 48 banks per channel; varies by device density/channel
- Bank grouping supported
- 2 KB page size per channel
- DBIac support configurable via MRS
- Data mask for masking write data per byte
- Self refresh modes
- I/O voltage 1.2 V
- DRAM core voltage 1.2 V, independent of I/O voltage
- Unterminated data/address/cmd/clk interfaces
- Temperature sensor with 3-bit encoded range output

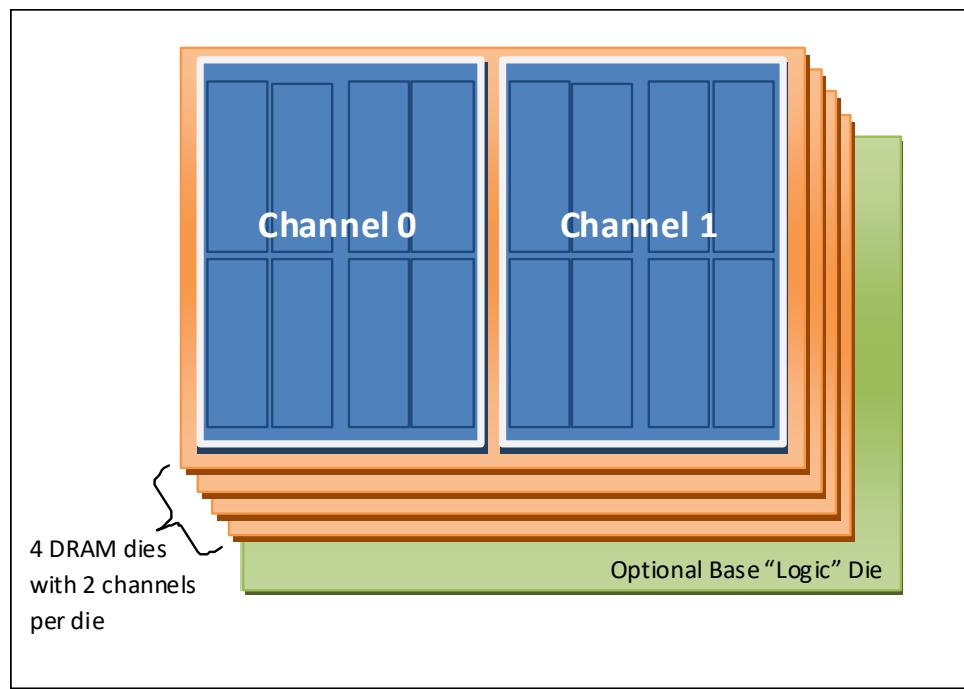
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### 3 Organization

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The HBM DRAM is optimized for high-bandwidth operation to a stack of multiple DRAM devices across a number of independent interfaces called channels. It is anticipated that each DRAM stack will support up to 8 channels. [Figure 1](#) shows an example stack containing 4 DRAM dies, each die supporting 2 channels. Each die contributes additional capacity and additional channels to the stack (up to a maximum of 8 channels per stack).

Each channel provides access to an independent set of DRAM banks. Requests from one channel may not access data attached to a different channel. Channels are independently clocked, and need not be synchronous.



**Figure 1 — General Overview of a DRAM Die Stack with Channels**

The DRAM vendor may choose to require an optional interface die that sits at the bottom of the stack and provides signal redistribution and other functions. The vendor may choose to implement many of the logic functions typically found on DRAM die on this logic die. This standard does not explicitly require nor prohibit such a solution.

The division of channels among the DRAM dies within a stack is left to the vendor. The example above, with the memory for two channels implemented on each die, is not a required organization. Organizations are permitted where the memory for a single channel is distributed among multiple dies; however, all accesses within a single channel must have the same latency for all accesses. Similarly, vendors may develop products where each memory die can flexibly support 1, 2, or 4 channels – enabling 8-channel configurations with stacks of 2 to 8 dies while keeping all data for a given channel on one die.

Since each channel is independent, much of this standard will describe a single channel. Where signal names are involved, families of signals belonging to a given channel will have the suffix a, b, ..., h for channels a through h. If no suffix is present, the signal(s) being described are generic instances of the various per-channel signals.

### 3.1 Channel Definition

Each channel consists of an independent command and data interface. RESET\_n, IEEE1500 test port and power supply signals are common to all channels. A channel provides access to a discrete pool of memory; no channel may access the memory storage for a different channel.

Each channel interface provides an independent interface to a number of banks of DRAM of a defined page size. See [HBM Channel Addressing](#).

#### 3.1.1 Summary of Per-Channel Signals

**Table 1** outlines the signals required for each channel, and **Table 2** adds global signals that are required once per HBM device. See also [Table 82](#) for 15 additional global signals associated with the IEEE1500 test access port.

**Table 1 — Single Channel Signal Count**

Function	# uBumps	Notes
Data	128	DQ[127:0]
Column Command/Address	8 or 9	C[7:0] or C[8:0]
Row Command/Address	6 or 7	R[5:0] or R[6:0]
DBI	16	1 DBI per 8 DQs
DM	16	1 DM per 8 DQs
PAR	4	1 PAR per 32 DQs
DERR	4	1 DERR per 32 DQs
Strobes	16	1 RDQS_t/RDQS_c, WDQS_t/WDQS_c per 32 DQs
Clock	2	CK_t/CK_c
CKE	1	CKE
AERR	1	AERR
Redundant Data	8	RD[7:0]
Redundant Row	1	RR
Redundant Column	1	RC
<b>Total</b>	<b>212 or 214</b>	

**Table 2 — Global Signal Count**

Function	# uBumps	Notes
Reset	1	RESET_n
TEMP[2:0]	3	TEMP[2:0]
CATTRIP	1	Catastrophic Temperature Sensor
<b>Total</b>	<b>5</b>	

### 3.1.2 Legacy Mode and Pseudo Channel Mode

HBM DRAM defines two modes of operation depending on channel density. The mode support is fixed by design and is indicated on bits [17:16] of the DEVICE\_ID wrapper register.

#### 3.1.2.1 Legacy Mode (HBM1)

Legacy mode provides 256 bit prefetch per memory Read and Write access when the burst length (BL) is set to 2. Address bit BA4 is a “Don’t Care” in this mode. Devices supporting legacy mode are also referred to as HBM1.

#### 3.1.2.2 Pseudo Channel Mode (HBM2)

Pseudo channel (PC) mode divides a channel into two individual sub-channels of 64 bit I/O each, providing 256 bit prefetch per memory read and write access for each pseudo channel. Devices supporting PC mode are also referred to as HBM2. PC mode requires that the burst length (BL) is set to 4. Each read or write access may internally be executed as two seamless array accesses or a single array access, depending on DRAM vendor’s implementation. Both implementations are equivalent for the memory controller as they result in the same prefetch per Read and Write access.

Both pseudo channels operate semi-independent: they share the channel’s row and column command bus as well as CK and CKE inputs, but decode and execute commands individually as illustrated in [Figure 2](#). Address BA4 is used to direct commands to either to pseudo channel 0 (PC0, BA4 = 0) or pseudo channel 1 (PC1, BA4 = 1). Power-down and self refresh are common to both pseudo channels due to the shared CKE pin.

Array access timings as listed in the table below are applicable for each individual pseudo channel. For example, an ACTIVATE to PC0 can be followed by an ACTIVATE to PC1 as shown in [Figure 2](#). However a subsequent ACTIVATE to PC0 can only be done after  $t_{RRD}$  (PC0). For commands that are common to both pseudo channels (PDE, PDX, SRE, SRX and MRS) it is required that the respective timing conditions are met by both pseudo channels when issuing that command. PC mode requires that burst length is set to 4. Both pseudo channels also share the channel’s mode registers.

All I/O signals of DWORD0 and DWORD1 are associated with pseudo channel 0, and all I/O signals of DWORD2 and DWORD3 with pseudo channel 1.

**Table 3 — Array Access Timings Counted Individually Per Pseudo Channel**

Array Timing Group	Timing Parameters
Row Access Timings	$t_{RC}$ , $t_{RAS}$ , $t_{RCDRD}$ , $t_{RCDWR}$ , $t_{RRDL}$ , $t_{RRDS}$ , $t_{FAW}$ , $t_{RTPL}$ , $t_{RTPS}$ , $t_{RP}$ , $t_{WR}$
Column Access Timings	$t_{CCDL}$ , $t_{CCDS}$ , $t_{CCDR}$ , $t_{WTRL}$ , $t_{WTRS}$ , $t_{RTW}$
Refresh Timings	$t_{RFC}$ , $t_{RFCSB}$ , $t_{RREFD}$ , $t_{REFI}$ , $t_{REFISB}$ , $t_{RTW}$

### 3.1.2.2 Pseudo Channel Mode (HBM2) (cont'd)

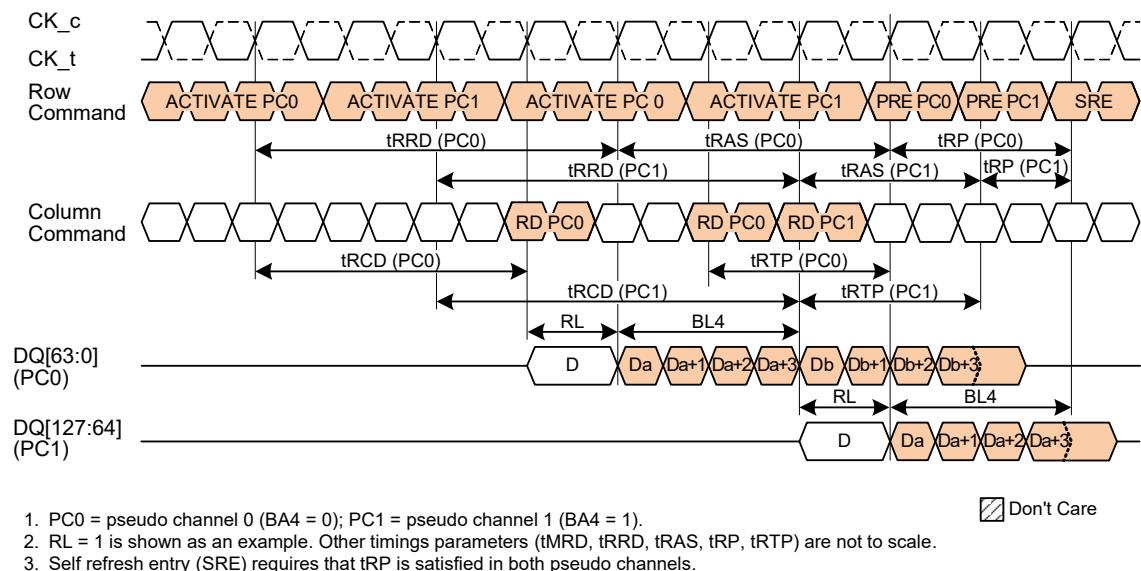


Figure 2 — Pseudo Channel Mode Operation

### 3.1.3 Dual Command Interfaces

To enable higher performance, HBM DRAMs exploit the increase in available signals in order to provide semi-independent row and column command interfaces for each channel. These interfaces increase command bandwidth and performance by allowing read and write commands to be issued simultaneously with other commands like activates and precharges. See [Commands](#).

### 3.2 Addressing

**Table 4 — HBM Channel Addressing**

Legacy Mode <sup>6</sup>							Notes
Density per Channel	1 Gb	2 Gb	4 Gb				
Prefetch Size (bits)	256	256	256				1,3
Row Address	RA[12:0]	RA[13:0]	RA[13:0]				
Column Address	CA[5:0]	CA[5:0]	CA[5:0]				1
Bank Address	BA[2:0]	BA[2:0]	BA[3:0]				8
Page Size	2 KB	2 KB	2 KB				1,3
Refresh	8K/32 ms	8K/32 ms	8K/32 ms				
Refresh Period	3.9 us	3.9 us	3.9 us				
Density Code	0001	0010	0011				11
Pseudo Channel (PC) Mode <sup>5,6</sup>							Notes
Density per Channel	2 Gb	4 Gb	6 Gb	8 Gb			
Density per PC	1 Gb	2 Gb	3 Gb	4 Gb			
Prefetch Size per PC (bits)	256	256	256	256	1,3		
Row Address	RA[13:0]	RA[13:0]	RA[14:0] <sup>9</sup>	RA[14:0]			
Column Address	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	1		
Bank Address	BA[2:0]	BA[3:0]	BA[3:0]	BA[3:0]			
Page Size per PC	1 KB	1 KB	1 KB	1 KB	1,3		
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms			
Refresh Period	3.9 us	3.9 us	3.9 us	3.9 us			
Density Code	0010	0011	0101	0110	11		
Pseudo Channel (PC) Mode <sup>5,6</sup>							Notes
Configuration <sup>7</sup>	8 Gb 8-High	8 Gb 12-High	12 Gb 8-High	12 Gb 12-High	16 Gb 8-High	16 Gb 12-High	
Density per Channel	8 Gb	12 Gb	12 Gb	18 Gb	16 Gb	24 Gb	
Density per PC	4 Gb	6 Gb	6 Gb	9 Gb	8 Gb	12 Gb	
Prefetch Size per PC (bits)	256	256	256	256	256	256	1,3
Row Address	RA[13:0]	RA[13:0]	RA[14:0] <sup>9</sup>	RA[14:0] <sup>9</sup>	RA[14:0]	RA[14:0]	
Column Address	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	CA[5:1]	1
Bank Address	SID, BA[3:0]	SID[1:0], BA[3:0] <sup>10</sup>	SID, BA[3:0]	SID[1:0], BA[3:0] <sup>10</sup>	SID, BA[3:0]	SID[1:0], BA[3:0] <sup>10</sup>	8
Page Size per PC	1 KB	1 KB	1 KB	1 KB	1 KB	1 KB	1,3
Refresh	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	8K/32 ms	
Refresh Period	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	3.9 us	
Density Code	0100	1001	1000	1011	1010	1100	11

**Table 4 — HBM Channel Addressing (cont'd)**

NOTE 1	Prefetch size and page size reflect the effective addressing along with row and column commands. Both do not include the optional ECC bits as described in <a href="#">6.2.2</a> .
NOTE 2	The burst order of a BL2 burst is fixed for Reads and Writes, and the HBM device does not assign a column address bit to distinguish between the first and second UI of a BL2 burst. A memory controller may internally assign such a column address bit but that column address bit is not transmitted to the HBM device. BL2 bursts are supported in legacy mode only.
NOTE 3	The burst order of a BL4 burst in PC mode is fixed for Reads and Writes, and the HBM device does not assign column address bits to distinguish between the four UI of a BL4 burst. A memory controller may internally assign such column address bits but those column address bits are not transmitted to the HBM device. PC mode requires that the burst length is set to 4 (BL4) in MR3 OP7.
NOTE 4	Page Size = $2^{\text{COLBITS}} \times (\text{Prefetch Size} / 8)$ ; where COLBITS is the number of column address bits. Page size and prefetch size are per channel in legacy mode, and per pseudo channel in PC mode.
NOTE 5	In PC mode, an additional address bit BA4 is provided for row and column commands to direct commands either to pseudo channel 0 (BA4 = 0) or pseudo channel 1 (BA4 = 1). See <a href="#">Table 30</a> and <a href="#">Table 31</a> .
NOTE 6	The HBM device indicates the support of legacy mode and/or PC mode in bits [17:16] of the .
NOTE 7	These configurations are optimized for HBM stacks using 8 or 12 DRAM dies. The stack height of all other configuration is vendor specific.
NOTE 8	SID, SID0, SID1 act as bank address bits in command execution. Specific AC timing parameters or variations on selected timing parameters may be linked to SID. <a href="#">Table 30</a> and <a href="#">Table 31</a> and the vendor datasheets should be consulted for details.
NOTE 9	RA[14:13] = 11 is invalid.
NOTE 10	SID[1:0] = 11 is invalid.
NOTE 11	The density code refers to the encoding of the per-channel density in the , bits [79:76].

### 3.2.1 Bank Groups

The activity within a bank group must be restricted to ensure proper operation of the device for HBM DRAMs operating at frequencies above a certain threshold  $f_{CKBG}$ . The banks within a device are divided into four or eight bank groups. The bank group feature is configurable via MRS. The assignment of banks to bank groups is shown in [Table 5](#).

Different timing parameters are specified depending on whether back-to-back accesses are within the same bank group or across bank groups as shown in [Table 6](#).

### 3.2.1 Bank Groups (cont'd)

**Table 5 — Bank Group Assignments**

Banks	8 Banks BA[2:0]	16 Banks BA[3:0]	32 Banks SID, BA[3:0]	48 Banks SID[1:0], BA[3:0]	
0 and 1	Group A	Group A	Group A	Group A	
2 and 3	Group B				
4 and 5	Group C	Group B	Group B	Group B	
6 and 7	Group D				
8 to 11	N/A	Group C	Group C	Group C	
12 to 15		Group D	Group D	Group D	
16 to 19		N/A	Group E	Group E	
20 to 23			Group F	Group F	
24 to 27			Group G	Group G	
28 to 31			Group H	Group H	
32 to 35			N/A	Group I	
36 to 39		Group J			
40 to 43		Group K			
44 to 47		Group L			

**Table 6 — Command Sequences Affected by Bank Groups**

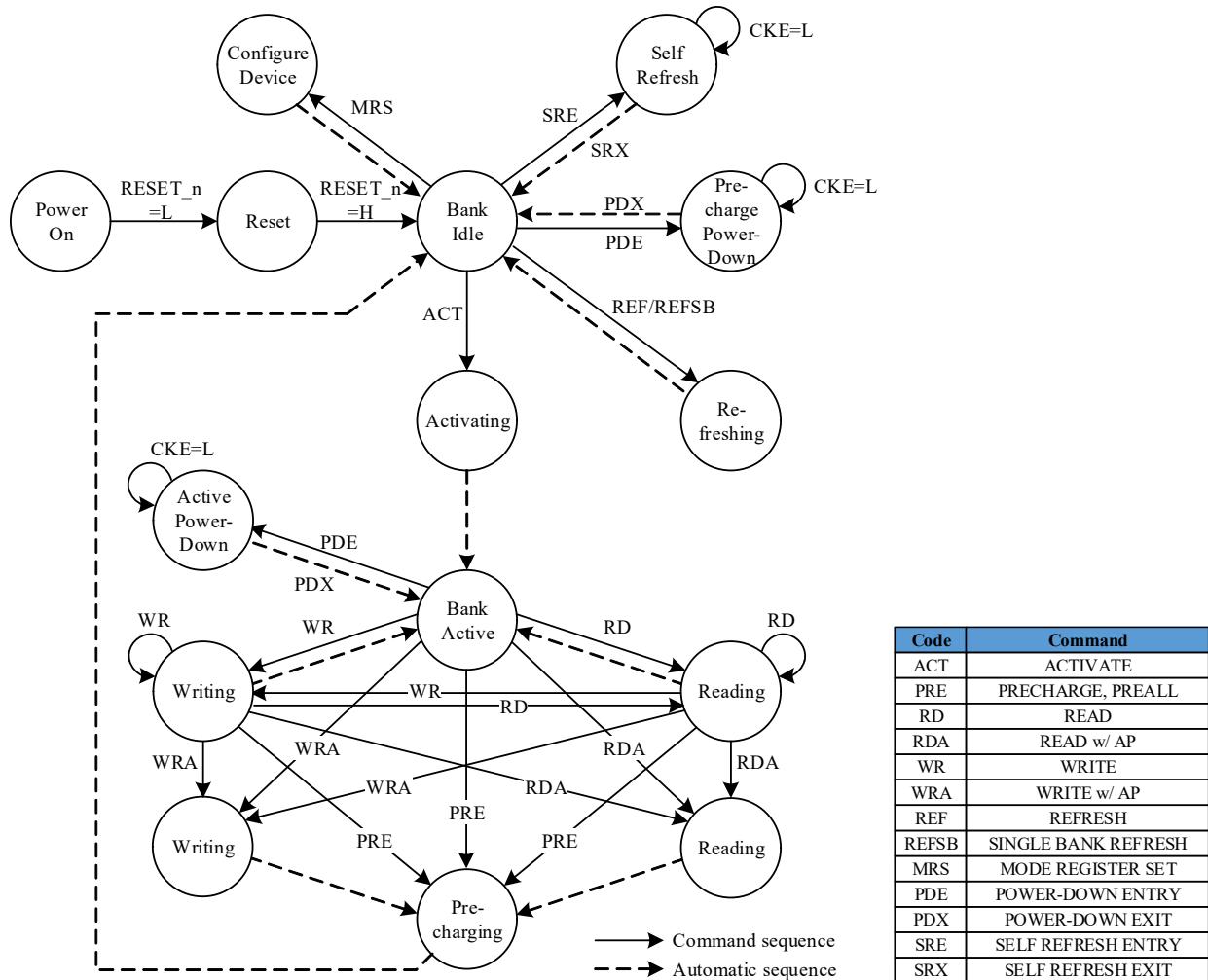
Command Sequence	Corresponding AC Timing Parameter			Notes	
	Bank Groups Disabled	Bank Groups Enabled			
		Accesses to different bank groups	Accesses within the same bank group		
ACTIVATE to ACTIVATE	$t_{RRDS}$	$t_{RRDS}$	$t_{RRDL}$		
WRITE to WRITE	$t_{CCDS}$	$t_{CCDS}$	$t_{CCDL}$		
READ to READ	$t_{CCDS}$	$t_{CCDS}$ or $t_{CCDR}$	$t_{CCDL}$		
Internal WRITE to READ	$t_{WTRS}$	$t_{WTRS}$	$t_{WTRL}$		
READ to PRECHARGE	$t_{RTPS}$	—	$t_{RTPL}$	1	
NOTE 1	Parameters $t_{RTPS}$ and $t_{RTPL}$ apply only when READ and PRECHARGE go to the same bank; use $t_{RTPS}$ when Bank Groups are disabled, and $t_{RTPL}$ when Bank Groups are enabled.				
NOTE 2	Parameters $t_{CCDR}$ replaces parameter $t_{CCDS}$ when consecutive READs go to banks with different stack IDs (SID).				

### 3.3 Simplified State Diagram

The state diagram provides a simplified illustration of the allowed state transitions and the related commands to control them. The following operations are not or not completely shown in the diagram:

- state transitions involving more than one bank;
- the state transition from bank active to bank idle and back to bank active initiated by an imPRE command;
- interactions from the use of IEEE1500 instructions to load mode registers or execute test functions;
- the immediate transition from any state to reset state by asserting RESET\_n LOW or by loading the IEEE1500 instructions HBM\_RESET.

For a complete description of the device behavior, use the information provided in the state diagram along with the command truth tables and AC timing specifications.



**Figure 3 — Simplified State Diagram**

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## 4 Initialization

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To power-up and initialize the HBM device into functional operation the sequence in Section 4.1 must be followed. At any time after the power-up initialization, the HBM device may be reset using the sequence in Section 4.2. A limited set of IEEE 1500 port instructions may be used within the initialization sequences, as described in Section 4.3.

The interactions between HBM functional reset and the IEEE 1500 port reset are as follows (also see Section 13):

- Functional reset requires that the IEEE 1500 port also be reset.
- The IEEE 1500 port can be reset at any time without impacting normal operation.
- The IEEE 1500 port may be brought out of reset and a limited set of instructions may be used after a minimum time after RESET\_n has been deasserted. See section 4.3.
- If not needed, the IEEE 1500 port may be left in reset (WRST\_n = LOW) during normal operation.

### 4.1 HBM Power-up and Initialization Sequence

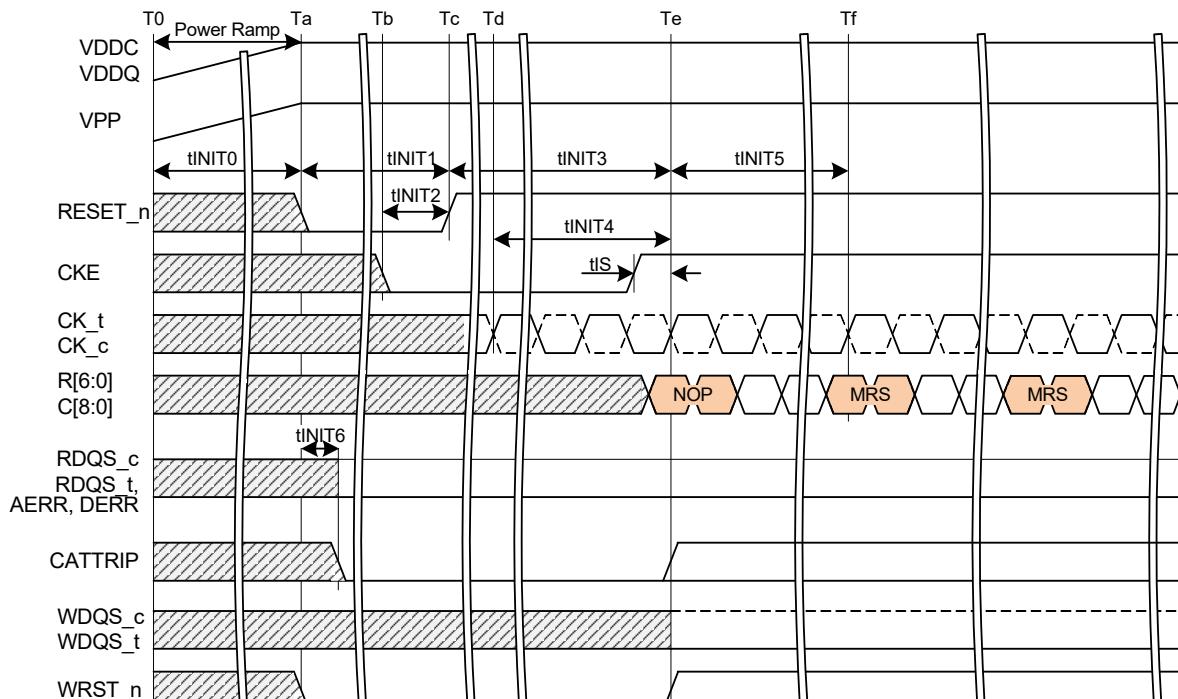
HBM device must be powered up and initialized in a predefined manner. The following sequence and timing must be satisfied for HBM power up and initialization sequence. Also refer to [Figure 4](#).

1. Apply power to the V<sub>DDC</sub>, V<sub>DDQ</sub> and V<sub>PP</sub> supplies. The V<sub>DDC</sub> supply must be applied before or at the same time as V<sub>DDQ</sub>. The power supply ramp time between 300 mV and V<sub>DDC</sub> must be less than or equal to t<sub>INIT0</sub>. During the power ramp, V<sub>DDC</sub> ≥ V<sub>DDQ</sub> and (V<sub>DDC</sub> - V<sub>DDQ</sub>) < 0.3 V. The V<sub>PP</sub> supply must be applied before or at the same time as V<sub>DDC</sub> and must be equal to or higher than V<sub>DDC</sub> at all times. During power supply ramp time t<sub>INIT0</sub>, RESET\_n, WRST\_n and all other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z).
2. RESET\_n must be driven LOW (below 0.2 × V<sub>DDQ</sub>) before or at the same time when t<sub>INIT0</sub> expires as shown in [Figure 4](#) (time Ta). WRST\_n must be driven LOW before or at the same time as RESET\_n. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET\_n must be maintained LOW for a minimum of t<sub>INIT1</sub> time with stable power. After t<sub>INIT6</sub> time has elapsed, the HBM device drives RDQS\_t and RDQS\_c to LOW and HIGH static levels, respectively, and AERR and DERR signals LOW. CKE must be driven LOW a minimum of t<sub>INIT2</sub> time before RESET\_n is driven HIGH.
3. After RESET\_n is driven HIGH, CKE must remain LOW for a minimum time of t<sub>INIT3</sub>. The HBM device resets into the precharged power-down state. During t<sub>INIT3</sub>, the HBM device will read and apply internal fuse configuration data and perform I/O driver impedance calibration. At the same time the WRST\_n signal may be optionally driven HIGH to enable a subset of the IEEE 1500 instructions (see [Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs](#) and [IEEE Standard 1500](#) sections). CATTRIP data must stay LOW from the end of t<sub>INIT6</sub> to the end of t<sub>INIT3</sub> and valid data must start after t<sub>INIT3</sub>.
4. The CK clock shall be started, and stable clocks shall be maintained for minimum of t<sub>INIT4</sub> time before driving CKE HIGH. Since CKE is a synchronous signal, the corresponding setup time to clock (t<sub>IS</sub>) must be met. Also, RNOP and CNOP commands must be registered (with t<sub>IS</sub> / t<sub>IH</sub> satisfied). After CKE is registered HIGH, a minimum t<sub>INIT5</sub> time must be satisfied before issuing a first MRS command. At or before the time that CKE is driven HIGH, WDQS\_t and WDQS\_c must be driven to LOW and HIGH static levels, respectively.
5. Issue all MRS commands to configure the HBM device appropriately for the application setting.
6. The HBM device is now ready for normal operation.

#### 4.1 HBM Power-up and Initialization Sequence (cont'd)

Table 7 — Initialization Timing Parameters

Symbol	Description	Min	Max	Unit
$t_{INIT0}$	Power supply ramp time	0.01	200	ms
$t_{INIT1}$	RESET_n signal LOW time at power-up (after stable power)	200	—	us
$t_{INIT2}$	CKE LOW time before RESET_n deassertion	10	—	ns
$t_{INIT3}$	CKE and WRST_n LOW time after RESET_n deassertion	500	—	us
$t_{INIT4}$	Stable clock before CKE HIGH	10	—	nCK
$t_{INIT5}$	Idle time before first MRS command	200	—	ns
$t_{INIT6}$	RDQS_t, RDQS_c driven valid and AERR, DERR driven LOW after RESET_n assertion	—	100	ns
$t_{PW\_RESET}$	RESET_n signal LOW time with stable power	1	—	us



1. CATTRIP is valid after tINIT3.

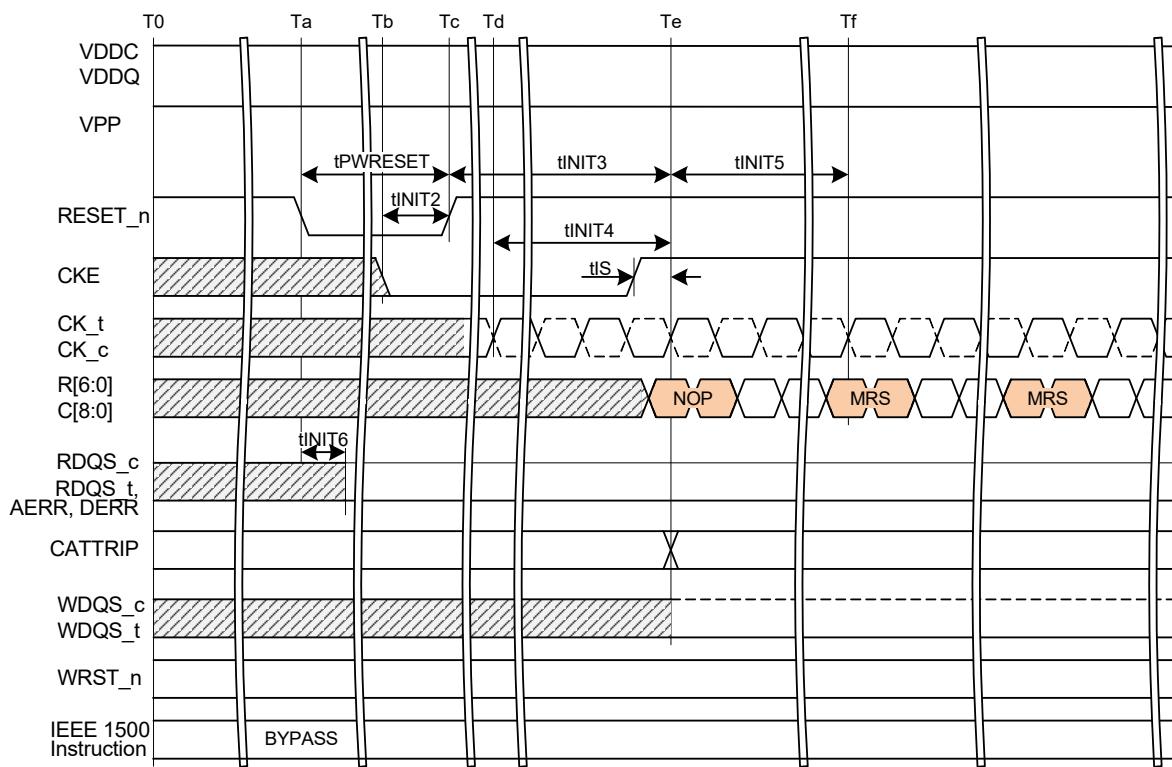
Don't Care

Figure 4 — Power-up and Initialization

## 4.2 Initialization Sequence with Stable Power

The following sequence must be satisfied to perform a functional reset when power is kept stable at the HBM DRAM. See [Figure 5](#).

1. RESET\_n must be driven LOW anytime when a functional reset is needed. WRST\_n must be driven LOW before or at the same time as RESET\_n. All other input signals may be in an undefined state (driven LOW or HIGH, or Hi-Z) at this point. RESET\_n must be maintained LOW for a minimum of t<sub>PW\_RESET</sub>. CKE must be driven LOW a minimum of t<sub>INIT2</sub> time before RESET\_n is driven HIGH. Alternately, the IEEE 1500 port HBM\_RESET instruction may be used to perform a re-initialization, with RESET\_n continuing to be driven HIGH. Refer to [HBM\\_RESET](#) section.
2. Follow steps 3 to 6 as described in section [HBM Power-up and Initialization Sequence](#). Note that the CATTRIP output is sticky and not cleared by a functional reset.



1. CATTRIP will maintain value as the one before reset until end of tINIT3.

Don't Care

**Figure 5 — HBM RESET and Initialization Sequence with Stable Power**

#### 4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs

All IEEE 1500 port instructions are allowed after  $t_{INIT3}$  without completing the full initialization sequence.

[Figure 6](#) illustrates usage of the EXTEST and SOFT\_LANE\_REPAIR instructions within the initialization sequence. This sequence may be applied as part of the power-up or stable-power initialization sequences to check for and correct failed connections on the row and column command buses, which must be correctly driven to RNOP and CNOP as part of the above initialization sequences. DWORD lane repairs are also allowed.

1. At time  $T_a$ , RESET\_n and WRST\_n must be driven LOW.
2. After a minimum time  $t_{INIT1}$  (if during an initial power-up sequence) or after  $t_{PW\_RESET}$  (if during a stable power initialization sequence) RESET\_n shall be driven HIGH.  $t_{INIT2}$  must also be met.
3. After  $t_{INIT3}$ , WRST\_n is driven HIGH. IEEE 1500 port instructions may now be used. (Note that the WRST\_n low pulse width  $t_{WRSTL}$  is met since  $t_{WRSTL}$  is less than the  $t_{INIT1}$  or  $t_{PW\_RESET}$ ). Refer to [IEEE1500 Port AC Timing Parameters](#) for timing requirements for operating the IEEE 1500 port, including  $t_{SWRST}$ . At this point, defective lane detection and soft lane repair may be executed. EXTEST operations may be applied to identify lanes needing repair. If soft lane repair is needed, SOFT\_LANE\_REPAIR operations can be applied after another RESET\_n toggle, which is required after EXTEST instruction operation. A IEEE 1500 port BYPASS instruction should be applied to return all HBM signals to their normal functional mode after SOFT\_LANE\_REPAIR operations. Alternately, WRST\_n may be driven LOW.
4. The initialization sequence may then continue per steps 4 to 6 of [HBM Power-up and Initialization Sequence](#), as needed.

During the  $t_{INIT3}$  period before WRST\_n is driven HIGH, the HBM device executes various internal configuration operations, including applying hard lane repairs based on previously fused data. Executing soft lane repair instructions after  $t_{INIT3}$  overwrites any previously programmed hard lane repair data. It is suggested that the hard lane repair data is read from the HBM device and merged in any new lane repairs before applying the new soft lane repair operations. Any applicable IEEE 1500 port instructions timings must be met before continuing to time point  $T_h$ , such as  $t_{SLREP}$  if a SOFT\_LANE\_REPAIR instruction has been applied.

The EXTEST instructions are not required before applying the soft lane repair(s). Previously determined needed lane repairs may be applied as part of each initialization event.

#### 4.3 Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs (Cont'd)

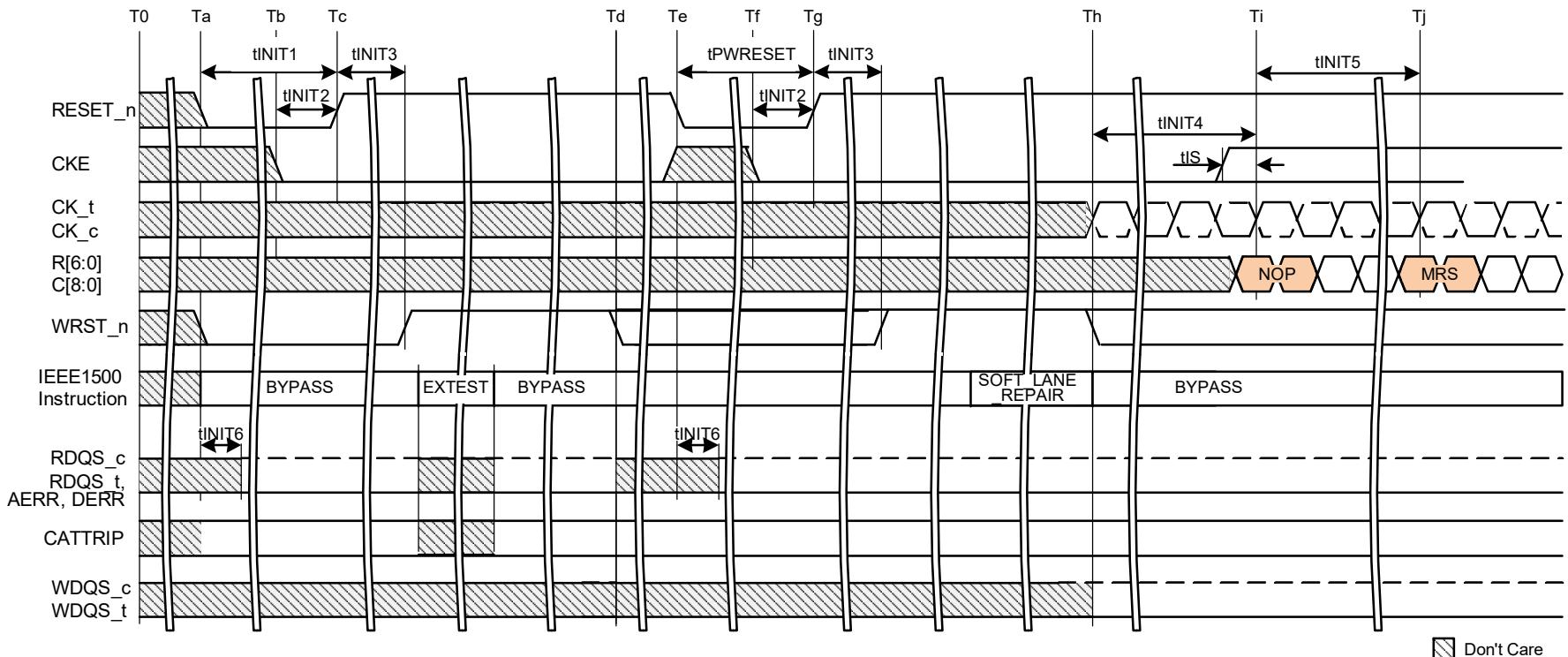


Figure 6 — Initialization Sequence with Lane Repairs

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## 5 Mode Registers

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The mode registers define the specific mode of operation for the HBM device. MR0 to MR8 and MR15 are defined as shown in Figure 1. MR9 to MR14 are reserved. Reprogramming the mode registers does not alter the contents of the memory array.

All mode registers are programmed via the [Mode Register Set \(MRS\)](#) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode registers must be loaded when all banks are idle and no bursts are in progress; the controller must wait the specified time  $t_{MOD}$  before initiating any subsequent operations. Violating either of these requirements results in unspecified operation.

No default states are defined for mode registers except when otherwise noted. Users therefore must fully initialize all mode registers to the desired values upon power-up.

Reserved bits must be programmed to 0.

**Table 8 — HBM Mode Register Overview**

Mode Register	BA[3:0]	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0					
MR0 ( <a href="#">Table 9</a> )	0000	Test Mode	ADD/CMD Parity	DQ Write Parity	DQ Read Parity	Reserved	TCSR	DBIac Write	DBIac Read					
MR1 ( <a href="#">Table 10</a> )	0001	Driver Strength			Write Recovery (WR)									
MR2 ( <a href="#">Table 11</a> )	0010	Read Latency (RL)					Write Latency (WL)							
MR3 ( <a href="#">Table 12</a> )	0011	BL	Bank Group	Active to Precharge (RAS)										
MR4 ( <a href="#">Table 15</a> )	0100	Reserved		Extended Read Latency (ERL)	Extended Write Latency (EWL)	Parity Latency (PL)		Write Data Mask (DM) and ECC						
MR5 ( <a href="#">Table 16</a> )	0101	TRR	TRR - PS Select	Reserved		TRR Mode BAn								
MR6 ( <a href="#">Table 17</a> )	0110	imPRE $t_{RP}$ Value					Reserved							
MR7 ( <a href="#">Table 18</a> )	0111	CATTRIP	Reserved	MISR Control			Read Mux Control	Loopback						
MR8 ( <a href="#">Table 19</a> )	1000	Reserved						DA28 Lockout						
MR9	1001	Reserved												
MR10	1010	Reserved												
MR11	1011	Reserved												
MR12	1100	Reserved												
MR13	1101	Reserved												
MR14	1110	Reserved												
MR15 ( <a href="#">Table 26</a> )	1111	Reserved					Optional Internal Vref (applies to DQ and ADD/CMD bus)							

## 5 Mode Registers (cont'd)

**Table 9 — Mode Register 0 (MR0)**

Field	Bits	Description	Notes
Test Mode	OP7	0 - Normal operation (default) 1 - Test mode (vendor specific)	
Address, Command Bus Parity for Row, Column Bus	OP6	0 - Disable (default) 1 - Enable	
DQ Bus Write Parity	OP5	0 - Disable (default) 1 - Enable	
DQ Bus Read Parity	OP4	0 - Disable (default) 1 - Enable	
Reserved	OP3	0	
Temperature Compensated Self Refresh (TCSR)	OP2	0 - Disable 1 - Enable (default)	
Write DBIac	OP1	0 - Disable 1 - Enable (default)	
Read DBIac	OP0	0 - Disable 1 - Enable (default)	

**Table 10 — Mode Register 1 (MR1)**

Field	Bits	Description	Notes
Nominal Driver Strength	OP[7:5]	000 - 6 mA driver (default) 001 - 9 mA driver 010 - 12 mA driver 011 - 15 mA driver 100 - 18 mA driver All other encoding are reserved	1
Write Recovery (WR) (for Auto-Precharge only)	OP[4:0]	00000 - Reserved 00001 - Reserved 00010 - Reserved 00011 - 3 nCK 00100 - 4 nCK 00101 - 5 nCK 00110 - 6 nCK 00111 - 7 nCK 01000 - 8 nCK ... 11111 - 31 nCK	2
NOTE 1 18mA driver encoding is not needed until higher speed operation such as 2 Gbps.			
NOTE 2 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.			

## 5 Mode Registers (cont'd)

**Table 11 — Mode Register 2 (MR2)**

Field	Bits	Description	Bits	Description	Notes
Read Latency (RL)	OP[7:3] MR4 OP5 = 0	00000 - Reserved 00001 - 3 nCK (minimum) 00010 - 4 nCK 00011 - 5 nCK 00100 - 6 nCK 00101 - 7 nCK 00110 - 8 nCK 00111 - 9 nCK ... 11111 - 33 nCK	OP[7:3] MR4 OP5 = 1	00000 - 34 nCK 00001 - 35 nCK 00010 - 36 nCK 00011 - 37 nCK ... 01101 - 47 nCK 01110 - 48 nCK 01111 - Reserved ... 11111 - Reserved	1
Write Latency (WL)	OP[2:0] MR4 OP4 = 0	000 - 1 nCK (minimum) 001 - 2 nCK 010 - 3 nCK 011 - 4 nCK 100 - 5 nCK 101 - 6 nCK 110 - 7 nCK 111 - 8 nCK	OP[2:0] MR4 OP4 = 1	000 - 9 nCK 001 - 10 nCK 010 - 11 nCK 011 - 12 nCK 100 - 13 nCK 101 - 14 nCK 110 - 15 nCK 111 - 16 nCK	1
NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.					

**Table 12 — Mode Register 3 (MR3)**

Field	Bits	Description	Notes
Burst Length (BL)	OP7	0 - BL2 1 - BL4	2
Bank Group	OP6	0 - Disable 1 - Enable (default)	
Activate to Precharge RAS	OP[5:0]	000000 - Reserved 000001 - Reserved 000010 - Reserved 000011 - 3 nCK 000100 - 4 nCK 000101 - 5 nCK 000110 - 6 nCK 000111 - 7 nCK 001000 - 8 nCK ... 111111 - 63 nCK	1
NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.			
NOTE 2 In pseudo channel mode, BL must be set to 4.			

## 5 Mode Registers (cont'd)

**Table 13 — MR3 - Burst Type and Burst Order Definition - BL2**

Burst Type	Burst Length	Read/Write	Burst Order
Sequential	2	Read	0, 1
		Write	0, 1

**Table 14 — MR3 - Burst Type and Burst Order Definition - BL4**

Burst Type	Burst Length	Read/Write	Starting Column Address CA0	Burst Order	Notes
Sequential	4	Read	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2
		Write	0	0, 1, 2, 3	1,2
			1	2, 3, 0, 1	1,2

NOTE 1 Reads and Write are treated as two consecutive access with BL=2.  
 NOTE 2 Burst re-order via address bit CA0 is supported in legacy mode only. The burst order is fixed in pseudo channel mode and address bit CA0 is not defined.

**Table 15 — Mode Register 4 (MR4)**

Field	Bits	Description	Notes
Reserved	OP[7:6]	0x00	
Extended Read Latency (ERL)	OP5	see <a href="#">Table 11</a>	
Extended Write Latency (EWL)	OP4	see <a href="#">Table 11</a>	
Parity Latency (PL)	OP[3:2]	00 - 0 nCK 01 - 1 nCK 10 - 2 nCK 11 - 3 nCK	
Write Data Mask (DM) and ECC	OP[1:0]	00 - Enable DM, disable ECC 01 - Reserved (DM and ECC cannot be enabled simultaneously) 10 - Disable DM, disable ECC 11 - Disable DM, enable ECC	

## 5 Mode Registers (cont'd)

**Table 16 — Mode Register 5 (MR5)**

Field	Bits	Description	Notes
TRR Mode	OP7	0 - Disable (default) 1 - Enable	
TRR Mode - Pseudo Channel Select	OP6	0 - Enable TRR mode for PC0 1 - Enable TRR mode for PC1	1,2
Reserved	OP[5:4]	00	
TRR Mode - Bank address	OP[3:0]	0000 - Bank 0 ... 1111 - Bank 15	

NOTE 1 Only applicable when MR5 OP7 = 1.  
 NOTE 2 Only applicable when DEVICE\_ID Wrapper Data Register bits [17:16] = 01.

**Table 17 — Mode Register 6 (MR6)**

Field	Bits	Description	Notes
imPRE $t_{RP}$ Value	OP[7:3]	00000 - 2nCK (Minimum) 00001 - 3 nCK 00010 - 4 nCK 00011 - 5 nCK ... 11111 - 33 nCK	1,2
Reserved	OP[2:0]	000	

NOTE 1 HBM device is not required to support all encodings. The supported encoding is based on the HBM speed bin and min-max range must be contiguous.  
 NOTE 2 imPRE is only available in pseudo channel mode. DEVICE\_ID Wrapper Data Register bits [17:16] = 01.

## 5 Mode Registers (cont'd)

**Table 18 — Mode Register 7 (MR7)**

Field	Bits	Description	Notes
CATTRIP	OP7	0 - Clear CATTRIP pin (default) 1 - Assert CATTRIP pin to “1”	1
Reserved	OP6	0	
DWORD MISR Control	OP[5:3]	Only applicable if Loopback is enabled in OP0  000 - Preset The DWORD MISR/LFSRs are set to 0xAAAAAh, and the DWORD LFSR_COMPARE_STICKY bits are set to all zeros.  001 - LFSR mode (read direction) 010 - Register mode (read and write directions) DWORD writes are captured directly into the MISR registers without compression. The MISR registers will contain the most recent write data. 011 - MISR mode (write direction) 100 - LFSR Compare mode (write direction)	2
DWORD Read Mux Control	OP[2:1]	Only applicable if Loopback is enabled in OP0  00 - Reserved 01 - Return data from MISR registers (default) 10 - Return data from Rx path sampler 11 - Return LFSR_COMPARE_STICKY (optional)	
DWORD Loopback	OP0	0 - Disable (default)  1 - Enable; enables link testing circuitry. All Writes and Reads will be to/from the MISR. (Does not require any additional Activation to Write/Reads - Column addresses are ignored in this mode.)	
NOTE 1 The CATTRIP pin can be asserted to “1” from any of the channels [a:h] MR7 OP7 bit (logic OR).			
NOTE 2 See <a href="#">HBM Loopback Test Modes</a> for DWORD MISR mode features and usage.			

**Table 19 — Mode Register 8 (MR8)**

Field	Bits	Description	Notes
Reserved	OP[7:1]	0x00	
DA28 lockout	OP0	0 - Disable (default) 1 - Enable (see <a href="#">DA28 Lockout</a> )	1
NOTE 1 DA28 lockout is defined for channels a and e only. Once enabled, the DA28 lockout can only be cleared when power is removed. The IEEE1500 <a href="#">MODE_REGISTER_DUMP_SET</a> instruction cannot be used to set or clear the DA28 lockout bit, but may optionally allow reading the DA28 lockout bit.			

**Table 20 — Mode Register 9 (MR9)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

## 5 Mode Registers (cont'd)

**Table 21 — Mode Register 10 (MR10)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

**Table 22 — Mode Register 11 (MR11)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

**Table 23 — Mode Register 12 (MR12)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

**Table 24 — Mode Register 13 (MR13)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

**Table 25 — Mode Register 14 (MR14)**

Field	Bits	Description	Notes
Reserved	OP[7:0]	0x00	

**Table 26 — Mode Register 15 (MR15)**

Field	Bits	Description	Notes
Reserved	OP[7:3]	00000	
Internal Vref	OP[2:0]	<p>Optional HBM feature.</p> <p>HBM may simply ignore these bits if there is no internal Vref generator.</p> <p>If there is internal Vref, these bits are programmed appropriately. Applies to both DQ bus as well as Row/Column address/cmd bus. HBM has only one internal Vref generator across all 8 channels. These bits must programmed identically in all eight mode registers.</p> <p>000 - <math>0.50 \times V_{DDQ}</math>            001 - <math>0.46 \times V_{DDQ}</math>            010 - <math>0.42 \times V_{DDQ}</math>            011 - <math>0.38 \times V_{DDQ}</math>            100 - <math>0.54 \times V_{DDQ}</math>            101 - <math>0.58 \times V_{DDQ}</math>            110 - <math>0.62 \times V_{DDQ}</math>            111 - <math>0.66 \times V_{DDQ}</math></p>	

## 6 Operation

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### 6.1 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK\_t/CK\_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS\_t/WDQS\_c) and Read strobes (RDQS\_t/RDQS\_c) per 32 DQ (DWORD). The data bus operates at double data rate (DDR).

The following nomenclature is being used throughout this specification:

- a rising CK (or WDQS, RDQS) edge is defined as the crossing of the positive edge of CK\_t (or WDQS\_t, RDQS\_t) and the negative edge of CK\_c (or WDQS\_c, RDQS\_c);
- a falling CK (or WDQS, RDQS) edge is defined as the crossing of the negative edge of CK\_t (or WDQS\_t, RDQS\_t) and the positive edge of CK\_c (or WDQS\_c, RDQS\_c).

## 6.1 Clocking Overview (Cont'd)

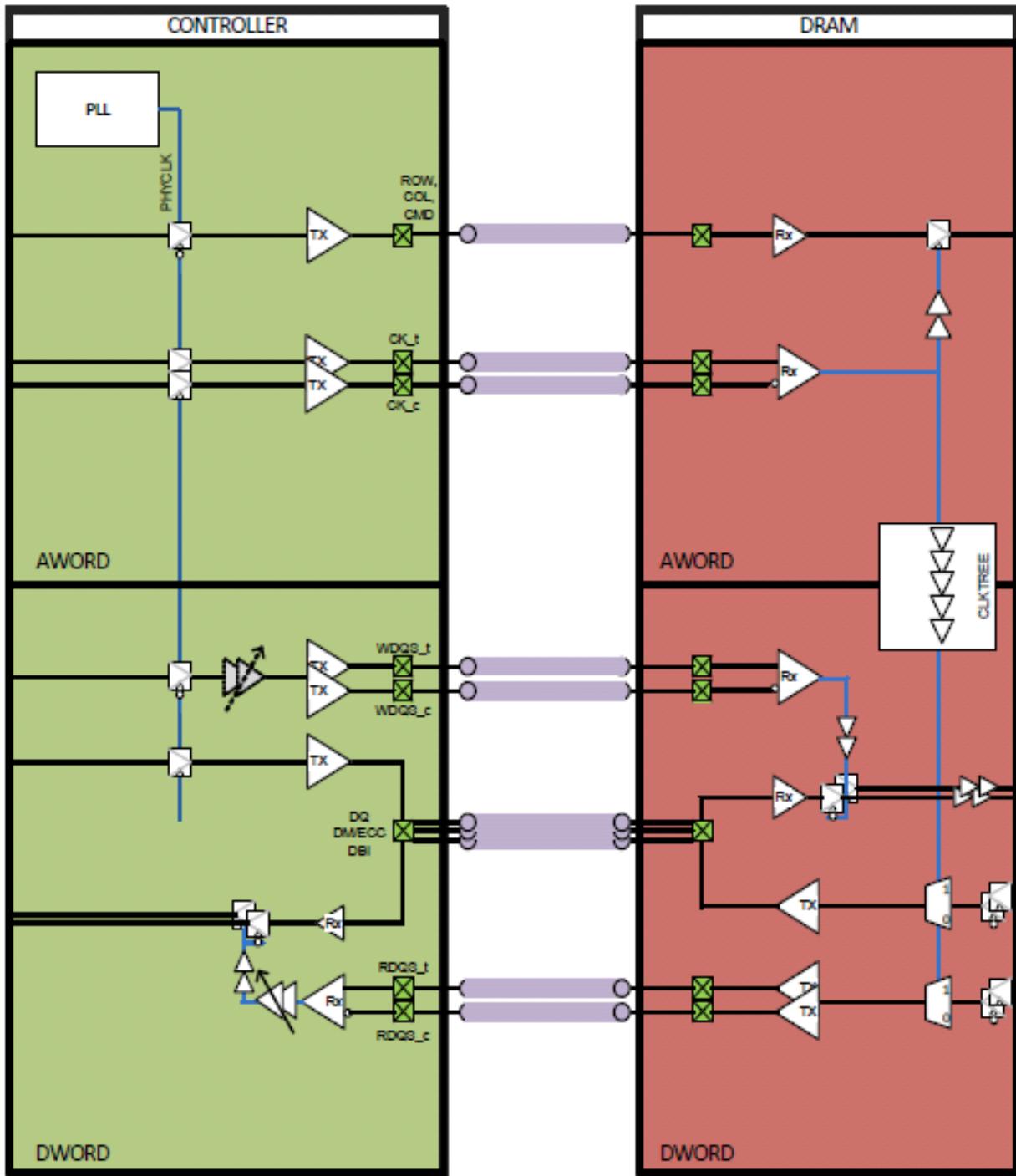


Figure 7 — High Level Block Diagram Example of Clocking Scheme

## 6.2 HBM Write Data Mask (DM), Data Bus Inversion (DBIac) and ECC

The HBM device supports Write Data Mask (DM), Data Bus Inversion (DBIac) and optionally ECC with byte granularity. One Data Mask (DM) pin and one Data Bus Inversion (DBI) pin per byte are provided as shown in [Table 27](#). DBI is a bi-directional DDR pin and driven or sampled along with the DQ pins for Read and Write operation. DM is a bi-directional DDR pin and driven or sampled along with DQ signals pins for Read or Write operation when used with ECC (see below); the pin is input only and used for Write operations when used with Write Data Mask.

**Table 27 — DM, DBI to DQ Correspondence and Even/Odd Byte Groups**

DQ	DBI	DM	Even/Odd Byte Group
DQ[7:0]	DBI0	DM0	Even Byte
DQ[15:8]	DBI1	DM1	Odd Byte
DQ[23:16]	DBI2	DM2	Even Byte
DQ[31:24]	DBI3	DM3	Odd Byte
DQ[39:32]	DBI4	DM4	Even Byte
DQ[47:40]	DBI5	DM5	Odd Byte
DQ[55:48]	DBI6	DM6	Even Byte
DQ[63:56]	DBI7	DM7	Odd Byte
DQ[71:64]	DBI8	DM8	Even Byte
DQ[79:72]	DBI9	DM9	Odd Byte
DQ[87:80]	DBI10	DM10	Even Byte
DQ[95:88]	DBI11	DM11	Odd Byte
DQ[103:96]	DBI12	DM12	Even Byte
DQ[111:104]	DBI13	DM13	Odd Byte
DQ[119:112]	DBI14	DM14	Even Byte
DQ[127:120]	DBI15	DM15	Odd Byte

### 6.2.1 Write Data Mask (DM)

Write data mask (DM) function can be enabled per MR4 OP1 (see [Table 15](#)). Write data received on the DQ inputs are masked in case DM is sampled HIGH and DQ input signals are don't care (either valid HIGH or LOW); DQ input signals are valid and write data is written to the DRAM array in case DM is sampled LOW.

Please note that when DQ parity is enabled for Writes, the data inputs are included in the parity calculation regardless whether a byte is masked by DM or not.

**Table 28 — Write Data Mask (DM)**

Function	DM	DQ
Write Enable	LOW	Valid
Write Inhibit	HIGH	Ignored

## 6.2.2 Error Correction Code (ECC)

HBM DRAM devices may optionally support ECC (one bit per data byte). The HBM DRAM itself does not compute any ECC. The HBM DRAM provides the additional DRAM cells to store ECC information. ECC bits are not included in parity calculation when Write or Read DQ Parity Function is enabled (see [Table 37](#)). The ECC function can be enabled or disabled per MR4 OP0.

## 6.2.3 DM & ECC Function Combinations

[Table 29](#) summarizes the DM pin function as configured by MR4 OP[1:0].

**Table 29 — DM Pin Function**

MR4		Write Data Mask (DM)	Error Correction Code (ECC)	DM Pin Function
OP1	OP0			
0	0	Enabled	Disabled	Input only
0	1	Not allowed		Undefined
1	0	Disabled	Disabled	Hi-Z (input receivers and output drivers turned off)
1	1	Disabled	Enabled	Bi-directional

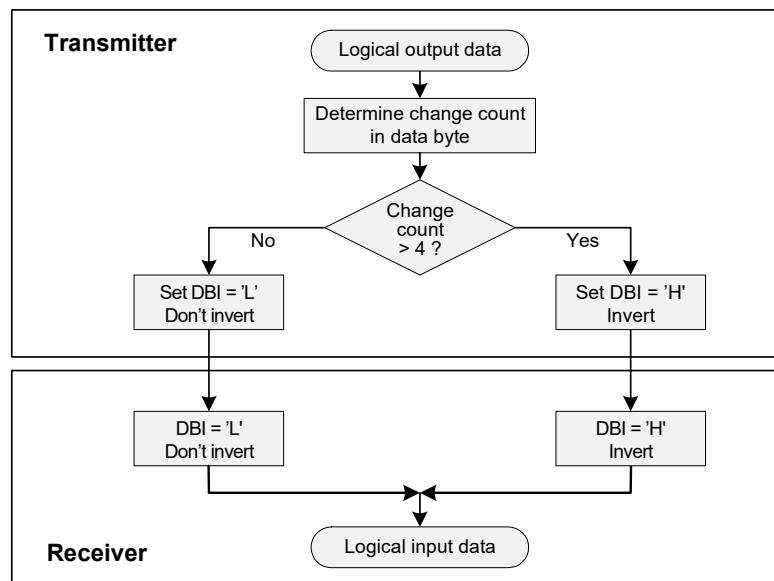
## 6.2.4 DBIac Function

DBIac function can be enabled or disabled independently for Write and Read operation per HBM mode register MR0 OP1 and OP0, respectively (see [Table 9](#)).

When both Write and Read DBIac function is disabled in mode register, DBI signal is a don't care for HBM device. HBM DBI input receivers and output drivers are turned off.

### 6.2.4.1 DBIac Enabled

HBM devices supports byte granular Data Bus Inversion during Write and Read operation. In this standard, the word DBI refers to internal state of the device unless explicitly noted as DBI signal or pin.



**Figure 8 — DBIac Algorithm**

### 6.2.4.1 DBIac Enabled (cont'd)

**Write Operation** - HBM device inverts Write data received on the DQ inputs in case DBI is sampled HIGH, or leaves the Write data non-inverted in case DBI is sampled LOW. Note that DM input is not affected by the DBIac function.

**Read Operation** - HBM device counts the number of DQ signals that are transitioning from previous state. Note that DM output is not affected by the DBIac function. See [Read Operation](#) under [DBIac States](#) section for bus pre-condition. The HBM device inverts Read data and sets DBI HIGH when the number of transitioning data bits within a byte is greater than 4, or when the number of transitioning data bits within a byte equals 4 and DBI was High; otherwise the HBM device does not invert the Read data and sets DBI LOW.

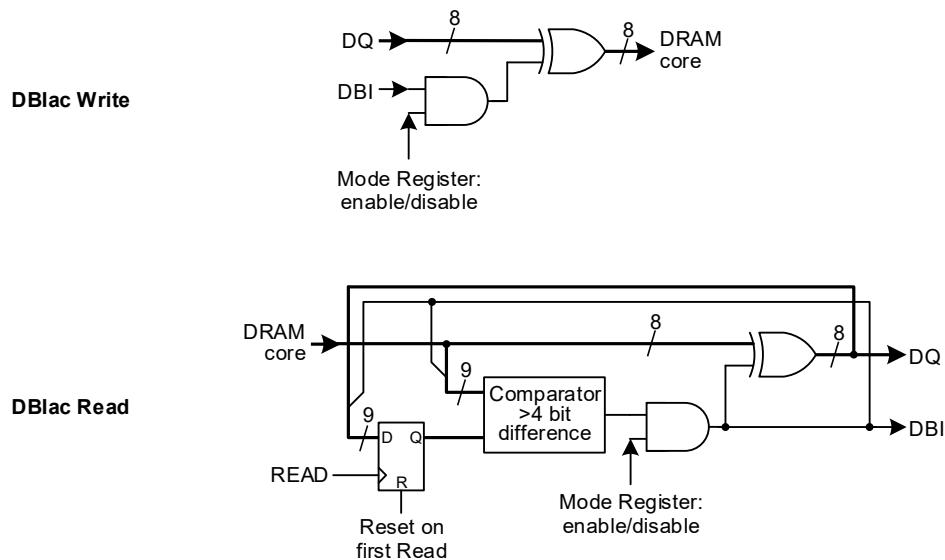


Figure 9 — Example DBIac Logic for Write and Read

### 6.2.5 DBIac States

The HBM device resets DBIac value to LOW (All eight DQs and DBI signals within a byte group) whenever any of the following four events occur:

- RESET\_n signal de-assertion
- The HBM device registers Mode Register Set command (MRS)
- The HBM device registers Read or Read w/AP command after Write command. Note that HBM device is only required to reset DBIac value 1/2 clock prior to Read operation begins and hence it may reset DBIac value anytime before that.
- Self Refresh exit

For all other events or commands registered by the HBM, the DBIac value is not reset to LOW and the HBM device will use its previous value for DBIac calculation.

## 6.2.5 DBIac States (cont'd)

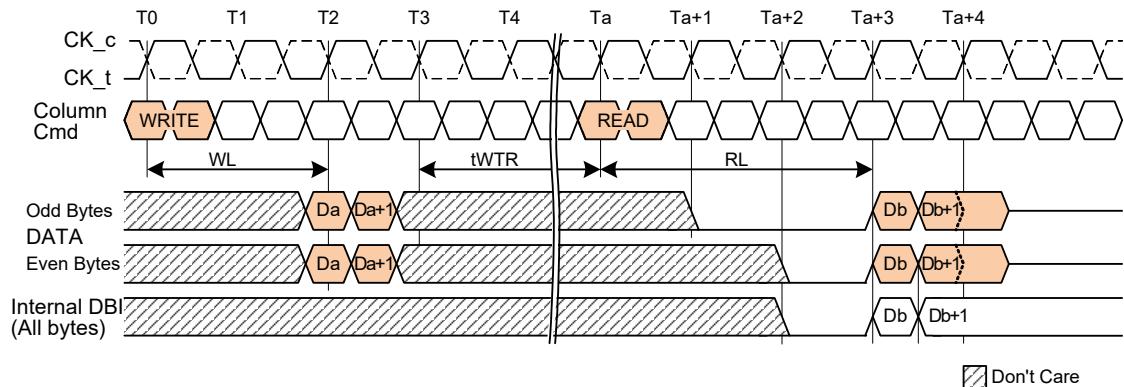


Figure 10 — Write followed by Read Timing;  $BL=2$

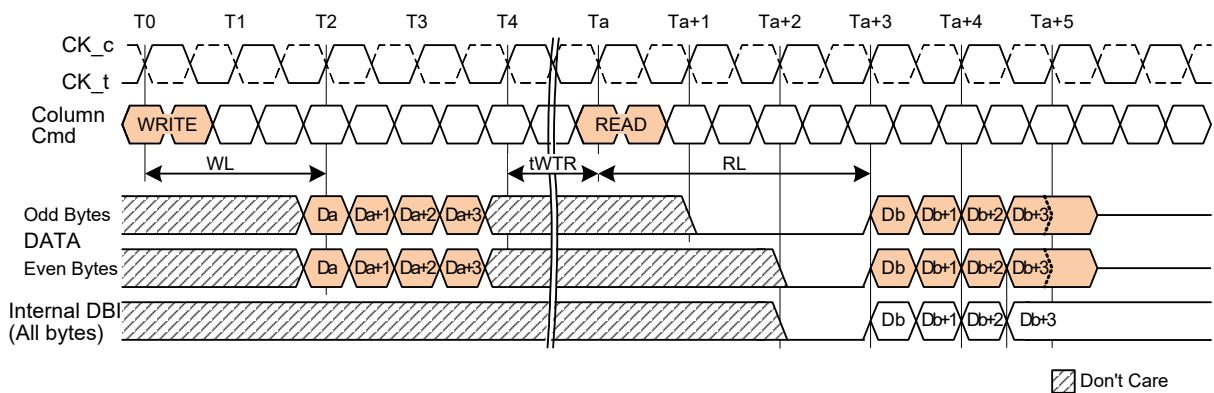


Figure 11 — Write followed by Read Timing;  $BL=4$

### 6.2.5.1 Read Operation

#### First Read Command:

When a first Read command is registered after a DBI reset, HBM device pre-conditions the bus to LOW over 2  $t_{CK}$  period prior to Read data. HBM drives odd byte signals to LOW 2  $t_{CK}$  prior to Read data and even byte signals to LOW 1  $t_{CK}$  prior to Read data. When DBIac function is disabled in MR, HBM device does not pre-condition the bus as described. The PAR signal is not included in the DBI calculation and therefore not preconditioned to LOW; its initial state is undefined (LOW or HIGH).

#### Consecutive Read Commands (Seamless and non-seamless):

Once the Read DQ burst is complete, the HBM device tri-states DBI, DM and all DQ output drivers. However, the HBM device must store the last data-out of all DQ, DM and DBI states and use that to pre-condition the bus prior to Read data and for Read DBIac calculation for any subsequent Read operation barring a condition to DBI reset. For back to back Read operation with a gap, the HBM device pre-conditions all DQ, DM and DBI to last beat of previous burst over 2  $t_{CK}$  period prior to Read data. HBM drives Odd byte signals to previous state 2  $t_{CK}$  prior to Read data and Even byte signals to previous state 1  $t_{CK}$  prior to Read data.

### 6.2.5.1 Read Operation (cont'd)

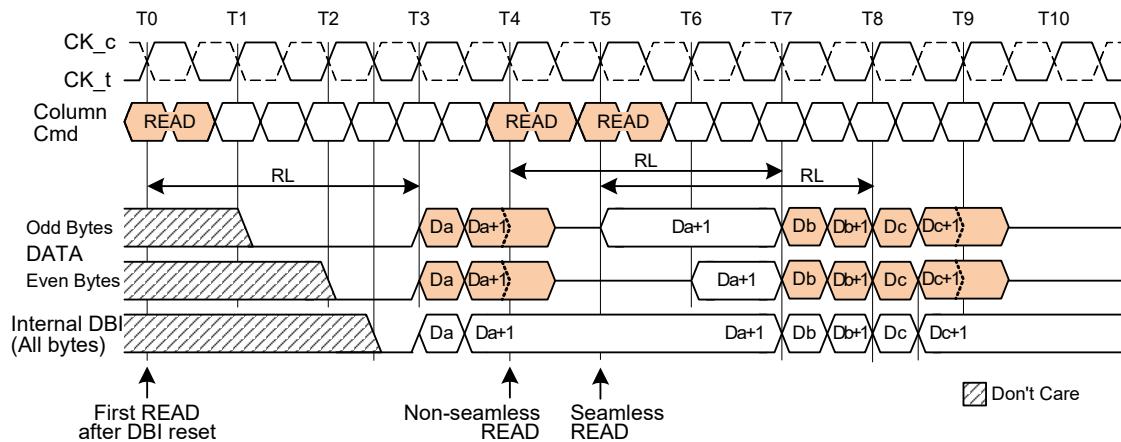


Figure 12 — Read Timing; BL=2

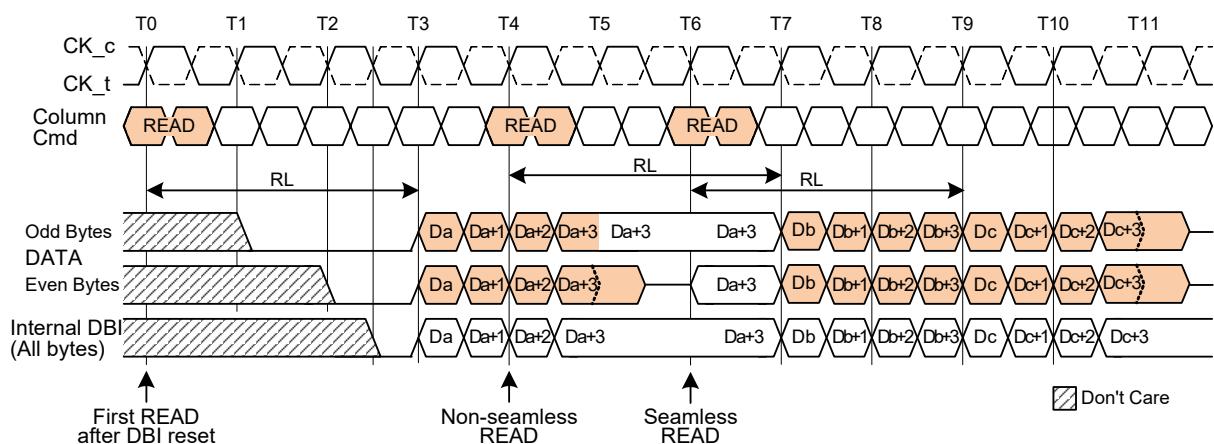


Figure 13 — Read Timing; BL=4

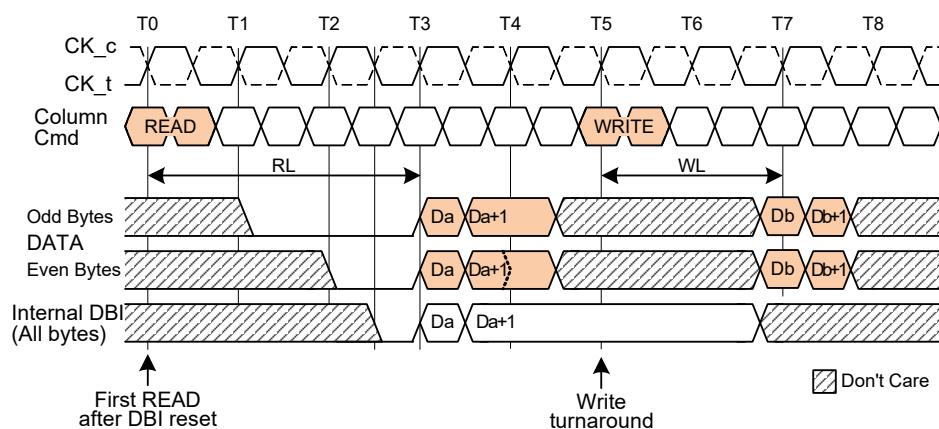


Figure 14 — Read followed by Write Timing; BL=2

### 6.2.5.1 Read Operation (cont'd)

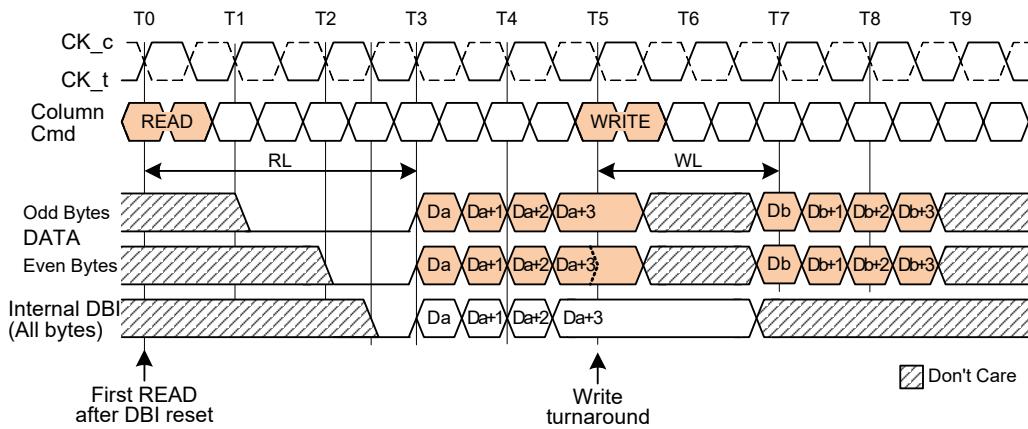


Figure 15 — Read followed by Write Timing; BL=4

### 6.3 Commands

The HBM DRAM features DDR commands entered on both rising and falling CK clock edges. Row Activate commands require two cycles, other row and column commands require only one cycle.

#### 6.3.1 Command Truth Tables

**Table 30 — Row Commands Truth Table**

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		R0	R1	R2	R3	R4	R5	R6 <sup>11</sup>	NOTES
			(N-1)	(N)								
Row No Operation	RNOP	Rising	H	H	H	H	H	V	V	V	V	1,4,7
		Falling			V	V	PAR	V	V	V	V	
Activate	ACT	Rising	H	H	L	H	V/SID/SID0	BA0	BA1	BA2	RA14	1,2,3,4,7,8,9,10
		Falling			RA11	RA12	PAR	BA4	RA13	BA3	V/SID1	
		Rising			RA5	RA6	RA7	RA8	RA9	RA10	V	
		Falling			RA0	RA1	PAR	RA2	RA3	RA4	V	
Precharge	PRE	Rising	H	H	H	H	L	BA0	BA1	BA2	V/SID1	1,3,4,7,8,9
		Falling			V	V/SID/SID0	PAR	BA4	L	BA3	V	
Precharge All	PREA	Rising	H	H	H	H	L	V	V	V	V	1,4,7,8
		Falling			V	V	PAR	BA4	H	V	V	
Single Bank Refresh	REFSB	Rising	H	H	L	L	H	BA0	BA1	BA2	V/SID1	1,3,4,7,8,9
		Falling			V	V/SID/SID0	PAR	BA4	L	BA3	V	
Refresh	REF	Rising	H	H	L	L	H	V	V	V	V	1,4,7,8
		Falling			V	V	PAR	BA4	H	V	V	
Power-Down Entry	PDE	Rising	H	L	H	H	H	V	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	V	
Self Refresh Entry	SRE	Rising	H	L	L	L	H	V	V	V	V	1,4,6,7
		Falling			V	V	PAR	V	V	V	V	
Power-Down & Self Refresh Exit	PDX/SRX	Rising	L	H	H	H	H	V	V	V	V	1,5,6,7
		Falling			V	V	V	V	V	V	V	

NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but not floating).  
 NOTE 2 The unused upper row address bits RA13 and RA14 must be driven to valid signal level depending on the DRAM density; they are evaluated in the parity calculation if the parity function is enabled in the mode register.  
 NOTE 3 For 8 bank device, BA3 must be driven to valid signal level; it is evaluated in the parity calculation if the parity function is enabled in the mode register.  
 NOTE 4 PAR signal must be driven to valid signal level even if parity function is disabled in DRAM mode register.  
 NOTE 5 No Parity checking at Power-Down Exit or Self Refresh Exit command. The HBM device requires RNOP and CNOP commands on Row and Column bus respectively with valid parity if enabled during power-down exit period ( $t_{XP}$ ) and self refresh exit period ( $t_{XS}$ ).  
 NOTE 6 CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising clock edge. Refer to the [CKE Truth Table](#) for more details with CKE transitions.  
 NOTE 7 All other command encoding not shown in the table for pins R[4:2:0] at the rising clock edge are reserved commands for future use.  
 NOTE 8 BA4 applies to only pseudo channel (PC) mode. BA4 = 0 means PC0; BA4 = 1 means PC1. See section [Legacy Mode and Pseudo Channel Mode](#) for a detailed explanation of PC mode operation and timing. The pseudo channel not selected by BA4 performs a RNOP.  
 NOTE 9 The SID bits act as bank address bits in conjunction with ACT, PRE and REFSB commands, and related timing diagrams shall be interpreted accordingly. PREA and REF commands do not use SID. Input R2 (ACT) or input R1 (PRE, REFSB) is SID for 8-High configurations, and SID0 for 12-High configurations. Input R6 is SID1 for 12-High configurations. The bits are V for all other configurations.

**Table 30 — Row Commands Truth Table (cont'd)**

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		R0	R1	R2	R3	R4	R5	R6 <sup>11</sup>	NOTES
			(N-1)	(N)								
NOTE 10	Timing parameter $t_{FAW}$ may have two values depending on whether related commands refer to the same or a different SID. Vendor datasheets should be checked for details.											
NOTE 11	Input R6 is only present with HBM2 configurations whose addressing includes the RA14 or SID1 address bit or both (see <a href="#">Table 4</a> ). If input C8 is present, input R6 for the row commands (see <a href="#">Table 30</a> ) is present as well.											

**Table 31 — Column Commands Truth Table**

FUNCTION	SYMBOL	CLOCK CYCLE	CKE		C0	C1	C2	C3	C4	C5	C6	C7	C8 <sup>10</sup>	NOTES
			(N-1)	(N)										
Column No Operation	CNOP	Rising	H	H	H	H	H	V	V	V	V	V	V	1,4,5,6
		Falling			V	V	PAR	V	V	V	V	V	V	
Read	RD	Rising	H	H	H	L	H	L	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8,9
		Falling			CA0/ V/SID/ SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/ BA4	V	
Read w/ AP	RDA	Rising	H	H	H	L	H	H	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8,9
		Falling			CA0/ V/SID/ SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/ BA4	V	
Write	WR	Rising	H	H	H	L	L	L	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8
		Falling			CA0/ V/SID/ SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/ BA4	V	
Write w/ AP	WRA	Rising	H	H	H	L	L	H	BA0	BA1	BA2	BA3	V/SID1	1,2,3,4,5,6,7,8
		Falling			CA0/ V/SID/ SID0	CA1	PAR	CA2	CA3	CA4	CA5	V/ BA4	V	
Mode Register Set	MRS	Rising	H	H	L	L	L	OP7	BA0	BA1	BA2	BA3	V	1,2,4,5,6
		Falling			OP0	OP1	PAR	OP2	OP3	OP4	OP5	OP6	V	

NOTE 1 BA = Bank Address; SID = Stack ID; PAR = Parity Signal; V = Valid Signal (either H or L, but not floating).

NOTE 2 CA0 is defined for legacy mode only. In pseudo channel mode the pin is either SID or ignored (V), depending on density.

NOTE 3 All pins must be driven to a valid signal level even if an address (SID, BA4, BA3, CA0) is not defined for a specific density, or if parity is disabled in the mode register.

NOTE 4 Parity is evaluated on all pins if the parity function is enabled in the mode register.

NOTE 5 CKE transition from HIGH to LOW or LOW to HIGH must be accompanied with a Column No Operation (CNOP) command. Refer to CKE Truth Table for more details with CKE transitions.

NOTE 6 All other command encodings not shown in the table for pins C[3:0] at the rising clock edge are reserved commands for future use.

NOTE 7 BA4 applies to only pseudo channel (PC) mode. BA4 = 0 means PC0; BA4 = 1 means PC1. See Section [Legacy Mode and Pseudo Channel Mode](#) for detailed explanation of pseudo channel mode operation and timing. The pseudo channel not selected by BA4 performs a CNOP.

NOTE 8 The SID bits act as bank address bit in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. The MRS command does not use SID. Input C0 is SID for 8-High configurations, and SID0 for 12-High configurations. Input C8 is SID1 for 12-High configurations. The bits are V for all other configurations.

NOTE 9 HBM configurations using the SID specify a timing parameter  $t_{CCDR}$  for consecutive READs to different SID. Vendor datasheets should be checked for details.

NOTE 10 Input C8 is only present with HBM2 configurations whose addressing includes the RA14 or SID1 address bit or both (see [Table 4](#)). If input C8 is present, input R6 for the row commands (see [Table 30](#)) is present as well.

### 6.3.1 Command Truth Tables (cont'd)

Table 32 — CKE Truth Table

CURRENT STATE	CKE		ROW COMMAND	ACTION	NOTES
	PREVIOUS CYCLE (N-1)	CURRENT CYCLE (N)			
Power-Down	L	L	X	Maintain Power-Down	1,4,6,7
	L	H	RNOP	Power-Down Exit	1,2,3,8
Self Refresh	L	L	X	Maintain Self Refresh	1,4,9
	L	H	RNOP	Self Refresh Exit	1,2,3,8
Bank(s) Active	H	L	RNOP	Active Power-Down Entry	2,3,6,7
Precharging	H	L	RNOP	Power-Down Entry	2,3,6,7
Refreshing	H	L	RNOP	Power-Down Entry	2,3,6,7
All Banks Idle	H	L	RNOP	Precharge Power-Down Entry	2,3,6,7
	H	L	REF	Self Refresh Entry	2,4,5,9

NOTE 1 X = Don't care (command decoder disabled).  
 NOTE 2 CKE is a single data rate input and CKE transition from HIGH to LOW or LOW to HIGH is evaluated only with the rising edge of CK.  
 NOTE 3 With CKE transition from HIGH to LOW or LOW to HIGH, CNOP commands must be registered on column bus.  
 NOTE 4 In power-down state (either active or precharge) and self refresh state, row and column bus signals are X (Don't care; either HIGH or LOW or floating).  
 NOTE 5 Self refresh mode can only be entered from all banks idle state. Idle state is defined as all banks are closed ( $t_{RP}$ ,  $t_{DAL}$ , etc. satisfied), no data bursts are in progress, CKE is HIGH and all timing from previous operations are satisfied as well as all Self refresh exit and power-down exit timing parameters are satisfied.  
 NOTE 6 The power-down state (either active or precharge) does not perform any refresh operation.  
 NOTE 7 In power-down mode, clocks may be turned off after  $t_{CKSRE}$ .  
 NOTE 8 Clocks must be valid and stable  $t_{CKSRX}$  time prior to power-down and self refresh exit.  
 NOTE 9 After self refresh entry, clocks may be turned off after  $t_{CKSRE}$ .

### 6.3.2 Row Commands

#### 6.3.2.1 Row No Operation Command (RNOP)

The ROW NO OPERATION (RNOP) command as shown in Figure 16 is used to instruct the HBM device to perform a NOP as row command; this prevents unwanted row commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated on all R[6:0] or R[5:0] inputs when the parity calculation is enabled in the Mode Register.

RNOP is assumed on subsequent timing diagrams unless other row commands are explicitly shown.

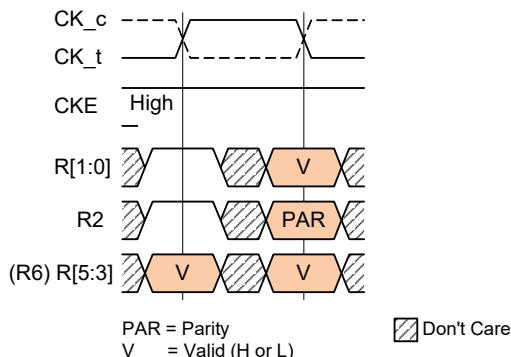


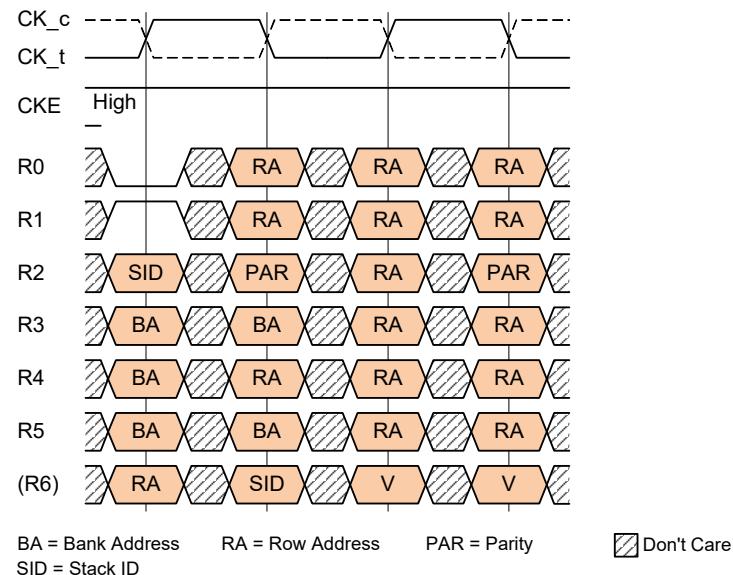
Figure 16 — RNOP Command

### 6.3.2.2 Bank and Row ACTIVATE Command (ACT)

Before a READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished via the ACTIVATE command, which selects both the bank and the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the  $t_{RCD}$  specification.

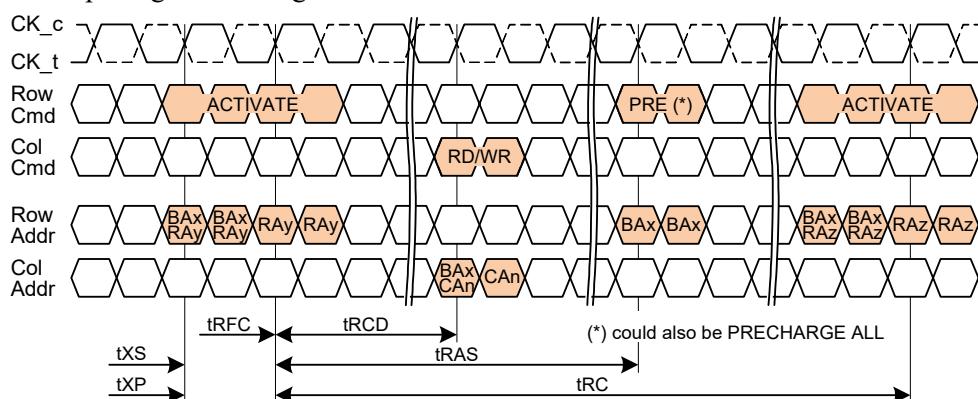
The ACTIVATE command is a 2-cycle command as shown in [Figure 17](#). The actual bank and row activation is initiated with the second clock cycle; therefore all relevant timing parameters refer to this second clock cycle as shown in subsequent timing diagrams.

Parity is evaluated on all R[6:0] or R[5:0] inputs separately on both clock cycles of the ACT command when the parity calculation is enabled in the Mode Register.



**Figure 17 — ACTIVATE Command**

A subsequent ACTIVATE command to another row in the same bank can only be issued after the previous active row has been closed (precharged). The minimum time interval between successive ACTIVATE commands to the same bank is defined by  $t_{RC}$ , as shown in [Figure 18](#). A minimum time  $t_{RAS}$  must have elapsed between opening and closing a row.



1. BAx = bank address x; RAY,y,z = row address y,z; CAN = column address n.
2. tRCD = tRCDRD or tRCDWR, depending on command.
3. An ACTIVATE command is allowed ( $t_{XP} + 1$  tCK) after power-down exit, and ( $t_{XS} + 1$  tCK) after self refresh exit.

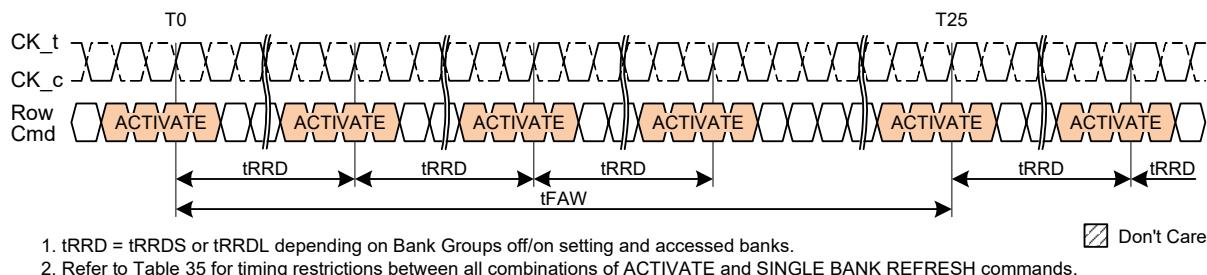
**Figure 18 — Bank and Row Activation Command Cycle**

### 6.3.2.2 Bank and Row ACTIVATE Command (ACT) (cont'd)

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVATE commands to different banks is defined by  $t_{RRD}$ . The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

#### 6.3.2.2.1 Bank Restrictions

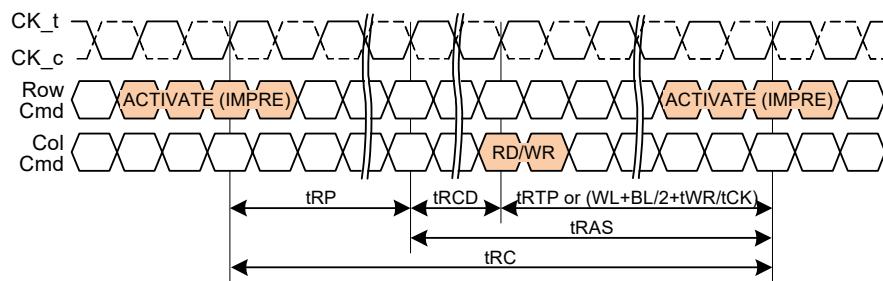
There is a need to limit the number of bank activations in a rolling window to ensure that the instantaneous current supplying capability of the device is not exceeded. To reflect the short term capability of the HBM device's current supply, the parameter  $t_{FAW}$  (four activate window) is defined: no more than 4 banks may be activated in a rolling  $t_{FAW}$  window. Converting to clocks is done by dividing  $t_{FAW}$  (ns) by  $t_{CK}$  (ns) and rounding up to next integer value. As an example of the rolling window, if  $(t_{FAW}/t_{CK})$  rounds up to 25 clocks, and an ACTIVATE command is issued at clock T0, no more than three further ACTIVATE commands may be issued at clocks T1 through T24 as illustrated in [Figure 19](#).



**Figure 19 — Multiple Bank Activations**

### 6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge

For devices operating in pseudo channel mode, a subsequent ACTIVATE command to another row in the same bank can be issued without closing the previous row. If a row is open and a new row within the bank is activated, the DRAM will internally issue a PRE command (imPRE) after the 2nd clock to precharge the row. After the imPRE command time has elapsed as set by MR6 (see [Table 17](#)), the requested ACTIVATE command is issued internally.

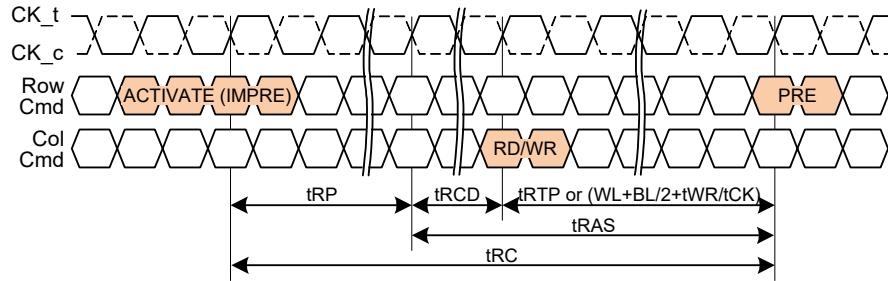


1. Two consecutive ACT commands with Implicit Precharge to the same bank are shown.
2.  $t_{RP}$  is the number of clock cycles programmed in the Mode Register.
3.  $t_{RCD}$  is IRCDRD for Reads and IRCDWR for Writes.

**Figure 20 — imPRE to imPRE Timing**

In the case of an imPRE to a row, a READ or WRITE to that row can be issued after  $t_{RP} + t_{RCD}$ . The minimum time interval between successive ACTIVATE commands to the same bank is defined by  $t_{RC}$  as shown in [Figure 21](#). A minimum time  $t_{RAS}$  must have elapsed between actual opening and closing a row (closing can be done by either imPRE or external PRE command).

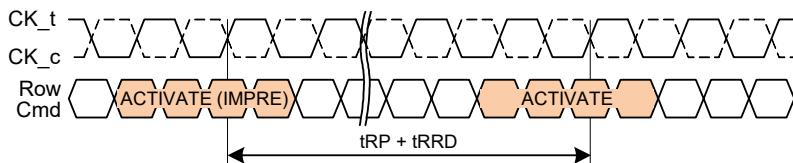
### 6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge (cont'd)



1. An ACT command with Implicit Precharge followed by an explicit PRE command to the same bank are shown.
2. PRE could also be PREALL.
3. tRP is the number of clock cycles programmed in the Mode Register.
4. tRCD is tRCDRD for Reads and tRCDWR for Writes.

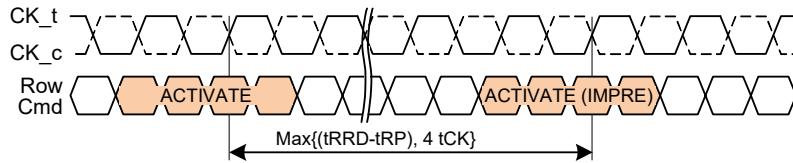
**Figure 21 — imPRE to Explicit PRE**

ACTIVATE to ACTIVATE times to different banks is limited by the  $t_{RRD}$  spec. For back to back activates to banks with open rows or back to back activates to banks with no open rows,  $t_{RRD}$  applies. For back to back ACTIVATE first to a bank with an open row and then an ACTIVATE to a bank that is idle (closed), the ACTIVATE to ACTIVATE time is  $t_{RRD} + t_{RP}$  to allow for the first bank to complete its internal precharge shown in [Figure 22](#). For back to back ACTIVATE first to a bank that is idle (closed) and then an ACTIVATE to a bank that has an open row, the ACTIVATE to ACTIVATE time is  $\text{MAX}\{(t_{RRD} - t_{RP}), 4 t_{CK}\}$  shown in [Figure 23](#).



1. An ACT command with Implicit Precharge followed by an ACT command to a different bank are shown.
2. tRP is the number of clock cycles programmed in the Mode Register.

**Figure 22 — imPRE to ACTIVATE**

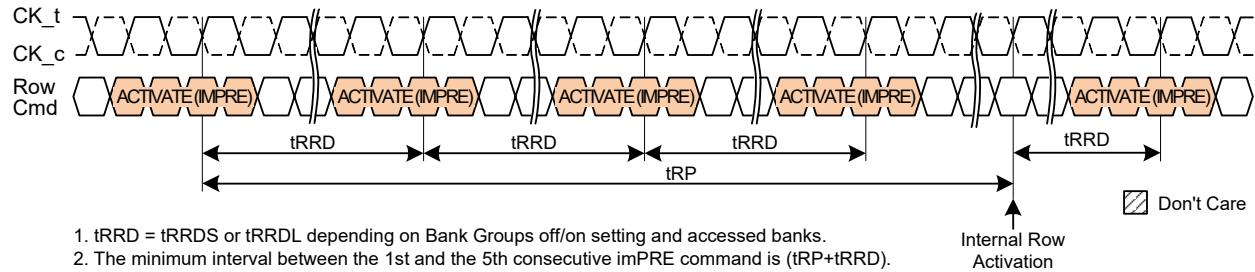


1. An ACT command followed by an ACT command with Implicit Precharge to a different bank are shown.
2. tRP is the number of clock cycles programmed in the Mode Register.

**Figure 23 — ACTIVATE to imPRE**

There is a limit to the number of concurrent imPRE commands. If an ACTIVATE command triggers an imPRE, a subsequent ACTIVATE command to a different bank with an already open row can be issued within the  $t_{RP}$  time of the previous imPRE. Only four concurrent imPRE commands can occur, meaning that the minimum interval between a first and a fifth consecutive imPRE command is given by  $(t_{RP} + t_{RRD})$  as shown in [Figure 24](#).

### 6.3.2.3 Bank and Row ACTIVATE Command (ACT) - Implicit Precharge (cont'd)



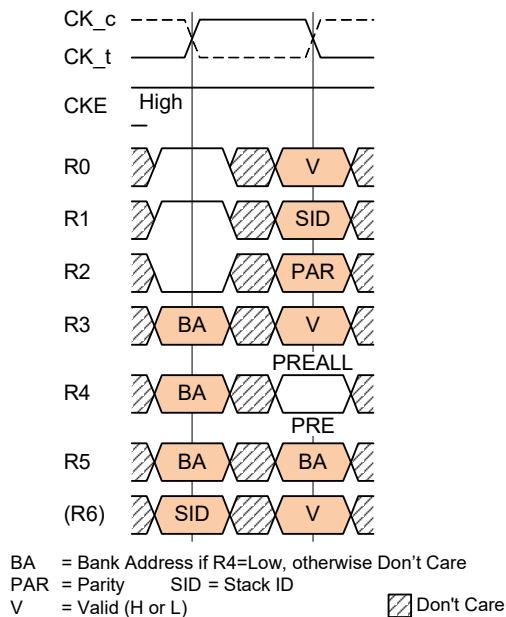
**Figure 24 — Concurrent Activations with Implicit Precharge**

An explicit PRE command can be issued to yet a different bank with one or two ongoing imPRE commands. PREALL cannot be issued with ongoing imPRE commands.

### 6.3.2.4 Precharge Command (PRE/PREALL)

The PRECHARGE command is used to deactivate the open row in a particular bank (PRE) or the open rows in all banks (PREALL). The bank(s) will be in idle state and available for a subsequent row access a specified time  $t_{RP}$  after the PRECHARGE command is issued.

Parity is evaluated with the PRECHARGE command when the parity calculation is enabled in the Mode Register.



**Figure 25 — PRECHARGE Command**

Input R4 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, bank addresses BA[3:0] select the bank. Otherwise the bank addresses are treated as “Don’t Care”.

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

#### 6.3.2.4.1 AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit PRECHARGE command. Auto Precharge is nonpersistent meaning that it is enabled or disabled along for each individual READ or WRITE command.

For read bursts an auto precharge of the bank and row that is addressed with the READ command begins  $t_{RTP}$  after the READ command was issued or after  $t_{RAS}$  has been met, with  $t_{RAS}$  as programmed in clock cycles in the RAS field of Mode Register MR3 OP[5:0].

For write bursts an auto precharge of the bank and row that is addressed with the WRITE command begins  $WL + BL/2 + WR$  clock cycles after the WRITE command was issued or after  $t_{RAS}$  has been met, with WR as programmed in clock cycles in the WR field of MR1 OP[4:0] ([Table 10](#)) and  $t_{RAS}$  as programmed in clock cycles in the RAS field of MR3 OP[5:0] ([Table 12](#)).

Auto Precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge ( $t_{RP}$ ) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for READ or WRITE commands. A precharge resulting from a READ or WRITE with Auto Precharge may occur in parallel with an explicit PRECHARGE or PREALL command.

### 6.3.2.4.1 AUTO PRECHARGE (cont'd)

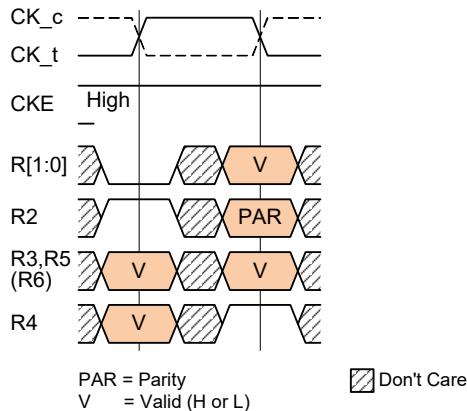
**Table 33 — Precharge and Auto Precharge Timings**

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN "FROM COMMAND" TO "TO COMMAND"	UNIT	NOTE
READ	PRECHARGE (same bank)	$t_{RTP}$	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	PREALL	$t_{RTP}$	nCK	5
	WRITE or WRITE w/ AP (any bank)	$t_{RTW}$	ns	
	READ or READ w/ AP (any bank)	$t_{CCD}$	nCK	6
READ w/ AP	PREALL	$t_{RTP}$	nCK	5
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$t_{RP} + RU(t_{RP}/t_{CK})$	nCK	2,5
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	$t_{RTW}$	ns	
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	$t_{CCD}$	nCK	6
WRITE	PRECHARGE (same bank)	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	PREALL	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	WRITE or WRITE w/ AP (any bank)	$t_{CCD}$	nCK	6
	READ w/ AP (same bank)	$WL + BL/2 + MAX[RU(t_{WR}/t_{CK}) - t_{RTP}, t_{WTR}]$	nCK	2,5,7,8
	READ (same bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
WRITE w/ AP	PREALL	$WL + BL/2 + RU(t_{WR}/t_{CK})$	nCK	2,7
	PRECHARGE (different bank)	0	nCK	4
	ACTIVATE or REFRESH SINGLE BANK (same bank)	$WL + BL/2 + WR + RU(t_{RP}/t_{CK})$	nCK	2,7
	WRITE or WRITE w/ AP (same bank)	Illegal		
	WRITE or WRITE w/ AP (different bank)	$t_{CCD}$	nCK	6
	READ or READ w/ AP (same bank)	Illegal		
	READ or READ w/ AP (different bank)	$WL + BL/2 + t_{WTR}$	nCK	7,8
PRECHARGE	PRECHARGE (same bank)	1	nCK	
	PREALL	1	nCK	3
PREALL	PRECHARGE or PREALL	1	nCK	3
NOTE 1 A command issued during the minimum delay time is illegal. NOTE 2 RU = round up to next integer. NOTE 3 PREALL is treated as a NOP for a bank when that bank is already idle or in the process of being precharged. NOTE 4 READ or WRITE and PRECHARGE commands may be issued simultaneously. NOTE 5 $t_{RTP}$ could either be $t_{RTPS}$ or $t_{RTPL}$ . NOTE 6 $t_{CCD}$ could either be $t_{CCDS}$ or $t_{CCDL}$ ; for READs, $t_{CCD}$ could also be $t_{CCDR}$ . NOTE 7 WL = write latency. BL = burst length. NOTE 8 $t_{WTR}$ could either be $t_{WTRS}$ or $t_{WTRL}$ .				

### 6.3.2.5 REFRESH Command (REF)

The REFRESH command is used during normal operation of the HBM device. The command is received on the row command inputs R[6:0] or R[5:0] as shown in [Figure 26](#) and requires a CNOP command on the column command inputs C[8:0] or C[7:0].

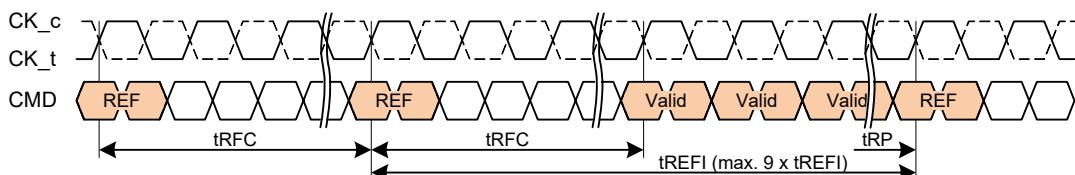
Parity is evaluated with the REFRESH command when the parity calculation is enabled in the Mode Register.



**Figure 26 — REFRESH Command**

The REFRESH command is nonpersistent, so it must be issued each time a refresh is required. A minimum time  $t_{RFC}$  is required between two REFRESH commands or a REFRESH command and any subsequent access command after the refresh operation. All banks must be precharged with  $t_{RP}$  satisfied prior to the REFRESH command. The banks are in idle state after completion of the REFRESH command.

The refresh addressing is generated by an internal refresh controller. This makes the address bits “Don’t Care” during a REFRESH command.



1. Only RNOP and CNOP commands allowed after REFRESH command registered until tRFC expires.
2. The time interval between two REFRESH commands may be extended to a maximum of 9 x tREFI.

**Figure 27 — Refresh Cycle**

In general, the HBM device requires REFRESH cycles at an average periodic interval of  $t_{REFI}$ . To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 REFRESH commands can be postponed during operation of the HBM device, meaning that at no point in time more than a total of 8 REFRESH commands are allowed to be postponed. In case that 8 REFRESH commands are postponed in a row, the resulting maximum interval between the surrounding REFRESH commands is limited to  $9 \times t_{REFI}$  (see [Figure 28](#)). A maximum of 8 additional REFRESH commands can be issued in advance (“pulled in”), with each one reducing the number of regular REFRESH commands required later by one. Note that pulling in more than 8 REFRESH commands in advance does not further reduce the number of regular REFRESH commands required later, so that the resulting maximum interval between two surrounding REFRESH commands is limited to  $9 \times t_{REFI}$  (see [Figure 29](#)). At any given time, a maximum of 16 REFRESH commands can be issued within  $2 \times t_{REFI}$ .

### 6.2.3.5 REFRESH Command (REF) (cont'd)

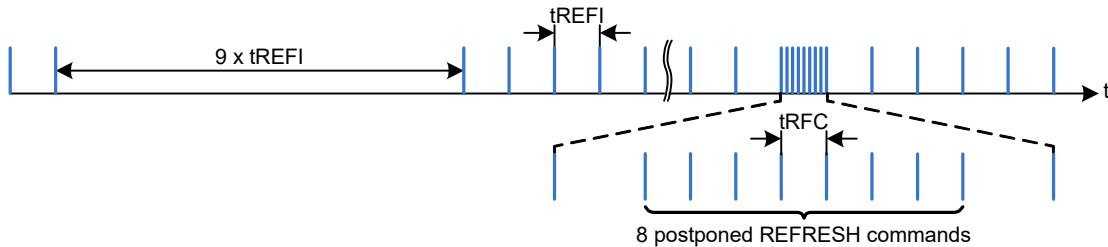


Figure 28 — Postponing Refresh Commands (Example)

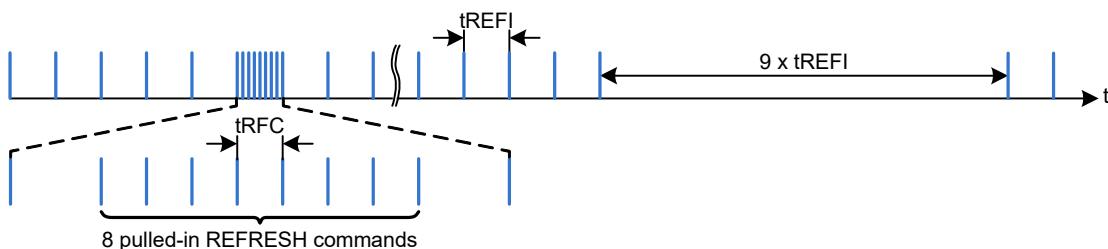


Figure 29 — Pulling-In Refresh Commands (Example)

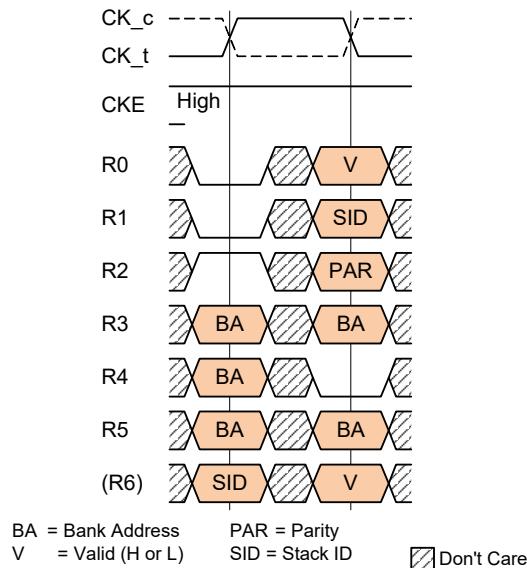
Self refresh mode may be entered with a maximum of eight REFRESH commands being postponed. After exiting self refresh mode with one or more REFRESH commands postponed, additional REFRESH commands may be postponed to the extent that the total number of postponed REFRESH commands (before and after the self refresh) will never exceed eight. During self refresh mode, the number of postponed or pulled-in REFRESH commands does not change.

### 6.3.2.6 SINGLE BANK REFRESH Command (REFSB)

The SINGLE BANK REFRESH command provides an alternative solution for the refresh of the HBM device. The command initiates a refresh cycle on a single bank while accesses to other banks including writes and reads are not affected. The command is received on the row command inputs R[6:0] or R[5:0] as shown in Figure 30.

Parity is evaluated with the SINGLE BANK REFRESH command when the parity calculation is enabled in the Mode Register.

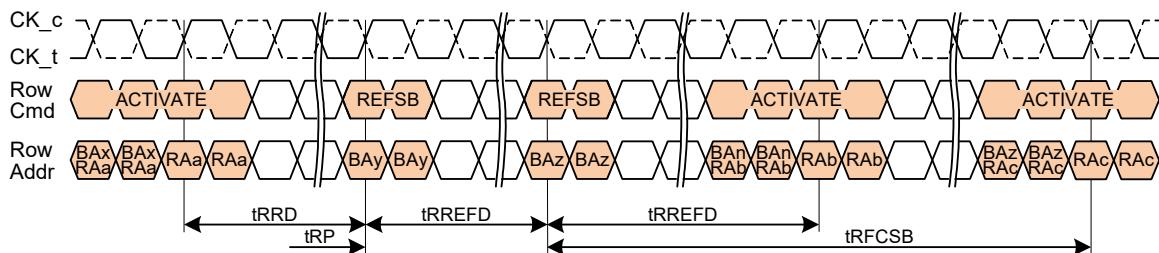
### 6.3.2.6 SINGLE BANK REFRESH Command (REFSB) (cont'd)



**Figure 30 — SINGLE BANK REFRESH Command**

The SINGLE BANK REFRESH command is nonpersistent, so it must be issued each time a refresh is required.

A minimum time  $t_{RRD}$  is required between an ACTIVATE command and a SINGLE BANK REFRESH command to a different bank. A minimum time  $t_{RREFD}$  is required between any two SINGLE BANK REFRESH commands (see below for an exception requiring  $t_{RFCSD}$ ), and between a SINGLE BANK REFRESH command and an ACTIVATE command to a different bank as shown in [Figure 31](#). A minimum time  $t_{RFCSD}$  is required between a SINGLE BANK REFRESH command and an access command to the same bank that follows. The selected bank must be precharged with  $t_{RP}$  satisfied prior to the SINGLE BANK REFRESH command. The bank is in idle state after completion of the SINGLE BANK REFRESH command.



1.  $BAn.x,y,z$  = bank address n,x,y,z;  $RAa,b,c$  = row address a,b,c.
2.  $t_{RRD}$  timing must be met between ACTIVATE commands and REFSB command to different banks.
3.  $t_{RREFD}$  timing must be met between consecutive REFSB commands to different banks, and between a REFSB command followed by an ACTIVATE command to the different bank.
4.  $t_{RFCSD}$  timing must be met between a REFSB command followed by an ACTIVATE command to the same bank.

**Figure 31 — Single Bank Refresh Command Cycle**

### 6.3.2.6 SINGLE BANK REFRESH Command (REFSB) (cont'd)

The row address for each bank is provided by internal refresh counters. This makes the row address bits “Don’t Care” during SINGLE BANK REFRESH commands.

A SINGLE BANK REFRESH command to one of the 8, 16, 32 or 48 (32 or 48 banks for HBM configurations with SID) banks can be issued in any order. After all banks have been refreshed using the SINGLE BANK REFRESH command and after waiting for at least  $t_{RFCSB}$ , the controller can issue another set of SINGLE BANK REFRESH commands in the same or different order. However, it is illegal to send another SINGLE BANK REFRESH command to a bank unless all banks have been refreshed using the SINGLE BANK REFRESH command. The controller must track the bank being refreshed by the SINGLE BANK REFRESH command.

The bank count is synchronized between the controller and the HBM device by resetting the bank count to zero. Synchronization can occur upon exit from reset state or by issuing a REFRESH or SELF REFRESH ENTRY command. Both commands may be issued at any time even if a preceding sequence of SINGLE BANK REFRESH commands has not completed cycling through all banks.

The example in [Table 34](#) (with 16 banks shown as an example) shows two full sets of REFSB commands with the bank counter reset to 0 and the refresh counter incremented after 16 REFSB commands each. The 3rd set of REFSB commands is interrupted by the REFRESH command which resets the bank counter to 0 and performs refreshes to all banks indicated by the refresh counter.

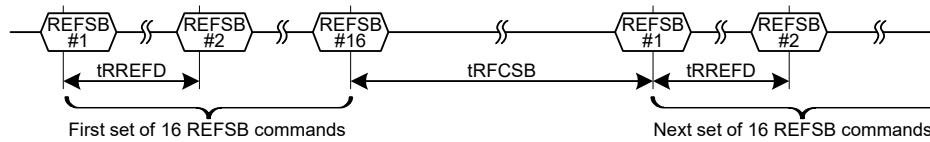
**Table 34 — Refresh Counter Increments**

COUNT	SUB-COUNT	COMMAND	BANK ADDR	REFRESH BANK	BANK COUNTER	REFRESH COUNTER
0	0	Reset, REFRESH or SRE command			To 0	
1	1	REFSB	0000	0	0 to 1	n
2	2	REFSB	0001	1	1 to 2	
3	3	REFSB	0010	2	2 to 3	
4	4	REFSB	0011	3	3 to 4	
...	...					
15	15	REFSB	1110	14	14 to 15	
16	16	REFSB	1111	15	15 to 0	
17	1	REFSB	0100	4	0 to 1	
18	2	REFSB	0111	7	1 to 2	
19	3	REFSB	1011	11	2 to 3	
20	4	REFSB	0110	6	3 to 4	
...	...					
31	15	REFSB	1100	12	14 to 15	
32	16	REFSB	0001	1	15 to 0	
33	1	REFSB	0010	2	0 to 1	n + 2
34	2	REFSB	1001	9	1 to 2	
35	3	REFSB	0000	0	2 to 3	
36	0	<b>REFRESH</b>	V	all	To 0	
37	1	REFSB	1010	10	0 to 1	n + 3
38	2	REFSB	0101	5	1 to 2	
...						

### 6.3.2.6 SINGLE BANK REFRESH Command (REFSB) (cont'd)

The average rate of SINGLE BANK REFRESH commands  $t_{REFISB}$  depends on the bank count N and can be calculated by the following formula:

$$t_{REFISB} = t_{REFI} / N.$$



**Figure 32 — Sets of Single Bank Refresh Commands (16-Bank HBM Devices assumed)**

**Table 35 — REFRESH and SINGLE BANK REFRESH Command Scheduling Requirements**

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN "FROM COMMAND" TO "TO COMMAND"	NOTE
REFRESH	REFRESH	$t_{RFC}$	
	SINGLE BANK REFRESH (any bank)	$t_{RFC}$	
	ACTIVATE	$t_{RFC}$	
SINGLE BANK REFRESH	REFRESH	$t_{RFCSB}$	
	SINGLE BANK REFRESH (different bank)	$t_{RREFD}$	
	SINGLE BANK REFRESH (any bank)	$t_{RFCSB}$	3
	ACTIVATE (same bank)	$t_{RFCSB}$	
	ACTIVATE (different bank with imPRE)	Max $\{(t_{RREFD} - t_{RP}), 4 t_{CK}\}$	1
	ACTIVATE (different bank without imPRE)	$t_{RREFD}$	1
ACTIVATE	REFRESH	$t_{RC}$	2
	SINGLE BANK REFRESH (same bank)	$t_{RC}$	2
	SINGLE BANK REFRESH (different bank)	$t_{RRD}$	1
ACTIVATE with imPRE	REFRESH	$t_{RC} + t_{RP}$	2
	SINGLE BANK REFRESH (same bank)	$t_{RC} + t_{RP}$	2
	SINGLE BANK REFRESH (different bank)	$t_{RRD} + t_{RP}$	1

NOTE 1  $t_{FAW}$  parameter must be observed as well.  
 NOTE 2 A bank must be in the idle state with  $t_{RP}$  satisfied before it is refreshed.  
 NOTE 3  $t_{RFCSB}$  parameter must be observed when the first RFSB command completes a set of 8, 16, 32 or 48 single bank refresh operations and the second RFSB command initiates the next set of 8, 16, 32 or 48 single bank refresh operations.

### 6.3.3 Column Commands

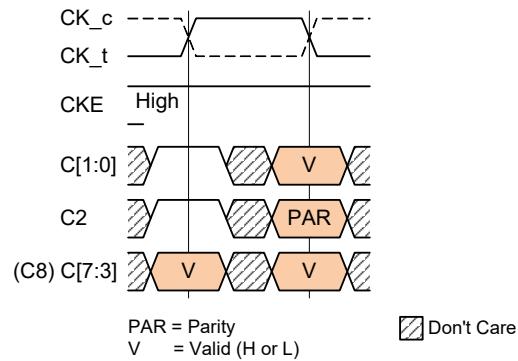
The column commands consist of NOP, Read, Read with Auto Precharge, Write, Write with Auto Precharge, and MRS. The column commands utilize C[8:0] or C[7:0] inputs. All column commands are transmitted in a single clock cycle.

#### 6.3.3.1 Column No Operation Command (CNOP)

The COLUMN NO OPERATION (CNOP) command as shown in [Figure 33](#) is used to instruct the HBM device to perform a NOP as column command; this prevents unwanted column commands from being registered during idle or wait states. Operations already in progress are not affected.

Parity is evaluated on all C[8:0] or C[7:0] inputs when the parity calculation is enabled in the MR0.

CNOP is assumed on subsequent timing diagrams unless other column commands are explicitly shown.

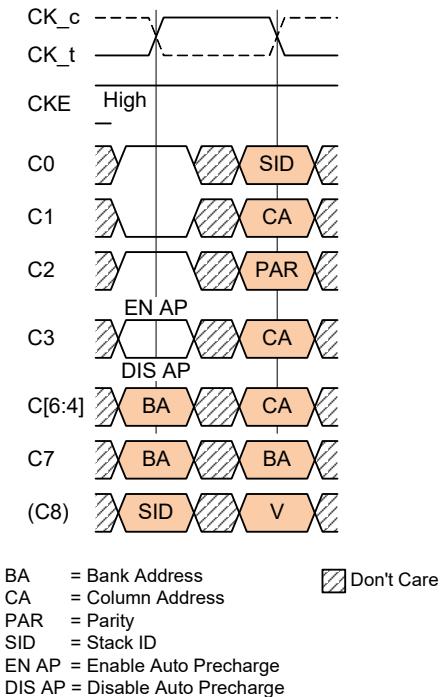


**Figure 33 — CNOP Command**

### 6.3.3.2 Read Command (RD, RDA)

A read burst is initiated with a READ command as shown in [Figure 34](#). The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the READ command when the parity calculation is enabled in the Mode Register.



**Figure 34 — READ Command**

The length of the burst initiated with a READ command is either two or four, depending on the burst length programmed in the BL field of MR3 OP7 (see [Table 12](#)). The column address is unique for this burst of two or four. There is no interruption nor truncation of read bursts.

The read latency (RL) is defined from the rising CK edge on which the READ command is issued to the rising CK edge from which the t<sub>DQSCK</sub> delay is measured, with the number of clock cycles as programmed in the ERL bit in MR4 OP5 and the RL field of MR2 OP[7:3] (see [Table 11](#)). The first valid data is available RL × t<sub>CK</sub> + t<sub>DQSCK</sub> + t<sub>DQSQ</sub> after the rising CK edge when the READ command was issued.

The output drivers are enabled and begin driving either HIGH or LOW nominally two clock cycles (odd bytes) and one clock cycle (even bytes) prior to the first valid data bit. See [Read Operation](#) under [DBIac States](#) section for bus pre-conditioning with RDBI enabled and disabled modes on a first READ command.

The output drivers will drive Hi-Z nominally one half clock cycle after the completion of the burst provided no other READ command has been issued.

The read data strobe provides a fixed one-cycle preamble and fixed one-cycle postamble; the first RDQS edge occurs (RL-1) × t<sub>CK</sub> + t<sub>DQSCK</sub> after the rising CK edge when the READ command was issued. The first data bit of the read burst is synchronized with the second rising edge of the RDQS strobe. Each subsequent data-out is edge-aligned with the data strobe. Pin timings for the data strobe are measured relative to the crosspoint of RDQS\_t and its complement, RDQS\_c.

### 6.3.3.2.1 Clock to Read Data Strobe Timings

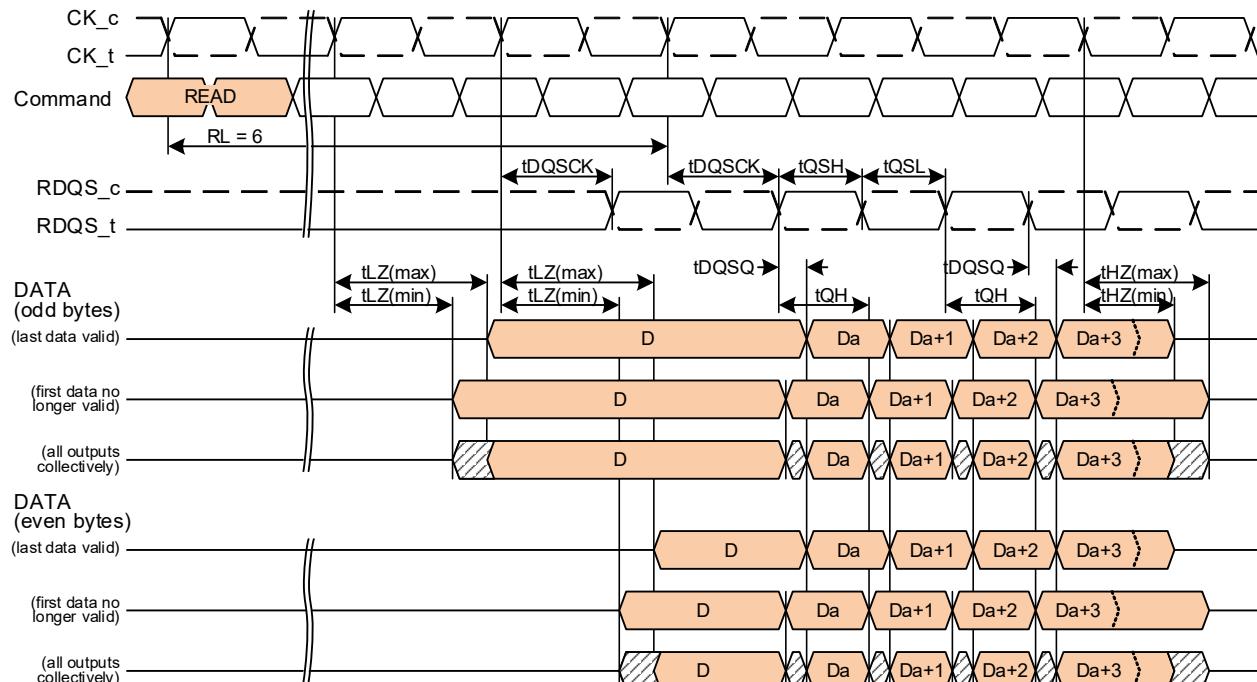
The clock to read data strobe (RDQS) relationship is shown in [Figure 35](#). Related parameters:

- $t_{DQSCK}(\min/\max)$  describes the allowed range for a rising or falling RDQS edge relative to CK.
- $t_{DQSCK}$  is the actual position of a RDQS edge relative to CK.
- $t_{QSH}$  describes the RDQS HIGH pulse width.
- $t_{QSL}$  describes the RDQS LOW pulse width.
- $t_{LZ}(\min/\max)$  describe the allowed range for the data output Hi-Z to low impedance transition relative to CK.
- $t_{HZ}(\min/\max)$  describe the allowed range for the data output low impedance to Hi-Z transition relative to CK.

### 6.3.3.2.2 Read Data Strobe and Data Out Timings

The read data strobe (RDQS) to data out (DQ, DM, DBI) relationship is shown in [Figure 35](#). Related parameters:

- $t_{DQSQ}$  describes the latest valid transition of any associated DQ or DM or DBI pin for both rising and falling RDQS edges.
- $t_{QH}$  describes the earliest invalid transition of any associated DQ or DM or DBI pin for both rising and falling RDQS edges.

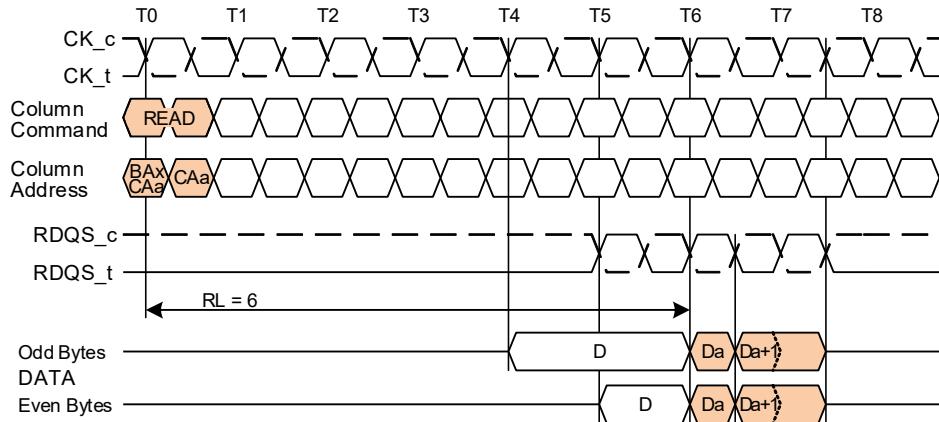


1.  $t_{DQSCK}$  may span multiple clock periods.
  2. A burst length of 4 is shown.
  3. Early/late data transition of a DQ or DM or DBI can vary within a burst.
  4.  $D, a, a+1, a+2, a+3$  = data-out for READ command a.
- D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).

**Figure 35 — Clock to RDQS and Data Out Timings**

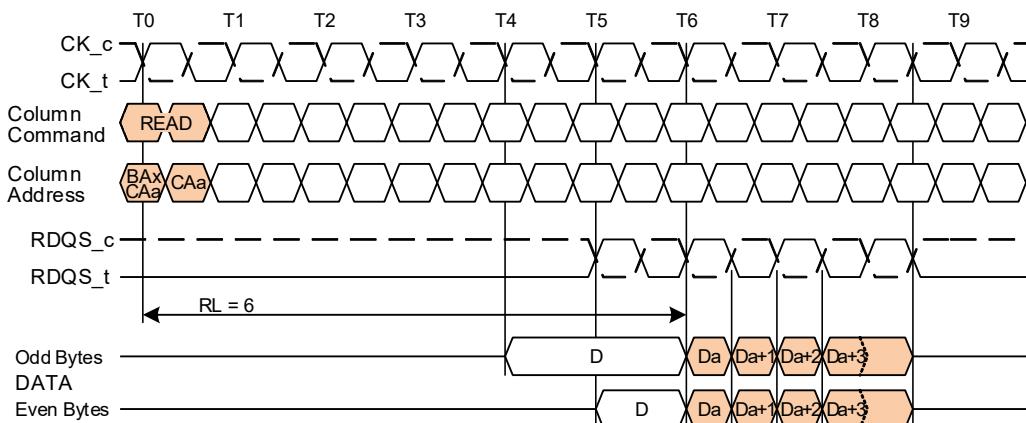
### 6.3.3.2.3 Read Operation

Single read bursts are shown in [Figure 36](#) for BL=2 and [Figure 37](#) for BL=4.



1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. RL = 6 is shown as an example.
3. RDQS = RDQS0..RDQS3; DATA = DQ0..DQ127, DBI0..DBI15.
4. Da,a+1 = data-out for READ command a.
5. D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
6. tDQSCK = 0 and nominal tLZ, tHZ is shown for illustration purposes.
7. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 36 — Single Read Burst with BL=2**

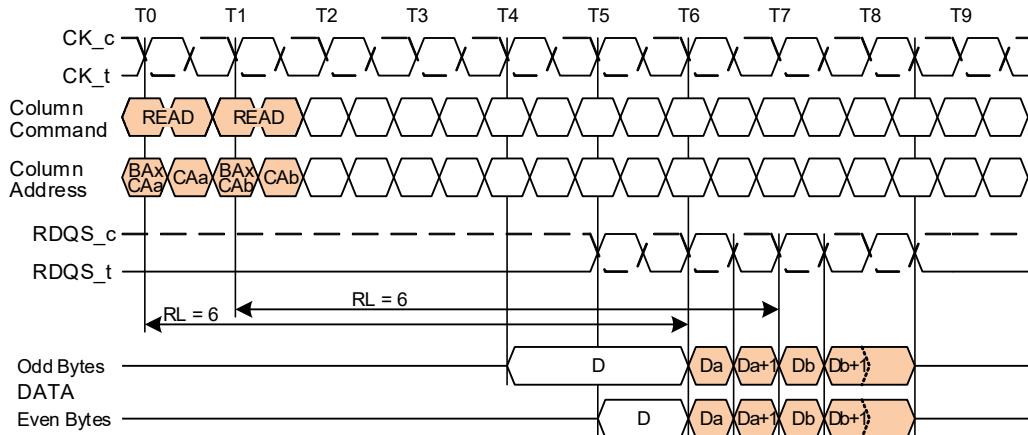


1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. RL = 6 is shown as an example.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DBI[15:0].
4. Da,a+1,a+2,a+3 = data-out for READ command a.
5. D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
6. tDQSCK = 0 and nominal tLZ, tHZ is shown for illustration purposes.
7. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 37 — Single Read Burst with BL=4**

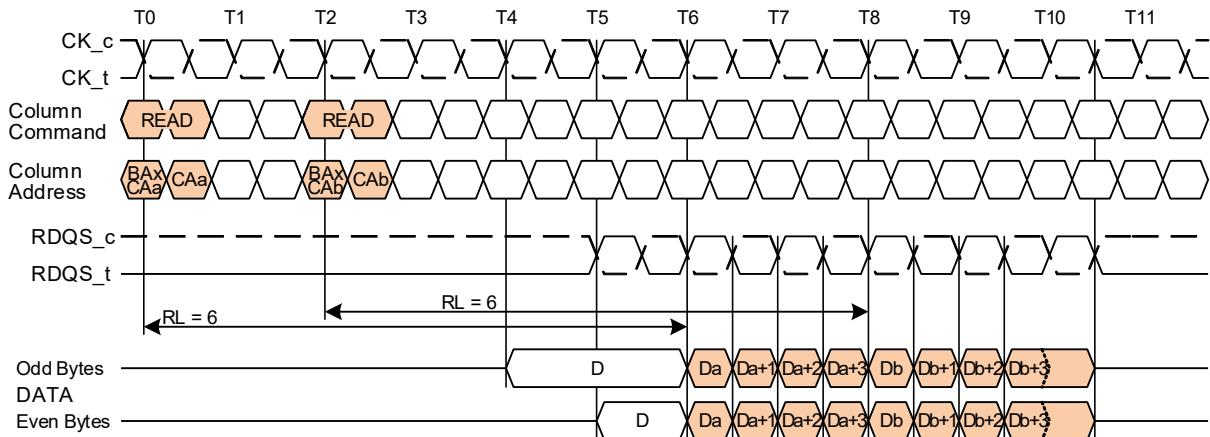
Data from any read burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained as shown in [Figure 38](#) for BL=2 and [Figure 39](#) for BL=4. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t<sub>CCD</sub> timing and the programmed burst length (BL). If that READ command is to another idle bank then an ACTIVATE command must precede the READ command and t<sub>RCDRD</sub> also must be met.

### 6.3.3.2.3 Read Operation (cont'd)



1.  $BA_x$  = bank address  $x$ ;  $CA_{a,b}$  = column address  $a,b$ .
2.  $RL = 6$  is shown as an example.
3.  $RDQS = RDQS[3:0]$ ;  $DATA = DQ[127:0]$ ,  $DM[15:0]$ ,  $DBI[15:0]$ .
4.  $Da, Da+1, Db, Db+1$  = data-out for READ commands  $a,b$ .  
 $D$  = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5.  $tDQSCK$ ,  $tLZ$ ,  $tHZ = 0$  is shown for illustration purposes.
6. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 38 — Seamless Read Bursts with  $BL=2$**



1.  $BA_x$  = bank address  $x$ ;  $CA_{a,b}$  = column address  $a,b$ .
2.  $RL = 6$  is shown as an example.
3.  $RDQS = RDQS[3:0]$ ;  $DATA = DQ[127:0]$ ,  $DM[15:0]$ ,  $DBI[15:0]$ .
4.  $Da, Da+1..Da+3, Db, Db+1..Db+3$  = output data for READ commands  $a,b$ .  
 $D$  = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5.  $tDQSCK$ ,  $tLZ$ ,  $tHZ = 0$  is shown for illustration purposes.
6. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 39 — Seamless Read Bursts with  $BL=4$**

Examples of non-seamless read bursts with  $BL=2$  are shown in [Figure 40](#) for  $t_{CCD}=2$  and [Figure 41](#) for  $t_{CCD}=4$ . The RDQS cycle at clock edge T7 in [Figure 40](#) represents the read postamble of the first read burst as well as the read preamble of the second read burst. The chosen  $t_{CCD}$  value leads to a continuous series of RDQS pulses over both read bursts, and the data bus does not return to Hi-Z between the read bursts.

With  $t_{CCD}=4$  as shown in [Figure 41](#) the timing of each of the two read bursts is identical to a single read burst as shown in [Figure 36](#). The data bus returns to Hi-Z between the read bursts, and the last data out of the first read burst ( $Da+1$ ) is re-driven at clock edge T8 (for odd bytes) and T9 (for even bytes) preceding the second read burst.

### 6.3.3.2.3 Read Operation (cont'd)

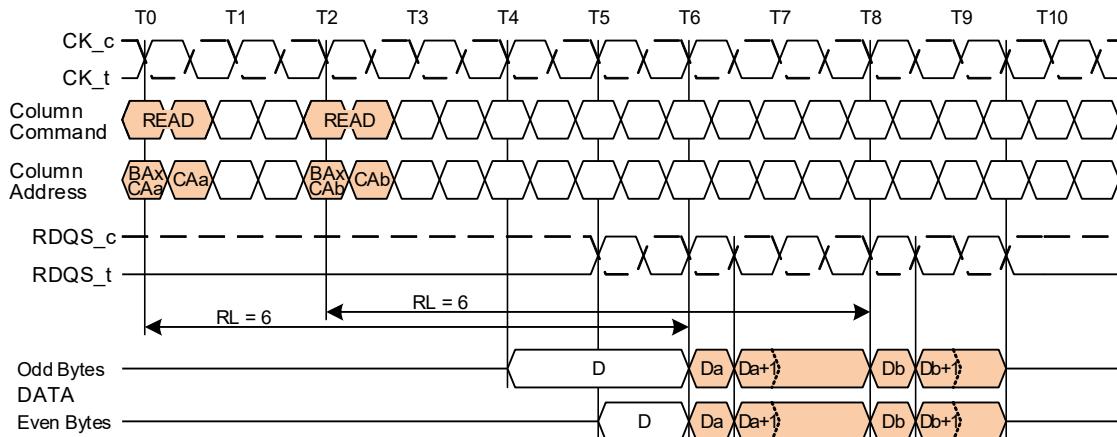


Figure 40 — Non-Seamless Read Bursts with  $t_{CCD}=2$  and  $BL=2$

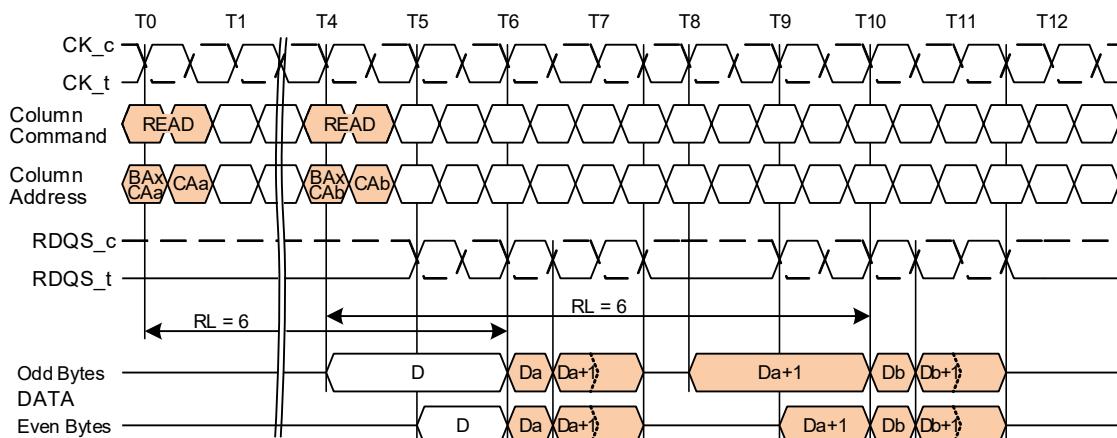
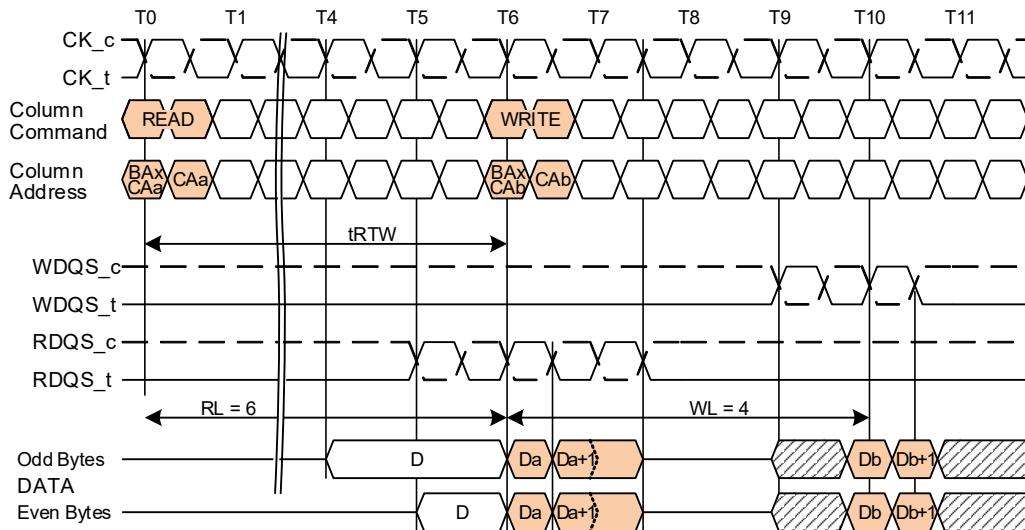


Figure 41 — Non-Seamless Read Bursts with  $t_{CCD}=4$  and  $BL=2$

### 6.3.3.2.3 Read Operation (cont'd)

A WRITE can be issued any time after a READ command as long as the bus turn around time  $t_{RTW}$  is met as shown in Figure 42 for BL=2. If that WRITE command is to another idle bank, then an ACTIVATE command must precede the WRITE command and  $t_{RCDWR}$  also must be met.

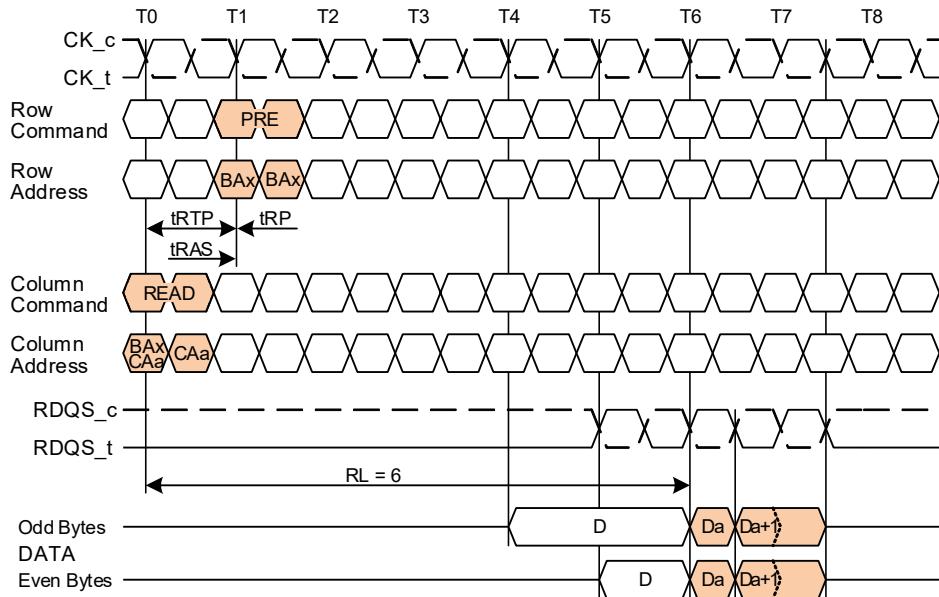


1.  $BAx$  = bank address  $x$ ;  $CAa$  = column address  $a$ .
2.  $RL=6$  and  $WL=4$  are shown as examples.
3.  $RDQS = RDQS[3:0]$ ;  $WDQS = WDQS[3:0]$ ;  $DATA = DQ[127:0]$ ,  $DM[15:0]$ ,  $DBI[15:0]$ .
4.  $Da,a+1$  = data-out for READ command  $a$ .
5.  $D$  = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
6.  $tDQSCK$ ,  $tDQSS = 0$  and nominal  $tLZ$ ,  $tHZ$  is shown for illustration purposes.
7.  $tRTW$  is not a device limit but determined by the system bus turnaround time.
8. RDBI and WDBI could be on or off. RDBI is controlled with MR0 OP0, and WDBI is controlled with MR0 OP1.

Figure 42 — Read to Write

### 6.3.3.2.3 Read Operation (cont'd)

A PRECHARGE can be issued  $t_{RTP}$  after the READ command as shown in [Figure 43](#) for BL=2. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until  $t_{RP}$  is met.



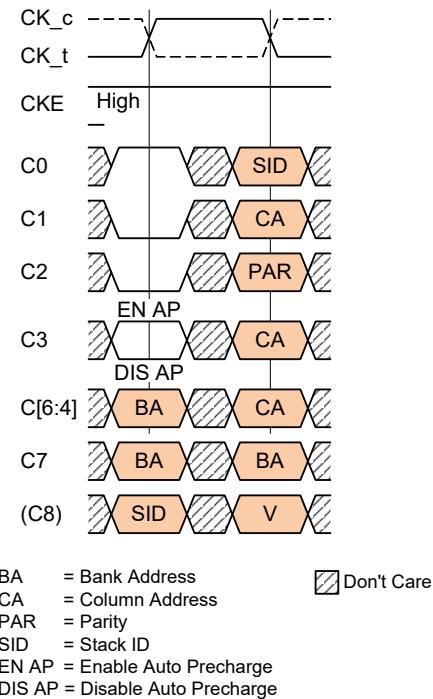
1. BAx = bank address x; CAa = column address a.
2. RL = 6 is shown as an example.
3. RDQS = RDQS0..RDQS3; DATA = DQ0..DQ127, DBI0..DBI15.
4. Da,a+1 = data-out for READ command a.  
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK = 0 and nominal tLZ, tHZ is shown for illustration purposes.
6. tRTP = 1 nCK is shown as an example. tRTP = tRTPL when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise tRTP = tRTPS.
7. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 43 — Read to Precharge**

### 6.3.3.3 Write Command (WR, WRA)

A Write burst is initiated with a WRITE command as shown in [Figure 44](#). The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access.

Parity is evaluated with the WRITE command when the parity calculation is enabled in MR0 ([Table 9](#)).



**Figure 44 — WRITE Command**

The length of the burst initiated with a WRITE command is either two or four, depending on the burst length programmed in the BL field of MR3 OP7. The column address is unique for this burst of two or four. There is no interruption nor truncation of Write bursts.

The write latency (WL) is defined from the rising CK edge on which the WRITE command is issued to the rising CK edge from which the t<sub>DQSS</sub> delay is measured, with the number of clock cycles as programmed in the EWL bit in MR4 OP4 and the WL field of MR2 OP[2:0]. The first valid data must be driven WL × t<sub>CK</sub> + t<sub>DQSS</sub> after the rising CK edge when the WRITE command was issued.

The write data strobe provides a fixed one-cycle preamble and no postamble; the first WDQS edge must be driven (WL-1) × t<sub>CK</sub> + t<sub>DQSS</sub> after the rising CK edge when the WRITE command was issued. The first data-in of the write burst must be driven center-aligned with the second rising edge of the WDQS strobe. Each subsequent data-in must be applied center-aligned with the data strobe edges. Pin timings for the data strobe are measured relative to the crosspoint of WDQS\_t and its complement, WDQS\_c.

#### 6.3.3.3.1 Clock to Write Data Strobe Timings

The clock to write data strobe (WDQS) relationship is shown in [Figure 45](#). Related parameters:

- t<sub>DQSS(min/max)</sub> describes the allowed range for a rising or falling WDQS edge relative to CK.
- t<sub>DQSS</sub> is the actual position of a WDQS edge relative to CK.
- t<sub>DQSH</sub> describes the WDQS HIGH pulse width.
- t<sub>DQSL</sub> describes the WDQS LOW pulse width.

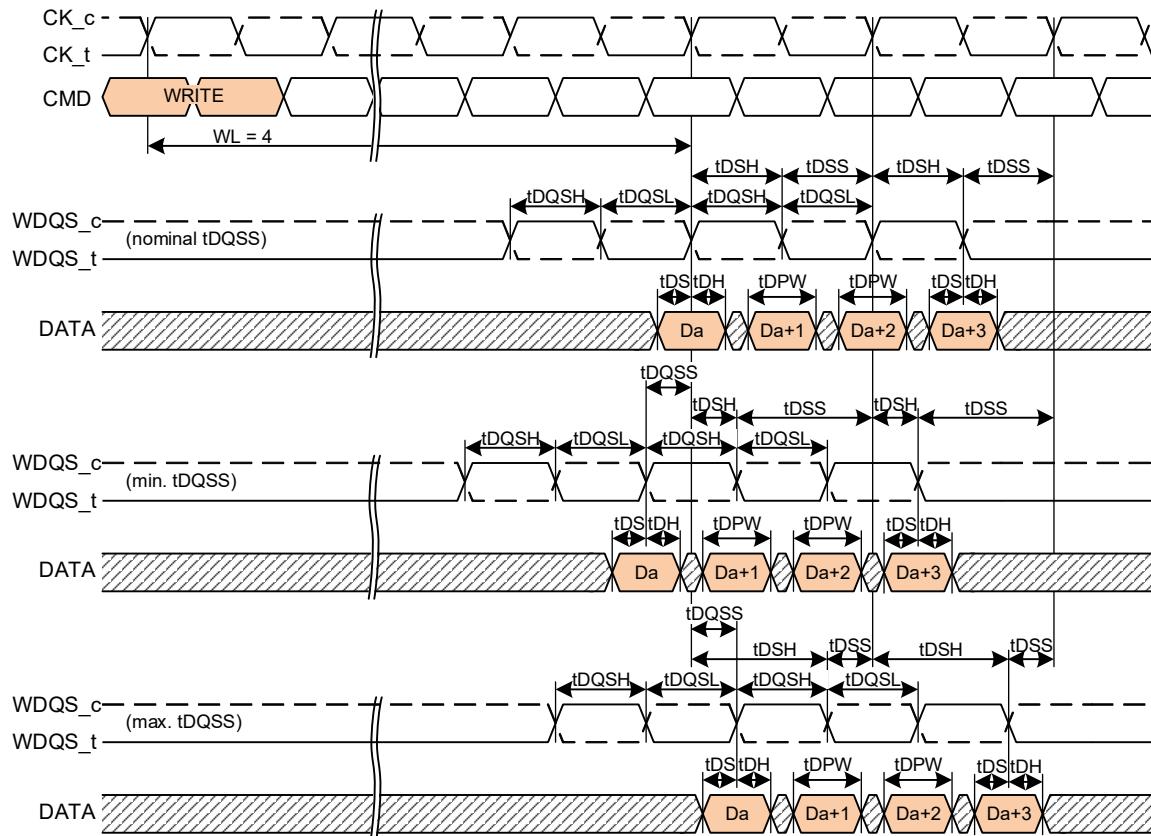
### 6.3.3.3.1 Clock to Write Data Strobe Timings (cont'd)

- $t_{DSS}$  describes falling WDQS edge to rising clock edge setup time.
- $t_{DSH}$  describes falling WDQS edge from rising clock edge hold time.

### 6.3.3.3.2 Write Data Strobe and Data In Timings

The write data strobe (WDQS) to data in relationship is shown in [Figure 45](#). Related parameters:

- $t_{DS}$  describes the required setup time of any associated input data pin for both rising and falling WDQS edges.
- $t_{DH}$  describes the required hold time of any associated input data pin for both rising and falling WDQS edges.

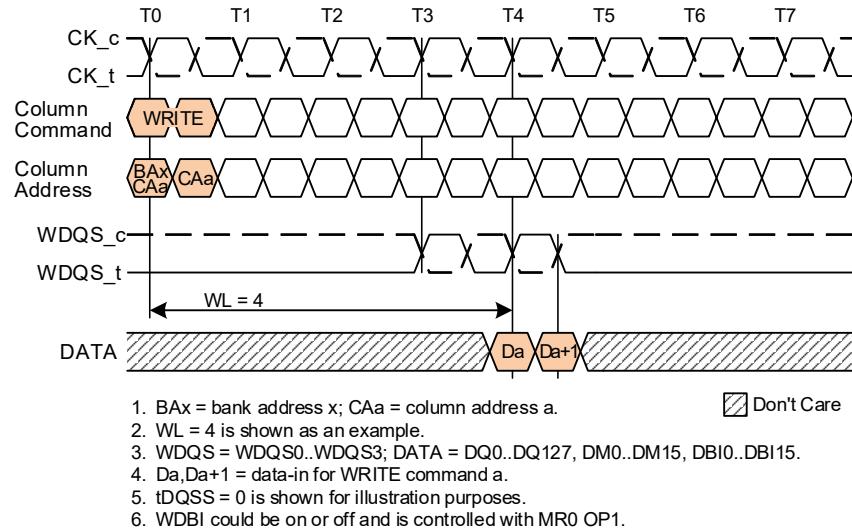


1. A burst length of 4 is shown.
2.  $t_{DS}$ ,  $t_{DH}$ ,  $t_{DPW}$  apply to each input individually.
3. DATA = DQ[127:0], DM[15:0], DBI[15:0].
4. Da, Da+1, Da+2, Da+3 = data-in for WRITE command a.

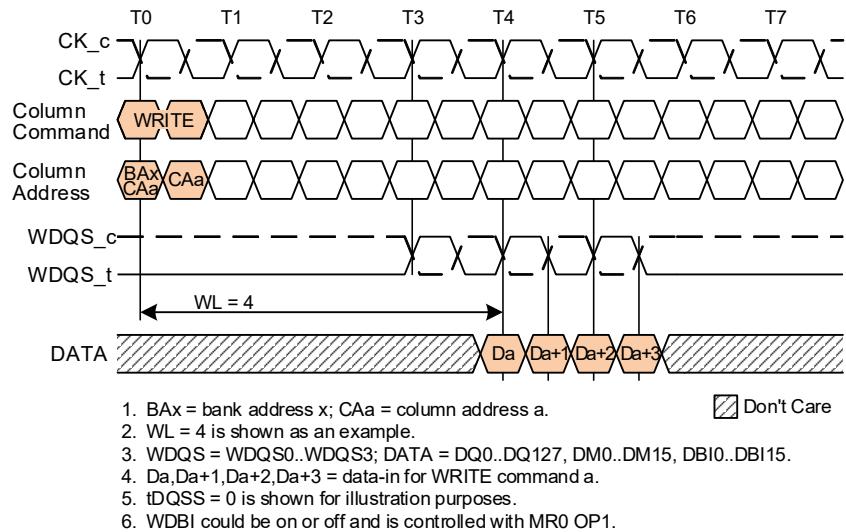
**Figure 45 — Clock to WDQS and Data Input Timings**

### 6.3.3.3.3 Write Operation

Single write bursts are shown in [Figure 46](#) for BL=2 and [Figure 47](#) for BL=4.



**Figure 46 — Single Write Burst with BL=2**



**Figure 47 — Single Write Burst with BL=4**

Data from any write burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained as shown in [Figure 48](#) for BL=2 and [Figure 49](#) for BL=4. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the  $t_{CCD}$  timing and the programmed burst length (BL). If that WRITE command is to another idle bank then an ACTIVE command must precede the WRITE command and  $t_{RCDWR}$  also must be met.

### 6.3.3.3.3 Write Operation (cont'd)

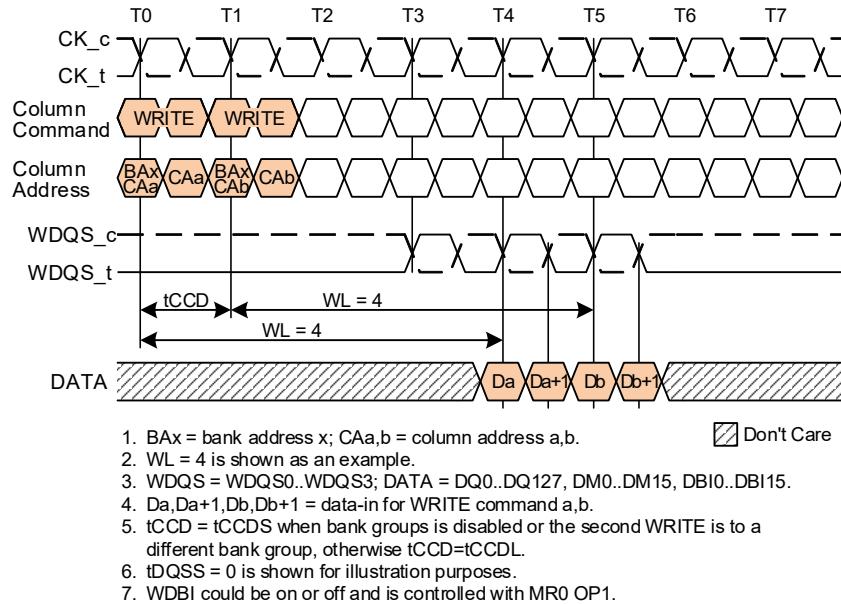


Figure 48 — Seamless Write Bursts with BL=2

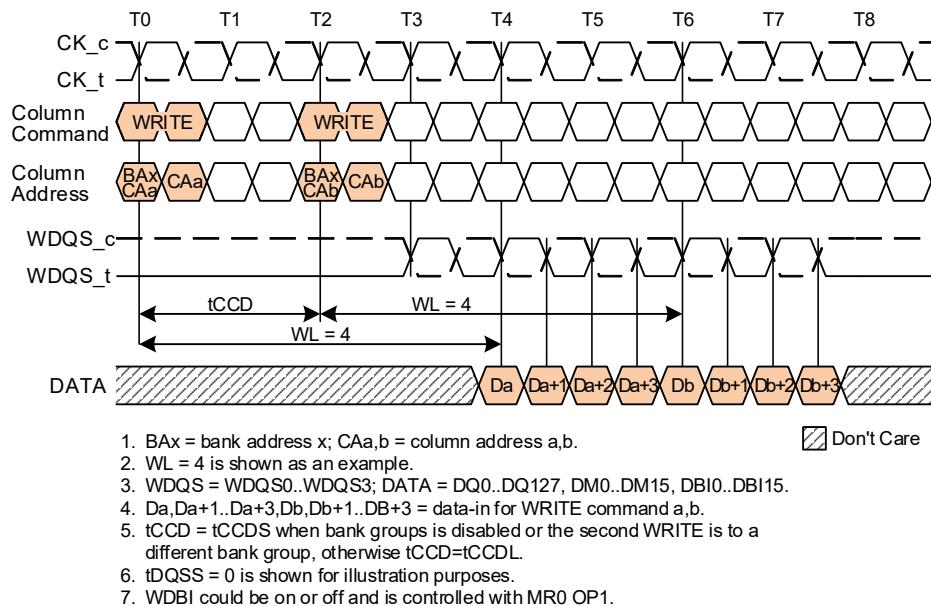
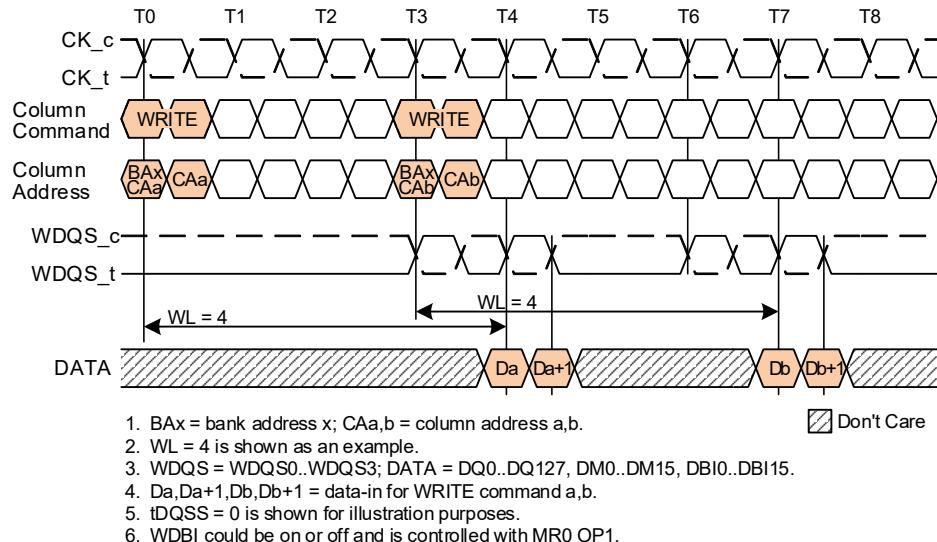


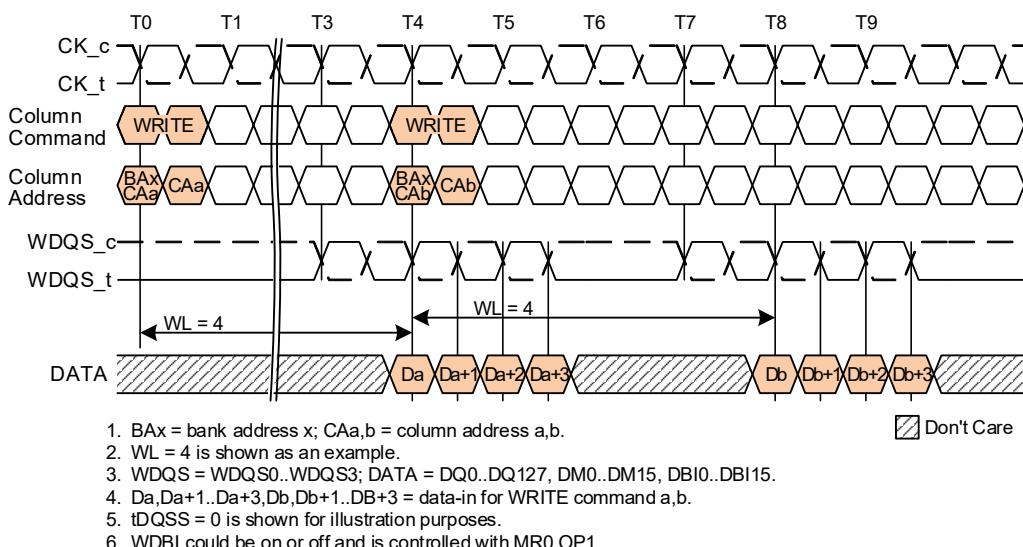
Figure 49 — Seamless Write Bursts with BL=4

### 6.3.3.3.3 Write Operation (cont'd)

Examples of non-seamless write bursts are shown in [Figure 50](#) for BL=2 and [Figure 51](#) for BL=4.



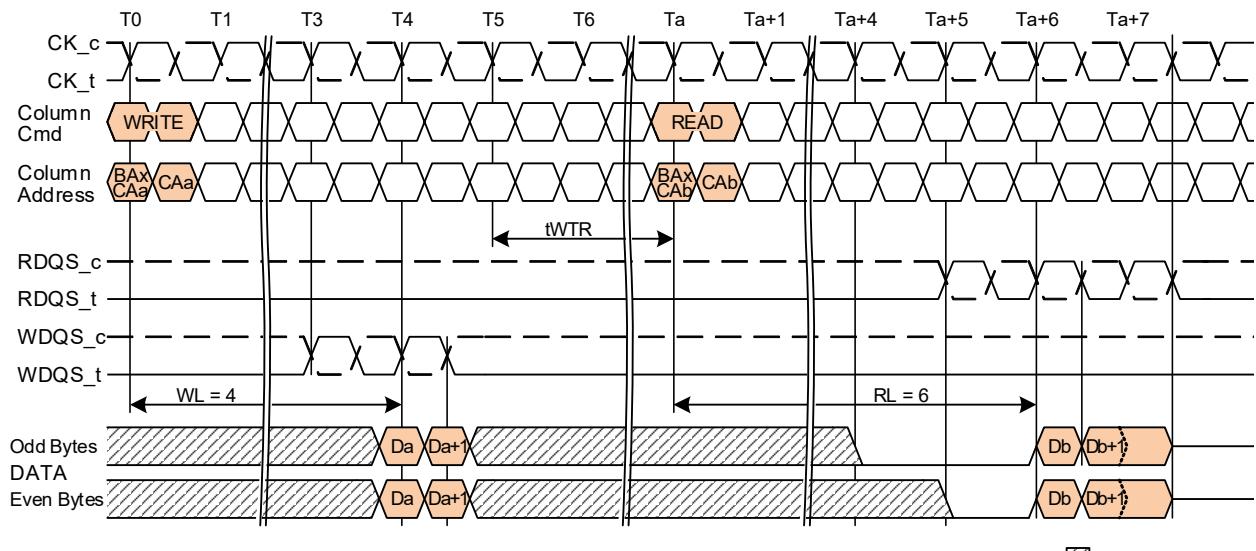
**Figure 50 — Non-Seamless Write Bursts with BL=2**



**Figure 51 — Non-Seamless Write Bursts with BL=4**

### 6.3.3.3.3 Write Operation (cont'd)

A READ can be issued any time after a WRITE command as long as the bus turn around time  $t_{WTR}$  is met as shown in Figure 52 for BL=2. If that READ command is to another idle bank, then an ACTIVATE command must precede the READ command and  $t_{RCDRD}$  also must be met. The bus is preconditioned for the first read burst by being driven LOW two clock cycles (even bytes) and one clock cycle (odd bytes) prior to the first valid data element of the read burst when RDBI is enabled in MR0 OP0. When RDBI is disabled the HBM device does not precondition the bus.

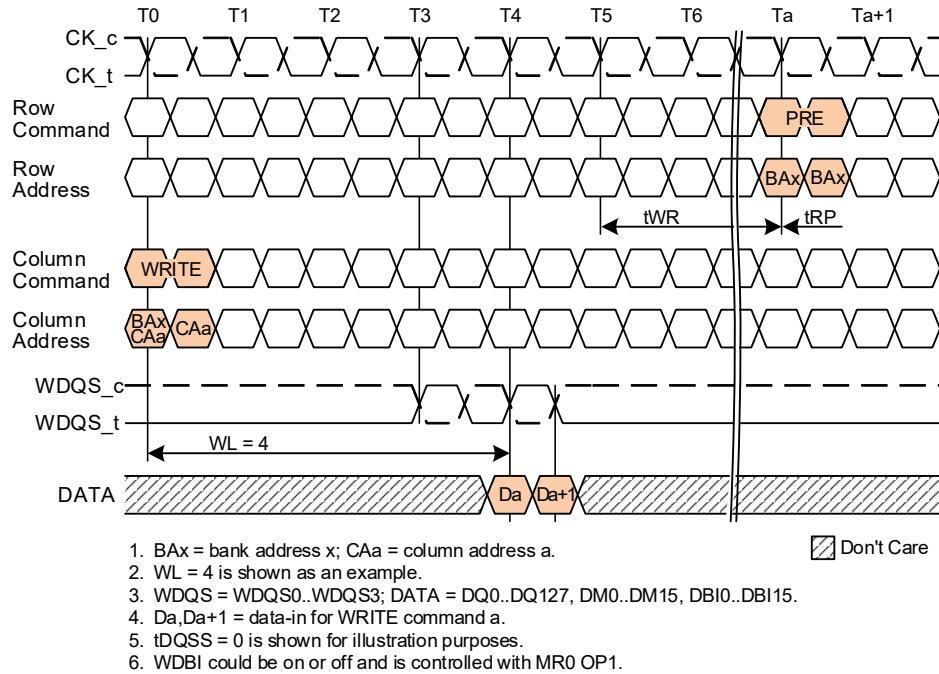


1. BA<sub>x</sub> = bank address x; CA<sub>a,b</sub> = column address a,b.
2. WL = 4 and RL = 6 are shown as examples.
3. RDQS = RDQS[3:0]; WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0].
4. Db,b+1 = data-in for WRITE command b. Da,a+1 = data-out for READ command a.
5. tDQSCK, tDQSS = 0 and nominal tLZ, tHZ is shown for illustration purposes.
6. tWTR = tWTRL when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise tWTR = tWTRS.
7. WDBI could be on or off and is controlled with MR0 OP1.
8. READ operation shown with RDBI enabled. RDBI is enabled/disabled with MR0 OP0.

Figure 52 — Write to Read

### 6.3.3.3.3 Write Operation (cont'd)

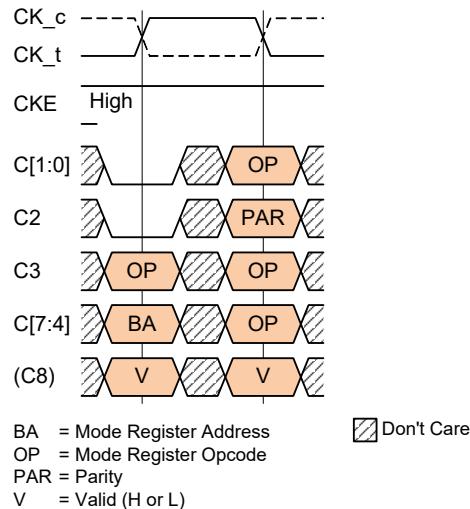
The write recovery time  $t_{WR}$  must have elapsed before a PRECHARGE command can be issued to that bank as shown in [Figure 53](#) for BL=2; the  $t_{WR}$  interval begins with the completion of the write burst at  $WL + BL/2$  clock cycles after the WRITE command was issued. Also,  $t_{RAS}$  must be met when the PRECHARGE is issued. After the PRECHARGE command, a subsequent ACTIVATE command to the same bank cannot be issued until  $t_{RP}$  is met.



**Figure 53 — Write to Precharge**

### 6.3.3.4 Mode Register Set (MRS)

The MODE REGISTER SET (MRS) command is used to load the Mode Registers of the HBM device. The command is received on the column command inputs C[8:0] as shown in [Figure 54](#) and requires a RNOP command on the row command inputs R[6:0].

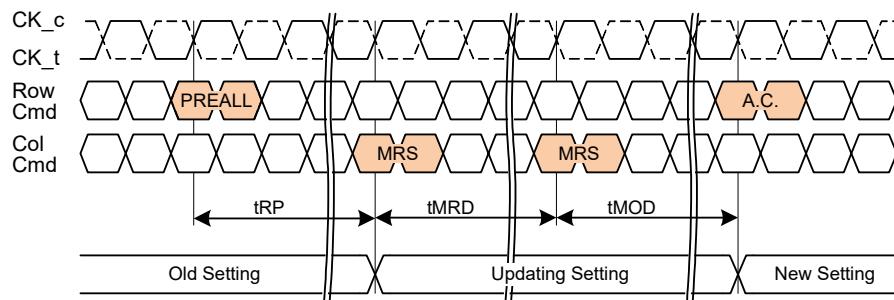


**Figure 54 — MODE REGISTER SET Command**

Inputs BA[3:0] select the Mode Register, and the inputs OP[7:0] determine the op-code to be loaded. See HBM Mode Register Overview ([Table 8](#)) for Mode Register definitions.

The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress. The MODE REGISTER SET command cycle time  $t_{MRD}$  is required to complete the write operation to the Mode Register and is the minimum time required between two MRS commands. The MRS command to Non-MRS command delay,  $t_{MOD}$ , is required by the HBM device to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding RNOP and CNOP.

Parity is evaluated on all R[6:0] and C[8:0] inputs when the parity calculation has already been enabled in the Mode Register prior to this MODE REGISTER SET command. When parity calculation is enabled by a MODE REGISTER SET command, the HBM requires all subsequent commands including RNOP and CNOP to be issued with correct parity until  $t_{MOD}$  has expired for the MODE REGISTER SET command that disables the parity calculation.



A.C. = any command allowed in bank idle state.

**Figure 55 — Mode Register Set Timings**

### 6.3.4 Power-Mode Commands

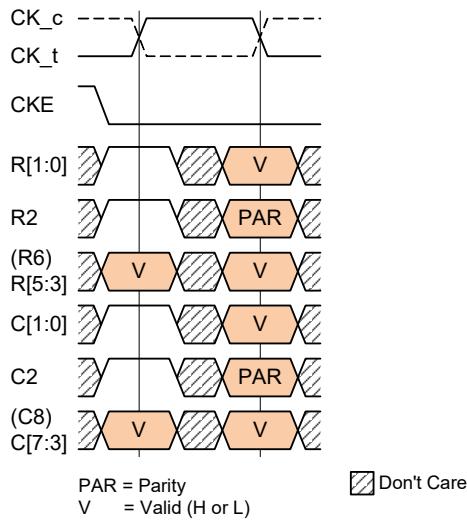
#### 6.3.4.1 Power-Down (PDE, PDX)

HBM devices require CKE to be HIGH at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For reads, a burst completion is defined as when the last data element has been transmitted on the data outputs, for writes, a burst completion is defined as when the last data element has been written to the memory array with  $t_{WR}$  satisfied.

Power-down is entered when CKE is registered LOW along with Rnop and Cnop commands as shown in [Figure 56](#).

CKE must not go LOW when read or write operations are in progress. A read operation is completed when the last data element including parity (when enabled) and RDQS postamble has been transmitted on the outputs. A write operation is completed when the last data element including parity (when enabled) has been written to the memory array with  $t_{WR}$  satisfied; for writes with auto-precharge, the number of clock cycles programmed in the mode register for WR must have elapsed instead.

CKE can go LOW while any other operations such as row activation, precharge, auto precharge, or refresh are in progress, but the power-down IDD specification will not apply until such operations are complete.



**Figure 56 — POWER-DOWN ENTRY Command**

If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK\_t, CK\_c, RESET\_n and CKE. To ensure that there is enough time to account for the internal delay on the CKE signal path, Rnop and Cnop commands are required for  $t_{CPDED}$  period after power-down entry.

While in power-down, CKE LOW must be maintained at the device inputs. The clock may be stopped or the clock frequency may be changed under the following conditions:

- The clock is held stable for  $t_{CKSRE}$  cycles and, in case of a preceding ACTIVATE, REFRESH or SINGLE BANK REFRESH command, until the number of clock cycles programmed in the Mode Register for RAS have elapsed;
- In case of clock stop CK\_t is held LOW and CK\_c is held HIGH;
- In case of a clock frequency change  $t_{CK}(\text{min})$  is met for each clock cycle;

### 6.3.4.1 Power-Down (PDE, PDX) (cont'd)

- The clock is stable with  $t_{CH}(\text{min})$  and  $t_{CL}(\text{min})$  satisfied at least  $t_{CKSRX}$  cycles prior to power-down exit.

No refresh operations are performed in power-down mode. The maximum duration in power-down mode is limited by the refresh requirements of the device.

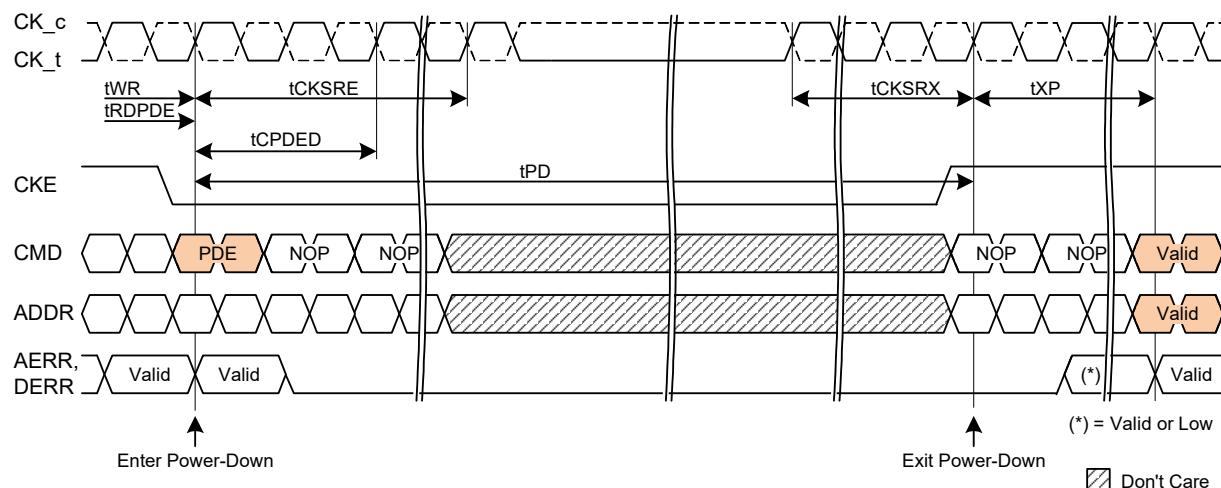
While in power-down the device will maintain the internal DBI state for the DBIac calculation when DBI is enabled in the Mode Register. It will also continue driving RDQS\_t and RDQS\_c to LOW and HIGH static levels, respectively, and TEMP and CATTRIP to valid HIGH or LOW levels.

Power-down is synchronously exited when CKE is registered HIGH (in conjunction with RNOP and CNOP commands). A valid executable command may be applied  $t_{XP}$  cycles later. The minimum power-down duration is specified by  $t_{PD}$ .

If enabled, parity is evaluated for the POWER-DOWN ENTRY command. The HBM device requires RNOP and CNOP commands with valid parity for the entire  $t_{CPDED}$  period, while it will suspend parity checking after power-down entry and drive AERR and DERR to a static LOW.

Parity is not evaluated for the POWER-DOWN EXIT command. The HBM device requires RNOP and CNOP commands with valid parity for the entire  $t_{XP}$  period, while within  $t_{XP}$  period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time.

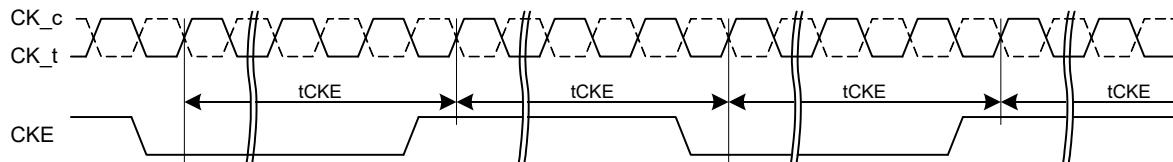
Power-down is entered when CKE is registered LOW along with RNOP and CNOP commands as shown in [Figure 57](#). RNOP and CNOP commands are required for  $t_{CPDED}$  period after power-down entry.



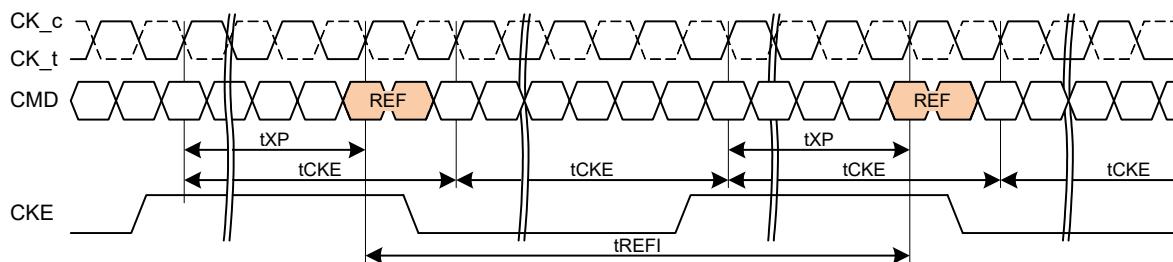
- Only RNOP and CNOP commands allowed during  $t_{CPDED}$  and  $t_{XP}$  periods.
- Write bursts must have been completed with  $tWR$  satisfied prior to power-down entry.
- Read bursts must have been completed with  $tRDPDE$  satisfied prior to power-down entry.
- Address inputs are „Don't Care“ for power-down entry and exit.
- AERR, DERR are driven LOW when parity check is suspended during power-down. Signals are shown with  $tPARAC=0$  and  $tPARAQ=0$  for illustration purpose.
- The CK clock may be stopped during power-down as shown, or toggling.

**Figure 57 — Power-Down Entry and Exit**

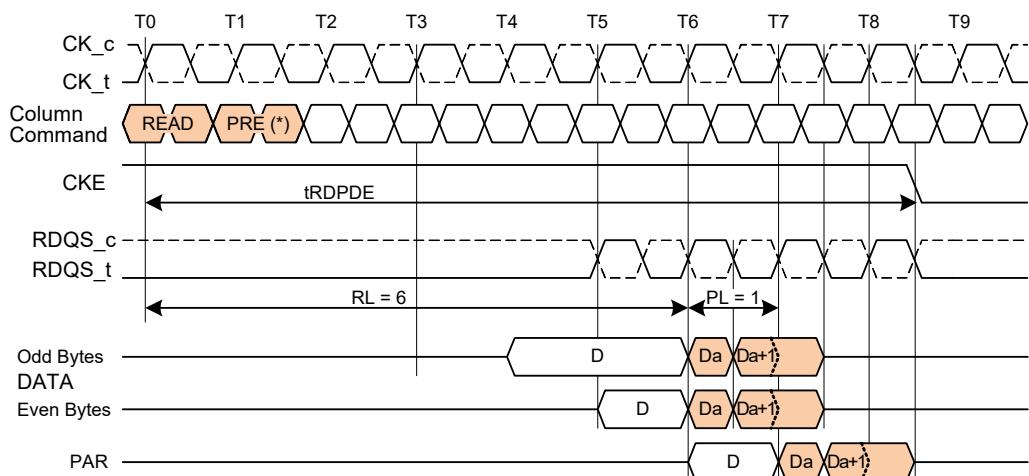
### 6.3.4.1 Power-Down (PDE, PDX) (cont'd)



**Figure 58 — CKE Intensive Environment**



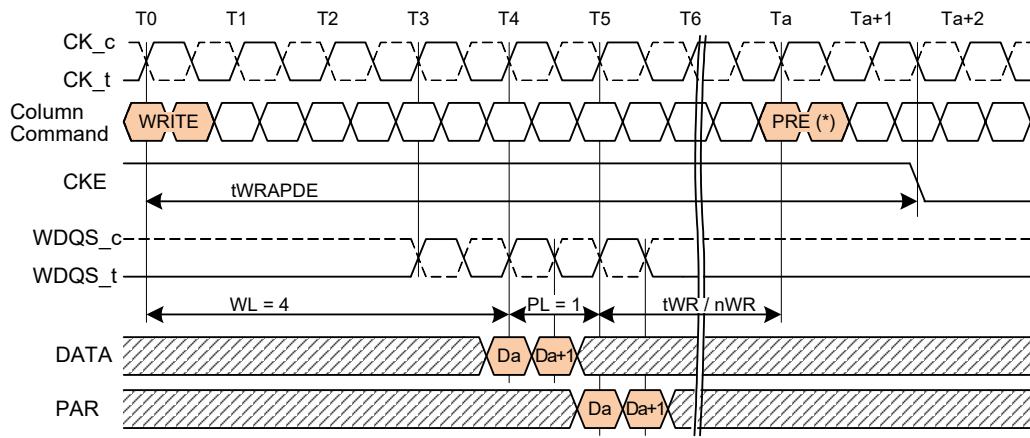
**Figure 59 — REFRESH-to-REFRESH Timing in CKE Intensive Environments**



1. PRE indicates the internal auto-precharge for RDA commands.
2. BL = 2, RL = 6 and PL = 1 are shown as examples.
3. CKE must be held high until the end of the read burst operation.

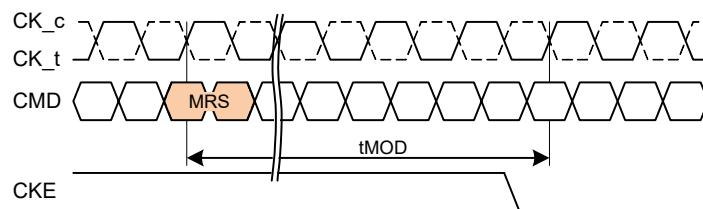
**Figure 60 — READ or READ with Auto Precharge to Power-Down Entry Timing**

### 6.3.4.1 Power-Down (PDE, PDX) (cont'd)

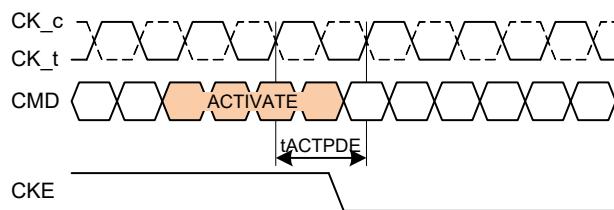


1. PRE indicates the internal auto-precharge for WRA commands.
2. BL = 2, WL = 4 and PL = 1 are shown as examples.
3. CKE must be held high until the end of the write burst operation.
4. tWR is the analog value used with WR commands
5. nWR is the number of clock cycles programmed for WR in the Mode Register and used with WRA commands.

**Figure 61 — WRITE or WRITE with Auto Precharge to Power-Down Entry Timing**



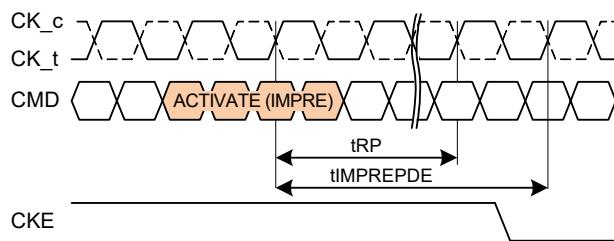
**Figure 62 — MODE REGISTER SET to Power-Down Entry Timing**



1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

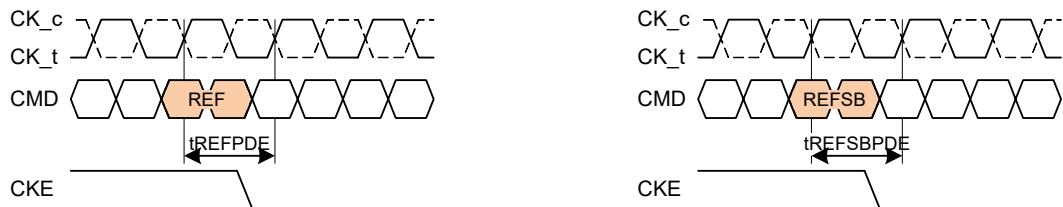
**Figure 63 — ACTIVATE to Power-Down Entry Timing**

### 6.3.4.1 Power-Down (PDE, PDX) (cont'd)



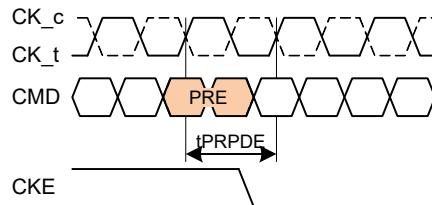
1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

**Figure 64 — ImPRE to Power-Down Entry Timing**



1. Upon power-down entry the clock must be kept active for the number of clock cycles programmed for RAS in the Mode Register.

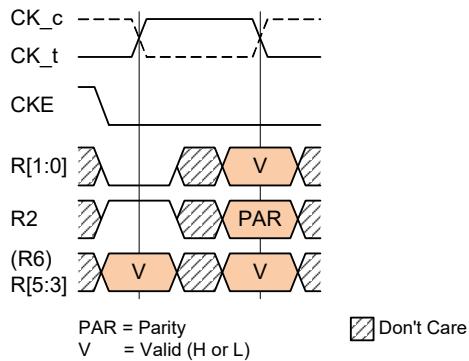
**Figure 65 — REFRESH or SINGLE BANK REFRESH to Power-Down Entry Timing**



**Figure 66 — PRECHARGE to Power-Down Entry Timing**

### 6.3.4.2 Self Refresh (SRE, SRX)

Self refresh can be used to retain data in the HBM device, even if the rest of the system is powered down. When in the self refresh mode, the HBM device retains data without external clocking. The SELF REFRESH ENTRY command is like a REFRESH command except that CKE is pulled LOW. The command is received on the row command inputs R[6:0] or R[5:0] as shown in [Figure 67](#) and requires a CNOP command on the column command inputs C[8:0] or C[7:0].



**Figure 67 — SELF REFRESH-ENTRY Command**

Self refresh entry is only allowed when all banks are precharged with  $t_{RP}$  satisfied, the last data elements from a preceding READ command have been pushed out ( $t_{RDSRE}$ ), or  $t_{MOD}$  from a preceding MODE REGISTER SET command is met. RNOP and CNOP commands are required after entering self refresh mode until  $t_{CPDED}$  is met.

Once the SELF REFRESH-ENTRY command is registered, CKE must be held LOW to keep the device in self refresh mode. When the device has entered the self refresh mode, all external control signals except CKE and RESET\_n are “Don’t care”. For proper self refresh operation, all power supply pins ( $V_{DDC}$ ,  $V_{DDQ}$ ,  $V_{PP}$ ) must be at valid levels. The HBM device initiates a minimum of one internal refresh within  $t_{CKE}$  period once it enters self refresh mode.

The clocks are internally disabled during self refresh operation to save power. The minimum time that the HBM device must remain in self refresh mode is  $t_{CKESR}$ . The user may halt the external clock or change the external clock frequency  $t_{CKSRE}$  after self refresh entry is registered. However, the clock must be restarted and stable  $t_{CKSRX}$  before the device can exit self refresh operation.

While in self refresh the device will continue driving RDQS\_t and RDQS\_c to LOW and HIGH static levels, respectively, and TEMP and CATTRIP to valid HIGH or LOW levels.

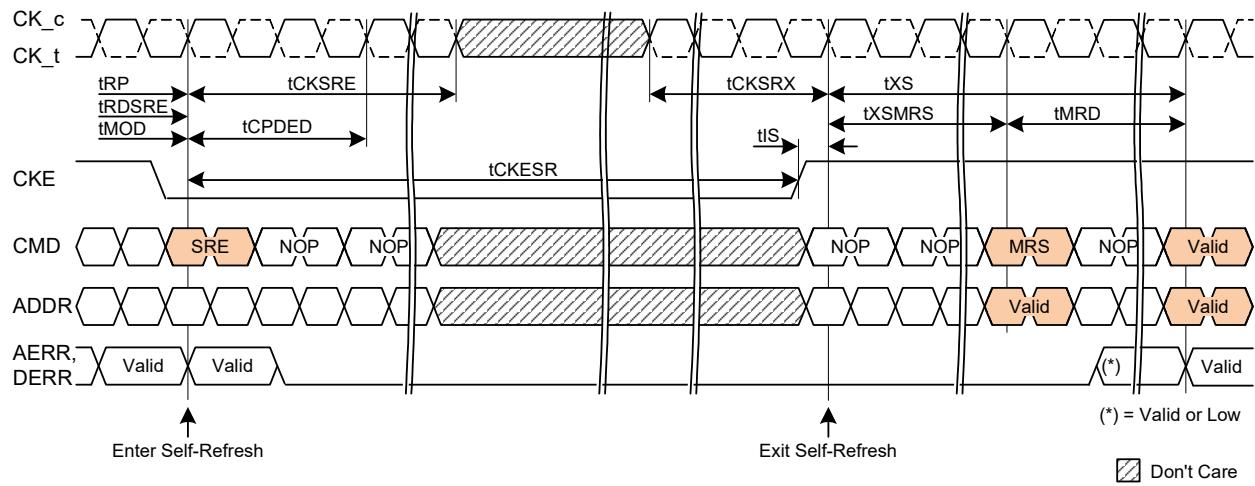
If enabled, parity is evaluated for the SELF REFRESH ENTRY command. The HBM device requires RNOP and CNOP commands with valid parity for the entire  $t_{CPDED}$  period, while it will suspend parity checking after self refresh entry and drive AERR and DERR to a static LOW.

Parity is not evaluated for the SELF REFRESH EXIT command. The HBM device requires RNOP and CNOP commands with valid parity for the entire  $t_{XS}$  period, while within  $t_{XS}$  period it will resume parity checking and indicating parity errors on AERR. DERR remains LOW as there are no data bursts in progress at this time.

The procedure for exiting self refresh requires a sequence of events. First, the CK clock must be stable prior to CKE going back HIGH. A delay of at least  $t_{XS}$  must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

### 6.3.4.2 Self Refresh (SRE, SRX) (cont'd)

Upon exit from self refresh, the HBM device can be put back into self refresh mode after waiting at least  $t_{XS}$  period and issuing one extra REFRESH command.



- Only RNOP and CNOP commands allowed during  $t_{CPDED}$  and  $t_{XS}$  periods, except for MRS commands which are allowed  $t_{XSMRS}$  after self-refresh exit.
- Write bursts must have been completed with  $t_{RP}$  satisfied prior to self-refresh entry.
- Read bursts must have been completed with  $t_{RDPE}$  satisfied prior to self-refresh entry.
- Address inputs are „Don't Care“ for self-refresh entry and exit.
- AERR, DERR are driven LOW when parity check is suspended during self refresh. Signals are shown with  $t_{PARAC}=0$  and  $t_{PARDQ}=0$  for illustration purpose.

Figure 68 — Self Refresh Entry and Exit

## 6.4 Parity

### 6.4.1 Command/Address Parity

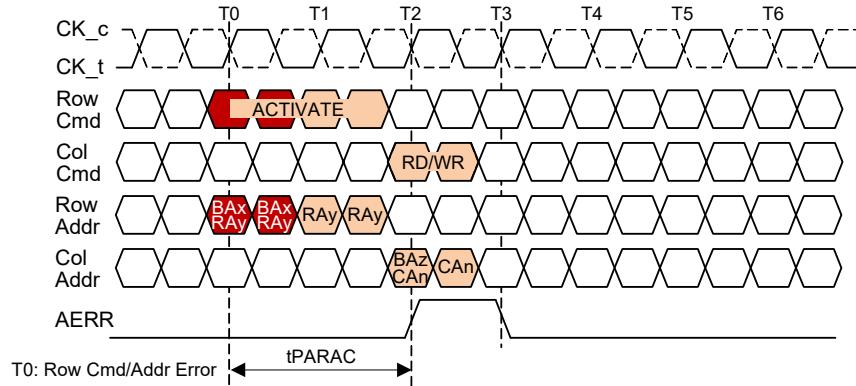
The HBM device includes a Command/Address parity checking function. There is one AERR output pin per AWORD. The HBM device accepts a parity input from the memory controller per the respective Row or Column command truth table, compares it with the data received on the rising and falling CK clock edges of the respective R or C inputs (R[5:0] and C[7:0] or R[6:0] and C[8:0], depending on device configuration) for that clock cycle, and indicates on the AERR pin whether a parity error has occurred. The HBM device executes the command(s) regardless of a command/address parity error.

The Command/Address Parity function is disabled by default. The parity function can be enabled in MR0 OP6 (see [Table 9](#)). The HBM device may begin to check parity on the next clock cycle following the MRS command that enables the parity checking function; it guarantees to check parity  $t_{MOD}$  after that MRS command. The host controller must drive valid parity next clock cycle after parity is enabled in the mode register. The HBM device guarantees to disable parity checking  $t_{MOD}$  after an MRS command disables the parity checking function. The host controller must drive valid parity until  $t_{MOD}$  after parity is disabled in MR0 OP6. The parity function should not be disabled within  $t_{PARAC}$  after an access command. See also section [Power-Down \(PDE, PDX\)](#) and section [Self Refresh \(SRE, SRX\)](#). AERR is always driven LOW by the HBM device at reset.

For every address parity error, AERR is driven HIGH for 1  $t_{CK}$ ,  $t_{PARAC}$  after the corresponding cycle of the error inputs. In the case of consecutive errors, the AERR signal will stay HIGH during the next cycle.

#### 6.4.1 Command/Address Parity (cont'd)

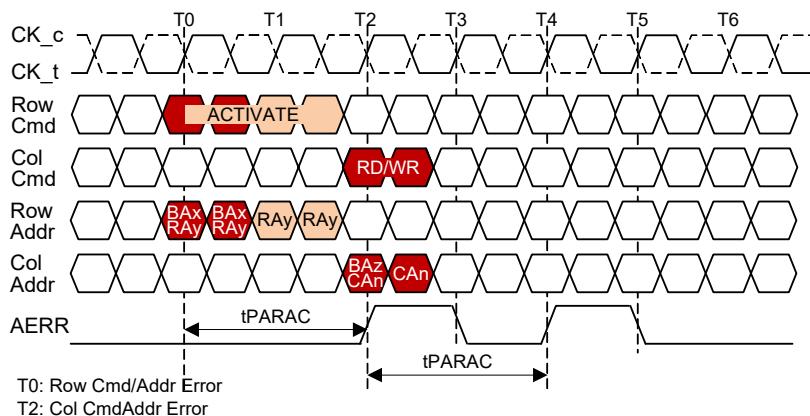
Figure 69 illustrates a single parity error occurrence on the R[6:0] or R[5:0] inputs. In this case, an error occurs in T0, the first cycle of the ACTIVATE command. After t<sub>PARAC</sub>, AERR is driven HIGH for 1 t<sub>CK</sub> and then LOW since no subsequent errors occur.



Note 1: For illustration purpose, t<sub>PARAC</sub> is shown with 2 tCK digital and 0 ns analog output delay.  
 Note 2: MR0 OP[6] shall be maintained as 1 for at least t<sub>PARAC</sub> after the access command.

**Figure 69 — Command/Address Parity Error**

Figure 70 illustrates parity error occurrences on the R-inputs and the C-inputs. In this case, an error occurs in T0, the first cycle of the ACTIVATE command. After t<sub>PARAC</sub>, AERR is driven HIGH for 1 t<sub>CK</sub> and then LOW for 1 t<sub>CK</sub>. Since an error also occurs in T2, the RD/WR command, AERR is again driven HIGH for 1 t<sub>CK</sub> and then LOW since no subsequent errors occur.

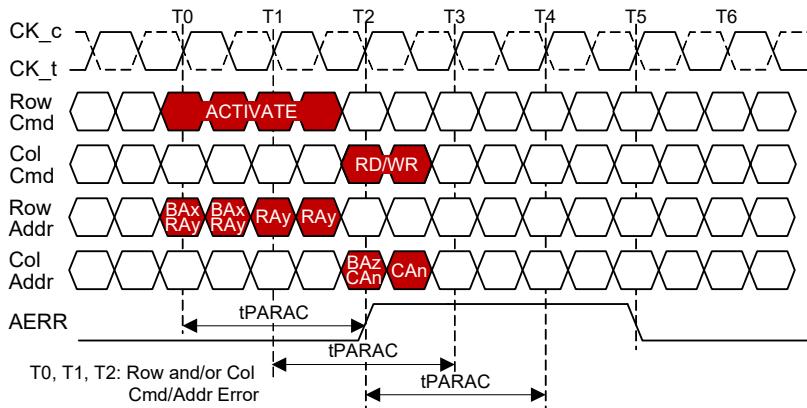


Note 1: For illustration purposes, the figure is shown with 2 tCK digital and 0 ns analog output delay.  
 Vendor datasheets should be consulted for actual value.  
 Note 2: MR0 OP[6] shall be maintained as 1 for at least t<sub>PARAC</sub> after the access command.

**Figure 70 — Separated Command/Address Parity Errors**

Figure 71 illustrates consecutive cycle errors, such that parity errors occur during the T0, T1, and T2 cycles on either or both interfaces. Due to the common AERR output, parity error occurrences on both interfaces on the same cycle are indistinguishable.

#### 6.4.1 Command/Address Parity (cont'd)



Note 1: For illustration purposes, the figure is shown with 2 tCK digital and 0 ns analog output delay.  
Vendor datasheets should be consulted for actual value.

Note 2: MR0 OP[6] shall be maintained as 1 for at least tPARAC after the access command.

**Figure 71 — Consecutive Command/Address Parity Errors**

Table 36 specifies the parity function for each clock cycle.

**Table 36 — Parity Function Table**

Inputs	? of Inputs	PAR	AERR Output	Note
Row R[(6),5:0] - Minus PAR bit	Even	L	L	1
		H	H	
	Odd	L	H	
		H	L	
Column C[(8),7:0] - Minus PAR bit	Even	L	L	1
		H	H	
	Odd	L	H	
		H	L	

NOTE 1 See [Command Truth Tables](#) for command and device state exceptions.

#### 6.4.2 DQ Parity

The HBM device includes a DQ parity checking function. There is one PAR bidirectional I/O and one DERR output signal per DWORD. On write transactions, the HBM device compares the PAR input with the corresponding data received on DQ, DM and DBI inputs, and indicates on the DERR pin whether a parity error has occurred. On read transactions, the HBM generates parity and transmits the parity on the PAR signal along with the corresponding data on DQ and DBI.

The DQ Parity function is disabled by default. The parity function can be enabled in MR0 OP5 for Writes and OP4 for Reads (see [Table 9](#)). The HBM device may begin to check parity on the next clock cycle following the MRS command that enables the parity checking function; it guarantees to check parity  $t_{MOD}$  after that MRS command. The HBM device guarantees to disable parity checking  $t_{MOD}$  after an MRS command disables the parity checking function. See also [Mode Register Set \(MRS\)](#). DERR is always driven LOW by the HBM device at reset. The parity function for Writes should not be disabled within  $(PL + t_{PARDQ})$  after the WRITE data. Also, the parity function for Reads should not be disabled within  $(RL + PL)$  after the READ command.

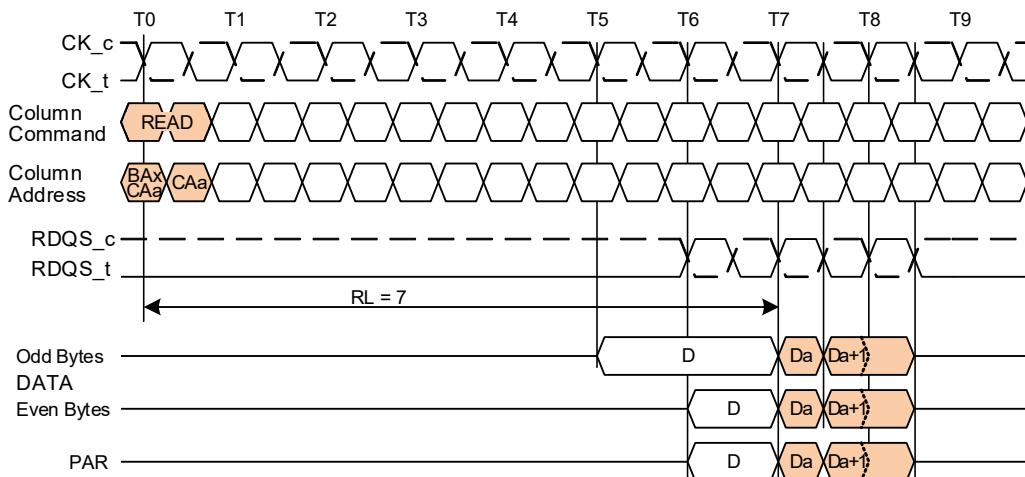
### 6.4.2 DQ Parity (cont'd)

The DQ Parity function includes a programmable parity latency PL between the PAR signal and the corresponding data with a range of 0 to 3 nCK. PL is programmed in MR4 OP[3:2] (see [Table 15](#)), and is the same for Writes and Reads. With a latency of 0 nCK the PAR signal and corresponding data are received and sent simultaneously; with all other values of PL the corresponding PAR signal will be received and sent PL cycles later. The WDQS and RDQS signals will have additional strobe cycles with the same preamble and postambles to accommodate the latching of the delayed PAR signal at both ends. The DRAM vendor's datasheet shall be consulted for the range of supported PL values.

If an error occurs in either or both UI of a write transaction, DERR is driven HIGH for 1  $t_{CK}$  at the input clock edge  $t_{PARDQ}$  clocks after the corresponding cycle of error inputs. In case of two consecutive cycle errors, DERR will stay HIGH during the next cycle.

When an error occurs, the HBM device does not block the Write data. The HBM device completes the Write transaction to the array as normal.

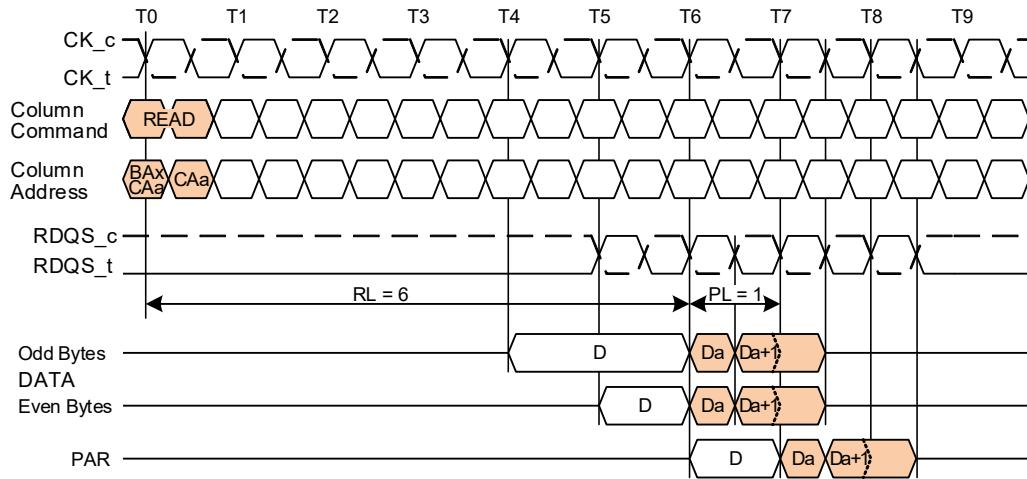
Examples of single read bursts with BL=2 are shown in [Figure 72](#) for the PL=0 case and [Figure 73](#) for the PL=1 case. The PAR output is preconditioned over 1 cycle like for the even data bytes. With PL=1 an additional RDQS postamble cycle for PAR is transmitted at cycle T8.



1. BAx = bank address x; CAa = column address a.
2. RL = 7 and PL = 0 are shown as examples.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DBI[15:0]. PAR = PAR[3:0].
4. Da,a+1 = data-out for READ command a.
5. D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
6. tDQSCK = 0 and nominal tLZ, tHZ is shown for illustration purposes.
7. MR0 OP[4] shall be maintained as 1 for at least (RL + PL) after the READ command.
7. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 72 — Read Parity Alignment with PL = 0**

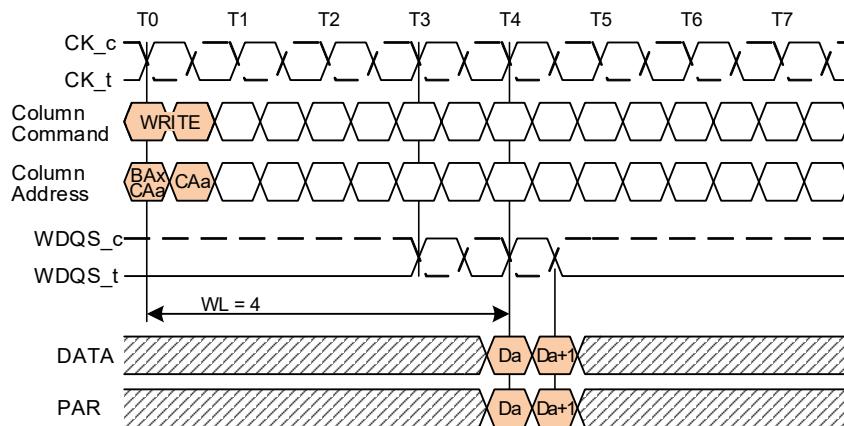
### 6.4.2 DQ Parity (cont'd)



1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. RL = 6 and PL = 1 are shown as examples.
3. RDQS = RDQS[3:0]; DATA = DQ[127:0], DBI[15:0]. PAR = PAR[3:0].
4. Da,a+1 = data-out for READ command a.  
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. tDQSCK = 0 and nominal tLZ, tHZ is shown for illustration purposes.
6. MR0 OP[4] shall be maintained as 1 for at least (RL + PL) after the READ command.
7. RDBI could be on or off and is controlled with MR0 OP0.

**Figure 73 — Read Parity Alignment with PL = 1**

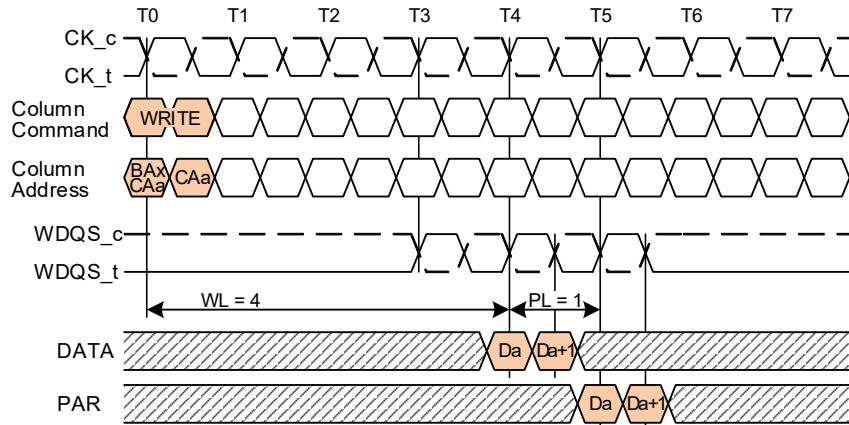
Examples of single write bursts with BL=2 are shown in [Figure 74](#) for the PL=0 case and [Figure 75](#) for the PL=1 case. With PL=1 an additional WDQS cycle for PAR is expected at cycle T5 to latch the PAR input.



1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. WL = 4 and PL = 0 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]. PAR = PAR[3:0].
4. Da, Da+1 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.
6. RDBI could be on or off and is controlled with MR0 OP1.

**Figure 74 — Write Parity Alignment with PL = 0**

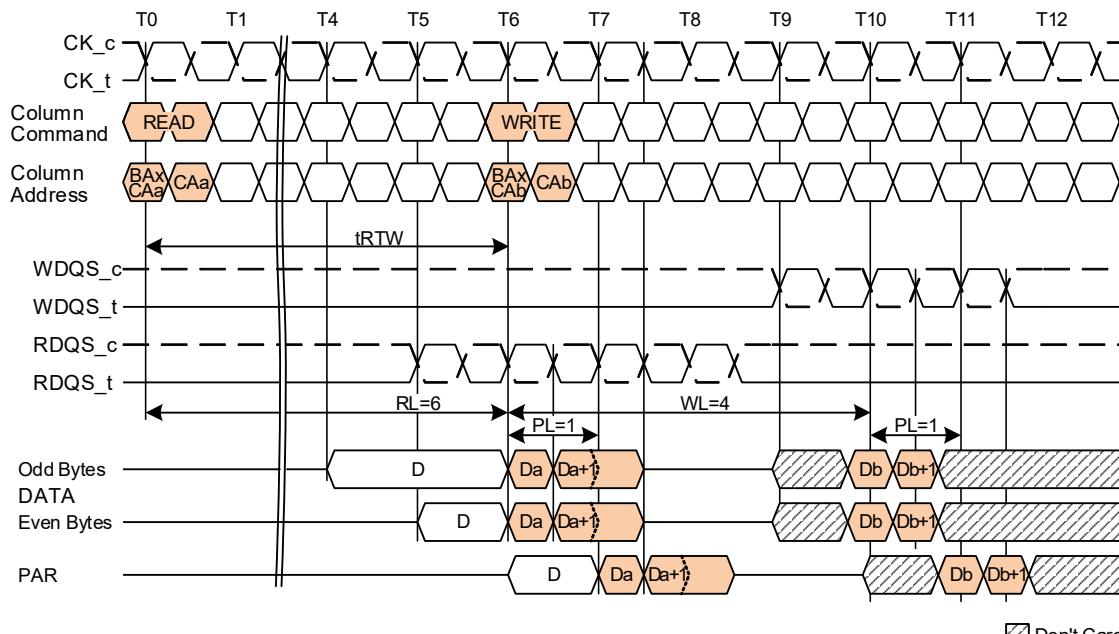
#### 6.4.2 DQ Parity (cont'd)



1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. WL = 4 and PL = 1 are shown as examples.
3. WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[15:0]. PAR = PAR[3:0].
4. Da, Da+1 = data-in for WRITE command a.
5. tDQSS = 0 is shown for illustration purposes.
6. WDBI could be on or off and is controlled with MR0 OP1.

Figure 75 — Write Parity Alignment with PL = 1

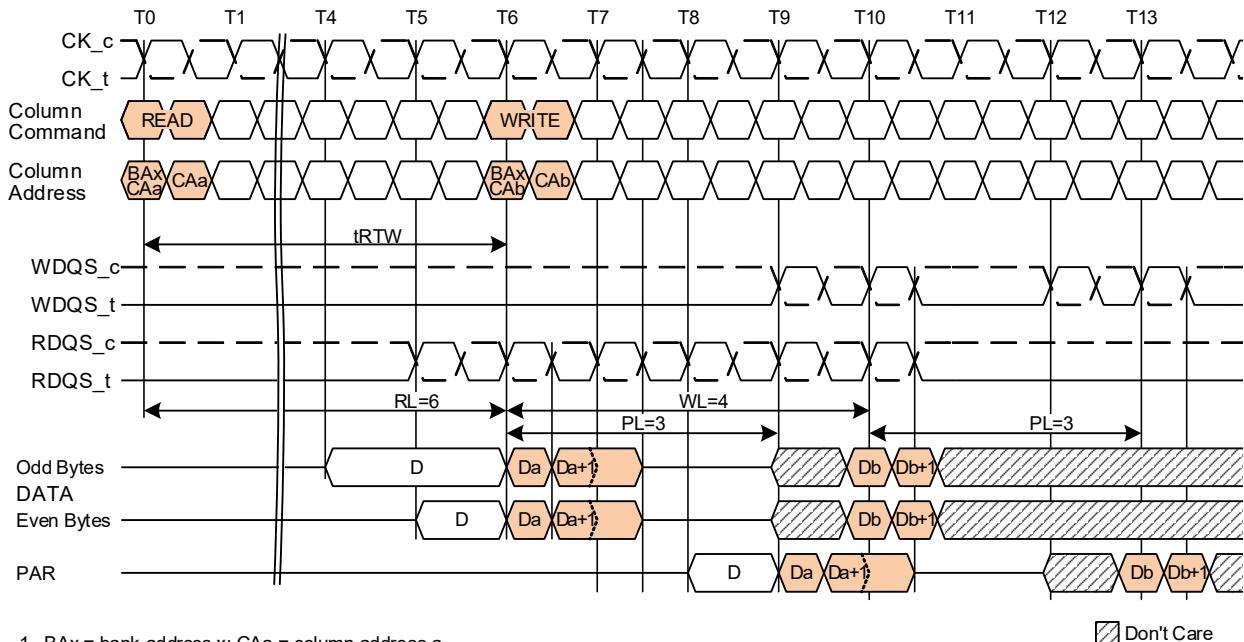
The parity latency PL has no impact on the minimum bus turnaround time. As the PAR signal is delayed by the same number of cycles for Reads and Writes, its turnaround is only delayed as compared to the data bytes by the programmed number of cycles as illustrated in [Figure 76](#) for PL=1 and [Figure 77](#) for the extreme case of PL=3.



1. BA<sub>x</sub> = bank address x; CA<sub>a</sub> = column address a.
2. RL=6, WL=4 and PL=1 are shown as examples.
3. RDQS = RDQS[3:0]; WDQS = WDQS[3:0]; DATA = DQ[127:0], DM[15:0], DBI[3:0]; PAR = PAR[3:0].
4. Da,a+1 = data-out for READ command a.  
D = last data-out from previous READ command (not if first READ after reset, MRS, self refresh or write-to-read).
5. Db,b+1 = data-in for WRITE command b.  
tDQCK, tDQSS = 0 and nominal tLZ, tHZ is shown for illustration purposes.
6. tRTW is not a device limit but determined by the system bus turnaround time.
7. RDBI and WDBI could be on or off. RDBI is controlled with MR0 OP0, and WDBI is controlled with MR0 OP1.

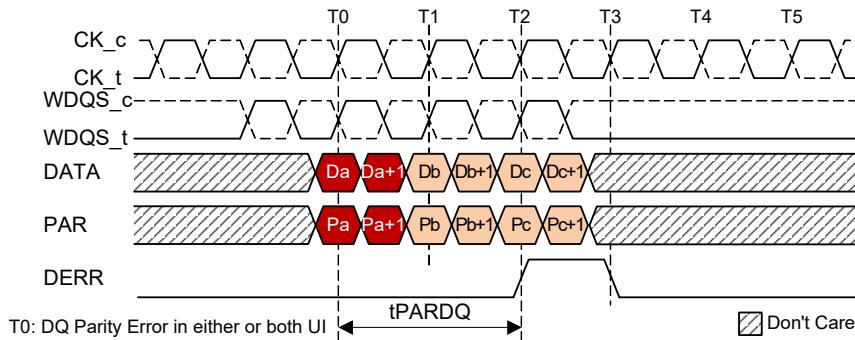
Figure 76 — Read-to-Write Bus Turnaround with PL = 1

### 6.4.2 DQ Parity (cont'd)



**Figure 77 — Read-to-Write Bus Turnaround with PL = 3**

Figure 78 illustrates a single cycle DQ parity error occurrence on a write transaction. In this case, an error occurs in T0, in either or both of the UI. After t<sub>PARDQ</sub>, DERR is driven HIGH for 1 t<sub>CK</sub> and then LOW since no subsequent errors occur.

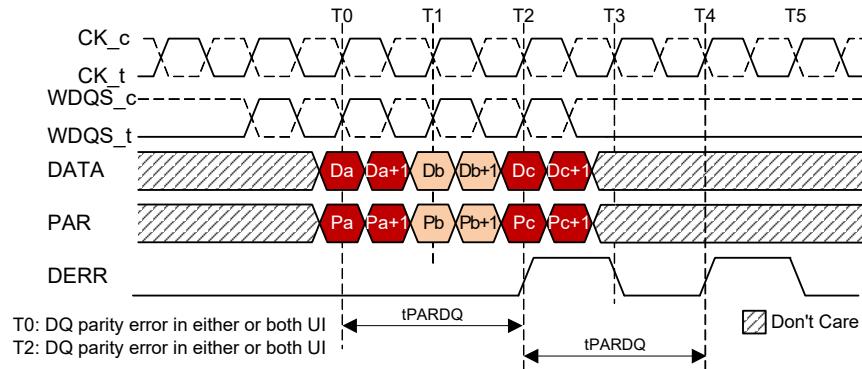


Note 1: For illustration purpose, tPARDQ is shown with 2 tCK digital and 0 ns analog output delay.  
Note 2: MR0 OP[5] shall be maintained as 1 for at least (PL + tPARDQ).

**Figure 78 — Write Parity Error**

#### 6.4.2 DQ Parity (cont'd)

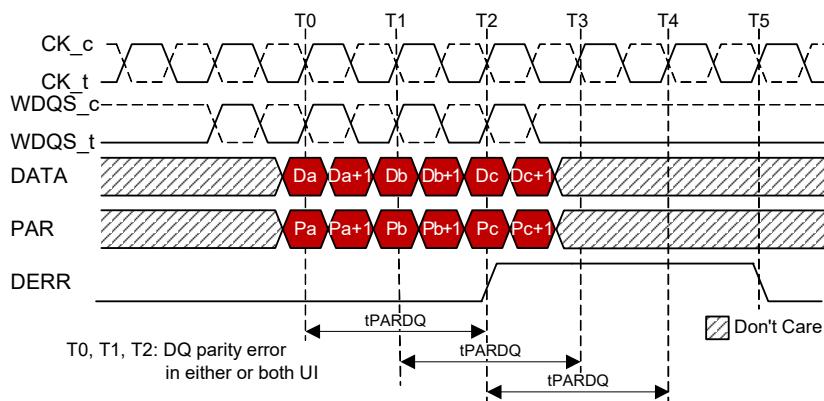
Figure 79 illustrates parity error occurrences on separated cycles. In this case, an error occurs in either or both UIs of T0. After  $t_{PARDQ}$ , DERR is driven HIGH for 1  $t_{CK}$ . Since an error also occurs in either or both UI of T2, DERR is again driven HIGH for 1  $t_{CK}$  and then LOW since no subsequent errors occurs.



Note 1: For illustration purposes, the figure is shown with 2 tCK digital and 0 ns analog output delay.  
Vendor datasheets should be consulted for actual value.  
Note 2: MR0 OP[5] shall be maintained as 1 for at least (PL + tPARDQ).

**Figure 79 — Separated Write Parity Errors**

Figure 80 illustrates consecutive cycle errors, such that parity errors occur during the T0, T1, and T2 cycles.



Note 1: For illustration purposes, the figure is shown with 2 tCK digital and 0 ns analog output delay.  
Vendor datasheets should be consulted for actual value.  
Note 2: MR0 OP[5] shall be maintained as 1 for at least (PL + tPARDQ).

**Figure 80 — Consecutive Write Parity Errors**

#### 6.4.2 DQ Parity (cont'd)

[DQ Parity Function Table](#) specifies the DQ parity function for each UI of the burst.

**Table 37 — DQ Parity Function Table**

Mode Register Configuration			Inputs	$\Sigma$ of Inputs	PAR	DERR Output	
DBI <sup>1</sup>	DM	ECC					
Enabled	Enabled	Disabled	DQ[31:0], DBI[3:0], DM[3:0] <sup>2</sup>	Even	L	L	
					H	H	
	Disabled	Enabled		Odd	L	H	
					H	L	
Enabled	Disabled	Enabled	DQ[31:0], DBI[3:0]	Even	L	L	
					H	H	
	Enabled	Disabled		Odd	L	H	
					H	L	
Enabled	Enabled	Disabled	DQ[31:0], DBI[3:0]	Even	L	L	
					H	H	
	Disabled	Enabled		Odd	L	H	
					H	L	
Disabled	Enabled	Disabled	DQ[31:0], DM[3:0] <sup>2</sup>	Even	L	L	
					H	H	
	Disabled	Enabled		Odd	L	H	
					H	L	
Disabled	Disabled	Enabled	DQ[31:0]	Even	L	L	
					H	H	
	Enabled	Disabled		Odd	L	H	
					H	L	
Disabled	Disabled	Disabled	DQ[31:0]	Even	L	L	
					H	H	
	Enabled	Enabled		Odd	L	H	
					H	L	

NOTE 1 Command types dependent on configuration. See [Table 9](#) for Read DBIac and Write DBIac.

NOTE 2 Write command only. DM[3:0] excluded from parity function of Read command.

NOTE 3 Data inputs are included in the parity calculation for writes regardless whether a byte is masked by DM or not.

#### 6.5 Clock Frequency Change Sequence

Clock Frequency changes can occur during power-down or self refresh mode. When the CK clock is stopped after self refresh entry, it can be restarted at a different frequency. If the change in clock-rate requires changes to configuration parameters, MRS commands immediately prior to or after self refresh mode may be required.

## 6.6 Target Row Refresh (TRR) Mode

The HBM DRAM's row has a limited number of times a given row can be accessed within a certain time period prior to requiring adjacent rows to be refreshed. The Maximum Activate Count (MAC) is the maximum number of activates that a single row can sustain within a time interval of equal to or less than the Maximum Activate Window ( $t_{MAW}$ ) before the adjacent rows needs to be refreshed regardless of how the activates are distributed over  $t_{MAW}$ . The row receiving the excessive activates is the Target Row (TRn), the two adjacent rows to be refreshed are the victim rows.

When the MAC limit is reached on TRn, either the SDRAM must receive roundup ( $t_{MAW}/t_{REFI}$ ) Refresh Commands (REF) before another row activate is issued, or the HBM DRAM should be placed into Target Row Refresh (TRR) mode. The TRR mode will refresh the rows adjacent to the TRn that encountered MAC limit. There could be one or two target rows in a bank associated to one victim row. The cumulative value of the Activates from two target rows on a victim row should not exceed MAC value as well.

[Table 16](#) shows fields required to support the new TRR settings. Setting MR5 OP7 = 1 enables TRR mode and setting MR5 OP7 = 0 disables TRR mode. MR5 OP[3:0] defines which bank (BAn) the target row is located in.

The TRR mode must be disabled during initialization as well as any other HBM DRAM calibration modes. The TRR mode is entered from a DRAM Idle State, once TRR mode has been entered, no other Mode Register commands are allowed until TRR mode is completed, except setting MR5 OP7 = 0 to interrupt and reissue the TRR mode is allowed in the case, such as the DRAM detecting a Parity error during TRR mode.

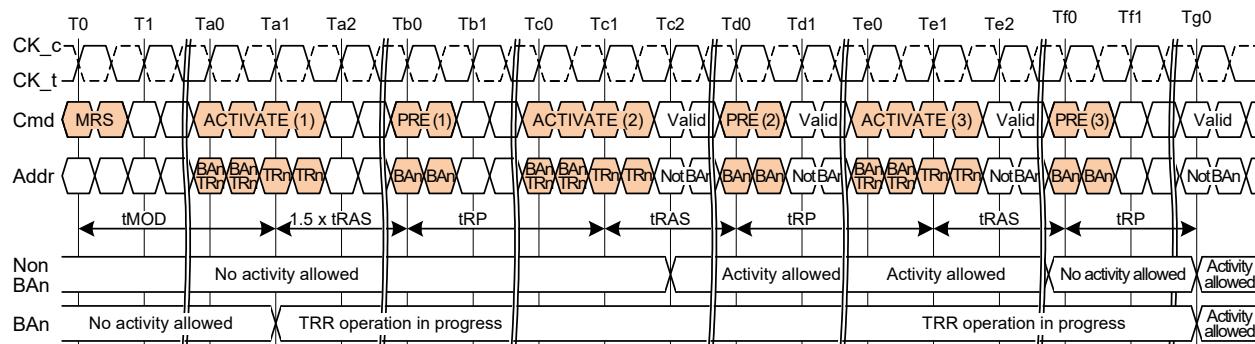
TRR mode is self-clearing: the mode will be disabled automatically after the completion of the 3<sup>rd</sup> BAn precharge plus  $t_{MOD}$ . Optionally the TRR mode can also be exited via another MRS command at the completion of TRR by setting MR5 OP7 = 0; if the TRR is exited via another MRS command, the value written to MR5 OP[3:0] are don't cares.

### 6.6.1 TRR Mode Operation

1. The timing diagram in [Figure 81](#) depicts TRR mode. The following steps must be performed when TRR mode is enabled. This mode requires all three ACT (ACT1, ACT2 and ACT3) and three corresponding PRE commands (PRE1, PRE2 and PRE3) to complete TRR mode. The Precharge All (PREA) command issued while the HBM DRAM is in TRR mode will also perform precharge to BAn and counts toward a PREn command. Implicit Precharge is not supported in TRR mode.
2. Prior to issuing the MRS command to enter TRR mode, the HBM DRAM should be in the idle state. A MRS command must be issued with MR5 OP7 = 1, MR5 OP[3:0] containing the targeted bank in which the targeted row is located. All other MR5 bits should remain unchanged.
3. No activity is to occur in the DRAM until  $t_{MOD}$  has been satisfied. Once  $t_{MOD}$  has been satisfied.
4. The first ACT to the BAn with the TRn address can now be applied, no other command is allowed at this point. All other banks must remain inactive from when the first BAn ACT command is issued until  $[(1.5 \times t_{RAS}) + t_{RP}]$  is satisfied. The only commands to BAn allowed are ACT and PRE until the TRR mode has been completed.
5. After the first ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued ( $1.5 \times t_{RAS}$ ) later; and then followed  $t_{RP}$  later by the second ACT to the BAn with the TRn address. Once the 2<sup>nd</sup> activate to the BAn is issued, non BAn bank groups are allowed to have activity.

### **6.6.1 TRR Mode Operation (cont'd)**

6. After the second ACT to the BAn with the TRn address is issued, a PRE to BAn is to be issued  $t_{RAS}$  later and then followed  $t_{RP}$  later by the third ACT to the BAn with the TRn address.
  7. After the third ACT to the BAn with the TRn address is issued, a PRE to BAn would be issued  $t_{RAS}$  later; and once the third PRE has been issued, non BAn banks are not allowed to have activity until TRR mode is exited. The TRR mode is completed once  $t_{RP}$  plus  $t_{MOD}$  is satisfied.
  8. TRR mode must be completed as specified to guarantee that adjacent rows are refreshed. Any time the TRR mode is interrupted and not completed, the interrupted TRR mode must be cleared and then subsequently performed again. To clean an interrupted TRR mode, an MR5 change is required with setting MR5 OP7 = 0, MR5 OP[3:0] are don't care, followed by three PRE to BAn,  $t_{RP}$  time in between each PRE command. The complete TRR sequence (Steps 2-7) must be then re-issued and completed to guarantee that the adjacent rows are refreshed.
  9. Refresh command to the HBM DRAM or entering self refresh mode is not allowed while the DRAM is in TRR mode.



1. TRn is the targeted row.
  2. BAn is the bank address of targeted row.
  3. TRR mode self-clears after tMOD+tRP measured from the 3rd BAn PRECHARGE at clock edge Tg0.
  4. TRR mode or any other activity can be re-engaged after tRP+tMOD from the 3rd BAn PRECHARGE. PREALL may be issued instead of PREn. TRR mode is cleared after 3rd PRE to bank BAn.
  5. ACTIVATE commands to BAn during TRR mode do not provide refreshing support, i.e. the refresh counter is unaffected,
  6. The HBM DRAM must restore the degraded row caused by excessive activation of the targeted row TRn necessary to meet refresh requirements.
  7. A new TRR mode must wait tMOD+tRP time after the 3rd PRECHARGE.
  8. ACT and PRE are the only allowed commands to BAn during TRR mode.
  9. REFRESH commands are not allowed during TRR mode. REFSB commands to non-BAn banks are allowed during TRR mode.
  10. All HBM DRAM timings such as tFAW are to be met during TRR mode. Issuing ACT(1), ACT(2), ACT(3) counts towards tFAW budget.

**Figure 81 — TRR Mode**

## 6.7 Temperature Compensated Refresh Reporting

The HBM DRAM provides temperature compensated refresh related information to the controller via an encoding on the TEMP[2:0] pins. The Gray-coded encoding defines the proper refresh rate expected by the DRAM to maintain data integrity. Absolute temperature values for each encoding are vendor specific and not defined in this specification.

The encoding on the TEMP[2:0] pins is expected to reflect the required refresh rate for the hottest device in the stack and will be updated when the temperature exceeds the vendor specific trip-point levels appropriate for each refresh rate.

### 6.7.1 Temperature Compensated Refresh Trip Points

The HBM DRAM provides three bit port (TEMP[2:0]) that exports temperature compensated refresh status bits.

**Table 38 — Temperature Compensated Refresh Trip Points**

TEMP[2:0]	Refresh Rate
000	4x $t_{REFI}$
001	2x $t_{REFI}$
011	1x $t_{REFI}$
010	0.5x $t_{REFI}$
110	0.25x $t_{REFI}$
111	Vendor Specific
101	
100	

### 6.7.2 Catastrophic Temperature Sensor

The CATTRIP sensor logic detects if the junction temperature of any die in the HBM stack exceeds the catastrophic trip threshold value CATTEMP. CATTEMP value is programmed by the manufacturer to a value below the temperature point that permanent damage would occur to the HBM stack. If the junction temperature anywhere in the stack exceeds the CATTEMP of the device, the HBM stack will drive the external CATTRIP pin to HIGH. This indicates that catastrophic damage may occur unless power is reduced. The CATTRIP output is sticky in that to clear a CATTRIP, power-off of the device is required to return the CATTRIP output to LOW. Sufficient time should be allowed for the device to cool after a CATTRIP event. See [HBM Power-up and Initialization Sequence](#) for the initialization of the CATTRIP pin during power-up.

If CATTEMP is higher than maximum operating junction temperature, CATTRIP circuit will operate correctly regardless of whether the external or internal clocks have stopped. Functionality testing of CATTRIP can be verified by writing a “1” to MR7 OP7 to force a CATTRIP and “0” to clear.

CATTRIP is a mandatory feature for the HBM device with 4 Gb/channel or higher for legacy mode and 2 Gb/channel or higher for pseudo channel mode operation.

## 6.8 Interconnect Redundancy Remapping

The HBM DRAM supports interconnect lane remapping to help improve SIP assembly yield and recover functionality of the HBM stack. The `SOFT_LANE_REPAIR` and `HARD_LANE_REPAIR` instructions are used to perform lane remapping. Lane remapping is independent for each channel.

The HBM DRAM can be programmed to retain the remapped lane information even when power is completely removed from the HBM stack.

### 6.8.1 AWORD Remapping

Row command bus and column command bus are allowed to remap one lane for each bus. CK\_c, CK\_t, CKE and AERR signals cannot be remapped. After a lane is remapped, the input buffer associated with the broken lane is turned off and the input buffer associated with the redundant pin (RR or RC) is turned on. All functionalities are preserved with row or column bus lane remapping.

### **6.8.1.1 Row Command Bus - Remapping Table**

**Table 39 — AWORD - Row Command Bus Remapping**

Description	Register Encoding	Rx6	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RRx
Repair Lane 0	0000	Rx6	XX	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5
Repair Lane 1	0001	Rx6	Rx0	XX	Rx1	Rx2	Rx3	Rx4	Rx5
Repair Lane 2	0010	Rx6	Rx0	Rx1	XX	Rx2	Rx3	Rx4	Rx5
Repair Lane 3	0011	Rx6	Rx0	Rx1	Rx2	XX	Rx3	Rx4	Rx5
Repair Lane 4	0100	Rx6	Rx0	Rx1	Rx2	Rx3	XX	Rx4	Rx5
Repair Lane 5	0101	Rx6	Rx0	Rx1	Rx2	Rx3	Rx4	XX	Rx5
Repair Lane 6	0110	XX	Rx6	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5
Reserved	0111 to 1110	Rx6	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RFU
Default - No Repair	1111	Rx6	Rx0	Rx1	Rx2	Rx3	Rx4	Rx5	RFU

### 6.8.1.2 Column Command Bus - Remapping Table

**Table 40 — AWORD - Column Command Bus Remapping**

Description	Register Encoding	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RCx
Repair Lane 0	0000	Cx8	XX	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 1	0001	Cx8	Cx0	XX	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 2	0010	Cx8	Cx0	Cx1	XX	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 3	0011	Cx8	Cx0	Cx1	Cx2	XX	Cx3	Cx4	Cx5	Cx6	Cx7
Repair Lane 4	0100	Cx8	Cx0	Cx1	Cx2	Cx3	XX	Cx4	Cx5	Cx6	Cx7
Repair Lane 5	0101	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	XX	Cx5	Cx6	Cx7
Repair Lane 6	0110	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	XX	Cx6	Cx7
Repair Lane 7	0111	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	XX	Cx7
Repair Lane 8	1000	XX	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7
Reserved	1001 to 1110	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RFU
Default - No Repair	1111	Cx8	Cx0	Cx1	Cx2	Cx3	Cx4	Cx5	Cx6	Cx7	RFU
NOTE 1	x = any channel [a:h]										
NOTE 2	XX = Lane is remapped										
NOTE 3	RFU = Pin is not used										
NOTE 4	Column AWORD encoding of '1000b' is only available for device configurations that include row address RA14 or bank address SID1 or both. See <a href="#">HBM Channel Addressing</a> table.										

### 6.8.1.3 AWORD Remapping Example

As an example, Ca6 and Ra0 are broken lanes for Column Command bus and Row Command bus respectively. The lanes are remapped by programming channel A LANE REPAIR WDR bits AWORD\_CA[3:0] to 6h and bits AWORD\_RA[3:0] to 0h.

**Table 41 — Original Lane Assignment - Channel A - AWORD**

	Ca7		Ca5		CKEa		Ca3		Ca1		Ca8
RCa		Ca6		Ca4		ARFUa1		Ca2		Ca0	
	ARFUa4		Ra5		CKa_c		Ra3		Ra1		Ra6
AERRa		RRa		Ra4		CKa_t		Ra2		Ra0	

**Table 42 — Remapped Lane Assignment - Channel A - AWORD**

	Ca6		Ca5		CKEa		Ca3		Ca1		Ca8
Ca7		XX		Ca4		ARFUa1		Ca2		Ca0	
	ARFUa4		Ra4		CKa_c		Ra2		Ra0		Ra6
AERRa		Ra5		Ra3		CKa_t		Ra1		XX	

## 6.8.2 DWORD Remapping

Two modes are provided to remap the data bus:

- In Mode 1 it is allowed to remap one lane per byte. No redundant pin is allocated in this mode, and DBI functionality is lost for that byte only however other bytes continue to support DBI function as long as the Mode Register setting for DBI function is enabled. If Data Parity function is enabled in the Mode Register and a lane is remapped, both DRAM and host assume DBI input as “0” for parity calculation for Read and Write operation in this mode.  
In Mode 1 each byte is treated independently.
- In Mode 2 it is allowed to remap one lane per double byte. One redundant pin (RD) per double byte is allocated in this mode, and DBI functionality is preserved as long as the Mode Register setting for DBI function is enabled. The use of Mode 2 has no impact on the Data Parity function.  
In Mode 2 two adjacent bytes (e.g., DQ[15:0]) are treated as a pair (double byte), but each double byte is treated independently.

The two modes are distinguished by the use of the “1110b” encoding as shown in the table below. The use of Mode 1 is assumed when a remapping code other than “1110b” is used. For Mode 2 it is required to program “1110b” for the intact byte within the double byte while the remapping for the broken lane in the other byte is encoded according to the table.

WDQS\_c, WDQS\_t, RDQS\_c, RDQS\_t, PAR and DERR signals cannot be remapped.

After a lane is remapped, the input buffer associated with the broken lane is turned off and the output driver is tri-stated; with Mode 2 the input buffer associated with the redundant pin (RD) is additionally turned on and the output driver is activated.

During Reads, the RD output drivers are enabled along with the DQ, DBI and DM pins of the physical byte the pin is located in: RD0, RD2, RD4 and RD6 are located within even bytes and thus enabled one clock cycle prior to the first valid data bit, and RD1, RD3, RD5 and RD7 are located within odd bytes and thus enabled two clock cycles prior to the first valid data bit.

A DWORD byte lane repair using Mode 1 leads to the loss of DBI functionality in that byte. Increased power supply noise shall be expected within the repaired and topologically adjacent byte lanes sharing common V<sub>SS</sub> and V<sub>DDQ</sub> power rails. The exact impact depends on the specific HBM design and characteristics of the power supply to the HBM device. It is suggested to characterize the effect during system qualification and e.g., restrict the allowed byte lane repairs within a region of the HBM’s ball matrix.

### **6.8.2.1 DWORD Remapping Table**

**Table 43 — DWORD Remapping (1 Byte)**

Description	Register Encoding	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RDx0
Repair Lane 0	0000	XX	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 1	0001	DMx0	XX	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 2	0010	DMx0	DQx0	XX	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 3	0011	DMx0	DQx0	DQx1	XX	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 4	0100	DMx0	DQx0	DQx1	DQx2	XX	DQx3	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 5	0101	DMx0	DQx0	DQx1	DQx2	DQx3	XX	DQx4	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 6	0110	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	XX	DQx5	DQx6	DQx7	RFU/DBIx0
Repair Lane 7	0111	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	XX	DQx6	DQx7	RFU/DBIx0
Repair Lane 8	1000	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	XX	DQx7	RFU/DBIx0
Repair Lane 9	1001	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	XX	RFU/DBIx0
Reserved	1010 to 1101	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU
Repair in other byte (Mode 2 only)	1110	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU
Default - No Repair	1111	DMx0	DQx0	DQx1	DQx2	DQx3	DQx4	DQx5	DQx6	DQx7	DBIx0	RFU

### 6.8.2.2 DWORD Remapping Examples

As an example for Mode 1, DMA0 and DQa12 are broken lanes for byte 0 and byte 1 respectively. The lanes are remapped as illustrated in [Table 45](#) by programming channel A LANE REPAIR WDR bits DWORD0\_BYT0[3:0] to 0h and bits DWORD0\_BYT1[3:0] to 5h.

As an example for Mode 2, DMA0 is a broken lane for byte 0 while all lanes for byte 1 are intact. The lane is remapped as illustrated in [Table 46](#) by programming channel A LANE REPAIR WDR bits DWORD0\_BYT0[3:0] to 0h and bits DWORD0\_BYT1[3:0] to Eh.

**Table 44 — Original DWORD Lane Assignment - Channel A; Byte [1:0]**

	DQa7		DQa5		RDa0		DQa3		DQa1		DMA0
DBIa0		DQa6		DQa4		PARa0		DQa2		DQa0	
	DQa15		DQa13		WDQSa 0_c		DQa11		DQa9		DMA1
DBIa1		DQa14		DQa12		WDQSa 0_t		DQa10		DQa8	

**Table 45 — Remapped DWORD Lane Assignment using Mode 1 - Channel A - Byte [1:0]**

	DQa6		DQa4		RDa0		DQa2		DQa0		XX
DQa7		DQa5		DQa3		PARa0		DQa1		DMA0	
	DQa14		DQa12		WDQSa 0_c		DQa11		DQa9		DMA1
DQa15		DQa13		XX		WDQSa 0_t		DQa10		DQa8	

**Table 46 — Remapped DWORD Lane Assignment using Mode 2 - Channel A - Byte [1:0]**

	DQa6		DQa4		DBIa0		DQa2		DQa0		XX
DQa7		DQa5		DQa3		PARa0		DQa1		DMA0	
	DQa15		DQa13		WDQSa 0_c		DQa11		DQa9		DMA1
DBIa1		DQa14		DQa12		WDQSa 0_t		DQa10		DQa8	

The circuit diagram in [Figure 82](#) illustrates the DQ lane remapping in more detail. Physical micro-bump DQ3 will be connected to internal logical DQ3 input and output paths when the DQ3 lane is not remapped; with re-mapping the internal DQ3 input and output paths would be routed to the physical DQ4 micro-bump.

### 6.8.2.2 DWORD Remapping Examples (cont'd)

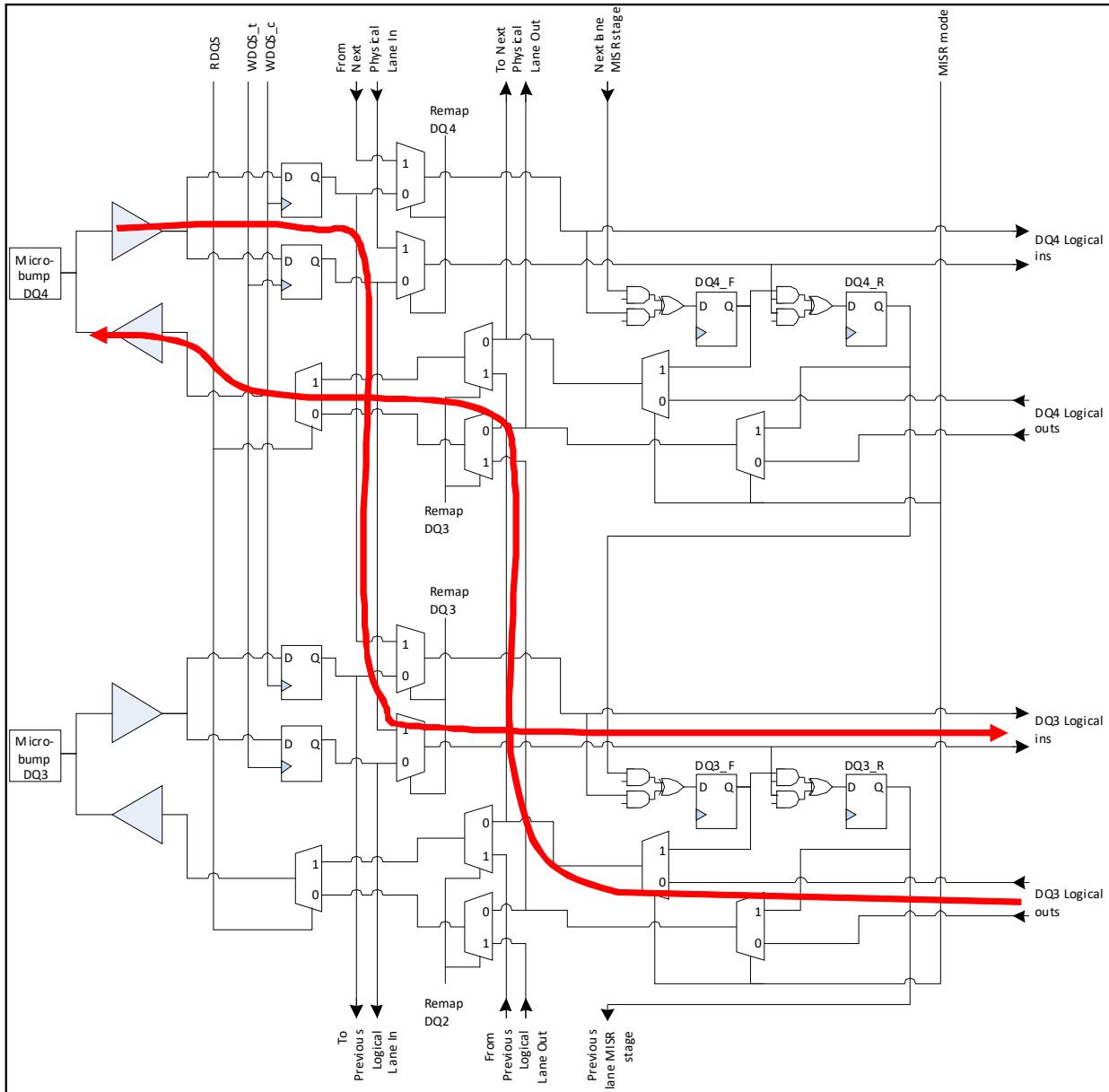
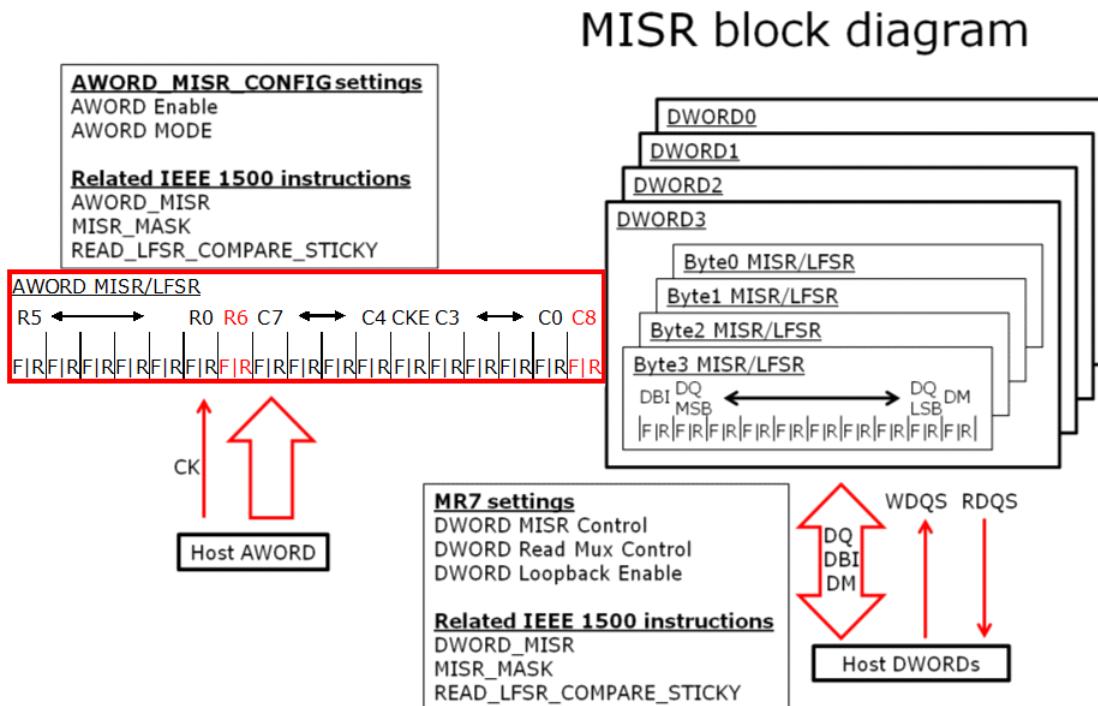


Figure 82 — Example Signal Paths with Lane Repair

## **6.9 HBM Loopback Test Modes**

A Multiple-input Shift Register (MISR) / Linear Feedback Shift Register (LFSR) circuit is defined within the HBM AWORD and DWORD I/O blocks. These circuits are intended for testing and training the link between the Host and the HBM device. Referring to [Figure 83](#), each byte within a DWORD implements a 20-bit MISR/LFSR circuit, comprised of double data rate Rise and Fall bits for each of the eight DQs plus DBI and DM signals. In operation, the MISR/LFSR circuits operate independently across the bytes. The AWORD implements a 30-bit MISR/LFSR circuit comprised of DDR Rise and Fall bits for the 15 row and column command bits, plus CKE. For HBM2 configurations that include the RA14 or SID1 address bit or both, AWORD implements both 30 bit and 34 bit MISR/LFSR circuit comprised of DDR Rise and Fall bits for the 15 and 17 row and column command bits respectively, plus CKE. When the MISR registers are read via the IEEE 1500 port DWORD\_MISR instruction, the four bytes per DWORD (80-bits) for the four DWORDs within a channel are serially shifted out, for a total of 320 bits. The 30-bit or 34-bit AWORD MISR content is read via the AWORD\_MISR instruction. See [Table 94](#) and [Table 95](#) for the bit-orders for these MISR registers.

The term MISR modes collectively refers to all of the modes - LFSR mode, Register mode, MISR mode, and LFSR Compare mode. AWORD MISR modes and DWORD MISR modes refer to all of the modes defined for the specific bus.



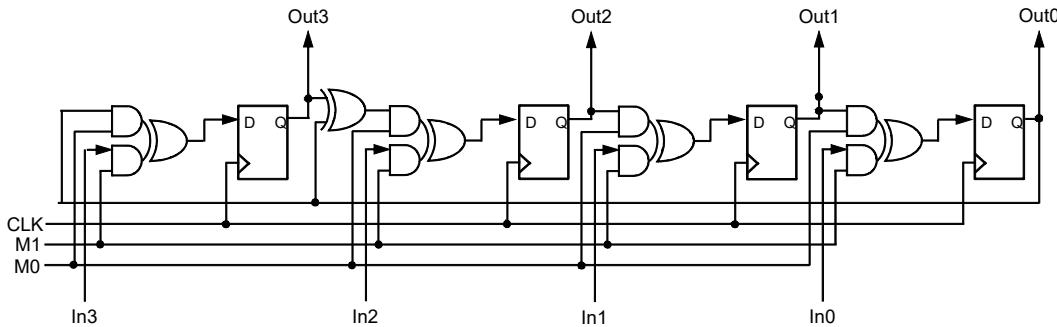
**Figure 83 — MISR Features Block Diagram**

### 6.9.1 HBM Polynomial Structures

[Figure 84](#) provides an example of a 4-bit Galois type MISR/LFSR structure that implements the following polynomial:

$$f(x) = X^4 + X^3 + 1$$

The example circuit and function table are for illustration only, and this circuit's modes are not fully representative of the actual DWORD and AWORD MISR definitions as outlined below. For example, the circuit shown in [Figure 84](#) implements a reset function, while the AWORD and DWORD MISRs instead implement a preset function, where specific bits are set to logic 1.



**Figure 84 — Example of 4 bit MISR-LFSR implementing  $f(x) = X^4 + X^3 + 1$**

**Table 47 — MISR Function Table**

M1	M0	Function
0	0	Reset
0	1	LFSR
1	0	Register
1	1	MISR

#### 6.9.1.1 AWORD MISR Polynomial

Two different AWORD MISR structures are possible in HBM depending on the device density. Consult supplier data sheets for implementation details.

All HBM devices will include a 30-bit MISR/LFSR with the following polynomial:

$$f(x) = X^{30} + X^6 + X^4 + X + 1$$

For HBM2 configurations that include the RA14 and SID1 address bit or both, an additional 34 bit AWORD MISR/LFSR structure is included with the following polynomial:

$$f(x) = X^{34} + X^{27} + X^2 + X + 1$$

For HBM devices with both 30 and 34 bit MISR/LFSR structures, selection of the two MISR/LFSR is through AWORD\_MISR\_CONFIG POLYNOMIAL\_SELECT. The default value is 0 which selects the 30-bit polynomial, a “1” will select the 34-bit polynomial (if included).

The AWORD MISR may be serially accessed via the AWORD\_MISR IEEE 1500 port instruction. See [Table 95](#) for the AWORD MISR wrapper data register bit order for both 30 and 34 bit implementations.

### 6.9.1.2 DWORD MISR Polynomial

The DWORD MISR structure is a 20-bit MISR/LFSR per byte with the following polynomial:

$$f(x) = X^{20} + X^{17} + 1$$

Note that when the DWORD MISRs are accessed via the DWORD\_MISR IEEE 1500 port instructions that all of the individual byte MISRs within a channel are concatenated into a 320-bit wrapper data register. See [Table 94](#) for the DWORD MISR bit order.

### 6.9.2 General Loopback Modes Features and Behavior

This section addresses features and behaviors that generally apply to all of the MISR modes.

- a) **Entering the MISR modes** - MISR modes may be entered any time after completing the initialization (see [Initialization](#)). DWORD MISR modes are controlled via Mode Register 7 (see [Table 18](#)), while AWORD MISR modes are controlled via the IEEE 1500 port AWORD\_MISR\_CONFIG instruction. AWORD and DWORD MISR modes cannot be used simultaneously since the DWORD MISR modes are driven via READ and WRITE commands on the AWORD bus.
- b) **Entering and exiting AWORD MISR modes** - HBM allows the AWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization, to enter the AWORD MISR modes on a given channel the host must put the HBM channel into either precharge power-down or self refresh modes. Self refresh mode may be used in order to retain memory content while using the AWORD MISR modes, as needed. AWORD MISR modes may also be enabled after  $t_{INIT3}$  within the initialization sequence. Enabling the AWORD MISR modes re-enables the AWORD I/O buffers that are normally disabled in power-down and self refresh modes, which may result in increased current draw over the IDD2P, IDD2P0 and IDD6x specifications. If returning to normal operation is not required, the host may assert an initialization sequence per section [Initialization](#) after operating the AWORD MISR modes. The sequence for entering AWORD MISR modes, and then exiting back to normal operation is as follows:
  - 1) At any time after initializing the HBM enter the all banks idle state.
  - 2) Enter either the precharge power-down state or the self refresh state. CKE = LOW while in these states.
  - 3) Stop toggling CK (CK\_t = LOW, CK\_c = HIGH).
  - 4) Enable/enter and operate the AWORD MISR modes (AWORD\_MISR\_CONFIG Enable = 1 - On). Finish these operations with CK stopped (CK\_t = LOW, CK\_c = HIGH) and CKE = LOW.
  - 5) Disable the AWORD MISR modes and follow the [Power-Down \(PDE, PDX\)](#) or [Self Refresh \(SRE, SRX\)](#) exit procedures.
  - 6) When using the AWORD MISR modes after  $t_{INIT3}$  within the initialization sequence, power-down or self refresh entry and exit does not apply.

If the DRAM is not required to continue with mission mode operation after AWORD MISR test, there is no requirement on row/column command bus and CKE lane state after loopback test. The AWORD MISR modes (AWORD\_MISR\_CONFIG Enable bit) can be reset by WRST\_n during a subsequent initialization sequence.

### 6.9.2 General Loopback Modes Features and Behavior (cont'd)

- c) **Entering and exiting DWORD MISR modes** - HBM allows the DWORD MISR modes to be utilized on one or more channels while the other channels continue to operate normally. After normal initialization (see [Initialization](#)), to enter the DWORD MISR modes on a given channel the host must put the HBM channel into the all banks idle, enable the DWORD MISR modes (MR7 Loopback Enable = 1 - Enable; see [Table 18](#)), and then enter precharge power-down or self refresh. Self refresh may be used in order to retain memory content while using the DWORD MISR modes, as needed. Enabling the DWORD MISR modes before entering precharge power-down or self refresh keeps the AWORD and DWORD I/O buffers enabled, and may result in increased current draw over the IDD2P, IDD2P0 and IDD6x specifications. DWORD MISR modes may also be enabled after  $t_{INIT3}$  within the initialization sequence. Also see items h), k), and n) for related DWORD MISR modes configuration setting. On the column command bus only READ (RD), WRITE (WR), and Column No Operation (CNOP) commands may be issued which operate the DWORD MISR modes, and MR7 MRS commands may be issued to select the DWORD MISR modes. On the row command bus only Row No Operation (RNOP) commands may be issued. The sequence for entering DWORD MISR modes, and then exiting back to normal operation is as follows:

- 1) At any time after initializing the HBM enter the all banks idle state.
- 2) Set all configuration mode registers as needed for use in the DWORD MISR modes (see items h), k), and n)).
- 3) Set MR7 DWORD Loopback Enable = 1 - Enable, and then wait  $t_{MOD}$ .
- 4) Enter either precharge power-down or self refresh. CKE = 0 while in these states.
- 5) Select and operate the DWORD MISR modes via MR7 settings and sending RD, WR, and CNOP commands. After completing DWORD MISR operations, send CNOP commands.
- 6) Follow the power-down exit (PDX) or self refresh exit (SRX) procedures.
- 7) Set MR7 DWORD Loopback Enable = 0 - Disable, and then wait  $t_{MOD}$  before continuing normal operation.

MRS commands are not supported until after  $t_{INIT5}$  in the initialization sequences; therefore, to configure and control the mode registers for DWORD MISR modes usage after  $t_{INIT3}$  the MODE\_REGISTER\_DUMP\_SET instruction must be used. The sequence for entering and operating the DWORD MISR modes after  $t_{INIT3}$  in the initialization sequence is as follows:

- 1) Start CK with RNOP and CNOP on the command busses, and CKE = 0.
- 2) Using MODE\_REGISTER\_DUMP\_SET sets all configuration mode registers as needed for use in the DWORD MISR modes (see items h), k), and n)), set MR7 DWORD Loopback Enable = 1 - Enable, and then wait  $t_{MOD}$ .
- 3) Select and operate the DWORD MISR modes via MR7 settings (using MODE\_REGISTER\_- DUMP\_SET) and sending RD, WR, and CNOP commands.
- 4) After completing DWORD MISR operations, send CNOP commands, set MR7 DWORD Loopback Enable = 0 - Disable using MODE\_REGISTER\_DUMP\_SET, then wait  $t_{MOD}$ .
- 5) CK clocking may be stopped if desired.
- 6) Proceed to other IEEE 1500 instructions, or proceed with the initialization sequence from [Figure 6](#), time  $T_d$ .

### 6.9.2 General Loopback Modes Features and Behavior (cont'd)

If the DRAM is not required to continue with mission mode operation after DWORD MISR test, there is no requirement to follow the power-down or self refresh procedures and set MR7 DWORD Loopback Enable = 0 - Disable. The Loopback Enable bit can be reset by a subsequent initialization sequence with RESET\_n = LOW.

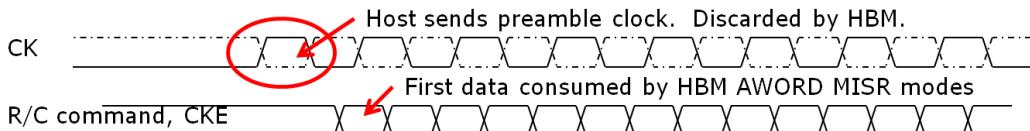
- d) **CKE signal is non-functional in AWORD MISR modes** - The CKE signal is functionally disabled when AWORD MISR modes are enabled (AWORD\_MISR\_CONFIG Enable = 1 - On). This prevents traffic on the CKE signal from causing the HBM device to exit the power-down or self refresh states during AWORD MISR modes testing.
- e) **CKE is handled as an SDR signal in AWORD MISR modes** - The AWORD MISR structure implements a Rise and a Fall bit; however the CKE signal is functionally a single data rate signal. The MISR CKE\_F bit has no functional purpose other than being active in MISR compression and LFSR pattern generation.
  - In AWORD MISR mode and AWORD Register mode, the CKE signal is only sampled on the rising CK edge. The captured CKE state is fed into both the CKE\_F and CKE\_R bits of the AWORD MISR.
  - In AWORD LFSR Compare mode, the CKE signal is only sampled on the rising CK edge, and only compared against the LFSR CKE\_R bit. The CKE\_F bit is not used for comparison.
  - For initialization, Preset (AWORD\_MISR\_CONFIG MODE[2:0] = 000 - Preset) sets the CKE bits to CKE\_F=1, CKE\_R=0. Setting the MISR value via the AWORD Register mode (AWORD\_MISR\_CONFIG MODE[2:0] = 0010 - Register) sets both MISR CKE bits to the value latched on the rising CK edge.
- f) **Command decode is disabled in AWORD MISR modes** - When AWORD MISR modes are enabled the traffic sent on the AWORD bus is not limited to valid commands. To prevent undefined states and operations, when AWORD MISR modes are enabled (AWORD\_MISR\_CONFIG Enable = 1 - On), command decoding is disabled.
- g) **With lane repairs the MISR bit positions remain with their logical signals** - The MISR bits are associated with their logic signals, not the physical microbumps (see [Figure 82](#)). For example, if DQ3 has been repaired (which routes the DQ3 data to the DQ4 microbump) the data received on the DQ4 microbump is routed to the DQ3 Rise and Fall MISR bits. Effectively, the behaviors for all MISR modes are unchanged when Mode 2 lane repairs are active - all 10 bits of the byte are captured in the MISR in the same bit locations, as if no lane repair were active.
- h) **HBM DBI, Write Mask, and ECC logic circuits are not functional in the DWORD MISR modes**
  - The DBI and DM signals are treated as pure data signals. Their raw values are captured, compared, or sent without regard to their normal bus inversion or masking/ECC functional meaning.
    - It is required to enable Write DBIac and Read DBIac in MR0 in order to enable the I/O buffers on the DBI signals.
    - Regardless whether an HBM device supports ECC or not, and regardless whether the ECC feature is enabled or not, setting MR7 DWORD Loopback Enable = 1 will enable the DM signal's I/O buffers.
    - The host may write DBI encoded or non-encoded data to the HBM. In MISR mode or Register mode, the raw data received from the host will be directly captured (not DBI decoded) to the MISR register.

### 6.9.2 General Loopback Modes Features and Behavior (cont'd)

- For LFSR Compare mode to match, the host must send the LFSR generated raw data on all 10 signals of the byte without write DBI encoding. The HBM will not DBI decode the received data, and thus the host must send the raw LFSR data in order for LFSR Compare to match.
  - For LFSR mode, the HBM will generate non-DBI encoded read data.
- i) **Mode 1 lane repair handling of the DBI signal** - In a Mode 1 lane repair, the DBI signal is lost from the interface.
- In MISR mode and Register mode, logical zeros are input into the MISR DBI Rise and Fall bits.
  - In LFSR Compare mode, the HBM LFSR will predict data for the DBI signal, which would miscompare since there is no incoming DBI data. When reading the READ\_LFSR\_COMPARE\_STICKY register the DBI bit for a lane with a Mode 1 repair will read as a pass (logic zero) to avoid indicating an extraneous error.
- j) **DWORD read path parity traffic generation** - In DWORD read LFSR mode, the HBM parity logic is not active and the MR0 DQ Bus Read Parity settings has no effect. To generate traffic on the DWORD parity signal a copy of a nearby DQ signal is produced on the Parity signal. Logical signals DQ2, DQ34, DQ66 and DQ98 are sent on the respective DWORD block parity signals, irrespective of any lane repairs. The parity signals are driven with the DQ data without any additional cycle delay - effectively with Parity Latency = 0. A suggested host-side implementation is to use signature register circuits for checking the validity of the received parity signal. When reading data back using MR7 DWORD Read Mux Control (see [DWORD Read Register Mode](#)), the parity signal output is unspecified.
- k) **AWORD and DWORD write parity checking** - In AWORD and DWORD Register mode, MISR mode, and LFSR Compare mode the HBM parity evaluation logic is active and outputs results on AERR after  $t_{PARAC}$  and DERR after  $t_{PARDQ}$ , respectively (if enabled in MR0, see [Table 9](#)). The MR4 Parity Latency setting (see [Table 15](#)) must be set to a vendor implementation-specific supported PL value, which may be interface speed specific. The HBM device will process write parity per the PL setting and protocol, including any required additional WDQS cycles. A suggested host-side implementation is to use signature register circuits for checking the correctness of the AERR and DERR signals. It is also suggested that the host generate data on the DWORD Parity signals in order to exercise these signal paths and logic.
- l) **Preset state AAAAAh and 2AAAAAAAh** - The Preset state for the DWORD MISR registers is AAAAAh, which initializes the Rise bit for each signal to 1'b0 and the Fall bit to 1'b1. This is a useful state for producing an alternating 0/1/0/1 pattern on all 10 bits associated with a DWORD byte when put into DWORD read Register mode (burst length 4 example). This basic pattern may be used by the host for RDQS eye centering. The AWORD MISR register is also preset to the same 0/1 pattern (2AAAAAAAh for the 30-bit polynomial and 0x2AAAAAAAh for the 34-bit polynomial) for implementation consistency; although the AWORD cannot be enabled to drive this data pattern back to the host. Any non-zero initialization pattern is sufficient for all of the MISR modes; however, an initial pattern of all zeros is a stuck-at-zero state for the DWORD LFSR mode. The Preset state may be overridden using the Write Register modes (see [AWORD and DWORD Write Register Modes](#)).
- m) **DWORD MISR registers are optionally writeable via IEEE 1500** - Optionally, an HBM implementation may permit setting the values of the DWORD MISR registers using the DWORD\_MISR IEEE 1500 port instruction. This feature enables setting alternate seed values, usually for the DWORD Read Register mode (see [DWORD Read Register Mode](#)).

### 6.9.2 General Loopback Modes Features and Behavior (cont'd)

- n) **The DWORD MISR modes operate only in the legacy or PC mode that the given HBM DRAM design supports** - For a legacy mode device, all 4 DWORDs respond to the column commands, exactly as in mission mode. For a PC mode device DWORDs 0 and 1 respond to PC0 column commands and DWORDs 2 and 3 respond to PC1 column commands, exactly as in mission mode.
- o) **DWORD read and write latencies and burst length must be set properly** - READ and WRITE commands are used to generate DWORD MISR modes traffic. Normal mode DWORD read and write protocol is followed using the latency and burst length settings, as supported by the operating frequency being used.
- p) **DWORD Write preamble clocks adhere to the normal protocol** - For DWORD write MISR modes (Register mode, MISR mode, and LFSR Compare mode), the host is expected to send WDQS preamble clocks, and the HBM samples the DWORD data, consistent with the write protocols defined in the section entitled [Write Command \(WR, WRA\)](#).
- q) **DWORD Read preamble and post-amble clocks adhere to the normal protocol** - For DWORD Read LFSR mode, and when returning data with the MR7 DWORD Read Mux Control options, the HBM will produce RDQS preamble and postamble clocks, and send DWORD data, consistent with the read protocols defined in the section entitled [Read Command \(RD, RDA\)](#).
- r) **AWORD MISR modes preamble clock filter** - In the AWORD MISR modes, the host is expected to stop CK toggling, enable the desired AWORD MISR mode, and then start sending CK toggles and AWORD data. To avoid timing impairment on the CK startup cycle, the HBM will treat the first received CK cycle as a preamble clock cycle and not process the data on the AWORD signals in MISR or Register mode, nor compare them in LFSR Compare mode. The MISR block will keep its state unchanged during filter cycle. The first clock cycle filter circuit is enabled by setting AWORD\_MISR\_CONFIG MODE = 3'b000 - Preset. The first data sampled by the HBM is on the second CK clock cycle. Only the very first CK clock cycle will be filtered - if the host were to stop and restart CK clocking while remaining in an AWORD MISR mode (without applying another Preset), the AWORD data will be sampled on the startup clock cycle, with possible CK edge timing impairment.



**Figure 85 — AWORD MISR Modes Preamble Clock Filter Behavior**

- s) **Cycles processed in the MISR modes** - AWORD MISR modes rely on stopping CK clocks before and after the test sequence. All AWORD cycles sent to the HBM after the filtered preamble clock cycle are processed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode), including the last cycle before CK is stopped. For DWORD MISR modes, all valid data cycles written to the HBM are processed into the MISR (MISR mode and Register mode) or compared (LFSR Compare mode) while the DWORD MISR modes are enabled, consistent with the DWORD write protocol and write latency setting. Data pin states during preamble and post-amble cycles are not processed into the MISR. For example, if 10 non-seamless Burst Length = 4 write operations are sent to the HBM in DWORD MISR mode a total of 40 data bit times (UI) will be processed into the MISR.

### 6.9.3 AWORD and DWORD Write MISR Modes

When the AWORD or DWORD MISR modes are active, the data on the AWORD or DWORD data signals is received based on the CK or WDQS clocks respectively, and compressed in the MISR circuits. The host is in complete control of the number of data cycles that are sent, and if successfully received by the HBM the values captured in the respective MISRs will be repeatable and deterministic.

The IEEE 1500 MISR\_MASK instruction may be used for forcing individual MISR inputs to logic 0 in the process of searching for a bad host-to-HBM signal interconnect. Masking a given signal has the effect of forcing it to a known state as input to the MISR. The host is suggested to iterate on masking individual signals and checking for expected MISR signatures. Alternately, see [AWORD and DWORD Write LFSR Compare Modes](#).

#### 6.9.3.1 Test Method for AWORD (Write) MISR Mode

- a) After the required HBM initialization, the host asserts either precharge power-down or self refresh mode (CKE = LOW) and stops sending CK clocks to the HBM (CK\_t = LOW, CK\_c = HIGH).
- b) Initialize the AWORD MISR by setting the AWORD\_MISR\_CONFIG Enable = 1'b1 - On and AWORD\_MISR\_CONFIG MODE = 3'b000 - Preset. The Preset operation also enables the preamble clock filter circuit.
- c) Enable the AWORD MISR mode by setting AWORD\_MISR\_CONFIG Mode = 3'b011 - MISR mode.
- d) The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM clocks the received data into the AWORD MISR and evaluates parity, if enabled. The ending clock state applied by the host is CK\_t = LOW, CK\_c = HIGH.
- e) The host reads the MISR content via the IEEE 1500 AWORD\_MISR instruction.

#### 6.9.3.2 Test Method for DWORD Write MISR Mode

- a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset.
- b) Enable DWORD MISR mode by setting MR7 DWORD MISR Control = 1'b011 - MISR mode.
- c) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM clocks the received data into the DWORD MISRs and evaluates parity, if enabled.
- d) The host reads the MISR content via the IEEE 1500 DWORD\_MISR instruction. The MISR content is also readable via the functional interface (see [DWORD Read Register Mode](#)).

### 6.9.4 AWORD and DWORD Write Register Modes

When the AWORD or DWORD Register modes are active, the data on the AWORD or DWORD data signals is received based on the CK or WDQS clocks respectively, and stored directly into the respective MISR registers without compression. Effectively the MISR register operates as a 2-bit storage register. On rising CK or WDQS edges the signal states on the AWORD or DWORD bus respectively are stored in the Rising bits within the MISR registers, and on falling CK or WDQS edges the bus signal states are stored in the Falling bits within the MISR registers. If the host sends multiple DDR cycles to the HBM, the MISRs will contain the last DDR cycle data, if successfully received by the HBM.

The Register modes are intended for basic, quick link testing and training, and for initializing the DWORD MISR seed values.

#### 6.9.4.1 Test method for AWORD (Write) Register Mode

- a) After the required HBM initialization, the host asserts either precharge power-down or self refresh mode (CKE = LOW) and stops sending CK clocks to the HBM (CK\_t = LOW, CK\_c = HIGH).
- b) Initialize the AWORD MISR by setting the AWORD\_MISR\_CONFIG Enable = 1'b1 - On and AWORD\_MISR\_CONFIG MODE = 3'b000 - Preset. The Preset operation enables the preamble clock filter circuit.
- c) Enable the AWORD Register mode by setting AWORD\_MISR\_CONFIG MODE = 3'b010 - Register mode.
- d) The host sends two or more CK clock cycles and data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM clocks the raw received data into the AWORD MISR register without MISR compression and evaluates parity, if enabled. The ending clock state applied by the host is CK\_t = LOW, CK\_c = HIGH. The last clocked DDR cycle data is retained in the AWORD MISR register.
- e) The host reads the MISR content via the IEEE 1500 AWORD\_MISR instruction.

Note that the AWORD write register mode cannot practically be used to apply an alternate seed value into the AWORD MISR register. In the above procedure in step d) the preamble clock filter circuit is exercised and cleared. At this point while it is allowed for the host to then stop sending AWORD cycles, set the AWORD\_MISR\_CONFIG MODE to MISR mode or LFSR Compare mode, and then send additional AWORD cycles, there may be timing impairment for the beginning of the second set of AWORD cycles. The preamble clock filter circuit cannot be re-enabled for these additional AWORD cycles without applying the AWORD MISR Preset function, which would also overwrite the alternate seed value applied by the AWORD write register operation. There is no expected application value for using an alternate MISR seed value for the AWORD MISR functions since the AWORD bus is receive-only.

#### 6.9.4.2 Test Method for DWORD Write Register Mode

- a) Enable DWORD Register mode by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b010 - Register mode. A Preset is not required prior to using Register mode.
- b) The host sends one or more DWORD write cycles following the write latency and burst length setting and following the normal write protocol. The HBM clocks the raw received data into the DWORD MISR registers without MISR compression and evaluates parity, if enabled. The last clocked DDR cycle data is retained in the DWORD MISR registers. In DWORD Write Register Mode, only PL=0 is allowed.
- c) The host reads the MISR content via the IEEE 1500 DWORD\_MISR instruction. The MISR content is also readable via the functional interface (see [DWORD Read Register Mode](#)).

#### 6.9.5 DWORD Read Register Mode

The content of various DWORD MISR mode related registers may be read over the functional interface, assuming that the read path with the host is properly trained (or used for read path training). The MR7 DWORD Read Mux Control bit field is used to select the data source. The host issues read commands and the HBM responds following the read command protocol (such as read latency and burst length) and timing (such as pre and post-amble clocks) per section [Read Command \(RD, RDA\)](#).

### 6.9.5      DWORD Read Register Mode (cont'd)

Intended uses for the various read data sources include the following:

- Reading the sticky error bits after an LFSR Compare mode test sequence (DWORD Read Mux Control = 2'b11 - Return LFSR\_COMPARE\_STICKY) - Sticky error data is a single data bit per signal and is output as static values on the interface for the full read burst length. Note that support for reading the DWORD LFSR Compare sticky error data over the functional interface is optional.
- NOTE When using the LFSR mode (see [DWORD Read LFSR Mode](#)) set the DWORD Read Mux Control = 2'b01 - Return data from MISR registers.
- Reading a basic clock pattern on all or select signals for DWORD read link training (DWORD Read Mux Control = 2'b01 - Return data from MISR registers) - Which signals toggle may be set with the Preset mode or a DWORD Register write (see [AWORD and DWORD Write Register Modes](#)).
  - Reading the MISR registers final values at the end of a MISR mode test sequence (DWORD Read Mux Control = 2'b01 - Return data from MISR registers) - The results of a MISR mode test sequence may be read back on the functional interface, or via the IEEE 1500 port DWORD\_MISR instruction.
  - Reading what has been captured in the DWORD receive path samplers - Independent from the data in the MISR registers, the last DDR cycle captured in the DWORD receive path functional latches may be read back using DWORD Read Mux Control = 2'b10 - Return data from Rx path sampler.

#### 6.9.5.1    Test Method for DWORD Read Register Mode

- a) Enable the test mode and select the desired read-back register by setting MR7 DWORD Loopback Enable = 1'b1 - Enable, DWORD MISR Control = 3'b010 - Register mode, and DWORD Read Mux Control = one of the defined register sources.
- b) The host sends one or more DWORD read commands. The HBM responds following the read latency and burst length setting and following the normal read protocol.

### 6.9.6      DWORD Read LFSR Mode

When in DWORD Read LFSR mode, the HBM generates DWORD data from the LFSR in response to read commands issued by the host. LFSR data is generated consistent with only the valid UIs of the read protocol. Read Preamble and post-amble RDQS clocks are generated consistent with the read protocol. The first data cycle generated will be the LFSR initial state, based on Preset or an alternate seed value if loaded.

NOTE: There is no AWORD LFSR mode since the AWORD bus cannot source data to the host.

#### 6.9.6.1    Test Method for DWORD Read LFSR Mode

- a) Initialize the test sequence by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and presetting the MISR registers by setting the DWORD MISR Control = 3'b000 - Preset. Optionally, load the DWORD MISR registers with an alternate seed value via the functional interface (see [AWORD and DWORD Write Register Modes](#)).
- b) Enable DWORD LFSR mode by setting MR7 DWORD MISR Control = 3'b001 - LFSR mode and DWORD Read Mux Control = 2'b01 - Return data from MISR registers.
- c) The host sends one or more DWORD read commands. The HBM responds following the read latency and burst length setting and following the normal read protocol, with data produced from the LFSR. A suggested host-side implementation is to use signature register circuits for checking the validity of the received data.

### 6.9.7 AWORD and DWORD Write LFSR Compare Modes

The LFSR Compare modes enable direct identification of failing signal connections between the Host and HBM. It is assumed that the Host implements LFSR data generators that match the lengths and polynomials of the HBM LFSRs, and that the Host and HBM LFSRs start and run in synch. The LFSRs generate DDR data on each signal, and the compare circuitry checks for matching data for each data unit interval (UI). Any mismatch between the data received at the HBM inputs (based on the respective CK or WDQS clocking) and the data predicted by the HBM LFSR will set the sticky error bit for the respective signals. The first data cycle expected from the host and compared by the HBM will be the LFSR initial state, based on Preset or an alternate seed value if loaded.

Once a miscompare is found on a signal, its sticky error bit is set (1'b1) for the remainder of the test sequence. The sticky error bits may be read via the IEEE 1500 port READ\_LFSR\_COMPARE\_STICKY instruction or via the functional interface (optional, see [DWORD Read Register Mode](#)). AWORD sticky error bits are only readable via the IEEE 1500 port. The sticky error bits are reset (1'b0) via the MR7 DWORD MISR Control = 3'b000 - Preset, or IEEE 1500 AWORD\_MISR\_CONFIG MODE = 3'b000 - Preset.

**NOTE:** With Mode 1 repairs on a given byte, the DBI sticky error bit will read as zero within the READ\_LFSR\_COMPARE\_STICKY WDR (see item i) in section entitled [General Loopback Modes Features and Behavior](#)).

Figure 86 illustrates the system-level configuration for LFSR Compare mode.

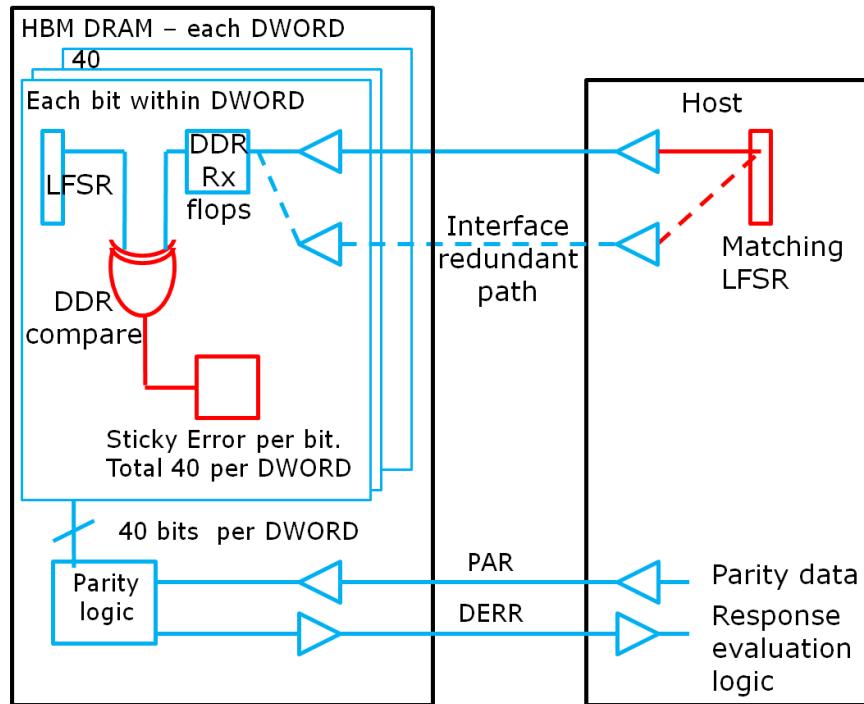


Figure 86 — LFSR Compare Mode Block Diagram

Note that data produced on the DWORD Parity signals from the host to the HBM is an implementation suggestion for exercising the parity signal paths and HBM input timing and logic. The host-side implementation for parity signal generation is not specified. This figure also illustrates that a host-driven logical signal is compared with the matching logical signal data by the HBM compare circuit, regardless of any active lane repairs which may shift the physical signal routing. The AWORD LFSR Compare circuit matches the DWORD circuit except for the non-existent Parity signals.

#### 6.9.7.1 Test method for AWORD (Write) LFSR Compare Mode

- a) After the required HBM initialization, the host asserts either precharge power-down or self refresh mode (CKE = 0) and stops sending CK clocks to the HBM (CK\_t = LOW, CK\_c = HIGH).
- b) Initialize the AWORD MISR (LFSR) register by setting the AWORD\_MISR\_CONFIG Enable = 1'b1 - On and AWORD\_MISR\_CONFIG MODE = 3'b000 - Preset. The Preset operation also clears the AWORD per-signal sticky error bits and enables the preamble clock filter circuit. The host-side LFSR data generator should also be initialized to the same value.
- c) Enable the AWORD LFSR Compare mode by setting AWORD\_MISR\_CONFIG MODE = 3'b100 - LFSR Compare mode.
- d) The host sends two or more CK clock cycles with LFSR-generated data on the AWORD signals. The first received CK clock cycle is discarded as a preamble clock by the HBM. The HBM LFSR predicts expected AWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled. The ending clock state applied by the host is CK\_t = LOW, CK\_c = HIGH.
- e) The host reads the Sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ\_LFSR\_COMPARE\_STICKY instruction.

#### 6.9.7.2 Test Method for DWORD Write LFSR Compare mode

- a) Initialize the DWORD LFSR (MISR) registers by setting MR7 DWORD Loopback Enable = 1'b1 - Enable and DWORD MISR Control = 3'b000 - Preset. The Preset operation also clears the DWORD per-signal sticky error bits. The host-side LFSR data generator should also be preset-initialized to the same value.
- b) Enable DWORD LFSR Compare mode by setting MR7 DWORD MISR Control = 3'b100 - LFSR Compare mode.
- c) The host sends one or more DWORD write cycles with LFSR-generated data on the DWORD signals following the write latency and burst length setting and following the normal write protocol. The HBM LFSRs predict expected DWORD data per cycle from the host, based on matching LFSR polynomials and starting seeds in the host and HBM. Any mismatches set sticky error for the respective signal. Parity is evaluated, if enabled.
- d) The host reads the sticky error bits to determine which signals failed. The bits are readable via the IEEE 1500 port READ\_LFSR\_COMPARE\_STICKY instruction. The sticky error bits are also readable via the functional interface (optional, see [DWORD Read Register Mode](#)).

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## 7 Operating Conditions

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### 7.1 Absolute Maximum DC Rating

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this standard is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 48 — Absolute Maximum DC Ratings**

Parameter	Symbol	Rating	Unit	Notes
Voltage on V <sub>DDC</sub> relative to V <sub>SS</sub>	V <sub>DDC</sub>	-0.3 to 1.5	V	1
Voltage on V <sub>DDQ</sub> relative to V <sub>SS</sub>	V <sub>DDQ</sub>	-0.3 to 1.5	V	1
Voltage on V <sub>PP</sub> relative to V <sub>SS</sub>	V <sub>PP</sub>	-0.3 to 3.0	V	1
Storage Temperature	T <sub>STORAGE</sub>		°C	2
NOTE 1	See <a href="#">HBM Power-up and Initialization Sequence</a> for relationship between power supplies.			
NOTE 2	Storage temperature is the case surface temperature on the center/top side of the HBM device. For the measurement conditions, please refer to JESD51-2 standard.			

### 7.2 Recommended DC Operating Condition

Table 49 specifies the operating condition for V<sub>DDC</sub>, V<sub>DDQ</sub> and V<sub>PP</sub> supply voltages.

**Table 49 — Recommended DC Operating Condition**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Core Supply Voltage	V <sub>DDC</sub>	1.14	1.2	1.26	V	1,2
Supply Voltage for I/O	V <sub>DDQ</sub>	1.14	1.2	1.26	V	1,2
Pump Voltage	V <sub>PP</sub>	2.375	2.5	2.75	V	2
NOTE 1	V <sub>DDC</sub> and V <sub>DDQ</sub> supplies are independent and must not be tied together internally on the HBM DRAM. HBM DRAM must tolerate separate V <sub>DDC</sub> and V <sub>DDQ</sub> power supply regulators.					
NOTE 2	The voltage ranges are defined at the HBM DRAM micropillars. DC bandwidth is limited to 20 MHz.					

### 7.3 Operating Temperature

**Table 50 — Operating Temperature**

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Operating Temperature	T <sub>N</sub>			°C	1
Operating Temperature (Optional)	T <sub>E</sub>			°C	1, 2
NOTE 1	Operating Temperature is the back side temperature of center of the HBM DRAM.				
NOTE 2	Optional and the HBM DRAM may require additional Refresh cycle. Refer to vendor datasheet.				

## 8 Electrical Characteristics

### 8.1 Leakage Current

**Table 51 — Input Leakage Current**

Parameter	Symbol	Minimum	Maximum	Unit	Notes
Input Leakage Current  For R[6:0], C[8:0], CKE, CK_t, CK_c. Any input 0 V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub> . (All inputs pins including IEEE1500 not under test = 0 V)	I <sub>L</sub>	-5	5	uA	

### 8.2 Capacitance

**Table 52 — Input Capacitance**

Parameter	Symbol	1 Gbps		2 Gbps		Unit	Notes
		Min	Max	Min	Max		
HBM Pad Capacitance - DQs, DBI, DM, PAR	C <sub>IO</sub>	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Row & Column Address	C <sub>ADDR</sub>	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Read Strobe	C <sub>RDQS</sub>	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Write Strobe	C <sub>WDQS</sub>	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - Clock	C <sub>CK</sub>	-	0.6	-	0.4	pF	1
HBM Pad Capacitance - DERR, AERR	C <sub>ERROR</sub>	-	0.6	-	0.4	pF	1

NOTE 1 This parameter is not subject to production test.

### 8.3 AC & DC Characteristics

**Table 53 — Input Receiver Voltage Level Specification**

Parameter	Symbol	Min	Max	Unit	Notes
Input HIGH Voltage	V <sub>IH</sub>	0.7 × V <sub>DDQ</sub>		V	1
Input LOW Voltage	V <sub>IL</sub>		0.3 × V <sub>DDQ</sub>	V	1
Differential Input HIGH Voltage	V <sub>IHD</sub>	V <sub>REF</sub> + 0.2	-	V	2
Differential Input LOW Voltage	V <sub>ILD</sub>	-	V <sub>REF</sub> - 0.2	V	2
Input HIGH Voltage for RESET_n and WRST_n	V <sub>IHR</sub>	0.8 × V <sub>DDQ</sub>	-	V	
Input LOW Voltage for RESET_n and WRST_n	V <sub>ILR</sub>	-	0.2 × V <sub>DDQ</sub>	V	

NOTE 1 CMOS input receivers enabled (default mode of operation). For CK\_t, CK\_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS\_t, WDQS\_c, WRCK, SELECTWIR, SHIFTWR, CAPTUREWR, UPDATEWR and WSI inputs.

NOTE 2 V<sub>REF</sub> based input receiver enabled (optional, see MR15). For CK\_t, CK\_c, CKE, C, R, DQ, DBI, DM, PAR, WDQS\_t and WDQS\_c inputs.

#### 8.4 Transmit Driver Currents

HBM drivers have programmable current settings with 20% accuracy. Driver targets, in mA are shown in [Table 54](#) below.

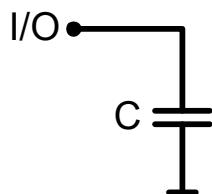
**Table 54 — Transmit Driver Current Specification**

Nominal (mA)	Min (mA)	Max (mA)	Notes
6.0	4.8	7.2	
9.0	7.2	10.8	
12.0	9.6	14.4	
15.0	12.0	18.0	
18.0	14.4	21.6	1

NOTE 1 Implementation support limited to 2 Gbps target EOL data rate products.

#### 8.5 Output Timing Reference Load

$C = C_{TOTAL} - C_{IO}$ ; where  $C_{TOTAL} = 2.4 \text{ pF}$ .



**Figure 87 — Timing Reference Load**

#### 8.6 Output Voltage Level

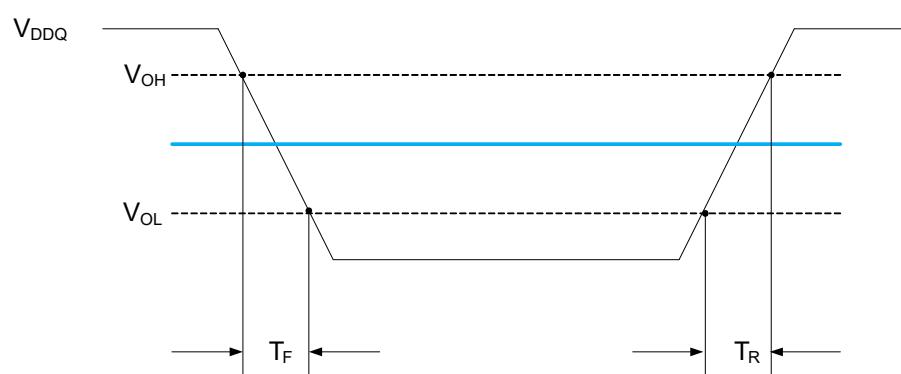
**Table 55 — Output Voltage Level**

Parameter	Symbol	Min	Max	Unit	Notes
Output HIGH Voltage	$V_{OH}$	$0.7 \times V_{DDQ}$		V	
Output LOW Voltage	$V_{OL}$		$0.3 \times V_{DDQ}$	V	

#### 8.7 Output Rise and Fall Time

$T_R = \{ C_{TOTAL} \times (V_{OH} - V_{OL}) \} / I$ ;  $T_F = \{ C_{TOTAL} \times (V_{OH} - V_{OL}) \} / I$ ;

Where  $I$  = Transmit Drive Current in mA.

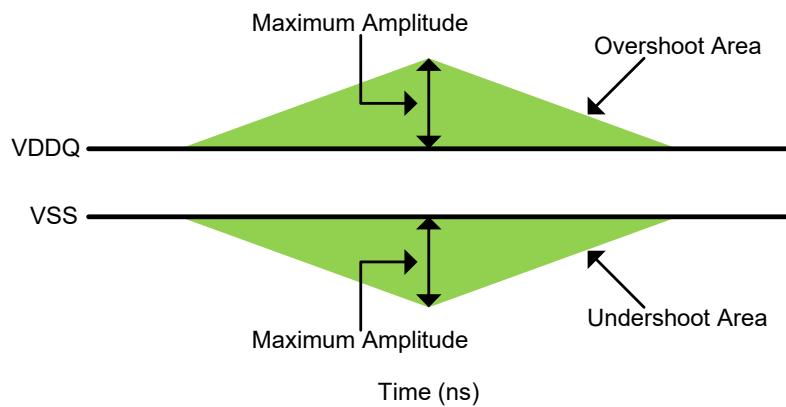


**Figure 88 — Output Rise and Fall Definition**

## 8.8 Overshoot/Undershoot

**Table 56 — Overshoot/Undershoot Specification for R[6:0], C[8:0], DQ[127:0], DM[15:0], DBI[15:0]**

Parameter	1.0 Gbps (BOL)	2.0 Gbps (EOL)	Unit	Notes
Maximum peak amplitude allowed for overshoot area	0.35	0.35	V	
Maximum peak amplitude allowed for undershoot area	0.35	0.35	V	
Maximum overshoot area above V <sub>DDQ</sub>	0.18	0.09	V-ns	
Maximum undershoot area below V <sub>SS</sub>	0.18	0.09	V-ns	



**Figure 89 — Overshoot, Undershoot Definition**

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## 9 IDD Specification

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### 9.1 IDD and IPP Specification Parameters and Test Conditions

This section defines operating current measurement conditions and loop pattern.

- $I_{DD}$  currents are measured as time-averaged currents with all  $V_{DDC}$  microbumps of the HBM device under test tied together.
- $I_{PP}$  currents use the same definitions as  $I_{DD}$  except that the current on the  $V_{PP}$  supply is measured. All  $V_{PP}$  microbumps of the HBM device under test are tied together for  $I_{PP}$  current measurements.
- $I_{DDQ}$  currents are not included in the measurements. Instead, DRAM vendors shall provide simulated values using the  $IDD4R$  measurement-loop pattern as defined in [Table 61](#) and [Table 62](#).
- $I_{DD}$  and  $I_{PP}$  measurements are taken with all channels of the HBM device simultaneously executing the same pattern. However, values in the vendor's datasheet shall be given per channel.

For  $I_{DD}$  measurements, the following definitions apply:

- “0” and “LOW” are defined as  $V_{IN} \leq V_{IL}(\max)$ ;
- “1” and “HIGH” are defined as  $V_{IN} \geq V_{IH}(\min)$ ;
- WL and RL are programmed to appropriate values;
- DBIac is enabled for Reads and Writes;
- DM and parity are disabled;
- ECC is enabled if supported by the device;
- Bank groups are enabled if required for device operation at  $t_{CK}(\min)$ ;
- Each data byte consists of eight DQs, one DM and one DBI pin;
- CNOP/RNOP commands and all address inputs are stable during idle command cycles;
- Some  $I_{DD}$  Measurement-Loop pattern use high order address bits RA14 and RA13 which are not defined for all densities. In those cases the respective undefined address bit(s) shall be kept LOW.
- Basic  $I_{DD}$  Measurement Conditions are described in [Table 57](#).
- $I_{DD}$  Measurements are done after properly initializing the HBM device. This includes the pre-load of the memory array with data pattern used with  $IDD4R$  measurements.
- The  $I_{DD}$  Measurement-Loop patterns shall be executed at least once before actual  $I_{DD}$  measurement is started.
- For timing parameters used with  $I_{DD}$  Measurement-Loop pattern:  $nRC = t_{RC}/t_{CK}$ ;  $nRAS = t_{RAS}/t_{CK}$ ,  $nRP = t_{RP}/t_{CK}$ ,  $nRFC = t_{RFC}/t_{CK}$ . If not already an integer, round up to the next integer.

## 9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

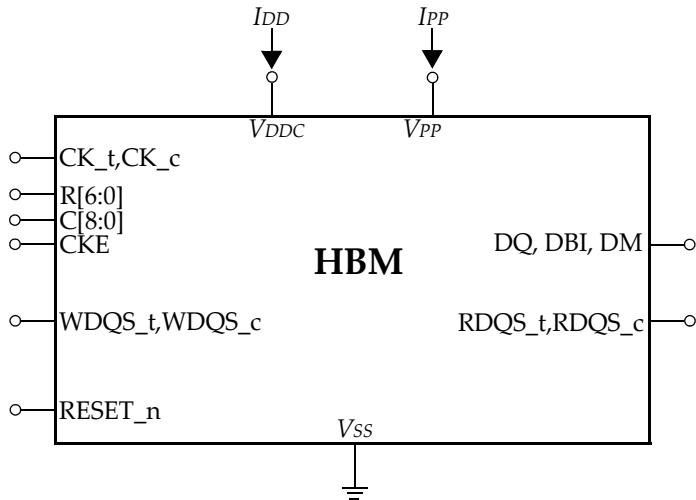


Figure 90 — Measurement Setup for IDD and IPP Measurements

Table 57 — Basic IDD Measurement Conditions

Parameter/Condition	Symbol
<b>One Bank Activate Precharge Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; $t_{RC}$ , $t_{RAS}$ and $t_{RP}$ as defined in <a href="#">Table 58</a> ; CKE is HIGH; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW; bank and row addresses with ACT and PRE commands as defined in <a href="#">Table 59</a> or <a href="#">Table 60</a>	I <sub>DD0</sub>
<b>Precharge Power-down Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; all banks are idle; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD2P</sub>
<b>Precharge Power-down Current with clock stop:</b> CK <sub>t</sub> is LOW; CK <sub>c</sub> is HIGH; all banks are idle; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD2P0</sub>
<b>Precharge Standby Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; all banks are idle; CKE is HIGH; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD2N</sub>
<b>Active Power-down Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; one bank is active; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD3P</sub>
<b>Active Power-down Current with clock stop:</b> CK <sub>t</sub> is LOW; CK <sub>c</sub> is HIGH; one bank is active; CKE is LOW; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD3P0</sub>
<b>Active Standby Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; one bank is active; CKE is HIGH; R and C inputs are HIGH; DQ, DM and DBI inputs are LOW	I <sub>DD3N</sub>
<b>Read Burst Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; CKE is HIGH; all banks activated; continuous read burst across bank groups as defined in <a href="#">Table 61</a> or <a href="#">Table 62</a> ; $I_{OUT} = 0\text{mA}$	I <sub>DD4R</sub>
<b>Write Burst Current:</b> $t_{CK} = t_{CK}(\text{min})$ ; CKE is HIGH; all banks activated; continuous write burst across bank groups as defined in <a href="#">Table 63</a> or <a href="#">Table 64</a>	I <sub>DD4W</sub>

**Table 57 — Basic IDD Measurement Conditions (cont'd)**

Parameter/Condition	Symbol
<b>All-bank Refresh Average Current:</b> $t_{CK} = t_{CK}(\min)$ ; $t_{RFC} = t_{REFI}(\min)$ ; CKE is HIGH between valid commands; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW	$I_{DD5A}$
<b>All-bank Refresh Burst Current:</b> $t_{CK} = t_{CK}(\min)$ ; $t_{RFC}$ as defined in <a href="#">Table 58</a> ; CKE is HIGH between valid commands; R and C inputs are HIGH between valid commands; DQ, DM and DBI inputs are LOW	$I_{DD5B}$
<b>Self Refresh Current:</b> CKE is LOW; R and C inputs are LOW; DQ, DM and DBI inputs are LOW	$I_{DD6x}$
<b>Reset Low Current:</b> RESET_n is LOW; CK_t, CK_c, WDQS_t, WDQS_c and CKE are LOW; R and C inputs are LOW; DQ, DM and DBI inputs are LOW; Note: Reset low current reading is valid once power is stable and RESET_n has been LOW for at least 1ms	$I_{DD8}$

**Table 58 — Timings used for IDD Measurement-Loop Pattern**

Parameter	Value	Unit	
$t_{RC}$	48	ns	
$t_{RAS}$	33	ns	
$t_{RP}$	15	ns	
$t_{RFC}$	1 Gb	110	ns
	2 Gb	160	ns
	4 Gb	260	ns
	8 Gb	350	ns
	16 Gb	450	ns
NOTE DRAM vendors may decide to use different values for $t_{RAS}$ and $t_{RP}$ ; however, nRAS + nRP = nRC must be achieved.			

**Table 59 — IDD0 Measurement-Loop Pattern - Legacy Mode**

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[13:0])	Col Address (CA[5:0])
0	0	ACT	CNOP	00h	01555h	N/A
	1		CNOP			N/A
	2	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRAS)				
	nRAS + 1	PRE	CNOP	00h	N/A	N/A
	nRAS + 2	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRC - 1)				
1	nRC	repeat sub-loop 0 pattern until cycle ( $2 \times nRC - 1$ ); use BA = 05h and RA = 02AAAh instead				
2	$2 \times nRC$	repeat sub-loop 0 pattern until cycle ( $3 \times nRC - 1$ ); use BA = 02h and RA = 01555h instead				
3	$3 \times nRC$	repeat sub-loop 0 pattern until cycle ( $4 \times nRC - 1$ ); use BA = 07h and RA = 02AAAh instead				
4	$4 \times nRC$	repeat sub-loop 0 pattern until cycle ( $5 \times nRC - 1$ ); use BA = 01h and RA = 01555h instead				
5	$5 \times nRC$	repeat sub-loop 0 pattern until cycle ( $6 \times nRC - 1$ ); use BA = 06h and RA = 02AAAh instead				
6	$6 \times nRC$	repeat sub-loop 0 pattern until cycle ( $7 \times nRC - 1$ ); use BA = 03h and RA = 01555h instead				
7	$7 \times nRC$	repeat sub-loop 0 pattern until cycle ( $8 \times nRC - 1$ ); use BA = 04h and RA = 02AAAh instead				
8 to 15	for 16-bank devices: repeat sub-loops 0 to 7 pattern; use BA3 = 1 instead					

## 9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

**Table 60 — IDD0 Measurement-Loop Pattern - Pseudo Channel Mode**

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[14:0])	Col Address (CA[5:1])
0	0	ACT - PC0	CNOP	00h	05555h	N/A
	1		CNOP			N/A
	2	ACT - PC1	CNOP	00h	05555h	N/A
	3		CNOP			N/A
	4	RNOP	CNOP	N/A	N/A	N/A
	...	repeat pattern until cycle (nRAS)				
	nRAS + 1	PRE - PC0	CNOP	00h	N/A	N/A
	nRAS + 2	RNOP	CNOP	N/A	N/A	N/A
	nRAS + 3	PRE - PC1	CNOP	00h	N/A	N/A
	nRAS + 4	RNOP	CNOP	N/A	N/A	N/A
1	...	repeat pattern until cycle (nRC - 1)				
	nRC	repeat sub-loop 0 pattern until cycle ( $2 \times nRC - 1$ ); use BA = 05h and RA = 02AAAh instead				
	$2 \times nRC$	repeat sub-loop 0 pattern until cycle ( $3 \times nRC - 1$ ); use BA = 02h and RA = 05555h instead				
	$3 \times nRC$	repeat sub-loop 0 pattern until cycle ( $4 \times nRC - 1$ ); use BA = 07h and RA = 02AAAh instead				
	$4 \times nRC$	repeat sub-loop 0 pattern until cycle ( $5 \times nRC - 1$ ); use BA = 01h and RA = 05555h instead				
	$5 \times nRC$	repeat sub-loop 0 pattern until cycle ( $6 \times nRC - 1$ ); use BA = 06h and RA = 02AAAh instead				
	$6 \times nRC$	repeat sub-loop 0 pattern until cycle ( $7 \times nRC - 1$ ); use BA = 03h and RA = 05555h instead				
	$7 \times nRC$	repeat sub-loop 0 pattern until cycle ( $8 \times nRC - 1$ ); use BA = 04h and RA = 02AAAh instead				
	8 to 15	for 16-bank devices: repeat sub-loops 0 to 7 pattern; use BA3 = 1 instead				
	16 to 31	for 8-High devices: repeat sub-loops 0 to 15 pattern; use SID = 1 instead for 12-High devices: repeat sub-loops 0 to 15 pattern; use SID[1:0] = 01 instead				
	32 to 47	for 12-High devices: repeat sub-loops 0 to 15 pattern; use SID[1:0] = 10 instead				

**Table 61 — IDD4R Measurement-Loop Pattern - Legacy Mode**

## 9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

**Table 62 — IDD4R Measurement-Loop Pattern - Pseudo Channel Mode**

**Table 63 — IDD4W Measurement-Loop Pattern - Legacy Mode**

## 9.1 IDD and IPP Specification Parameters and Test Conditions (cont'd)

**Table 64 — IDD4W Measurement-Loop Pattern - Pseudo Channel Mode**

Sub-Loop	Cycle Number	Row Command	Column Command	Bank Address (BA[3:0])	Row Address (RA[14:0])	Col Address (CA[5:1])	Data Pattern (1 Byte)
0	0	RNOP	WRITE - PC0	00h	05555h	01010b	00h, 55h, FFh, AAh
	1	RNOP	WRITE - PC1	00h	05555h	01010b	00h, 55h, FFh, AAh
	2	RNOP	WRITE - PC0	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	3	RNOP	WRITE - PC1	05h	02AAAh	10101b	00h, 55h, FFh, AAh
	4	RNOP	WRITE - PC0	02h	05555h	01010b	00h, 55h, FFh, AAh
	5	RNOP	WRITE - PC1	02h	05555h	01010b	00h, 55h, FFh, AAh
	6	RNOP	WRITE - PC0	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	7	RNOP	WRITE - PC1	07h	02AAAh	10101b	00h, 55h, FFh, AAh
	8	RNOP	WRITE - PC0	01h	05555h	01010b	00h, 55h, FFh, AAh
	9	RNOP	WRITE - PC1	01h	05555h	01010b	00h, 55h, FFh, AAh
	10	RNOP	WRITE - PC0	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	11	RNOP	WRITE - PC1	06h	02AAAh	10101b	00h, 55h, FFh, AAh
	12	RNOP	WRITE - PC0	03h	05555h	01010b	00h, 55h, FFh, AAh
	13	RNOP	WRITE - PC1	03h	05555h	01010b	00h, 55h, FFh, AAh
	14	RNOP	WRITE - PC0	04h	02AAAh	10101b	00h, 55h, FFh, AAh
	15	RNOP	WRITE - PC1	04h	02AAAh	10101b	00h, 55h, FFh, AAh
1	for 16-bank devices: repeat sub-loop 0 pattern; use BA3 = 1 instead						
2	for 8-High devices: repeat sub-loops 0 and 1 pattern; use SID = 1 instead for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 01 instead						
3	for 12-High devices: repeat sub-loops 0 and 1 pattern; use SID[1:0] = 10 instead						

## 9.2 IDD and IPP Specifications

IDD and IPP values are valid for the full operating range of voltage and temperature unless otherwise noted.

**Table 65 — IDD and IPP Specification Example**

SYMBOL	Speed Bin			Notes
	IDD (Max)	IPP (Max)	Unit	
IDD0			mA	
IDD2P			mA	
IDD2P0			mA	
IDD2N			mA	
IDD3P			mA	
IDD3P0			mA	
IDD3N			mA	
IDD4R			mA	
IDD4W			mA	
IDD5A			mA	
IDD5B			mA	
IDD6x	see separate table		mA	
IDD8			mA	

### 9.3 IDD6 Specification

**Table 66 — IDD6 Specification**

Symbol	Temperature Range	Value	Unit	Notes
IDD6N	0°C - T <sub>N</sub>		mA	2, 3, 7
IDD6E (Optional)	0°C - T <sub>E</sub>		mA	1, 3, 4, 7
IDD6R (Optional)	0°C - T <sub>R</sub>		mA	3, 5, 7
IDD6A (Optional)	0°C - T <sub>a</sub>		mA	3, 5, 5, 6
	T <sub>b</sub> - T <sub>y</sub> (optional)		mA	3, 5, 5, 6
	T <sub>z</sub> - T <sub>OPERmax</sub>		mA	3, 5, 5, 6, 8
NOTE 1	Max. values for IDD currents considering worst case conditions of process, temperature and voltage.			
NOTE 2	Applicable for MR0 settings OP2=0.			
NOTE 3	Supplier data sheets include a max value.			
NOTE 4	IDD6E is only specified for devices which support the Extended Temperature Range feature.			
NOTE 5	IDD6A is only specified for devices which support the Temperature Controlled Self Refresh feature enabled by MR0 with OP2=1.			
NOTE 6	The number of discrete temperature ranges supported and the associated T <sub>a</sub> - T <sub>z</sub> , and T <sub>OPERmax</sub> values are supplier/design specific. Temperature ranges are intended to denote the nominal trip points for the internal temperature sensor to bracket discrete self refresh rates internal to the DRAM. Refer to supplier datasheet for more information.			
NOTE 7	T <sub>R</sub> represents the temperature used to reflect the current consumed in a typical room temperature environment.			
NOTE 8	T <sub>OPERmax</sub> represents the max temperature supported by the DRAM when TCSR is enabled.			

## 10 AC Timings

**Table 67 — Timing Parameters (Part 1)**

Parameter	Symbol	Speed Bin														Unit	Notes		
		1.0 Gbps/pin		1.6 Gbps/pin		2.0 Gbps/pin		2.4 Gbps/pin		2.8 Gbps/pin		3.2 Gbps/pin		3.6 Gbps/pin					
		Min	Max																
<b>CK Timings</b>																			
CK clock frequency	$f_{CK}$	50	500	50	800	50	1000	50	1200	50	1400	50	1600	50	1800	MHz			
CK clock frequency with bank groups disabled	$f_{CKBG}$	$f_{CK}(\min)$		MHz	4,5														
CK clock period	$t_{CK}$	2.0	20	1.25	20	1.0	20	0.833	20	0.714	20	0.625	20	0.555	20	ns	6		
CK clock differential HIGH-level width	$t_{CH}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK}$			
CK clock differential LOW-level width	$t_{CL}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK}$			
<b>Command and Address Input Timings</b>																			
CKE, command and address input setup time based on $V_{IH}/V_{IL}$	$t_{IS}$	200	—	125	—	100	—	84	—	72	—	63	—	56	—	ps	7		
CKE, command and address input hold time based on $V_{IH}/V_{IL}$	$t_{IH}$	200	—	125	—	100	—	84	—	72	—	63	—	56	—	ps	7		
CKE, command and address input setup time based on $V_{IHD}/V_{ILD}$	$t_{IS2}$	204	—	129	—	104	—	88	—	80	—	71	—	63	—	ps	8		
CKE, command and address input hold time based on $V_{IHD}/V_{ILD}$	$t_{IH2}$	204	—	129	—	104	—	88	—	80	—	71	—	63	—	ps	8		
Command and address input pulse width	$t_{IPW}$	600	—	375	—	300	—	250	—	228	—	200	—	178	—	ps	33		
<b>Data Input Timings</b>																			
WDQS rising edge to CK rising edge delay	$t_{DQSS}$	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	-0.2	0.2	$t_{CK}$			
WDQS differential input HIGH pulse width	$t_{DQSH}$	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	$t_{CK}$			
WDQS differential input LOW pulse width	$t_{DQLS}$	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	—	$t_{CK}$			
WDQS falling edge to CK rising edge setup time	$t_{DSS}$	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	$t_{CK}$			
WDQS falling edge from CK rising edge hold time	$t_{DSH}$	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	—	$t_{CK}$			

**Table 67 — Timing Parameters (Part 1) (cont'd)**

Parameter	Symbol	Speed Bin														Unit	Notes		
		1.0 Gbps/pin		1.6 Gbps/pin		2.0 Gbps/pin		2.4 Gbps/pin		2.8 Gbps/pin		3.2 Gbps/pin		3.6 Gbps/pin					
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max				
<b>Data Input Timings (cont'd)</b>																			
DQ, DM, DBI input to WDQS rising or falling edge setup time based on $V_{IH}/V_{IL}$	$t_{DS}$	200	—	125	—	100	—	84	—	72	—	63	—	56	—	ps	7		
DQ, DM, DBI input to WDQS rising or falling edge hold time based on $V_{IH}/V_{IL}$	$t_{DH}$	200	—	125	—	100	—	84	—	72	—	63	—	56	—	ps	7		
DQ, DM, DBI input to WDQS rising or falling edge setup time based on $V_{IHD}/V_{ILD}$	$t_{DS2}$	204	—	129	—	104	—	88	—	80	—	71	—	63	—	ps	8		
DQ, DM, DBI input to WDQS rising or falling edge hold time based on $V_{IHD}/V_{ILD}$	$t_{DH2}$	204	—	129	—	104	—	88	—	80	—	71	—	63	—	ps	8		
DQ, DM, DBI input pulse width	$t_{DPW}$	600	—	500	—	400	—	250	—	228	—	200	—	178	—	ps	33		
<b>Data Output Timings</b>																			
RDQS rising edge output access time from CK rising edge	$t_{DQSCK}$			0.6	3.5	0.6	3.5	0.6	3.5	0.6	3.5	0.6	3.5	0.6	3.5	ns	9		
RDQS differential output HIGH time	$t_{QSH}$	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	$t_{CK}$	9		
RDQS differential output LOW time	$t_{QSL}$	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	$t_{CK}$	9		
RDQS edge to DQ, DBI skew	$t_{DQSQ}$	—	170	—	106	—	85	—	71	—	61	—	53	—	47	ps	9		
DQ, DBI output hold time from RDQS	$t_{QH}$	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	0.38	—	$t_{CK}$	9		
DQ, DBI high impedance to low impedance time from CK	$t_{LZ}$	Min: $t_{DQSCK}(\text{min}) - t_{QH}(\text{min})$ Max: $t_{DQSCK}(\text{max}) + t_{DQSQ}(\text{max})$												ns	9				
DQ, DBI low impedance to high impedance time from CK	$t_{HZ}$	Min: $t_{DQSCK}(\text{min})$ Max: $t_{DQSCK}(\text{max}) + t_{DQSQ}(\text{max})$												ns	9				

## 10 AC Timings (cont'd)

**Table 68 — Timing Parameters (Part 2)**

Parameter <sup>1,3</sup>	Symbol	Values		Unit	Notes
		MIN	MAX		
<b>Row Access Timings</b>					
ACTIVATE to ACTIVATE command period	$t_{RC}$		—	ns	
ACTIVATE to PRECHARGE command period	$t_{RAS}$		$9 \times t_{REFI}$	ns	10
ACTIVATE to READ command delay	$t_{RCDRD}$		—	ns	
ACTIVATE to WRITE command delay	$t_{RCDWR}$		—	ns	
ACTIVATE to ACTIVATE or SINGLE BANK REFRESH bank B command delay same bank group	$t_{RRDL}$		—	ns	11
ACTIVATE to ACTIVATE or SINGLE BANK REFRESH bank B command delay different bank groups	$t_{RRDS}$		—	ns	12
Four bank activate window	$t_{FAW}$		—	ns	13
READ to PRECHARGE command delay same bank with bank groups enabled	$t_{RTPL}$	BL=2	—	nCK	14,15
BL=4			—	nCK	
READ to PRECHARGE command delay same bank with bank groups disabled	$t_{RTPS}$	BL=2	—	nCK	
BL=4			—	nCK	
PRECHARGE command period	$t_{RP}$		—	ns	
WRITE recovery time	$t_{WR}$		—	ns	
Auto precharge write recovery + precharge time	$t_{DAL}$	—	—	nCK	17
Maximum Activate Window	$t_{MAW}$			μs	
Maximum Activate Count	MAC			-	
<b>Column Access Timings</b>					
RD/WR bank A to RD/WR bank B command delay same bank group	$t_{CCDL}$	BL=2	2	—	nCK
		BL=4	MAX(4, $2.8ns / t_{CK}$ )	—	nCK
RD/WR bank A to RD/WR bank B command delay different bank groups	$t_{CCDS}$	BL=2	1	—	nCK
		BL=4	2	—	nCK
RD SID A to RD SID B command delay	$t_{CCDR}$	BL=4		—	nCK
Internal WRITE to READ command delay same bank group	$t_{WTRL}$			—	nCK
Internal WRITE to READ command delay different bank groups	$t_{WTRS}$			—	nCK
READ to WRITE command delay	$t_{RTW}$			—	ns
<b>Power-Down Timings</b>					
Power-down entry to exit time	$t_{PD}$	$t_{CKE}(\min)$	$9 \times t_{REFI}$	ns	
Power-down exit time	$t_{XP}$		—	nCK	
CKE min. HIGH and LOW pulse width	$t_{CKE}$	MAX(7.5, $5 \times t_{CK}$ )	—	ns	
Command path disable delay	$t_{CPDED}$	2	—	nCK	
ACTIVATE to POWER-DOWN ENTRY command delay	$t_{ACTPDE}$	1	—	nCK	24
Implicit Precharge to POWER-DOWN ENTRY command delay	$t_{IMPREPDE}$	$(t_{RP} / t_{CK}) + 1$	—	nCK	24

**Table 68 — Timing Parameters (Part 2) (cont'd)**

Parameter <sup>1,3</sup>	Symbol	Values		Unit	Notes
		MIN	MAX		
<b>Power-Down Timings (cont'd)</b>					
PRECHARGE to POWER-DOWN-ENTRY command delay	$t_{PRPDE}$	1	—	nCK	
REFRESH to POWER-DOWN ENTRY command delay	$t_{REFPDE}$	1	—	nCK	24
SINGLE BANK REFRESH to POWER-DOWN ENTRY command delay	$t_{REFSBPDE}$	1	—	nCK	24
MODE REGISTER SET to POWER-DOWN ENTRY command delay	$t_{MRSPDE}$	$t_{MOD}(\min)$	—	nCK	
READ or READ w/ AP to POWER-DOWN ENTRY command delay	$t_{RDPDE}$	$RL + PL + BL/2 + 1$	—	nCK	
WRITE to POWER-DOWN-ENTRY command delay	$t_{WRPDE}$	$WL + PL + BL/2 + 1 + (t_{WR} / t_{CK})$	—	nCK	25
WRITE w/ AP to POWER-DOWN-ENTRY command delay	$t_{WRAPDE}$	$WL + PL + BL/2 + 1 + WR$	—	nCK	26
<b>Self Refresh Timings</b>					
CKE min. LOW width for self refresh entry to exit	$t_{CKESR}$	$t_{CKE}(\min) + 1$	—	nCK	
Valid CK clocks required after self refresh or power-down entry	$t_{CKSRE}$	$\text{MAX}(5, 10\text{ns} / t_{CK})$	—	nCK	
Valid CK clocks required before self refresh or power-down exit	$t_{CKSRX}$	$\text{MAX}(5, 10\text{ns} / t_{CK})$	—	nCK	
READ or READ w/ AP to SELF REFRESH ENTRY command delay	$t_{RDSRE}$	$RL + PL + BL/2 + 1$	—	nCK	
Exit self refresh command delay	$t_{XS}$	$\text{MAX}(5 \times t_{CK}, t_{RFC}(\min) + 10)$	—	ns	
Exit self refresh to MODE REGISTER SET command delay	$t_{XSMRS}$	$t_{XP}(\min)$	—	ns	
<b>Refresh Timings</b>					
REFRESH command period	1 Gb / channel	$t_{RFC}$	110	—	ns 27
	2 Gb / channel		160	—	
	4 Gb / channel		260	—	
	8 Gb / channel		350	—	
	16 Gb / channel		450	—	
SINGLE BANK REFRESH command period (same bank)	1 Gb / die, 2 Gb / die, 4 Gb / die, 8 Gb / die	$t_{RFCB}$	160	—	ns 34
	12 Gb / die, 16 Gb / die		200	—	
SINGLE BANK REFRESH command period (different bank) and SINGLE BANK REFRESH to ACTIVATE (different bank without imPRE) command delay	$t_{RREFD}$	8	—	ns	
Average periodic refresh interval for REFRESH command	$t_{REFI}$	—	3.9	$\mu\text{s}$	28

**Table 68 — Timing Parameters (Part 2) (cont'd)**

Parameter <sup>1,3</sup>	Symbol	Values		Unit	Notes
		MIN	MAX		
<b>Refresh Timings (cont'd)</b>					
Average periodic refresh interval for SINGLE BANK REFRESH command	t <sub>REFISB</sub>	1 Gb / channel, 2 Gb / channel	—	0.4875	μs
		4 Gb / channel, 8 Gb / channel	—	0.2438	μs
		8 Gb 8-High	—	0.1219	μs
<b>Miscellaneous Timings</b>					
MODE REGISTER SET command update delay	t <sub>MOD</sub>		—	nCK	
MODE REGISTER SET command cycle time	t <sub>MRD</sub>		—	nCK	
Internal VREFD offset single step settling time	t <sub>VREFD</sub>		—	ns	30
Internal VREFD offset full range settling time	t <sub>FVREFD</sub>		—	ns	30
ADD/CMD parity error output delay	t <sub>PARAC</sub>			ns	31
Write data parity error output delay	t <sub>PARDQ</sub>			ns	32
NOTE 1	AC timing parameters apply to each channel of the HBM device independently. No timing parameters are specified across channels, and all channels operate independently of each other.				
NOTE 2	Speed bins are shown as examples. Vendors may define different speed bins; in this case it is recommended to scale the values for the related timing parameters.				
NOTE 3	All parameters assume proper device initialization.				
NOTE 4	HBM devices must support device operation with bank groups disabled up to 500MHz or the maximum rated operating clock frequency, whatever is the lower value. Vendor datasheets should be consulted for further details.				
NOTE 5	Bank Group Frequency ranges (not to scale):				
NOTE 6	Parameter t <sub>CK</sub> is calculated as the average clock period across any consecutive 1,000 cycle window, where each clock period is calculated both from rising CK edge to rising CK edge and falling CK edge to falling CK edge.				
NOTE 7	Parameter is based on V <sub>IH</sub> and V <sub>IL</sub> . V <sub>ref</sub> based setup/hold times are calculated by adding ?tDS or ?tDH to these numbers according to Table 69 and the figure below.				
NOTE 8	Parameter is based on V <sub>IHD</sub> and V <sub>ILD</sub> . V <sub>ref</sub> based setup/hold times are calculated by adding ?tDS or ?tDH to these numbers according to Table 69				
NOTE 9	Parameter is measured with Output Timing reference load and Read DBI enabled.				
NOTE 10	For Reads and Writes with auto precharge enabled the device will hold off the internal precharge until t <sub>RAS(min)</sub> has been satisfied or the number of clock cycles as programmed for RAS in MR3 have elapsed.				
NOTE 11	Parameter applies when bank groups are enabled and consecutive commands access the same bank group.				
NOTE 12	Parameter applies when bank groups are disabled or consecutive commands access different bank groups.				
NOTE 13	Not more than 4 ACTIVATE or SINGLE BANK REFRESH commands are allowed within tFAW period.				
NOTE 14	Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.				
NOTE 15	In legacy mode, device operation with bank groups enabled requires BL = 2.				

**Table 68 — Timing Parameters (Part 2) (Cont'd)**

NOTE 16	Parameter applies when bank groups are disabled and READ and PRECHARGE commands access the same bank.
NOTE 17	$t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round up to the next integer.
NOTE 18	Parameter applies when bank groups are enabled and consecutive commands access the same bank group.
NOTE 19	$t_{CCDL}$ is either for seamless consecutive READ or seamless consecutive WRITE commands.
NOTE 20	Parameter applies when bank groups are disabled or consecutive commands access different bank groups.
NOTE 21	$t_{CCDS}$ is either for seamless consecutive READ or seamless consecutive WRITE commands.
NOTE 22	$t_{CCDR}$ is a vendor specific parameter for 8-High HBM devices (DEVICE_ID WDR bit 7 = 1) that should be used for seamless consecutive READ commands between different stack IDs (SID) instead of $t_{CCDS}$ . The $t_{CCDR}(\min)$ value is vendor specific and a range of 2 to 4 nCK is supported. The vendor datasheet should be consulted for details. For seamless WRITE commands the normal $t_{CCDS}$ parameter applies. $t_{CCDR}$ does not apply to DWORD MISR operations when DWORD Loopback is enabled in MR7.
NOTE 23	$t_{RTW}$ is not a DRAM device limit but determined by the system bus turnaround time. Avoid bus contention by setting $t_{RTW} (\min) = (RL + BL/2 - WL + t_{DQSS}(\min) + 0.5) \times t_{CK} + t_{DQSCK}(\max) + t_{DQSQ}(\max)$ , and round up to the next integer.
NOTE 24	Upon entering power-down the CK clock may be stopped after the number of clock cycles as programmed for RAS in MR3.
NOTE 25	$t_{WR}$ is defined in ns. For calculation of $t_{WRPDE}$ round up $t_{WR}/t_{CK}$ to the next integer.
NOTE 26	WR in clock cycles as programmed in MR1.
NOTE 27	Density is given per channel.
NOTE 28	A maximum of 8 consecutive REFRESH commands can be posted to an HBM device, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is $9 \times t_{REFI}$ .
NOTE 29	$t_{REFISB} = t_{REFI} / N$ ; N = no. of banks.
NOTE 30	Internal VREFD offset is optional.
NOTE 31	$t_{PARAC}$ may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The nominal AERR HIGH time in case of a parity error is 1 nCK.
NOTE 32	$t_{PARDQ}$ may be specified as an analog delay or as a combination of n clock cycles and an analog delay. The nominal DERR HIGH time in case of a parity error is 1 nCK.
NOTE 33	$t_{IPW}$ and $t_{DPW}$ are based on $V_{REF}$ level.
NOTE 34	Density is given per die.

**Table 69 — Derating Value Table for Setup/Hold Timings**

Slew Rate [V/ns]	$(V_{IH} = 0.7 \times V_{DDQ}, V_{IL} = 0.3 \times V_{DDQ})$		VREF Based Input Receiver $(V_{IHD} = V_{REF} + 0.2V, V_{ILD} = V_{REF} - 0.2V)$		Unit
	$\Delta t_{DS}$	$\Delta t_{DH}$	$\Delta t_{DS}$	$\Delta t_{DH}$	
2	120	120	100	100	ps
3	80	80	67	67	ps
4	60	60	50	50	ps
5	48	48	40	40	ps
6	40	40	33	33	ps
7	34	34	29	29	ps
8	30	30	25	25	ps
9	27	27	22	22	ps
10	24	24	20	20	ps

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## 11 Package (Die) Specification

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### 11.1 Signals

**Table 70 — I/O Signal Description**

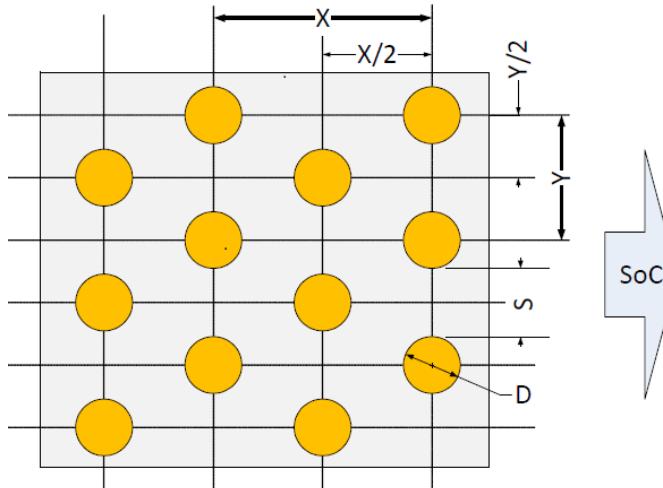
Signals	Type	Description
CK[a:h]_t, CK[a:h]_c	Input	Clock: CK_t and CK_c are differential clock inputs. Row and column command and address inputs are latched on the rising and falling edges of CK. CKE is latched on the rising edge of CK only. All latencies are referenced to the rising edge of CK.
CKE[a:h]	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, device input buffers, and output drivers. Taking CKE LOW provides precharge power-down and self refresh operations (all banks idle), or active power-down (row activated in any bank). CKE must be maintained HIGH throughout read and write accesses.
C[a:h][8:0]	Input	Column command and address: the command code, bank and column address for Write and Read operations and the mode register address and code to be loaded with MODE REGISTER SET commands are received on the C[8:0] inputs. Input C8 (along with input R6) is only present for device configurations that include row address RA14 or bank address SID1 or both; otherwise, this input is reserved (ARFU0). See <a href="#">HBM Channel Addressing table</a> .
R[a:h][6:0]	Input	Row command and address: the command code, bank and row address for Activate, Precharge and Refresh commands are received on the R[6:0] inputs. Input R6 (along with input C8) is only present for device configurations that include row address RA14 or bank address SID1 or both; otherwise, this input is reserved (ARFU2). See <a href="#">HBM Channel Addressing table</a> .
DQ[a:h][127:0]	I/O	Data Input/Output: 128-bit data bus
DBI[a:h][15:0]	I/O	Data Bus Inversion: DBI0 is associated with DQ[7:0], DBI1 is associated with DQ[15:8], ..., and DBI15 is associated with DQ[127:120].
DM[a:h][15:0]	I/O	Data Mask: DM0 is associated with DQ[7:0], DM1 is associated with DQ[15:8], ..., and DM15 is associated with DQ[127:120].
PAR[a:h][3:0]	I/O	Data Parity: one data parity bit per DWord. PAR0 is associated with DQ[31:0], PAR1 is associated with DQ[63:32], PAR2 is associated with DQ[95:64], and PAR3 is associated with DQ[127:96].
DERR[a:h][3:0]	Output	Data parity error: one data parity error bit per DWord. DERR0 is associated with DQ[31:0], DERR1 is associated with DQ[63:32], DERR2 is associated with DQ[95:64], and DERR3 is associated with [127:96].
AERR[a:h]	Output	Address parity error. One address parity error bit for row and column address and command per channel.
WDQS[a:h][3:0]_t, WDQS[a:h][3:0]_c	Input	Write Data Strobe: WDQS_t and WDQS_c are differential strobe inputs. Write input data are latched on the rising and falling edges of WDQS. One WDQS pair per DWord. WDQS0 is associated with DQ[31:0], WDQS1 is associated with DQ[63:32], WDQS2 is associated with DQ[95:64], and WDQS3 is associated with DQ[127:96].
RDQS[a:h][3:0]_t, RDQS[a:h][3:0]_c	Output	Read Data Strobe: RDQS_t and RDQS_c are differential strobe outputs. Read output data are sent on the rising and falling edges of RDQS. One RDQS pair per DWord. RDQS0 is associated with DQ[31:0], RDQS1 is associated with DQ[63:32], RDQS2 is associated with DQ[95:64], and RDQS3 is associated with DQ[127:96].

**Table 70 — I/O Signal Description (cont'd)**

Signals	Type	Description
DA[59:0]	I/O	Direct Access Input/Output: These pins are provided for direct access test. They must be routed directly to an external package I/O pin. The function is defined by the memory vendor.
RESET_n	Input	Reset: RESET_n LOW asynchronously initiates a full chip reset of the HBM device.
NC		No connect pad: electrically isolated
WRCK	Input	IEEE-1500 Wrapper Serial Port Clock
WRST_n	Input	IEEE-1500 Wrapper Serial Port Reset
SelectWIR	Input	IEEE-1500 Wrapper Serial Port Instruction Register Select
ShiftWR	Input	IEEE-1500 Wrapper Serial Port Shift
CaptureWR	Input	IEEE-1500 Wrapper Serial Port Capture
UpdateWR	Input	IEEE-1500 Wrapper Serial Port Update
WSI	Input	IEEE-1500 Wrapper Serial Port Data
WSO[a:h]	Output	IEEE-1500 Wrapper Serial Port Data Out
RSVD[5:0]		Reserved pad: reserved for future use for TEST (DRAM Vendor Probe only point)
RD[a:h][7:0]	I/O	Redundant microbumps in DWORD
RC[a:h]	Input	Redundant column command and address microbump in AWORD
RR[a:h]	Input	Redundant row command and address microbump in AWORD
ARFU[a:h][3:0]		Reserved for future use; unused microbumps in AWORD. Device configurations that include row address RA14 or bank address SID1 or both use inputs ARFU0 and ARFU2 as command and address inputs C8 and R6, respectively.
MRFU[23:0]		Reserved for future use, unused microbumps in mid-stack region
NOBUMP		Depopulated pad: reserved as test pad for probing
TEMP[2:0]	Output	DRAM Temperature Report
CATTRIP	Output	DRAM Catastrophic Temperature Report
Vss	Supply	Ground
VDDC, V <sub>DDQ</sub> , V <sub>PP</sub>	Supply	Power supply
NOTE 1	Index [a:h] represents the channel indicator “a” to “h” of the HBM device; signal names including the channel indicator are used whenever more than one channel is referenced, as e.g., with the HBM ball-out. The channel indicator is omitted whenever features and functions common to all channels are described.	
NOTE 2	A 4-channel HBM device comprises channels a to d.	
NOTE 3	HBM devices supporting less than 8 channels are allowed to have input/output buffers physically present at the pins associated with the unavailable channels, however these input/output buffers will be disabled. The host shall leave those pins floating. The availability of each channel [a:h] has to be coded in IEEE1500 bits [15:8].	
NOTE 4	All power supply microbumps defined in <a href="#">Table 76</a> to <a href="#">Table 79</a> must be present and connected with their respective power nets even if the related channel is not present or marked non-working.	

## 11.2 MicroBump Positions

The MicroBump array of the DRAM stack employs a staggered pattern as depicted in [Figure 91](#) where a ‘staggered’ bump is located halfway between major row and column, hence its location is determined by  $X/2$  and  $Y/2$ . [Table 71](#) shows geometric parameters of the Staggered MicroBump pattern. Parameter  $P_{Min}$  is the minimum bump pitch anywhere in the MicroBump field; for chosen X and Y parameters, it coincides with the vertical pitch, i.e.,  $P_{Min} = Y$ .



**Figure 91 — Staggered MicroBump Pattern**

**Table 71 — Geometric Parameters of the Staggered MicroBump Pattern**

Label	Nominal Value	Description
X	96 $\mu\text{m}$	Horizontal pitch of two adjacent MicroBumps
Y	55 $\mu\text{m}$	Vertical pitch of two adjacent MicroBumps
$P_{Min}$	55 $\mu\text{m}$	Minimum pitch of the bump field; Same as Y for chosen X and Y parameters
D	25 $\mu\text{m}$	MicroBump diameter
S		Bump-to-bump air gap; $S = P_{Min} - D$

Two HBM bump matrices are defined as shown in subsequent tables. Vendor datasheets should be consulted regarding the supported bump matrix, however, HBM devices that include input pins R6 and C8 (see [Table 70](#)) are required to support the larger bump matrix (Footprint B). Please refer to MO-316B for device dimensions.

- Footprint A consists of 220 rows with a pitch of  $Y/2$  and 68 columns with a pitch of  $X/2$ . The overall array size is  $(67 \times X/2 + D) \times (219 \times Y/2 + D) = 3241 \mu\text{m} \times 6047.5 \mu\text{m}$ . The ball matrix is center aligned with the die. The ball array center is the origin of the ball location coordinates. Ball A1 is located at the top left at  $X = -1608 \mu\text{m}$ ,  $Y = +3011.25 \mu\text{m}$ .
- Footprint B consists of 300 rows with a pitch of  $Y/2$  and 68 columns with a pitch of  $X/2$ . The overall array size is  $(67 \times X/2 + D) \times (299 \times Y/2 + D) = 3241 \mu\text{m} \times 8247.5 \mu\text{m}$ . The ball matrix is center aligned with the die. The ball array center is the origin of the ball location coordinates. Ball A1 is located at the top left at  $X = -1608 \mu\text{m}$ ,  $Y = +4111.25 \mu\text{m}$ .

### 11.3 HBM Stack Height

**Table 72 — Stack Height**

Configuration	Minimum	Typical	Maximum	Unit
2-High	695	720	745	μm
4-High	695	720	745	μm
8-High	695	720	745	μm
12-High				μm

NOTE 1 The configuration refers to the number of memory dies in the stack. The stack may include an additional base (interface) die.

NOTE 2 HBM stack height refers to the "A2" dimension and is compliant to package code "W" of MO-316 Rev. B. The "A2" dimension does not include the microbumps.

### 11.4 HBM Ballout

A geographical overview of the HBM bump matrices is provided in [Table 74](#) for Footprint A and in [Table 75](#) for Footprint B, and the detailed bump matrices are provided in [Table 76](#) thru [Table 79](#).

Due to space constraints these tables use abbreviations for specific functions as given in [Table 73](#). The orientation of the ballout shown is the bottom view looking at the microbumps.

HBM devices supporting less than 8 channels must have all microbumps physically present as shown in the tables below.

**Table 73 — Legend**

VPP	A	VSS	D
NC	B	VDDC	E
No Bump	C	VDDQ	M

## 11.4 HBM Ballout (cont'd)

**Table 74 — HBM Ballout Footprint A - Geographical Overview (not to scale)**

		See <a href="#">Table</a>			See <a href="#">Table 77</a>			
Columns		1 ... 8	9 ... 20	21 ... 44	45 ... 56	57 ... 68		
R o w s	A ... M	Mechanical Bumps	Direct Access Test Port	Power Supply Region	DWORD0 Channel e	DWORD0 Channel a		
	N ... AD				DWORD0 Channel f	DWORD0 Channel b		
	AE ... AT				DWORD1 Channel e	DWORD1 Channel a		
	AU ... BH				DWORD1 Channel f	DWORD1 Channel b		
	BJ ... BP				AWORD Channel e	AWORD Channel a		
	BR ... BY				AWORD Channel f	AWORD Channel b		
	CA ... CM				DWORD2 Channel e	DWORD2 Channel a		
	CN ... DD				DWORD2 Channel f	DWORD2 Channel b		
	DE ... DT				DWORD3 Channel e	DWORD3 Channel a		
	DU ... ED				DWORD3 Channel f	DWORD3 Channel b		
	EE ... EH	Depopulated micropillar area dedicated for (optional) probe pads			Reset, IEEE1500 Port, Temperature			
	EJ ... EM				DWORD0 Channel g	DWORD0 Channel c		
	EN ... ET				DWORD0 Channel h	DWORD0 Channel d		
	EU ... FD	Mechanical Bumps	Direct Access Test Port	Power Supply Region	DWORD1 Channel g	DWORD1 Channel c		
	FE ... FT				DWORD1 Channel h	DWORD1 Channel d		
	FU ... GH				AWORD Channel g	AWORD Channel c		
	GJ ... GY				AWORD Channel h	AWORD Channel d		
	HA ... HF				DWORD2 Channel g	DWORD2 Channel c		
	HG ... HM				DWORD2 Channel h	DWORD2 Channel d		
	HN ... JD				DWORD3 Channel g	DWORD3 Channel c		
	JE ... JT				DWORD3 Channel h	DWORD3 Channel d		
	JU ... KH							
	KJ ... KY							

## 11.4 HBM Ballout (cont'd)

**Table 75 — HBM Ballout Footprint B - Geographical Overview (not to scale)**

		See <b>Table 78</b>			See <b>Table 79</b>	
Columns		1 ... 8	9 ... 20	21 ... 44	45 ... 56	57 ... 68
R o w s	A ... AY	Mechanical Bumps	Upper Left Power Supply Region		Upper Right Power Supply Region	
	BA ... BM				DWORD0 Channel e	DWORD0 Channel a
	BN ... CD				DWORD0 Channel f	DWORD0 Channel b
	CE ... CT				DWORD1 Channel e	DWORD1 Channel a
	CU ... DH				DWORD1 Channel f	DWORD1 Channel b
	DJ ... DP				AWORD Channel e	AWORD Channel a
	DR ... DY				AWORD Channel f	AWORD Channel b
	EA ... EM				DWORD2 Channel e	DWORD2 Channel a
	EN ... FD				DWORD2 Channel f	DWORD2 Channel b
	FE ... FT				DWORD3 Channel e	DWORD3 Channel a
	FU ... GD				DWORD3 Channel f	DWORD3 Channel b
	GE ... GH		Depopulated micropillar area dedicated for (optional) probe pads		Reset, IEEE1500 Port, Temperature	
	GJ ... GM				DWORD0 Channel g	DWORD0 Channel c
	GN ... GT				DWORD0 Channel h	DWORD0 Channel d
	GU ... HD				DWORD1 Channel g	DWORD1 Channel c
	HE ... HT				DWORD1 Channel h	DWORD1 Channel d
	HU ... JH				AWORD Channel g	AWORD Channel c
	JJ ... JY				AWORD Channel h	AWORD Channel d
	KA ... KF				DWORD2 Channel g	DWORD2 Channel c
	KG ... KM				DWORD2 Channel h	DWORD2 Channel d
	KN ... LD				DWORD3 Channel g	DWORD3 Channel c
	LE ... LT				DWORD3 Channel h	DWORD3 Channel d
	LU ... MH	Mechanical Bumps	Lower Left Power Supply Region		Lower Right Power Supply Region	
	MJ ... MY					
	NA ... PY					

## 11.4 HBM Ballout (cont'd)

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
A	B		B		C		B		C		D		B		C		D		A		C		D		E		C		D		E		C		D		E		C		D			
B		C		B		B		C		B		D		C		B		C		D		C		A		D		C		E		D		C		E		D		C				
C	B		B		C		B		B		C		D		B		C		D		A		C		D		E		C		D		E		C		D		C					
D		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
E	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
F		C		B		B		C			D		C		C		D		C		C		A		C		C		E		C		C		E		C		C					
G	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
H		C		B		B		C		D		RSVD 0		C		D		RSVD 1		C		A		D		C		E		C		C		E		D		C						
J	B		B		C		B		D		C		RSVD 0		D		C		RSVD 1		A		C		D		E		C		D		E		C		D							
K		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						
L	B		B		C		B		C		C		B		C		C		B		C		C		D		C		D		C		D		C		D							
M		C		B		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C						
N	B		B		C		B		C		C		E		C		C		E		C		C		D		C		D		C		D		C		D							
P		C		B		B		C		DA0		E		C		DA1		E		C		A		D		C		E		D		C		E		D		C						
R	B		B		C		B		DA0		C		E		DA1		C		E		A		C		D		E		C		D		E		C		D							
T		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
U	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
V		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
W	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
Y		C		B		B		C		E		DA2		C		E		DA3		C		A		D		C		E		D		C		E		D		C						
AA	B		B		C		B		E		C		DA2		E		C		DA3		A		C		D		E		C		D		E		C		D							
AB		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						
AC	B		B		C		B		C		C		B		C		C		B		C		C		D		C		D		C		D		C		D							
AD		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C								
AE	B		B		C		B		C		C		D		C		D		C		C		D		C		C		D		C		C		D		C							
AF		C		B		B		C		DA4		D		C		DA5		D		C		A		D		C		E		D		C		E		D		C						
AG	B		B		C		B		DA4		C		D		DA5		C		D		A		C		D		E		C		D		E		C		D							
AH		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
AJ	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
AK		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
AL	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
AM		C		B		B		C		D		DA6		C		D		DA7		C		A		D		C		E		D		C		E		D		C						
AN	B		B		C		B		D		C		DA6		D		C		DA7		A		C		D		E		C		D		E		C		D							
AP	C		B		B		C		C		B		C		C		B		C		B		C		D		C		E		D		C		E		D							

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
AR	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
AT		C		B		B		C		C		E		C		C		E		C		C		C		D		C		C		D		C		C		D		C				
AU	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D							
AV		C		B		B		C		DA8		E		C		DA9		E		C		A		D		C		E		D		C		E		D		C		C				
AW	B		B		C		B		DA8		C		E		DA9		C		E		A		C		D		E		C		D		E		C		D							
AY		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C		C				
BA	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C		C					
BB		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C				
BC	B		B		C		B		E		C		C		C		E		DA10		C		E		DA11		C		A		C		E		C		C		E		C		C	
BD		C		B		B		C		E		C		C		E		DA10		C		E		DA11		C		A		C		D		C		E		D		C				
BE	B		B		C		B		E		C		DA10		E		C		DA11		A		C		D		E		C		D		E		C		D							
BF		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C		C				
BG	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
BH	C		B		B		C		C		D		C		C		D		C		C		C		D		C		C		D		C		C		D		C					
BJ	B		B		C		B		C		C		D		C		C		C		D		C		C		D		C		C		D		C		D							
BK		C		B		B		C		DA12		D		C		DA13		D		C		A		D		C		E		D		C		E		D		C						
BL	B		B		C		B		DA12		C		D		DA13		C		D		A		C		D		E		C		D		E		C		D							
BM		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
BN	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C		C					
BP		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C		C				
BR	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C		C					
BT		C		B		B		C		D		DA14		C		D		DA15		C		A		D		C		E		D		C		E		D		C						
BU	B		B		C		B		D		C		DA14		D		C		DA15		A		C		D		E		C		D		E		C		D							
BV	C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C		C					
BW	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
BY		C		B		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C		C						
CA	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D							
CB		C		B		B		C		DA16		E		C		DA17		E		C		A		D		C		E		D		C		E		D		C						
CC	B		B		C		B		DA16		C		E		DA17		C		E		A		C		D		E		C		D		E		C		D							
CD		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
CE	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C		C					
CF		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C				
CG	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C					
CH		C		B		B		C		E		DA18		C		E		DA19		C		A		D		C		E		D		C		E		D		C		E		D		C
CJ	B		B		C		B		E		C		DA18		E		C		DA19		A		C		D		E		C		D		E		C		D		C					
CK		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
CL	B		B		C		B		C		C		B		C		C		B		C	C	D		C	C	C	D	C	C	C	D	C	C	D									
CM		C		B		B		C		C		D		C		C		D		C	C	C	D	C	C	C	D	C	C	C	D	C	C	D	C									
CN	B		B		C		B		C		C		D		C		C		D		C	C	D		C	C	C	D	C	C	C	D	C	C	C	D								
CP		C		B		B		C		DA20		D		C		DA21		D		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
CR	B		B		C		B		DA20		C		D		DA21		C		D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	C									
CT		C		B		B		C		B		C		C		B		C		C	A	C	C	E	D	C	C	E	D	C	E	D	C											
CU	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	C									
CV		C		B		B		C		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	C								
CW	B		B		C		B		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	C									
CY		C		B		B		C		D		DA22		C		D		DA23		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
DA	B		B		C		B		D		C		DA22		D		C		DA23		A	C	D	E	C	D	E	C	D	E	C	D	E	C	D									
DB		C		B		B		C		C		B		C		B		C		C	D	C	E	D	C	E	D	C	E	D	C	E	D	C										
DC	B		B		C		B		C		C		B		C		C		B		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D									
DD		C		B		B		C		E		C		C		E		C		C	D	C	C	D	C	C	D	C	C	D	C	C	D	C										
DE	B		B		C		B		C		E		C		C		E		C		C	D	C	C	D	C	C	D	C	C	D	C	C	D										
DF		C		B		B		C		DA24		E		C		DA25		E		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
DG	B		B		C		B		DA24		C		E		DA25		C		E	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D										
DH		C		B		B		C		B		C		C		B		C		C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C									
DJ	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
DK		C		B		B		C		E		C		C		E		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C									
DL	B		B		C		B		E		C		C		E		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
DM		C		B		B		C		E		DA26		C		E		DA27		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
DN	B		B		C		B		E		C		DA26		E		C		DA27		A	C	D	E	C	D	E	C	D	E	C	D	E	C	D									
DP		C		B		B		C		C		B		C		B		C		C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
DR	B		B		C		B		C		C		B		C		C		B		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D									
DT		C		B		B		C		D		C		C		D		C		C	D	C	C	D	C	C	D	C	C	D	C	C	D	C										
DU	B		B		C		B		C		D		C		C		D		C		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D									
DV		C		B		B		C		DA28		D		C		DA29		D		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
DW	B		B		C		B		DA28		C		D		DA29		C		D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D										
DY		C		B		B		C		B		C		C		B		C		C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C									
EA	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
EB		C		B		B		C		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C									
EC	B		B		C		B		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
ED		C		B		B		C		D		B		C		D		B		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44						
EE	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
EF		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
EG	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
EH		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
EJ	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
EK		C		C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
EL	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
EM		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C
EN	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
EP		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C
ER	C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C	
ET		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
EU	B		B		C		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D									
EV		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
EW	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
EY		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
FA	B		B		C		B		B		C		DA30		B		C		DA31		A		C		D		E		C		D		E		C		D							
FB		C		B		B		C		B		DA30		C		B		DA31		C		A		D		C		E		C		D		C		E		D		C				
FC	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		E		C		D					
FD		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C						
FE	B		B		C		B		C		C		E		C		C		C		C		D		C		C		D		C		C		D		C		D					
FF		C		B		B		C		C		E		C		C		C		C		D		C		C		D		C		C		D		C		D		C				
FG	B		B		C		B		DA32		C		E		DA33		C		E		A		C		D		E		C		D		E		C		D		D					
FH		C		B		B		C		DA32		E		C		DA33		E		C		A		D		C		E		D		C		E		D		C		D				
FJ	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D							
FK		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
FL	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
FM		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
FN	B		B		C		B		E		C		DA34		E		C		DA35		A		C		D		E		C		D		E		C		D							
FP		C		B		B		C		E		DA34		C		E		DA35		C		A		D		C		E		D		C		E		D		C						
FR	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
FT		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C						
FU	B		B		C		B		C		D				C		C		D		C		C		D		C		C		D		C		C		D							
FV		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D						
FW	B		B		C		B		DA36		C		D		DA37		C		D		A		C		D		E		C		D		E		C		D							
FY		C		B		B		C		DA36		D		C		DA37		D		C		A		D		C		E		D		C		E		D		C						
GA	B		B		C		B		C		C		B		C		C		C		A		C		C		E		C		D		E		C		D							
GB		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
GC	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
GD		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
GE	B		B		C		B		D		C		DA38		D		C		DA39		A		C		D		E		C		D		E		C		D							
GF		C		B		B		C		D		DA38		C		D		DA39		C		A		D		C		E		D		C		E		D		C						
GG	B		B		C		B		C		B		C		C		B		C		C		D		E		C		D		E		C		D									
GH		C		B		B		C		B		C		C		B		C		C		D		C		C		D		C		D		C		D		C						
GJ	B		B		C		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D									
GK		C		B		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C		D						
GL	B		B		C		B		DA40		C		E		DA41		C		E		A		C		D		E		C		D		E		C		D							
GM		C		B		B		C		DA40		E		C		DA41		E		C		A		D		C		E		D		C		E		D		C						

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
GN	B		B		C		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D									
GP		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
GR	B		B		C		B		E			C		C		E			C		C		A		C		C		E		C		C		E		C		C					
GT		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
GU	B		B		C		B		E		C		DA42		E		C		DA43		A		C		D		E		C		D		E		C		D							
GV		C		B		B		C		E		DA42		C		E		DA43		C		A		D		C		E		D		C		E		D		C						
GW	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
GY		C		B		B		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C								
HA	B		B		C		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D							
HB		C		B		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C						
HC	B		B		C		B		DA44		C		D		DA45		C		D		A		C		D		E		C		D		E		C		D		D					
HD		C		B		B		C		DA44		D		C		DA45		D		C		A		D		C		E		D		C		E		D		C						
HE	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D							
HF		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
HG	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
HH		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
HJ	B		B		C		B		D		C		DA46		D		C		DA47		A		C		D		E		C		D		E		C		D							
HK		C		B		B		C		D		DA46		C		D		DA47		C		A		D		C		E		D		C		E		D		C						
HL	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
HM		C		B		B		C		C		B		C		B		C		C		B		C		C		D		C		C		D		C		D		C				
HN	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D							
HP		C		B		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C								
HR	B		B		C		B		DA48		C		E		DA49		C		E		A		C		D		E		C		D		E		C		D							
HT		C		B		B		C		DA48		E		C		DA49		E		C		A		D		C		E		D		C		E		D		C						
HU	B		B		C		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D		E		C					
HV		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
HW	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
HY		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
JA	B		B		C		B		E		C		DA50		E		C		DA51		A		C		D		E		C		D		E		C		D							
JB		C		B		B		C		E		DA50		C		E		DA51		C		A		D		C		E		D		C		E		D		C						
JC	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
JD		C		B		B		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C		D						
JE	B		B		C		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D									
JF		C		B		B		C		D		C		D		C		D		A		C		D		C		C		D		C		C		D		C						
JG	B		B		C		B		DA52		C		D		DA53		C		D		A		C		D		C		E		D		C		E		C		D					
JH		C		B		B		C		DA52		D		C		DA53		D		C		A		D		C		E		D		C		E		D		C						

**Table 76 — HBM Ballout Footprint A Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
JJ	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D							
JK		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
JL	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
JM		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
JN	B		B		C		B		D		C		DA54		D		C		DA55		A		C		D		E		C		D		E		C		D							
JP		C		B		B		C		D		DA54		C		D		DA55		C		A		D		C		E		D		C		E		D		C						
JR	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
JT		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C						
JU	B		B		C		B		C		C		E		C		C		C		E		C		C		D		C		D		C		C		D							
JV		C		B		B		C		C		E		C		C		C		E		C		C		D		C		C		D		C		C		D						
JW	B		B		C		B		DA56		C		E		DA57		C		E		C		A		C		D		E		C		D		E		C		D					
JY		C		B		B		C		DA56		E		C		DA57		E		C		A		D		C		E		D		C		E		D		C						
KA	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D							
KB		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
KC	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
KD		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
KE	B		B		C		B		E		C		DA58		E		C		DA59		A		C		D		E		C		D		E		C		D							
KF		C		B		B		C		E		DA58		C		E		DA59		C		A		D		C		E		D		C		E		D		C						
KG	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D							
KH		C		B		B		C		C		B		C		B		C		C		D		C		C		D		C		C		D		C		D						
KJ	B		B		C		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C							
KK		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D						
KL	B		B		C		B		RSVD <sub>2</sub>		C		D		RSVD <sub>3</sub>		C		D		A		C		D		E		C		D		E		C		D							
KM		C		B		B		C		RSVD <sub>2</sub>		D		C		RSVD <sub>3</sub>		D		C		A		D		C		E		D		C		E		D		C						
KN	B		B		C		B		C		C		B		C		C		C		A		C		C		E		C		D		E		C		D							
KP		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C						
KR	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
KT		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
KU	B		B		C		B		D		C		RSVD <sub>4</sub>		D		C		RSVD <sub>5</sub>		A		C		D		E		C		D		E		C		D							
KV		C		B		B		C		D		RSVD <sub>4</sub>		C		D		RSVD <sub>5</sub>		C		A		D		C		E		D		C		E		D		C						
KW	B		B		C		B		C		B		B		C		B		B		A		C		D		E		C		D		E		C		D							
KY		C		B		B		C		B		B		C		B		B		C		A		D		C		E		D		C		E		D		C						

## 11.4 HBM Ballout (cont'd)

Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68)

	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	
A	D		D		D		D		D		D		D		D		D		D		D		D		
B		DQe7		DQe5		RDe0		DQe3		DQe1		DMe0		DQa7		DQa5		RDa0		DQa3		DQa1		DMa0	
C	DBIe0		DQe6		DQe4		PARE0		DQe2		DQe0		DBIa0		DQa6		DQa4		PARA0		DQa2		DQa0		
D		DQe15		DQe13		WDQSe_0_c		DQe11		DQe9		DMe1		DQa15		DQa13		WDQSa_0_c		DQa11		DQa9		DMa1	
E	DBIe1		DQe14		DQe12		WDQSe_0_t		DQe10		DQe8		DBIa1		DQa14		DQa12		WDQSa_0_t		DQa10		DQa8		
F		M		M		M		M		M		M		M		M		M		M		M		M	
G	M		M		M		M		M		M		M		M		M		M		M		M		
H		DQe23		DQe21		RDQSe_0_c		DQe19		DQe17		DMe2		DQa23		DQa21		RDQSa_0_c		DQa19		DQa17		DMa2	
J	DBIe2		DQe22		DQe20		RDQSe_0_t		DQe18		DQe16		DBIa2		DQa22		DQa20		RDQSa_0_t		DQa18		DQa16		
K		DQe31		DQe29		RDe1		DQe27		DQe25		DMe3		DQa31		DQa29		RDa1		DQa27		DQa25		DMa3	
L	DBIe3		DQe30		DQe28		DERRe0		DQe26		DQe24		DBIa3		DQa30		DQa28		DERRa0		DQa26		DQa24		
M		D		D		D		D		D		D		D		D		D		D		D		D	
N	D		D		D		D		D		D		D		D		D		D		D		D		
P		DQf7		DQf5		RDf0		DQf3		DQf1		DMf0		DQb7		DQb5		RDb0		DQb3		DQb1		DMb0	
R	DBIf0		DQf6		DQf4		PARf0		DQf2		DQf0		DBIb0		DQb6		DQb4		PARb0		DQb2		DQb0		
T		DQf15		DQf13		WDQSF_0_c		DQf11		DQf9		DMf1		DQb15		DQb13		WDQSB_0_c		DQb11		DQb9		DMb1	
U	DBIf1		DQf14		DQf12		WDQSF_0_t		DQf10		DQf8		DBIb1		DQb14		DQb12		WDQSB_0_t		DQb10		DQb8		
V		M		M		M		M		M		M		M		M		M		M		M		M	
W	M		M		M		M		M		M		M		M		M		M		M		M		
Y		DQf23		DQf21		RDQSF_0_c		DQf19		DQf17		DMf2		DQb23		DQb21		RDQSB_0_c		DQb19		DQb17		DMb2	
AA	DBIf2		DQf22		DQf20		RDQSF_0_t		DQf18		DQf16		DBIb2		DQb22		DQb20		RDQSB_0_t		DQb18		DQb16		
AB		DQf31		DQf29		RDf1		DQf27		DQf25		DMf3		DQb31		DQb29		RDb1		DQb27		DQb25		DMb3	
AC	DBIf3		DQf30		DQf28		DERRf0		DQf26		DQf24		DBIb3		DQb30		DQb28		DERRb0		DQb26		DQb24		
AD		D		D		D		D		D		D		D		D		D		D		D		D	

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77—HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	
EJ	MRFU 1		MRFU 0		WSOh		WSOF		WSOd		WSOb		WSI		UPDATE WR		SHIFT WR		WRST_n		B		B		
EK		MRFU 5		MRFU 4		WSOg		WSOe		WSOc		WSOa		SELECT WIR		CAPTURE WR		WRCK		MRFU 3		RESET_n		MRFU 2	
EL	MRFU 13		MRFU 12		MRFU 11		MRFU 10		MRFU 9		MRFU 8		MRFU 7		TEMP2		TEMP0		MRFU 6		B		B		
EM		MRFU 23		MRFU 22		MRFU 21		MRFU 20		MRFU 19		MRFU 18		MRFU 17		TEMP1		CAT-TRIP		MRFU 16		MRFU 15		MRFU 14	

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77—HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

**Table 77 — HBM Ballout Footprint A Part 2 (Columns 45 to 68) (cont'd)**

## 11.4 HBM Ballout (cont'd)

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
A	B		B	C	B	E		C	D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D											
B	C	B	B	B	C	E		D	C	E	D	C	C	D	C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
C	B	B	C	B	C	C		D	C	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D											
D	C	B	B	B	C	C		D	C	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D											
E	B	B	C	B	C	C		D	C	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D											
F	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
G	B	B	C	B	C	E		D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
H	C	B	B	C	C	E		D	C	E	D	C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
J	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
K	C	B	B	C	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
L	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
M	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
N	B	B	C	B	C	E		D	E	D	C	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
P	C	B	B	C	C	E		D	C	E	D	C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
R	B	B	C	B	C	E		D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D												
T	C	B	B	C	C	D		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C												
U	B	B	C	B	C	D		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C												
V	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
W	B	B	C	B	C	E		D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
Y	C	B	B	C	C	E		C	C	E	D	C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AA	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AB	C	B	B	C	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AC	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AD	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AE	B	B	C	B	C	E		D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
AF	C	B	B	C	C	E		D	C	E	D	C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AG	B	B	C	B	C	E		D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D												
AH	C	B	B	C	C	D		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C												
AJ	B	B	C	B	C	D		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C												
AK	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AL	B	B	C	B	C	E		D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
AM	C	B	B	C	C	E		C	C	E	D	C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AN	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AP	C	B	B	C	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AR	B	B	C	B	C	E		C	C	E	C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C	E	C	C												
AT	C	B	B	C	C	E		D	C	E	D	C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AU	B	B	C	B	C	E		D	E	C	D	A	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D	E	C	D												
AV	C	B	B	C	C	E		D	C	E	D	C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C											
AW	B	B	C	B	C	E		D	C	E	D	C	C	D	C	E	D	C	E	D	C	E	D	C	E	D	C	E	D	C	C	D												
AY	C	B	B	C	C	D		C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C	C	D	C												

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
BA	B		B		C		B		C		C		D		B		C		D		C		C		D		C		C		C		D		C		C		D					
BB		C		B		B		C		B		D		C		B		D		C		A		D		C		E		D		C		E		D		C						
BC	B		B		C		B		B		C		D		B		C		D		A		C		D		E		C		D		E		C		D							
BD		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
BE	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
BF		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
BG	B		B		C		B		D		C		D		C		C		A		C		C		E		C		C		E		C		C									
BH		C		B		B		C		D		RSVD 0		C		D		RSVD 1		C		A		D		C		E		D		C		E		D		C						
BJ	B		B		C		B		D		C		RSVD 0		D		C		RSVD 1		A		C		D		E		C		D		E		C		D							
BK		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						
BL	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
BM		C		B		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C								
BN	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D							
BP		C		B		B		C		DA0		E		C		DA1		E		C		A		D		C		E		D		C		E		D		C						
BR	B		B		C		B		DA0		C		E		DA1		C		E		A		C		D		E		C		D		E		C		D							
BT		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
BU	B		B		C		B		C		C		B		C		C		B		C		A		C		C		E		C		C		E		C		C					
BV		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
BW	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
BY		C		B		B		C		E		DA2		C		E		DA3		C		A		D		C		E		D		C		E		D		C						
CA	B		B		C		B		E		C		DA2		E		C		DA3		A		C		D		E		C		D		E		C		D							
CB		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						
CC	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
CD		C		B		B		C		D		C		D		C		D		C		C		D		C		C		D		C		C		D		C						
CE	B		B		C		B		C		D		C		D		C		D		C		C		D		C		C		D		C		C		D							
CF		C		B		B		C		DA4		D		C		DA5		D		C		A		D		C		E		D		C		E		D		C						
CG	B		B		C		B		DA4		C		D		DA5		C		D		A		C		D		E		C		D		E		C		D							
CH		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
CJ	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
CK		C		B		B		C		D		C		D		C		D		C		A		C		C		E		C		C		E		C		C						
CL	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
CM		C		B		B		C		D		DA6		C		D		DA7		C		A		D		C		E		D		C		E		D		C						
CN	B		B		C		B		D		C		DA6		D		C		DA7		A		C		D		E		C		D		E		C		D							
CP		C		B		B		C		C		B		C		C		B		C		C		D		C		E		D		C		E		D		C						

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
CR	B		B		C		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D							
CT		C		B		B		C		C		E		C		C		C		C		C		D		C		C		D		C		C		D		C						
CU	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D							
CV		C		B		B		C		DA8		E		C		DA9		E		C		A		D		C		E		D		C		E		D		C						
CW	B		B		C		B		DA8		C		E		DA9		C		E		A		C		D		E		C		D		E		C		D		C					
CY		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
DA	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
DB		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
DC	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
DD		C		B		B		C		E		DA10		C		E		DA11		C		A		D		C		E		D		C		E		D		C						
DE	B		B		C		B		E		C		DA10		E		C		DA11		A		C		D		E		C		D		E		C		D							
DF		C		B		B		C		C		B		C		B		C		C		D		C		E		D		C		E		D		C								
DG	B		B		C		B		C		B		C		B		C		C		B		C		D		C		C		D		C		C		D							
DH		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C								
DJ	B		B		C		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D									
DK		C		B		B		C		DA12		D		C		DA13		D		C		A		D		C		E		D		C		F		D		C						
DL	B		B		C		B		DA12		C		D		DA13		C		D		A		C		D		E		C		D		E		C		D							
DM		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
DN	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
DP		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C						
DR	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C							
DT		C		B		B		C		D		DA14		C		D		DA15		C		A		D		C		E		D		C		E		D		C						
DU	B		B		C		B		D		C		DA14		D		C		DA15		A		C		D		E		C		D		E		C		D							
DV		C		B		B		C		C		B		C		B		C		C		D		C		E		D		C		E		D		C								
DW	B		B		C		B		C		C		B		C		C		B		C		C		D		C		D		C		D		C		D							
DY		C		B		B		C		E		C		C		E		E		C		C		D		C		C		D		C		C		D		C						
EA	B		B		C		B		C		E		C		C		E		C		C		D		C		C		D		C		C		D		C							
EB		C		B		B		C		DA16		E		C		DA17		E		C		A		D		C		E		D		C		E		D		C						
EC	B		B		C		B		DA16		C		E		DA17		C		E		A		C		D		E		C		D		E		C		D							
ED		C		B		B		C		B		C		C		B		C		C		A		C		C		E		D		C		E		D		C						
EE	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C							
EF		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C						
EG	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C							
EH		C		B		B		C		E		DA18		C		E		DA19		C		A		D		C		E		D		C		E		D		C						
EJ	B		B		C		B		E		C		DA18		E		C		DA19		A		C		D		E		C		D		E		C		D							
EK		C		B		B		C		C		B		C		C		B		C		D		C		E		D		C		E		D		C								

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
EL	B		B		C		B		C			B		C		C		B		C	C	D		C	C	D		C	C	D		C	C	D										
EM		C		B		B		C		C		D		C		C		D		C	C	D	C	C	D		C	C	D		C													
EN	B		B		C		B		C		C		D		C		C		D		C	C	D		C	C	D		C	C	D													
EP		C		B		B		C		DA20		D		C		DA21		D		C	A	D	C	E	D	C	E	D		C	E	D		C										
ER	B		B		C		B		DA20		C		D		DA21		C		D		A	C	D	E	C	D	E	C	D	E	C	C	D											
ET		C		B		B		C		B		C		B		C		C		A	C	C	E	C	C	E	D	C	E	D	C	E	D		C									
EU	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
EV		C		B		B		C		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C									
EW	B		B		C		B		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
EY		C		B		B		C		D		DA22		C		D		DA23		C	A	D	C	E	D	C	E	D	C	E	D	C	E	D	C									
FA	B		B		C		B		D		C		DA22		D		C		DA23		A	C	D	E	C	D	E	C	D	E	C	D	E	C	D									
FB		C		B		B		C		C		B		C		B		C		C	D	C	E	D	C	E	D	C	E	D	C	E	D	C										
FC	B		B		C		B		C		C		B		C		C		B	C	C	D	C	C	D	C	C	D	C	C	D	C	D											
FD		C		B		B		C		C		E		C		C		E		C	C	D	C	C	D	C	C	D	C	C	D	C	D	C										
FE	B		B		C		B		C		C		E		C		C		E	C	C	D	C	C	D	C	C	D	C	C	D	C	D											
FF		C		B		B		C		DA24		E		C		DA25		E		C	A	D	C	E	D	C	E	D	C	E	D	C	D	C										
FG	B		B		C		B		DA24		C		E		DA25		C		E	A	C	D	E	C	D	E	C	D	E	C	D													
FH		C		B		B		C		B		C		B		C		C	A	C	C	E	D	C	C	D	C	C	D	C	D	C												
FJ	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
FK		C		B		B		C		E		C		C		E		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C											
FL	B		B		C		B		E		C		C		E		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
FM		C		B		B		C		E		DA26		C		E		DA27		C	A	D	C	E	D	C	E	D	C	E	D	C	D											
FN	B		B		C		B		E		C		DA26		E		C		DA27		A	C	D	E	C	D	E	C	D	E	C	D												
FP		C		B		B		C		C		B		C		B		C		C	C	D	C	E	D	C	E	D	C	E	D	C	D	C										
FR	B		B		C		B		C		C		B		C		C		B	C	C	D	C	C	D	C	C	D	C	C	D	C	D											
FT		C		B		B		C		D		C		C		D		C		C	C	D	C	C	D	C	C	D	C	C	D	C	D	C										
FU	B		B		C		B		C		C		D		C		C		D	C	C	D	C	C	D	C	C	D	C	C	D	C	D											
FV		C		B		B		C		DA28		D		C		DA29		D		C	A	D	C	E	D	C	E	D	C	E	D	C	D											
FW	B		B		C		B		DA28		C		D		DA29		C		D	A	C	D	E	C	D	E	C	D	E	C	D													
FY		C		B		B		C		B		C		B		C		C	A	C	C	E	D	C	E	D	C	E	D	C	E	D	C											
GA	B		B		C		B		B		C		C		B		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
GB		C		B		B		C		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	C											
GC	B		B		C		B		D		C		C		D		C		C	A	C	C	E	C	C	E	C	C	E	C	C	E	C	C										
GD		C		B		B		C		D		B		C		D		B		C	A	D	C	E	D	C	E	D	C	E	D	C	D	C										

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44				
GU	B		B		C		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D													
GV		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C										
GW	B		B		C		B		C		C		B		C		C		C		A		C		C		E		C		C		E		C		C											
GY		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C										
HA	B		B		C		B		B		C		DA30		B		C		DA31		A		C		D		E		C		D		E		C		D											
HB		C		B		B		C		B		DA30		C		B		DA31		C		A		D		C		E		D		C		E		D		C										
HC	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D											
HD		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C										
HE	B		B		C		B		C		C		E		C		C		E		C		C		D		C		C		D		C		C		D											
HF		C		B		B		C		C		E		C		C		C		C		D		C		C		D		C		C		D		C												
HG	B		B		C		B		DA32		C		E		DA33		C		E		A		C		D		E		C		D		E		C		D											
HH		C		B		B		C		DA32		E		C		DA33		E		C		A		D		C		E		D		C		E		D		C										
HJ	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D											
HK		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C										
HL	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C											
HM		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C										
HN	B		B		C		B		E		C		DA34		E		C		DA35		A		C		D		E		C		D		E		C		D		E		C		D					
HP		C		B		B		C		E		DA34		C		E		DA35		C		A		D		C		E		D		C		E		D		C		E		D		C				
HR	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D		E		C		D					
HT		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C		D		C						
HU	B		B		C		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D							
HV		C		B		B		C		C		D		C		D		C		C		D		C		C		D		C		C		D		C		D		C								
HW	B		B		C		B		DA36		C		D		DA37		C		D		A		C		D		E		C		D		E		C		D		E		C		D					
HY		C		B		B		C		DA36		D		C		DA37		D		C		A		D		C		E		D		C		E		D		C		E		D		C				
JA	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D		E		C		D					
JB		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C		E		C		C				
JC	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C		E		C		C					
JD		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C		E		C		C				
JE	B		B		C		B		D		C		DA38		D		C		DA39		A		C		D		E		C		D		E		C		D		E		C		D					
JF		C		B		B		C		D		DA38		C		D		DA39		C		A		D		C		E		D		C		E		D		C		E		D		C				
JG	B		B		C		B		C		C		B		C		C		B		C		C		D		E		C		D		E		C		D		E		C		D					
JH		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C		D		C		D		C		
JJ	B		B		C		B		C		E		C		C		E		C		C		D		C		C		D		C		D		C		C		D		C		D					
JK		C		B		B		C		E		C		C		E		C		C		A		C		D		E		C		D		E		C		C		D		C		D		C		
JL	B		B		C		B		DA40		C		E		DA41		C		E		A		C		D		E		C		D		E		C		D		E		C		D		C			
JM		C		B		B		C		DA40		E		C		DA41		E		C		A		D		C		E		D		C		E		D		C		E		D		C				

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44							
JN	B		B		C		B		B		C		C		B		C		C		A		C		C		E		C		D		E		C		D														
JP		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C													
JR	B		B		C		B		E			C		C		E		C		C		A		C		C		E		C		C		E		C		C													
JT		C		B		B		C		E			C		C		E		C		C		A		C		C		E		C		C		E		C		C												
JU	B		B		C		B		E		C		DA42		E		C		DA43		A		C		D		E		C		D		E		C		D														
JV		C		B		B		C		E		DA42		C		E		DA43		C		A		D		C		E		D		C		E		D		C													
JW	B		B		C		B		C			B		C		C		B		C		C		D		E		C		D		E		C		D															
JY		C		B		B		C			C		B		C		C		B		C		C		D		C		C		D		C		C		D		C												
KA	B		B		C		B		C			D		C		C		D		C		C		D		C		C		D		C		C		D															
KB		C		B		B		C		D			C		C		D		C		C		D		C		C		D		C		C		D		C														
KC	B		B		C		B		DA44		C		D		DA45		C		D		A		C		D		E		C		D		E		C		D														
KD		C		B		B		C		DA44		D		C		DA45		D		C		A		D		C		E		D		C		E		D		C													
KE	B		B		C		B			B		C		C		B		C		C		A		C		C		E		C		D		E		C		D													
KF		C		B		B		C			B		C		C		B		C		C		A		C		C		E		C		C		E		C		C												
KG	B		B		C		B		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C														
KH		C		B		B		C		D		C		C		D		C		C		A		C		C		E		C		C		E		C		C													
KJ	B		B		C		B		D		C		DA46		D		C		DA47		A		C		D		E		C		D		E		C		D		E		C		D								
KK		C		B		B		C		D		DA46		C		D		DA47		C		A		D		C		E		D		C		E		D		C		E		D		C							
KL	B		B		C		B		C			B		C		C		B		C		C		D		C		C		D		E		C		D		E		C		D									
KM		C		B		B		C		C		B		C		C		B		C		C		D		C		C		D		C		C		D		C													
KN	B		B		C		B		C		E			C		C		E		C		C		D		C		C		D		C		C		D		C													
KP		C		B		B		C		E			C		C		E		C		C		D		C		C		D		C		C		D		C														
KR	B		B		C		B		DA48		C		E		DA49		C		E		A		C		D		E		C		D		E		C		D		E		C		D								
KT		C		B		B		C		DA48		E			C		DA49		E		C		A		D		C		E		D		C		E		D		C		E		D		C						
KU	B		B		C		B			B		C		C		B		C		C		A		C		C		E		C		D		E		C		D		E		C		D							
KV		C		B		B		C		B		C		C		B		C		C		A		C		C		E		C		C		E		C		C		E		C		C							
KW	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		E		C		C								
KY		C		B		B		C		E			C		C		E		C		C		A		C		C		E		C		C		E		C		C		E		C		C						
LA	B		B		C		B		E		C		DA50		E		C		DA51		A		C		D		E		C		D		E		C		D		E		C		D								
LB		C		B		B		C		E		DA50		C		E		DA51		C		A		D		C		E		D		C		E		D		C		E		D		C							
LC	B		B		C		B		C			B		C		C		B		C		C		D		E		C		D		E		C		D		E		C		D		E		C		D			
LD		C		B		B		C			B		C		C		B		C		C		D		C		C		D		C		C		D		C		C		D		C								
LE	B		B		C		B		C			D		C		C		D		C		C		D		C		C		D		C		D		C		C		D		C		D							
LF		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D		C					
LG	B		B		C		B		DA52		C		D		DA53		C		D		A		C		D		E		C		D		E		C		D		E		C		D		C		D				
LH		C		B		B		C		DA52		D		C		DA53		D		C		A		D		C		E		D		C		E		D		C		E		D		C		D		C			

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

**Table 78 — HBM Ballout Footprint B Part 1: Columns 1 to 44 (cont'd)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
NA	B		B		C		B		C			D		C		C		D		C		C		D		C		C		D		C		C		D		C		D		C		D
NB		C		B		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D				
NC	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		E		C		D	
ND		C		B		B		C		E		D		C		E		D		C		A		A		D		C		E		D		C		E		D		C		D		
NE	B		B		C		B		E		C		C		E		C		D		A		C		C		E		C		D		E		C		D		E		C		D	
NF		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		E		C		E		C		C		C		
NG	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C		C			
NH		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		E		C		E		C		C		C		
NJ	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		C		D			
NK		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		E		C		E		D		C		D		
NL	B		B		C		B		E		C		D		E		C		D		C		C		D		E		C		D		E		C		D		C		D			
NM		C		B		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		C				
NN	B		B		C		B		C		C		D		C		C		D		C		C		D		C		C		D		C		D		C		C		D			
NP		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D				
NR	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		C		D			
NT		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		C		E		D		C		D				
NU	B		B		C		B		E		C		C		E		C		D		A		C		C		E		C		D		E		C		D		C		D			
NV		C		B		B		C		E		C		C		E		C		A		C		C		E		C		C		E		C		C		C		C				
NW	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C					
NY		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C				
PA	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		C		D			
PB		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		C		E		D		C		D				
PC	B		B		C		B		E		C		D		E		C		D		C		C		D		E		C		D		E		C		D		C		D			
PD		C		B		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D				
PE	B		B		C		B		C		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D			
PF		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		C		D		C		D		C		D		
PG	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		C		D			
PH		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		C		E		D		C		D				
PJ	B		B		C		B		E		C		C		E		C		D		A		C		E		C		D		E		C		D		E		C		D			
PK		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C				
PL	B		B		C		B		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C					
PM		C		B		B		C		E		C		C		E		C		C		A		C		C		E		C		C		E		C		C		C				
PN	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		E		C		D	
PP		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		C		E		D		C		D				
PR	B		B		C		B		E		C		D		E		C		D		C		C		D		E		C		D		E		C		D		C		D			
PT		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		D		C		C		D		C		D		
PU	B		B		C		B		C		D		C		C		D		C		C		D		C		C		D		C		D		C		C		D		C		D	
PV		C		B		B		C		D		C		C		D		C		C		D		C		C		D		C		D		C		C		D		C		D		
PW	B		B		C		B		E		C		D		E		C		D		A		C		D		E		C		D		E		C		D		C		D			
PY		C		B		B		C		E		D		C		E		D		C		A		D		C		E		D		C		E		D		C		E		D		

## 11.4 HBM Ballout (cont'd)

Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68)

	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68
A	E	C	D		E	C	D		E	C	D		E	C	D		E	C	D		D		C	
B	E	D	C		E	C	D		C	D	C		E	C	D		C	E	D		D		C	
C	C	C	D		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
D	C	D	C		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
E	C	C	D		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
F	E	D	C		E	C	D		C	D	C		E	C	D		C	E	D		D		C	
G	E	C	D		E	C	D		E	D	E		C	C	D		E	C	D		D		C	
H	E	D	C		E	D	C		E	D	C		E	D	C		E	E	D		D		C	
J	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
K	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
L	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
M	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
N	E	C	D		E	C	D		E	D	E		C	C	D		E	C	D		D		C	
P	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
R	C	C	D		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
T	C	D	C		C	D	C		C	D	C		C	D	C		C	C	D		D		C	
U	C	C	D		C	C	C		D	D	C		C	C	D		C	C	D		D		C	
V	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
W	E	C	D		E	C	D		E	D	E		C	C	D		E	C	D		D		C	
Y	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
AA	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
AB	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
AC	E	C	C		E	C	C		E	C	C		E	C	C		E	C	C		C		C	
AD	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
AE	E	C	D		E	C	D		E	D	E		C	C	D		E	C	D		D		C	
AF	E	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
AG	C	C	D		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
AH	C	D	C		C	D	C		C	D	C		C	D	C		C	C	D		D		C	
AJ	C	C	D		C	C	D		C	D	C		C	C	D		C	C	D		D		C	
AK	M	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
AL	M	C	D		E	C	D		E	D	C		E	C	D		E	C	D		D		C	
AM	M	D	C		E	D	C		E	D	C		E	D	C		E	D		D		C		
AN	M	C	C		C	C	C		C	C	C		C	C	C		C	C	C		C		C	
AP	M	C	C		C	C	C		C	C	C		C	C	C		C	C	C		C		C	
AR	M	C	C		C	C	C		C	C	C		C	C	C		C	C	C		C		C	
AT	M	M	M		M	M	M		M	M	M		M	M	M		M	M	M		M		M	
AU	M	M	M		M	M	M		M	M	M		M	M	M		M	M	M		M		M	
AV	C	C	C		C	C	C		C	C	C		C	C	C		C	C	C		C		C	
AW	C	C	C		C	C	C		C	C	C		C	C	C		C	C	C		C		C	
AY	D	D	D		D	D	D		D	D	D		D	D	D		D	D	D		D		D	

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	
GJ	MRFU 1		MRFU 0		WSOh		WSOF		WSOd		WSOb		WSI		UPDATE WR		SHIFT WR		WRST_n		B		B		
GK		MRFU 5		MRFU 4		WSOg		WSOe		WSOc		WSOa		SELECT WIR		CAPTURE WR		WRCK		MRFU 3		RESET_n		MRFU 2	
GL	MRFU 13		MRFU 12		MRFU 11		MRFU 10		MRFU 9		MRFU 8		MRFU 7		TEMP2		TEMP0		MRFU 6		B		B		
GM		MRFU 23		MRFU 22		MRFU 21		MRFU 20		MRFU 19		MRFU 18		MRFU 17		TEMP1		CAT-TRIP		MRFU 16		MRFU 15		MRFU 14	

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

**Table 79 — HBM Ballout Footprint B Part 2 (Columns 45 to 68) (cont'd)**

	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68
NA	D		D		D		D		D		D		D		D		D		D		D		D	
NB	C		C		C		C		C		C		C		C		C		C		C		C	
NC	C		C		C		C		C		C		C		C		C		C		C		C	
ND	M		M		M		M		M		M		M		M		M		M		M		M	
NE	M		M		M		M		M		M		M		M		M		M		M		M	
NF	M		C		C		C		C		C		C		C		C		C		C		C	
NG	M		C		C		C		C		C		C		C		C		C		C		C	
NH	M		C		C		C		C		C		C		C		C		C		C		C	
NJ	M		C		D		E		C		D		E		C		D		E		C		D	
NK	M		D		C		E		D		C		E		D		C		E		D		C	
NL	M		C		D		E		C		D		E		C		D		E		C		D	
NM	C		D		C		C		D		C		C		D		C		C		D		C	
NN	C		C		D		C		C		D		C		C		D		C		C		D	
NP	C		D		C		C		D		C		C		D		C		C		D		C	
NR	E		C		D		E		C		D		E		C		D		E		C		D	
NT	E		D		C		E		D		C		E		D		C		E		D		C	
NU	E		C		D		E		C		D		E		C		D		E		C		D	
NV	E		C		C		E		C		C		E		C		C		E		C		C	
NW	E		C		C		E		C		C		E		C		C		E		C		C	
NY	E		C		C		E		C		C		E		C		C		E		C		C	
PA	E		C		D		E		C		D		E		C		D		E		C		D	
PB	E		D		C		E		D		C		E		D		C		E		D		C	
PC	E		C		D		E		C		D		E		C		D		E		C		D	
PD	C		D		C		C		D		C		C		D		C		C		D		C	
PE	C		C		D		C		C		D		C		C		D		C		C		D	
PF	C		D		C		C		D		C		C		D		C		C		D		C	
PG	E		C		D		E		C		D		E		C		D		E		C		D	
PH	E		D		C		E		D		C		E		D		C		E		D		C	
PJ	E		C		D		E		C		D		E		C		D		E		C		D	
PK	E		C		C		E		C		C		E		C		C		E		C		C	
PL	E		C		C		E		C		C		E		C		C		E		C		C	
PM	E		C		C		E		C		C		E		C		C		E		C		C	
PN	E		C		D		E		C		D		E		C		D		E		C		D	
PP	E		D		C		E		D		C		E		D		C		E		D		C	
PR	E		C		D		E		C		D		E		C		D		E		C		D	
PT	C		D		C		C		D		C		C		D		C		C		D		C	
PU	C		C		D		C		C		D		C		C		D		C		C		D	
PV	C		D		C		C		D		C		C		D		C		C		D		C	
PW	E		C		D		E		C		D		E		C		D		E		C		D	
PY	E		D		C		E		E		D		E		D		C		E		D		C	

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## 12 HBM DRAM Assembly

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The HBM DRAM assembly is not defined by this standard. The shape and materials of the die to die interfaces between the die in the HBM DRAM are not defined in this standard and the shape (annular, cone, cylinder, etc.) and materials (Cu, W) are not defined or restricted in this standard. However these interfaces must fit within the electrical requirements of the channel interface.

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## 13 Test and Boundary Scan

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HBM DRAMs provide two separate test interfaces as described below:

- a direct access (DA) test port, intended for the vendor to access the HBM device independent of the host;
- an IEEE 1500 Standard test port, to be controlled by the host.

### 13.1 Direct Access (DA) Test Port

A DRAM direct access port is available via DA[59:0] for vendor specific test implementations. Two microbumps and a depopulated area for probing are associated with each DA pin (see [HBM Ballout](#)).

When DA28 = LOW, DA[59:29, 27:0] drivers are in Hi-Z and input receivers are disabled allowing the bus to float. When DA28 = HIGH, DA[59:29, 27:0] are enabled for vendor specific test features; and the IEEE 1500 port is disabled.

The DA28 input is equipped with an internal pull-down resistor which ensures that DA28 = LOW if the pin is left floating.

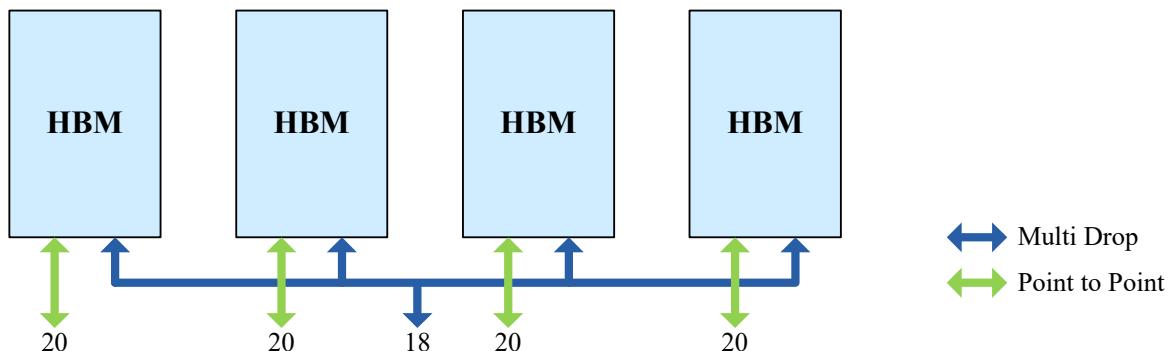
For implementations of multiple HBM devices in a package, there is a large burden on the package pin count to bring out separate DA[59:0] buses for each HBM device. Optionally, a user can bring out a subset of the DA[59:0] pins to connect up to 4 HBMs in a package to connect the devices in parallel ([Figure 92](#)).

20 DA pins are designated to connect point to point to each DRAM. 18 pins are designated to connect in parallel to up to four HBM devices on a multi drop bus. The function of each of these pins is vendor specific. [Table 80](#) defines which DA pins are allocated for point to point and for multi drop.

**Table 80 — Direct Access (DA) Pin Allocation**

Pin Group	DA Pin List	Pin Count
Point to Point	DA13, DA16, DA17, DA18, DA20, DA22, DA24, DA25, DA26, DA28, DA29, DA30, DA32, DA34, DA36, DA38, DA49, DA53, DA57, DA59	20
Multi Drop	DA4, DA5, DA6, DA8, DA10, DA12, DA14, DA21, DA40, DA42, DA44, DA46, DA48, DA50, DA52, DA54, DA56, DA58	18

NOTE 1 The remaining 22 DA pins are Hi-Z when DA28 = LOW; the pin's state is vendor specific when DA28 = HIGH.



**Figure 92 — DA Port Connection Diagram For Multiple HBM Devices**

### 13.1.1 DA28 Lockout

MR8 OP0 bit if set on channel a or e, disables DA28 from enabling the DA direct access port. Once the bit is set to 1, DA port will remain disabled unless power is removed from the HBM device. Any chip reset through pulling RESET\_n LOW or IEEE1500 [HBM\\_RESET](#) instruction, or writing a 0 via an MRS command or IEEE1500 instruction [MODE\\_REGISTER\\_DUMP\\_SET](#) will not clear the bit.

## 13.2 IEEE Standard 1500

IEEE Standard 1500 port is required for direct connection between host and HBM DRAM. The HBM DRAM provides one IEEE Standard 1500 port, extending the standard specification to replicate the WSO output per channel. This extension allows some commands to execute in parallel across channels, and eliminates the need for cross-channel arbitration for WSO.

Pin DA28 = LOW selects the IEEE 1500 test port and DA28 = HIGH selects the DA port. It is possible to operate the HBM DRAM without using the test ports. In this case DA28 and WRST\_n must be tied LOW to prevent the device from entering test modes.

[Table 81](#) summarizes the status of the test access port signals.

**Table 81 — Test Access Port Pin Status**

WRST_n	DA28, MR8 OP0	Pin Name	Type	Status	
LOW	DA28 = LOW or MR8 OP0 = 1	Other IEEE1500 inputs <sup>1</sup>	Input	X (Don't Care)	
		WSO	Output	V (Valid) <sup>2</sup>	
		DA[59:29, 27:0]	I/O	X (Don't Care)	
HIGH	DA28 = LOW or MR8 OP0 = 1	Other IEEE1500 inputs <sup>1</sup>	Input	Active	
		WSO	Output	V (Valid) <sup>2</sup>	
		DA[59:29, 27:0]	I/O	X (Don't Care)	
Don't Care	DA28 = HIGH and MR8 OP0 = 0	Other IEEE1500 inputs <sup>1</sup>	Input	X (Don't Care)	
		WSO	Output	V (Valid) <sup>2</sup>	
		DA[59:29, 27:0]	I/O	Vendor specific <sup>3</sup>	
NOTE 1 WRCK, SelectWIR, ShiftWR, CaptureWR, UpdateWR, WSI.					
NOTE 2 V = Valid Signal (either HIGH or LOW, but not floating).					
NOTE 3 Please refer to vendor's datasheet.					

IEEE Standard 1500 operations may be asserted at any time after device initialization and during normal memory operation including when the HBM memory device is in power-down or self refresh mode. See [Interaction with Mission Mode Operation](#) for how the various instructions interact with normal operation, and requirements for returning to normal operation. See also [Initialization Sequence For Use Of IEEE 1500 Instruction Including Lane Repairs](#) for a subset of operations that are allowed before the device initialization has been completed.

The implementation will feature a 12-bit Wrapper Instruction Register (WIR) format. WIR[11:8] used to address the target channel. Supported WRCK frequency range is 0-50 MHz.

Please refer to IEEE standards at [ieee.org](http://ieee.org) for functional standard.

### 13.2.1 Test Access Port I/O Signals

Table 82 — Signal List and Description

Symbol	Type	Description
WRCK	Input	Dedicated clock used to operate IEEE Std 1500 functions.
WRST_n	Input	When pulled LOW, WRST_n asynchronously puts the wrapper into its normal system mode. No WRCK clocks are required when WRST_n is LOW. See <a href="#">WDR Reset State</a> .
WSI	Input	IEEE Std 1500 wrapper serial input.
SelectWIR	Input	SelectWIR determines what type of WR operation, i.e., instruction or data, is to be performed.
CaptureWR	Input	Used to enable and control a Capture operation in the selected IEEE Std 1500 wrapper register (WR).
ShiftWR	Input	Used to enable and control a Shift operation in the selected IEEE Std 1500 wrapper register (WR).
UpdateWR	Input	Used to enable and control an Update operation in the selected IEEE Std 1500 wrapper register (WR).
WSO[a:h]	Output	IEEE Std 1500 per-channel wrapper and WIR(S) serial output.

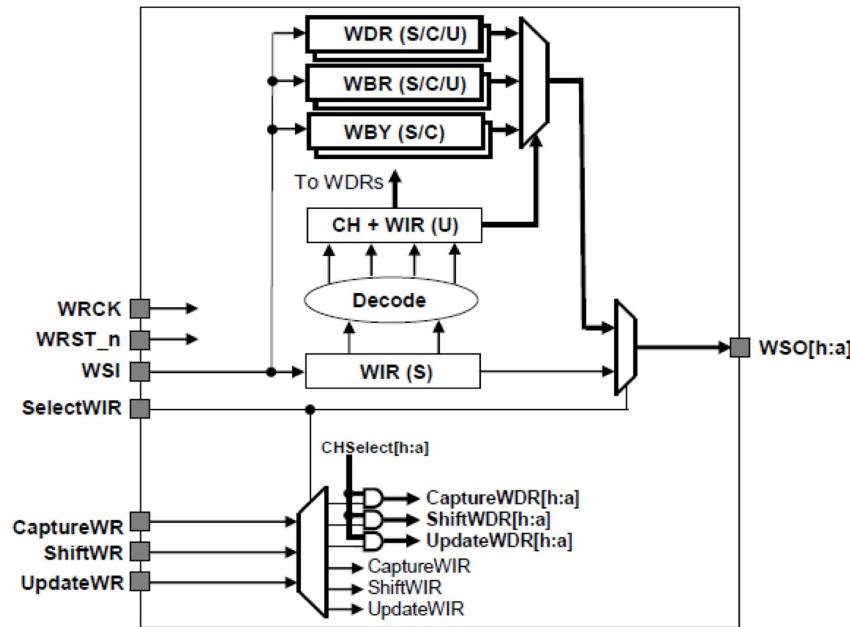


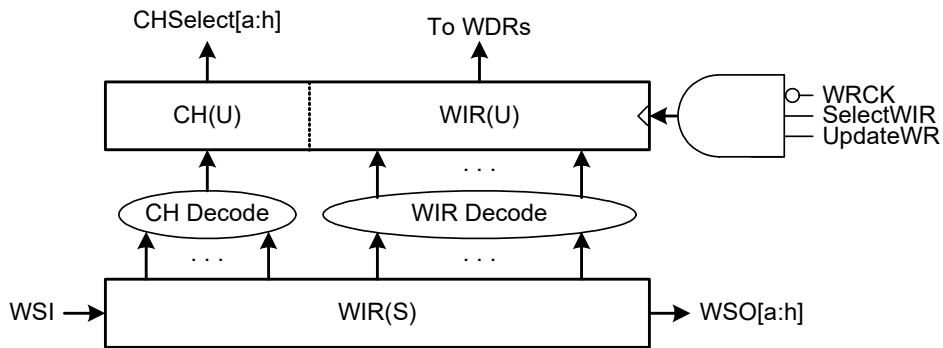
Figure 93 — IEEE Std 1500 Logic Diagram

### 13.2.1 Test Access Port I/O Signals (cont'd)

[Figure 93](#) shows a diagram of the HBM IEEE 1500 architecture. This is a compliant IEEE 1500 architecture that uses an asymmetrical WSP (Wrapper Serial Port) with a single WSI and per channel WSOs. The standard 1500 register stack is shown in the diagram, including the WBY (Wrapper BYPASS), WBR (Wrapper Boundary Register), and WDRs (Wrapper Data Registers). The C, S and U notation for the registers refer to Capture, Shift and Update respectively, and indicate for each of the registers which functions are required for that register. So for example the WBY only requires a Shift/Capture stage, whereas the WDRs require Shift/Capture and Update stages. In HBM implementations the WBR may be implemented without an Update stage to save silicon area, however separate \_TX and \_RX instructions must then be provided (see [Table 84](#)) in this case.

The WSO[a:h] output drivers are permanently enabled, with their drive state being LOW, HIGH, or undefined based on the current instruction loaded into the WIR. For example, if BYPASS is the current instruction, then WSO output data is defined only after one or more WRCK clock cycles have been applied.

The 1500 WIR (Wrapper Instruction Register) logic is also shown in [Figure 93](#). [Figure 94](#) shows further details of the WIR implementation for the HBM IEEE 1500 architecture. The WIR and instruction opcodes are described in [Wrapper Instruction Register Encodings](#). The four channel select bits of the WIR shift stage in [Figure 94](#) are decoded to generate the CHSelect[a:h] outputs. These channel ID selects are used to control the per channel operation of the instructions. When a channel is not selected for an active instruction, then the CaptureWDR[a:h], ShiftWDR[a:h] and UpdateWDR[a:h] enables of the WSP are gated off. This will disable the WDRs of unselected channels for the decoded instruction. This gating is shown at the output of the de-multiplexer in [Figure 93](#).



**Figure 94 — WIR Channel Select Logic Diagram**

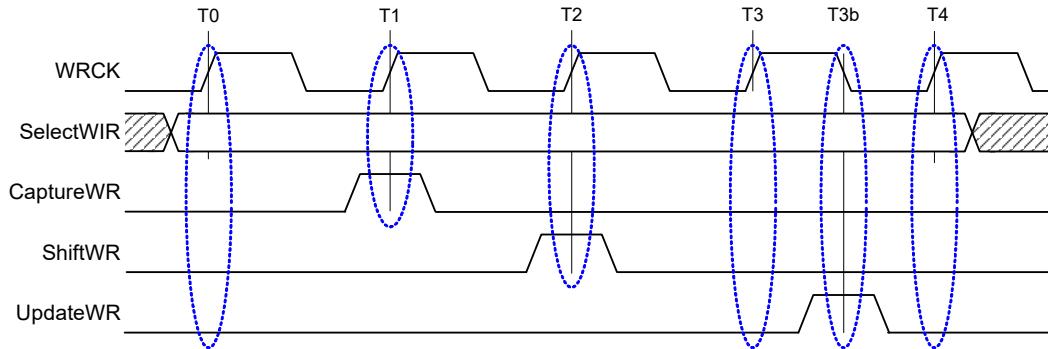
HBM devices are allowed to support less than 8 channels. The availability of each channel is coded in IEEE1500 bits [15:8]. Unavailable channels are not required to respond to IEEE1500 instructions with the exception of the global instructions BYPASS and HBM\_RESET that must be supported for all channels. This includes that all WSO[a:h] outputs are always present.

[Figure 95](#) illustrates an IEEE1500 port operation sequence with a minimum number of WRCK cycles:

- Signal SelectWIR is set at clock edge T0. Control signals CaptureWR, ShiftWR and UpdateWR are all inactive as they are not allowed to change coincident with SelectWIR. SelectWIR must be kept stable until after completion of the complete sequence which spans until clock edge T4.
- A WDR capture operation is performed at clock edge T1 with CaptureWR sampled High at T1.
- A single WDR shift operation is performed at clock edge T2 with ShiftWR sampled High at T2.

### 13.2.1 Test Access Port I/O Signals (cont'd)

- A WDR update operation is performed at clock edge T3b with UpdateWR sampled High at T3b. Please note that the update operation occurs on the falling WRCK clock edge.
- For some IEEE1500 port instructions a capture, shift or update event may not be specified; please refer to the description of each instruction for details.



**Figure 95 — IEEE1500 Port Operation**

### 13.2.2 Register Definition and Programming

Standard test registers are defined here that are accessible via IEEE Std 1500.

#### 13.2.2.1 Wrapper Instruction Register Encodings

The HBM device is required to support a twelve bit Wrapper Instruction Register (WIR). The four most significant bits are used for channel identification and the remaining eight least significant bits encode the test instruction. When SelectWIR is asserted, the WIR will not respond to CaptureWR signal and nothing will be captured into the WIR.

**Table 83 — WIR Channel Selection Definition**

WIR[11:8]	Channel Select
Xh	Ignored
0h	Channel a
1h	Channel b
2h	Channel c
3h	Channel d
4h	Channel e
5h	Channel f
6h	Channel g
7h	Channel h
Eh-8h	Reserved
Fh	All

### 13.2.2.1 Wrapper Instruction Register Encoding (cont'd)

Table 84 — Instruction Register Encodings

WIR [11:8]	WIR [7:0]	Instruction	Description	Register Type	WDR Length	Required/Optional
Xh	00h	BYPASS	Bypass	R/W	1	Required
Fh, 7h-0h	01h	EXTEST_RX	Microbump boundary scan Rx test (open/short)	R	215 or 217 <sup>1</sup>	Required
Fh, 7h-0h	02h	EXTEST_TX	Microbump boundary scan Tx test (open/short)	W	215 or 217 <sup>1</sup>	Required
	03h	INTEST_RX	Vendor INTEST for HBM inputs	R	Vendor specific	Optional
	04h	INTEST_TX	Vendor INTEST for HBM outputs	W	Vendor specific	Optional
Xh	05h	HBM_RESET	Update initiates DRAM functional reset excluding Wrapper Data Registers (WDRs) and any IEEE Std 1500 logic or IOs	W	1	Optional
Fh, 7h-0h	06h	MBIST	DRAM resident Memory MBIST engine test	R/W	Vendor specific	Required
7h-0h	07h	SOFT_REPAIR	Soft repair of failing DRAM bit cell	W	Vendor specific	Required
7h-0h	08h	HARD_REPAIR	Hard repair of DRAM failing DRAM bit cell	W	Vendor specific	Required
Fh, 7h-0h	09h	DWORD_MISR	Read back for DWORD MISR and optionally write a seed value	R (/W)	320	Required
Fh, 7h-0h	0Ah	AWORD_MISR	Read back for AWORD MISR	R	30 or 34 <sup>2</sup>	Required
Fh, 7h-0h	0Bh	CHANNEL_ID	All TX IOs go high (except MID stack region)	W	1	Required
Fh, 7h-0h	0Ch	MISR_MASK	Mask MISR bit(s)	W	72	Optional
Fh, 7h-0h	0Dh	AWORD_MISR_CONFIG	Allows IEEE Std 1500 access to configuration of the AWORD MISR test feature setup	W	8	Required
Fh, 7h-0h	0Eh	DEVICE_ID	Returns the DRAM's unique identification code	R	82	Required
Xh	0Fh	TEMPERATURE	Returns an 8-bit binary temperature code	R	8	Required
Fh, 7h-0h	10h	MODE_REGISTER_DUMP_SET	Returns and set the DRAM's Mode Register values.	W/R	128	Required
Fh, 7h-0h	11h	READ_LFSR_COMPARE_STICKY	Reads the sticky bit error for LFSR Compare feature	R	175 or 177 <sup>3</sup>	Required
7h-0h	12h	SOFT_LANE_REPAIR	Soft Lane Remapping	W/R	72	Required
7h-0h	13h	HARD_LANE_REPAIR	Hard Lane Remapping	W/R	72	Required
	14h-7Fh	RFU				
	80h-FFh	Vendor specific				

NOTE 1 The WDR length depends on the device configuration. See [Table 86](#).

NOTE 2 The WDR length depends on the device configuration and supported MISR polynomial. See [Table 95](#).

NOTE 3 The WDR length depends on the device configuration. See [Table 102](#).

### 13.2.2.2 Wrapper Data Register Types

#### 13.2.2.2.1 Read Only (R)

WDR bit fields that are specified as read only are required to capture data into the shift stage register when a CaptureWR event is performed. The read only WDRs are required to keep their state during an UpdateWR event and are not required to have an update stage register. Read only WDRs are shifted out during a ShiftWR event. Data shifted into WSI to the shift register during the ShiftWR event is required to be don't care.

#### 13.2.2.2.2 Write Only (W)

WDR bit fields that are specified as write only are required to update all data bits into the update stage register simultaneously when an UpdateWR event is performed. When a write only WDR is connected between WSI and WSO, any CaptureWR event would have no effect on the WDR. Write only WDRs are shifted out during the ShiftWR event.

#### 13.2.2.2.3 Read and Write (R/W)

R/W WDRs are required to operate as merged function of write only and read only WDRs. WDR bit fields that are specified as read/write types are required to capture data bits into the shift stage register during a CaptureWR event and they are also required to update bits from the shift stage into the update stage simultaneously when the UpdateWR event is performed.

#### 13.2.2.2.4 WDR Reset State

All WDRs are required to place their update and or shift stages where applicable in a state that ensures the HBM device returns to mission mode operation and all test modes are disabled when WRST\_n is logic LOW.

Asserting WRST\_n asynchronously asserts these states on the HBM device's IEEE 1500 port logic:

- Sets WIR to BYPASS, effectively clearing any prior EXTEST\_RX, EXTEST\_TX, INTEST\_RX, INTEST\_TX, or CHANNEL\_ID instruction, thus returning all functional pins to their normal functional mode. Boundary scan chains content is undefined.
- No change to any previously loaded SOFT\_REPAIR, HARD\_REPAIR, SOFT\_LANE\_REPAIR, HARD\_LANE\_REPAIR.
- The states of the DWORD\_MISR and AWORD\_MISR registers are undefined.
- Any previously loaded MISR\_MASK is cleared (WDR set to all 1s).
- Sets AWORD\_MISR\_CONFIG Enable to 0 – Off.
- Terminates and disables any MBIST hardware.

### 13.2.3 Test Instructions

This section will outline test instructions that are supported for the HBM device. All instructions are required to have access through the standard IEEE Std 1500 HBM test port. Test instructions are used to enable test features that will be used at the final test steps of the assembled System in Package (SiP). Please refer to the test port description for connectivity details per channel.

Unused and unimplemented instructions will default to BYPASS instruction when the WIR is updated with the unimplemented encoding. Channels that are not selected by WIR[11:8] do not respond to the instruction. Unselected channels are required to ignore any Update, Capture and Shift signals. The CaptureWR, ShiftWR and UpdateWR are required to be qualified by respective channel ID WIR[11:8]. WDRs are required to shift out the least significant bit on WSO port at the first WRCK of the shift sequence. WSO output timing and valid data window are defined per IEEE Std 1500 standard.

#### 13.2.3.1 BYPASS

The BYPASS instruction selects a single bit WDR and connects this register between WSI and each WSO. Upon update of the BYPASS instructions, all channels should connect their respective BYPASS register in parallel between WSI and the channel specific WSO. Data is clocked from WSI to WSO through the one bit WDR by WRCK. BYPASS is the default instruction after assertion of WRST\_n.

##### Wrapper Data Register

When the BYPASS instruction is updated the data register as shown in [Table 85](#) is connected between WSI and WSO.

##### CaptureWR

When BYPASS is the current instruction, the CaptureWR event will have no effect. The BYPASS instruction requires only the shift stage of the data register.

##### UpdateWR

When BYPASS is the current instruction, the UpdateWR event will have no effect. The BYPASS instruction does not require an update register and only requires the shift register stage.

**Table 85 — BYPASS Wrapper Data Register**

Bit Position	Bit Field	Type	Description
0	BYPASS	R/W	Single bit bypass register per IEEE Std 1500

### 13.2.3.2 EXTEST\_RX

EXTEST\_RX is intended for DC I/O connectivity testing similar to board level boundary scan. The receive notation designates that the HBM I/O will sample the logic value and capture into the data register the value that is present at the micro bump interface. All HBM bidirectional I/O and inputs are required to support this instruction. HBM differential inputs and outputs are also required to support EXTEST\_RX on both the true and complement pins. Optionally, vendors may support EXTEST\_RX on outputs as well.

While EXTEST\_RX is the current instruction, all functional pins of the selected channel(s) enter a Hi-Z state, including the output-only pins AERR, DERR, RDQS\_t/RDQS\_c, TEMP[2:0] and CATTRIP. See also [Boundary Scan](#).

#### Wrapper Data Register

When the EXTEST\_RX instruction is updated the data register as shown in [Table 86](#) is connected between WSI and WSO. Please note that the same WDR is specified for EXTEST\_RX and EXTEST\_TX instructions.

#### CaptureWR

When EXTEST\_RX is the current instruction, the CaptureWR event will capture the HBM input and bidirectional I/O values into the shift stage of the WDR. The captured data is shifted out WSO during subsequent ShiftWR event.

#### UpdateWR

When EXTEST\_RX is the current instruction, the UpdateWR event will have no effect.

### 13.2.3.3 EXTEST\_TX

EXTEST\_TX is intended for DC I/O connectivity testing similar to board level boundary scan. The transmit notation designates that the HBM I/O will preload the logic value shifted into the data register at the micro bump interface. All HBM bidirectional I/O and outputs are required to support this instruction. HBM differential inputs and outputs are also required to support EXTEST TX on both the true and complement pins. Optionally, vendors may support EXTEST\_TX on inputs as well.

I/O signals are required to power up as input mode by default. Upon update of EXTEST\_TX, the IOs will change to output mode and must at least remain in output mode until reset of the test logic or until a different instruction is updated on the channel.

#### Wrapper Data Register

When the EXTEST\_TX instruction is updated the data register as shown in [Table 86](#) is connected between WSI and WSO as specified by the vendor. Please note that the same WDR is specified for EXTEST\_RX and EXTEST\_TX instructions.

#### CaptureWR

When EXTEST\_TX is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When EXTEST\_TX is the current instruction, the UpdateWR event will update the outputs and bidirectional IOs in output mode to drive the values shifted into the WDR shift stage. Outputs are required to update simultaneously.

### 13.2.3.3 EXTEST\_RX (cont'd)

**Table 86 — EXTEST\_RX and EXTEST\_TX (Boundary Scan) Wrapper Data Register**

Bit Position	Bit Field	Type	Description
216	R6	I	AWORD
215	C8	I	AWORD
214	TEMP0 0	O I	Signals in MIDSTACK region - channel A only - channels B to H (reserved bit)
213	TEMP1 0	O I	Signals in MIDSTACK region - channel A only - channels B to H (reserved bit)
212	TEMP2 CATTRIP 0	O O I	Signals in MIDSTACK region - channel A only - channel B only - channels C to H (reserved bit)
[211:164]	DWORD3		DWORD 3 (same ordering as DWORD 0)
[163:116]	DWORD2		DWORD 2 (same ordering as DWORD 0)
115	AERR	O	AWORD
114	RR	I	
113	R5	I	
112	R4	I	
111	CK_c	I	
110	CK_t	I	
109	R3	I	
108	R2	I	
107	R1	I	
106	R0	I	
105	RC	I	
104	C7	I	
103	C6	I	
102	C5	I	
101	C4	I	
100	CKE	I	
99	C3	I	
98	C2	I	
97	C1	I	
96	C0	I	
[95:48]	DWORD1		DWORD 1 (same ordering as DWORD 0)
47	DWORD0_DBI3	I/O	Byte 3 of DWORD 0
46	DWORD0_DQ31	I/O	
45	DWORD0_DQ30	I/O	
44	DWORD0_DQ29	I/O	
43	DWORD0_DQ28	I/O	
42	RD1	I/O	
41	DERR0	O	
40	DWORD0_DQ27	I/O	
39	DWORD0_DQ26	I/O	
38	DWORD0_DQ25	I/O	
37	DWORD0_DQ24	I/O	
36	DWORD0_DM3	I/O	

**Table 86 — EXTEST\_RX and EXTEST\_TX (Boundary Scan) Wrapper Data Register (cont'd)**

Bit Position	Bit Field	Type	Description
35	DWORD0_DB12	I/O	Byte 2 of DWORD 0
34	DWORD0_DQ23	I/O	
33	DWORD0_DQ22	I/O	
32	DWORD0_DQ21	I/O	
31	DWORD0_DQ20	I/O	
30	RDQS_c	O	
29	RDQS_t	O	
28	DWORD0_DQ19	I/O	
27	DWORD0_DQ18	I/O	
26	DWORD0_DQ17	I/O	
25	DWORD0_DQ16	I/O	
24	DWORD0_DM2	I/O	
23	DWORD0_DB11	I/O	Byte 1 of DWORD 0
22	DWORD0_DQ15	I/O	
21	DWORD0_DQ14	I/O	
20	DWORD0_DQ13	I/O	
19	DWORD0_DQ12	I/O	
18	WDQS_c	I	
17	WDQS_t	I	
16	DWORD0_DQ11	I/O	
15	DWORD0_DQ10	I/O	
14	DWORD0_DQ9	I/O	
13	DWORD0_DQ8	I/O	
12	DWORD0_DM1	I/O	
11	DWORD0_DB10	I/O	Byte 0 of DWORD 0
10	DWORD0_DQ7	I/O	
9	DWORD0_DQ6	I/O	
8	DWORD0_DQ5	I/O	
7	DWORD0_DQ4	I/O	
6	RD0	I/O	
5	PAR0	I/O	
4	DWORD0_DQ3	I/O	
3	DWORD0_DQ2	I/O	
2	DWORD0_DQ1	I/O	
1	DWORD0_DQ0	I/O	
0	DWORD0_DM0	I/O	

NOTE 1 The WDR length depends on the device configuration: bits 215 and 216 are only present with HBM devices whose channel addressing includes row address RA14 or bank address SID1 or both and which thus provide input pins R6 and C8. See [HBM Channel Addressing](#) table.

### 13.2.3.4 INTEST\_RX

INTEST\_RX is intended for applying test data patterns internally to the inputs of the HBM device. The receive notation designates that the HBM I/O will preload the logic value shifted into the data register to the HBM receiver. It is required that the HBM intest cell design will block the logic values at the micro bump once the HBM is in intest mode. All HBM bidirectional I/O and receive only inputs are required to support this instruction.

#### Wrapper Data Register

When the INTEST\_RX instruction is updated the data register as shown in [Table 87](#) is connected between WSI and WSO as specified by the vendor.

#### CaptureWR

When INTEST\_RX is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When INTEST\_RX is the current instruction, the UpdateWR event will update and apply the values shifted into the WDR shift stage to the inputs and bidirectional IOs in input mode into the HBM. All values must update and apply simultaneously.

**Table 87 — INTEST\_RX Wrapper Data Register**

Bit Position	Bit Field	Type	Description
vendor specific	vendor specific	R	Each vendor is required to provide some type of description language view or connectivity description of the HBM device describing the boundary scan connection scheme per channel ID.

### 13.2.3.5 INTEST\_TX

INTEST\_TX is intended for capturing output results internal to the HBM device. The transmit notation designates that the HBM I/O will capture the logic value into the data register at the transmitter output and shift the data out via the WDR after the Capture event. It is required that the HBM intest cell design will block the input logic values at the micro bump once the HBM is in INTEST\_TX mode. All HBM bidirectional I/O and transmit only outputs are required to support this instruction.

#### Wrapper Data Register

When the INTEST\_TX instruction is updated the data register as shown in [Table 88](#) is connected between WSI and WSO as specified by the vendor.

#### CaptureWR

When INTEST\_TX is the current instruction, the CaptureWR event will capture the internal signal values present at the HBM outputs and IOs in output mode into the shift stage of the WDR.

#### UpdateWR

When INTEST\_TX is the current instruction, the UpdateWR event will have no effect.

### 13.2.3.5 INTEST\_TX (cont'd)

**Table 88 — INTEST\_TX Wrapper Data Register**

Bit Position	Bit Field	Type	Description
vendor specific	vendor specific	W	Each vendor is required to provide some type of description language view or connectivity description of the HBM device describing the boundary scan connection scheme per channel ID.

### 13.2.3.6 HBM\_RESET

The HBM\_RESET instruction is intended to initiate an asynchronous functional reset of the HBM upon update, equivalent to assertion of RESET\_n. Mode registers and HBM functional logic are reset upon update of HBM\_RESET instruction. All HBM logic is reset except for the following exclusions:

- IEEE Std 1500 WSP is not reset by HBM\_RESET instruction update
- IEEE Std 1500 controller logic is not reset by HBM\_RESET instruction update
- No IEEE Std 1500 WDRs are reset by HBM\_RESET instruction update
- Direct access port signal pins are not reset by HBM\_RESET instruction update

#### Wrapper Data Register (Optional)

When the HBM\_RESET instruction is updated the data register as shown in [Table 89](#) is connected between WSI and WSO as specified by the vendor. The HBM\_RESET WDR is optional. If no data register is implemented, then the initiation of HBM\_RESET is required upon update of the instruction. The reset assertion must have a minimum period of t<sub>PW\_RESET</sub>.

#### CaptureWR

When HBM\_RESET is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When HBM\_RESET is the current instruction, the UpdateWR event will load the value from the shift stage into the update stage and initiate the reset sequence.

**Table 89 — HBM\_RESET Wrapper Data Register**

Bit Position	Bit Field	Type	Description
0	HBM_RESET	W	Setting this bit to 1 and updating the WDR will initiate the reset described above. The vendor shall specify time period and/or WRCK requirements if they are needed to perform the reset.

The HBM\_RESET condition is not self-clearing. The host must explicitly set and clear the HBM\_RESET state. To accomplish an HBM reset, the HBM\_RESET state should be applied a minimum duration of t<sub>PW\_RESET</sub> (see [Initialization Sequence with Stable Power](#)).

Note that the implementation of the WDR is optional for the HBM\_RESET instruction. If interoperability is desired across HBM designs where some designs do and other designs do not implement the WDR bit, the suggested sequence the host should apply when using HBM\_RESET is:

1. Shift in and update WIR = HBM\_RESET;
2. Shift in and update WDR = 1;
3. Wait t<sub>PW\_RESET</sub> minimum;

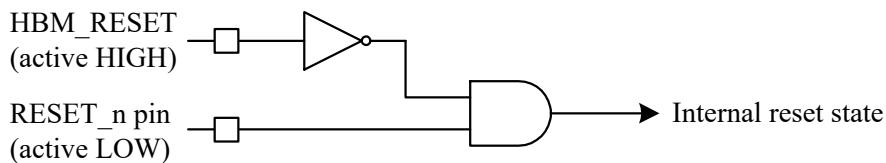
### 13.2.3.6 HBM\_RESET (cont'd)

4. Shift in and update WDR = 0;
5. Shift in and update WIR = BYPASS.

For HBM designs that do not implement the WDR bit, steps 1 and 5 accomplish asserting and clearing the internal reset signal, and steps 2 and 4 are ignored. At step 5, other methods of clearing the HBM\_RESET instruction from the WIR include shifting in and updating a different instruction, and driving WRST\_n LOW.

For HBM designs that do implement the WDR bit, steps 2 and 4 accomplish asserting and clearing the internal reset state. It is recommended, but not required, to clear the HBM\_RESET instruction from the WIR.

Internally, the RESET\_n pin and the HBM\_RESET instruction are logically combined such that when either is true then the internal reset state is true. During power-up it is required that WRST\_n be driven LOW, thus ensuring that the uninitialized 1500 port logic does not interfere with the power-up initialization sequence.



**Figure 96 — RESET\_n and HBM\_RESET Logic**

After the power-up initialization, the RESET\_n pin is HIGH, and subsequent stable-power resets may be asserted by either driving the RESET\_n pin LOW, or by using the HBM\_RESET instruction. Note that the HBM\_RESET instruction may not be used to bring the HBM device out of reset while the external RESET\_n pin is driven LOW. Similarly, the HBM device may not be brought out of reset using the RESET\_n pin while reset is asserted using the HBM\_RESET instruction.

**Table 90 — RESET\_n and HBM\_RESET Truth Table**

RESET_n	HBM_RESET	Internal Reset State
LOW	0	Reset asserted by RESET_n
LOW	1	Reset asserted by both RESET_n and HBM_RESET
HIGH	0	Out of reset state
HIGH	1	Reset asserted by HBM_RESET

### 13.2.3.7 MBIST

The MBIST instruction is used for HBM device hosted memory built in self-test. HBM devices must support memory MBIST. This instruction format and data register field configuration is required for IEEE Std 1500 access to the test feature. MBIST engine clock source can be WRCK as a direct clock source or reference clock source or an internal clocked mode independent of WRCK and independent of any I/O functional clocks is also acceptable.

#### Wrapper Data Register

When the MBIST instruction is updated the data register as shown in [Table 91](#) is connected between WSI and WSO.

### 13.2.3.7 MBIST (cont'd)

#### CaptureWR

When MBIST is the current instruction, the CaptureWR event will capture read or read/write bit fields into the shift stage of the WDR.

#### UpdateWR

When MBIST is the current instruction, the UpdateWR event will load the write and read/write bit fields from the shift stage to the update stage of the WDR simultaneously.

**Table 91 — MBIST Wrapper Data Register**

Bit Position	Bit Field	Type	Description
MSB	MBIST_START	W	Initiates the MBIST test on the HBM. MBIST test is initiated by writing a 1 to this field and updating the WDR.
[(MSB-1):0]	OPTIONS and STATUS	R/W	Vendor specific registers.

### 13.2.3.8 SOFT\_REPAIR

The SOFT\_REPAIR instruction allows the user to temporarily repair bit cells in the HBM without using permanent fusing mechanism to initiate the repair. This feature is intended to enable validation that the intended repair works as expected. Once a soft repair is validated, the user may choose to perform a fused hard repair via the HARD\_REPAIR instruction.

#### Wrapper Data Register

When the SOFT\_REPAIR instruction is updated the data register as shown in [Table 92](#) is connected between WSI and WSO as specified by the vendor.

#### CaptureWR

When SOFT\_REPAIR is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When SOFT\_REPAIR is the current instruction, the UpdateWR event will load the write only bit fields from the shift stage into the update stage simultaneously. Completion of the update event will initiate the soft repair sequence.

**Table 92 — SOFT\_REPAIR Wrapper Data Register**

Bit Position	Bit Field	Type	Description
vendor specific	SOFT_REPAIR_START	W	Initiates the soft repair when updated.
	REPAIR_VECTOR	W	Vendor specific failing address from MBIST WDR. Vendor may also provide “logical address”-to-“repair vector” encoding.

### 13.2.3.9 HARD\_REPAIR

The HARD\_REPAIR instruction is used to permanently repair failing bit cells detected in the HBM. It is required that a fuse rupture scheme is used to implement the repair. The repair sequence will be initiated on update of the data register. After some vendor specified time period fuse rupture automatically completes and repair is affected. Hard repair will be permanent. Completion of HARD\_REPAIR requires a subsequent chip reset as described in [Interaction with Mission Mode Operation](#). The HBM vendor is required to specify the time to wait after updating the HARD\_REPAIR WDR as well as any requirements for WRCK clocking if required to perform the repair.

#### Wrapper Data Register

When the HARD\_REPAIR instruction is updated the data register as shown in [Table 93](#) is connected between WSI and WSO as specified by the vendor.

#### CaptureWR

When HARD\_REPAIR is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When HARD\_REPAIR is the current instruction, the UpdateWR event will load the write only bit fields from the shift stage into the update stage simultaneously. Completion of the update event will initiate the hard repair sequence.

**Table 93 — HARD\_REPAIR Wrapper Data Register**

Bit Position	Bit Field	Type	Description
vendor specific	HARD_REPAIR_START	W	Initiates the hard repair when updated.
	REPAIR_VECTOR	W	Vendor specific failing address from MBIST WDR. Vendor may also provide “logical address”-to-“repair vector” encoding.

### 13.2.3.10 DWORD\_MISR

This instruction is used to capture the DWORD MISR value and allows the value to be shifted out on the WSO output. The MISR in this instruction is associated with the Data Word I/O test feature. Required data register bit positions are specified in the Data Register section of this instruction. Data register notation is "...\_F" for bits clocked on falling edge and "...R" for bits clocked on rising edge. Note that some implementations may destroy the content of the MISR registers when read, thus the content of the MISR registers is not specified after shifting out MISR content. The host should reinitialize the MISR registers (such as MR7 Preset) before additional testing. See section [HBM Loopback Test Modes](#) for MISR mode features and usage.

#### Wrapper Data Register

When the DWORD\_MISR instruction is updated the data register as shown in [Table 94](#) is connected between WSI and WSO.

#### CaptureWR

When DWORD\_MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR.

### 13.2.3.10 DWORD\_MISR (cont'd)

#### UpdateWR (optional)

When DWORD\_MISR is the current instruction, the UpdateWR event will load the bits from the shift stage into the DWORD MISRs. The UpdateWR event will have no effect when the optional feature is not supported by the device.

**Table 94 — DWORD\_MISR Wrapper Data Register**

Bit Position	Bit Field	Type	Description
[319:240]	DWORD3	R	DWORD3 (Same bit ordering as DWORD0)
[239:160]	DWORD2	R	DWORD2 (Same bit ordering as DWORD0)
[159:80]	DWORD1	R	DWORD1 (Same bit ordering as DWORD0)
[79:60]	DWORD0_BYTE3	R	Byte 3 of DWORD0 (Same ordering as BYTE0)
[59:40]	DWORD0_BYTE2	R	Byte 2 of DWORD0 (Same ordering as BYTE0)
[39:20]	DWORD0_BYTE1	R	Byte 1 of DWORD0 (Same ordering as BYTE0)
19	DWORD0_DBI0_F	R	Byte 0 of DWORD0
18	DWORD0_DBI0_R	R	
17	DWORD0_DQ_F7	R	
16	DWORD0_DQ_R7	R	
15	DWORD0_DQ_F6	R	
14	DWORD0_DQ_R6	R	
13	DWORD0_DQ_F5	R	
12	DWORD0_DQ_R5	R	
11	DWORD0_DQ_F4	R	
10	DWORD0_DQ_R4	R	
9	DWORD0_DQ_F3	R	
8	DWORD0_DQ_R3	R	
7	DWORD0_DQ_F2	R	
6	DWORD0_DQ_R2	R	
5	DWORD0_DQ_F1	R	
4	DWORD0_DQ_R1	R	
3	DWORD0_DQ_F0	R	
2	DWORD0_DQ_R0	R	
1	DWORD0_DM0_F	R	
0	DWORD0_DM0_R	R	

### 13.2.3.11 AWORD\_MISR

This instruction is used to capture the AWORD MISR value and allows the value to be shifted out on the configured WSO outputs. The MISR in this instruction is associated with the Address Word loopback test feature. Required data register bit positions are specified in the Data Register section of this instruction. Data register notation is "...\_F" for bits clocked on falling edge and "...R" for bits clocked on rising edge. Note that some implementations may destroy the content of the MISR registers when read, thus the content of the MISR registers is not specified after shifting out MISR content. The host should reinitialize the MISR registers (such as AWORD\_MISR\_CONFIG Preset) before additional testing. See [HBM Loopback Test Modes](#) for MISR mode features and usage.

#### Wrapper Data Register

When the AWORD\_MISR instruction is updated the data register as shown in [Table 95](#) is connected between WSI and WSO. Please note that two different lengths are defined for this WDR in the presence of the R6 and C8 input pins. For those devices the WDR length depends on the POLYNOMIAL\_SELECT bit in the [AWORD\\_MISR\\_CONFIG](#) WDR.

#### CaptureWR

When AWORD\_MISR is the current instruction, the CaptureWR event will load the respective MISR values into the shift stage of the WDR.

#### UpdateWR

When AWORD\_MISR is the current instruction, the UpdateWR event will have no effect.

## 13.2.3.11 AWORD\_MISR (cont'd)

Table 95 — AWORD\_MISR Wrapper Data Register

30-bit Polynomial		34-bit Polynomial		Type	Description
Bit Position	Bit Field	Bit Position	Bit Field		
29	R_F5	33	R_F5	R	The POLYNOMIAL_SELECT bit in the AWORD_MISR_CONFIG Wrapper Data Register selects between the 30-bit and 34-bit register options. This selection is only available for HBM devices whose channel addressing includes row address RA14 or bank address SID1 or both and which thus provide input pins R6 and C8. For other HBM devices only the 30-bit register is defined.
	R_R5	32	R_R5	R	
	R_F4	31	R_F4	R	
	R_R4	30	R_R4	R	
29	R_F5	29	R_F3	R	
28	R_R5	28	R_R3	R	
27	R_F4	27	R_F2	R	
26	R_R4	26	R_R2	R	
25	R_F3	25	R_F1	R	
24	R_R3	24	R_R1	R	
23	R_F2	23	R_F0	R	
22	R_R2	22	R_R0	R	
21	R_F1	21	R_F6	R	
20	R_R1	20	R_R6	R	
19	R_F0	19	C_F7	R	
18	R_R0	18	C_R7	R	
17	C_F7	17	C_F6	R	
16	C_R7	16	C_R6	R	
15	C_F6	15	C_F5	R	
14	C_R6	14	C_R5	R	
13	C_F5	13	C_F4	R	
12	C_R5	12	C_R4	R	
11	C_F4	11	CKE_F	R	
10	C_R4	10	CKE_R	R	
9	CKE_F	9	C_F3	R	
8	CKE_R	8	C_R3	R	
7	C_F3	7	C_F2	R	
6	C_R3	6	C_R2	R	
5	C_F2	5	C_F1	R	
4	C_R2	4	C_R1	R	
3	C_F1	3	C_F0	R	
2	C_R1	2	C_R0	R	
1	C_F0	1	C_F8	R	
0	C_R0	0	C_R8	R	

NOTE 1 The POLYNOMIAL\_SELECT bit in the AWORD\_MISR\_CONFIG Wrapper Data Register selects between the 30-bit and 34-bit register options. This selection is only available for HBM devices whose channel addressing includes row address RA14 or bank address SID1 or both and which thus provide input pins R6 and C8. For other HBM devices only the 30-bit register is defined.

### 13.2.3.12 CHANNEL\_ID

This instruction is intended to enable HBM channel identification. The channel(s) specified in WIR[11:8] will drive all TX IOs including RD, DM and PAR associated with the channel(s) upon update of this instruction with ENABLE=1. DM and PAR are driven even if the respective mission mode functions are disabled in the mode registers.

Updating the channel to ENABLE=0 will return the TX I/O to default state. WRST should also clear the enable bit returning all TX IOs to default state if modified.

#### Wrapper Data Register (Optional)

When the CHANNEL\_ID instruction is updated the data register as shown in [Table 96](#) is connected between WSI and WSO. The CHANNEL\_ID WDR is optional. If no data register is implemented, then the initiation of TX drive is required upon update of the instruction and all TXs return to default state when any instruction other than CHANNEL\_ID is updated to the WIR.

#### CaptureWR

When CHANNEL\_ID is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When CHANNEL\_ID is the current instruction, the UpdateWR event will load the enable bit from the shift stage into the update stage of the WDR. Completion of the UpdateWR event will initiate transmitters for the specified channel to drive based on the bit field value updated.

**Table 96 — CHANNEL\_ID Wrapper Data Register**

Bit Position	Bit Field	Type	Description
0	ENABLE	W	Setting this bit to 1 and updating the instruction will drive all TX IOs to logical High.

### 13.2.3.13 MISR\_MASK

MISR\_MASK instruction is used with AWORD MISR and DWORD MISR test modes. The DWORD MISR and AWORD MISR test modes must be configured prior to using the MISR\_MASK instruction. The DWORD MISR test mode is enabled and configured via MODE\_REGISTER\_SET\_DUMP instruction or mission mode access to Mode Register 7 and the AWORD MISR test mode is enabled and configured via the AWORD\_MISR\_CONFIG instruction. Updating this instruction's data register will mask out desired bit(s) during the MISR test according to the WDR bit field descriptions. See [HBM Loopback Test Modes](#) for MISR mode features and usage.

#### Wrapper Data Register

When the MISR\_MASK instruction is updated the data register as shown in [Table 97](#) is connected between WSI and WSO.

#### CaptureWR

When MISR\_MASK is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When MISR\_MASK is the current instruction, the UpdateWR event will load the mask bit from the shift stage into the update stage of the WDR. Completion of the UpdateWR event will enable the mask for the specified MISR input. All mask values are required to update simultaneously.

### 13.2.3.13 MISR\_MASK (cont'd)

**Table 97 — MISR\_MASK Wrapper Data Register**

Bit Position	Bit Field	Type	Description
[71:56]	DWORD3_MASK[15:0]	W	Mask applied to DWORD 3. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
[55:40]	DWORD2_MASK[15:0]	W	Mask applied to DWORD 2. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
[39:36]	AWORD_RA_MASK[3:0]	W	Mask applied to address word. Masked bit is forced to 0 on corresponding MISR input. 0h - 5h: R0 - R5 mask 6h: CKE mask 7h: R6 mask 8h - Eh: Reserved Fh: No mask. Default.
[35:32]	AWORD_CA_MASK[3:0]	W	Mask applied to address word. Masked bit is forced to 0 on corresponding MISR input. 0h - 8h: C0 - C8 mask 9h - Eh: Reserved Fh: No mask. Default
[31:16]	DWORD1_MASK[15:0]	W	Mask applied to DWORD 1. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_MASK description
[15:12]	DWORD0_BYTE3_MASK[3:0]	W	Mask applied to DWORD 0 Byte 3. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description
[11:8]	DWORD0_BYTE2_MASK[3:0]	W	Mask applied to DWORD 0 Byte 2 Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description
[7:4]	DWORD0_BYTE1_MASK[3:0]	W	Mask applied to DWORD 0 Byte 1. Masked bit is forced to 0 on corresponding MISR input. Encoding shown in DWORD0_BYTE0_MASK description
[3:0]	DWORD0_BYTE0_MASK[3:0]	W	Mask applied to DWORD 0 Byte 0. Masked bit is forced to 0 on corresponding MISR input. 0h: DM0 Mask 1h - 8h: DQ0 - DQ7 Mask 9h: DBI Mask Ah - Eh: Reserved Fh: No mask. Default.

### 13.2.3.14 AWORD\_MISR\_CONFIG

This instruction will provide IEEE Std 1500 access to the AWORD MISR test instruction configuration specified in the data register. Configuration bits are set after the UpdateWR event. See [HBM Loopback Test Modes](#) for MISR mode features and usage.

#### Wrapper Data Register

When the AWORD\_MISR\_CONFIG instruction is updated the data register as shown in [Table 98](#) is connected between WSI and WSO.

#### CaptureWR

When AWORD\_MISR\_CONFIG is the current instruction, the CaptureWR event will have no effect.

#### UpdateWR

When AWORD\_MISR\_CONFIG is the current instruction, the UpdateWR event will load the configuration bits from the shift stage into the update stage of the WDR. Completion of the update event will enable the AWORD MISR and configure the register into the proper mode. All values are required to update simultaneously.

**Table 98 — AWORD\_MISR\_CONFIG Wrapper Data Register**

Bit Position	Bit Field	Type	Description
[7] <sup>1</sup>	POLYNOMIAL_SELECT or VENDOR_SPECIFIC	W	0 - 30-bit polynomial 1 - 34-bit polynomial  See bits [6:4]
[6:4]	VENDOR_SPECIFIC	W	Vendor will specify bit fields needed to enable and configure the AWORD MISR.
3	ENABLE	W	0 - Off 1 - On
[2:0]	MODE[2:0]	W	000 - Preset The AWORD MISR/LFSR is set to 0x2AAAAAAAh for the 30-bit polynomial and 0x2AAAAAAAAh for the 34-bit polynomial, the AWORD LFSR_COMPARE_STICKY bits are set to all zeros, and the AWORD preamble clock filter circuit is enabled. 001 - Reserved 010 - Register mode AWORD transfers are captured directly to the MISR register without compression to directly set an alternate MISR seed value. Note: Register mode cannot be used to set an alternate seed value (see <a href="#">Test method for AWORD (Write) Register Mode</a> ) 011 - MISR mode 100 - LFSR Compare mode
NOTE 1 Bit 7 is POLYNOMIAL_SELECT for HBM devices whose channel addressing includes row address RA14 or bank address SID1 or both and which thus provide input pins R6 and C8. For other HBM devices bit 7 is VENDOR_SPECIFIC.			

### 13.2.3.15 DEVICE\_ID

This instruction allows shift out of the DEVICE\_ID WDR. WDR fields are required for both a global ID and a per channel ID. The per channel ID data registers are intended to support vendors who require additional resolution for identifying the device.

#### Wrapper Data Register

When the DEVICE\_ID instruction is updated the data register as shown in [Table 99](#) is connected between WSI and WSO.

#### CaptureWR

When DEVICE\_ID is the current instruction, the CaptureWR event will load the respective identification field values into the shift stage of the WDR.

#### UpdateWR

When DEVICE\_ID is the current instruction, the UpdateWR event will have no effect.

**Table 99 — DEVICE\_ID Wrapper Data Register**

Bit Position	Bit Field	Type	Description
81	GEN2_TEST	R	Gen-2 feature support: – Lane Remapping modes 1 & 2 with hard/soft repair and readable – RD, RR, RC micro-bumps in the BScan chains – MISR Preset to 0xAAAAAh / 0x2AAAAAAAh / 0x2AAAAAAAAh – MISRs writable for setting seeds (optional) – LFSR Compare – 3-bit AWORD_MISR_CONFIG – MISR/LFSR Compare features expect and preamble clock filter 0 - features not support 1 - features supported (see vendor datasheet for optional features)
80	ECC	R	ECC support 0 - no ECC support 1 - ECC supported
[79:76]	DENSITY <sup>1</sup>	R	Memory density per channel (see <a href="#">HBM Channel Addressing</a> ) 0001 - 1 Gb 0010 - 2 Gb 0011 - 4 Gb 0100 - 8 Gb (8 Gb 8-High) 0101 - 6 Gb 0110 - 8 Gb 1000 - 12 Gb (12 Gb 8-High) 1001 - 12 Gb (8 Gb 12-High) 1010 - 16 Gb (16 Gb 8-High) 1011 - 18 Gb (12 Gb 12-High) 1100 - 24 Gb (16 Gb 12-High) All others - Reserved
[75:72]	MANUFACTURER_ID[3:0]	R	0000 - Reserved 0001 - Samsung 0010 - Reserved 0011 - Reserved 0100 - Reserved 0101 - Reserved 0110 - SK Hynix 0111 .. 1110 - Reserved 1111 - Micron

**Table 99 — DEVICE\_ID Wrapper Data Register (cont'd)**

<b>Bit Position</b>	<b>Bit Field</b>	<b>Type</b>	<b>Description</b>
[71:68]	MANUFACTURING_LOCATION[3:0]	R	Vendor specific
[67:60]	MANUFACTURING_YEAR[7:0]	R	Binary encoded year from 2011 2011 = 0000000; 2015 = 00000100
[59:52]	MANUFACTURING_WEEK[7:0]	R	Binary encoded week WW52 = 00110100
[51:18]	SERIAL_NUMBER[33:0]	R	Unique ID per device
[17:16]	ADDRESSING_MODE[1:0]	R	Addressing Mode Support 01 = Only Pseudo Channel Mode Supported 10 = Only Legacy Mode Supported 00 = Illegal 11 = Illegal
[15:8]	CHANNEL_AVAILABLE[7:0]	R	Channel Available 0 - Channel not present / not working 1 - Channel present / working Channel encoding (1 bit per channel): 0] channel a 1: channel b ... 6: channel g 7: channel h
7	HBM_STACK_HEIGHT	R	HBM Stack Height 0 = 2- or 4-High Stack 1 = 8-High Stack
[6:0]	MODEL_PART_NUMBER[6:0]	R	Vendor reserved
NOTE 1 The addressing table defines 2 different configurations for 8 Gb/channel and 12 Gb/channel, which have 2 entries each.			

### 13.2.3.16 TEMPERATURE

This instruction captures the temperature sensor reading from the WDR. The digital value of the HBM temperature sensor is latched into the data register on Capture and shifted out on WSO. Temperature reporting in this register is specified as an 8-bit field. The MSB indicates temperature sensor valid status. The remaining 7 bits indicate the temperature in degrees Celsius.

#### Wrapper Data Register

When the TEMPERATURE instruction is updated the data register as shown in [Table 100](#) is connected between WSI and WSO.

#### CaptureWR

When TEMPERATURE is the current instruction, the CaptureWR event will load the respective temperature field values into the shift stage of the WDR.

#### UpdateWR

When TEMPERATURE is the current instruction, the UpdateWR event will have no effect.

**Table 100 — TEMPERATURE Wrapper Data Register**

Bit Position	Bit Field	Type	Description
7	VALID[0]	R	Temperature sensor output valid 0 - Valid 1 - Invalid
[6:0]	TEMP[6:0]	R	Temperature in Degrees Celsius. Examples: 7'b 0000000 = 0 °C (or less) 7'b 0011001 = 25 °C 7'b 1111111 = 127 °C

### 13.2.3.17 MODE\_REGISTER\_DUMP\_SET

This instruction provides IEEE Std 1500 access to read and write the HBM Mode Registers. When this instruction is updated into the WIR, the Mode Registers values are loaded into the MODE\_REGISTER\_DUMP\_SET WDR on Capture and the values in the shift data register are updated to the Mode Register upon update. During a Capture event the existing MR state should be preserved while not affecting device operation. Per channel MR is accessed by selected channel WIR[11:8]. All channel select, WIR[11:8] = 4'hF, captures all MR values in parallel into each channel's WDR and shifts out each channel's WSO in parallel.

#### Wrapper Data Register

When the MODE\_REGISTER\_DUMP\_SET instruction is updated the data register as shown in [Table 101](#) is connected between WSI and WSO.

#### CaptureWR

When MODE\_REGISTER\_DUMP\_SET is the current instruction, the CaptureWR event will capture bit fields into the shift stage of the WDR. The MODE REGISTER DUMP SET instruction is required to allow bit fields that correspond to unimplemented MRs to capture an unknown 'X' value.

#### UpdateWR

When MODE\_REGISTER\_DUMP\_SET is the current instruction, the UpdateWR event will load the bit fields from the shift stage to the update stage of the WDR simultaneously. When the update event is complete the mode register settings are required to take effect.

**Table 101 — MODE\_REGISTER\_DUMP\_SET Wrapper Data Register**

Bit Position	Bit Field	Type	Description
[127:120]	MR15	R/W	MR15[7:0]
[119:112]	MR14	R/W	MR14[7:0]
[111:104]	MR13	R/W	MR13[7:0]
[103:96]	MR12	R/W	MR12[7:0]
[95:88]	MR11	R/W	MR11[7:0]
[87:80]	MR10	R/W	MR10[7:0]
[79:72]	MR9	R/W	MR9[7:0]
[71:64]	MR8	R/W	MR8[7:0]
[63:56]	MR7	R/W	MR7[7:0]
[55:48]	MR6	R/W	MR6[7:0]
[47:40]	MR5	R/W	MR5[7:0]
[39:32]	MR4	R/W	MR4[7:0]
[31:24]	MR3	R/W	MR3[7:0]
[23:16]	MR2	R/W	MR2[7:0]
[15:8]	MR1	R/W	MR1[7:0]
[7:0]	MR0	R/W	MR0[7:0]

### 13.2.3.18 READ\_LFSR\_COMPARE\_STICKY

This instruction is used to capture the LFSR Compare Sticky error data to be shifted out on the WSO output. The register in this instruction is associated with the AWORD and DWORD I/O loopback test features. Required data register bit positions are specified in the Data Register section of this instruction in [Table 102](#). Note that some implementations may destroy the content of the related MISR registers when the sticky error data is read, thus the content of the MISR registers is not specified after shifting out sticky error content. The host should reinitialize the MISR registers (such as with MR7 Preset and AWORD\_MISR\_CONFIG preset) before additional testing. See section [HBM Loopback Test Modes](#) for MISR mode features and usage.

While both the AWORD and DWORD sticky error bits share this common WDR, the bits are set and cleared only by their respective AWORD or DWORD Preset and LFSR Compare operations. For example, an AWORD\_MISR\_CONFIG Preset operation is defined to clear the AWORD sticky error bits, and the state of the DWORD sticky error bits is undefined; therefore, the host should ignore the DWORD sticky error bits when operating the AWORD LFSR Compare mode. Conversely, the DWORD\_MISR\_CONFIG Preset operation is defined to clear the DWORD sticky error bits, and the state of the AWORD sticky error bits is undefined; therefore, the host should ignore the AWORD sticky error bits when operating the DWORD LFSR Compare mode.

#### Wrapper Data Register

When the READ\_LFSR\_COMPARE\_STICKY instruction is updated the data register as shown in [Table 102](#) is connected between WSI and WSO. Please note that two different lengths are defined for this WDR, depending on the presence of the R6 and C8 input pins. In a device that provides input pins R6 and C8, the WDR length is 175 bits (Var. 1 in [Table 102](#)) if a 30-bit polynomial is selected through the POLYNOMIAL\_SELECT bit in the AWORD\_MISR\_CONFIG WDR, and 177 bits (Var. 2 in [Table 102](#)) if a 34-bit polynomial is selected. The WDR length is 175 bits in a device that does not provide input pins R6 and C8.

#### CaptureWR

When READ READ\_LFSR\_COMPARE\_STICKY is the current instruction, the CaptureWR event will load the sticky error values into the shift stage of the WDR.

#### UpdateWR

When READ\_LFSR\_COMPARE\_STICKY is the current instruction, the UpdateWR event will have no effect.

### 13.2.3.18 READ\_LFSR\_COMPARE\_STICKY (cont'd)

**Table 102 — READ\_LFSR\_COMPARE\_STICKY Wrapper Data Register**

Var. 1	Var. 2			
Bit Position	Bit Position	Bit Field	Type	Description
174	176	DWORD3_DBI3	R	Byte 3 of DWORD3
173	175	DWORD3_DQ31	R	
172	174	DWORD3_DQ30	R	
171	173	DWORD3_DQ29	R	
170	172	DWORD3_DQ28	R	
169	171	DWORD3_DQ27	R	
168	170	DWORD3_DQ26	R	
167	169	DWORD3_DQ25	R	
166	168	DWORD3_DQ24	R	
165	167	DWORD3_DM3	R	
[164:155]	[166:157]	DWORD3_BYT2	R	Byte 2 of DWORD3 (Same bit ordering as BYTE3)
[154:145]	[156:147]	DWORD3_BYT1	R	Byte 1 of DWORD3 (Same bit ordering as BYTE3)
[144:135]	[146:137]	DWORD3_BYT0	R	Byte 0 of DWORD3 (Same bit ordering as BYTE3)
[134:95]	[136:97]	DWORD2	R	DWORD2 (Same bit ordering as DWORD3)
94	96	R5	R	AWORD
93	95	R4	R	
92	94	R3	R	
91	93	R2	R	
90	92	R1	R	
89	91	R0	R	
—	90	R6 (Variation 2 only)	R	
88	89	C7	R	
87	88	C6	R	
86	87	C5	R	
85	86	C4	R	
84	85	CKE	R	
83	84	C3	R	
82	83	C2	R	
81	82	C1	R	
80	81	C0	R	
—	80	C8 (Variation 2 only)	R	
[79:40]	[79:40]	DWORD1	R	DWORD1 (Same bit ordering as DWORD3)
[39:0]	[39:0]	DWORD0	R	DWORD0 (Same bit ordering as DWORD3)

NOTE 1 Variation 2 of this WDR is provided for HBM devices whose channel addressing includes row address RA14 or bank address SID1 or both and which thus provide input pins R6 and C8. Variation 1 of this WDR is provided for all other HBM devices.

### 13.2.3.19 SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR

The SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR instructions are used to convey lane remapping and repair information. Both instructions use the same LANE\_REPAIR WDR.

#### Wrapper Data Register

When SOFT\_LANE\_REPAIR or HARD\_LANE\_REPAIR is the current instruction, the LANE\_REPAIR wrapper data register as shown in [Table 103](#) is connected between WSI and WSO.

Please note that the encoding of the LANE\_REPAIR WDR has intentionally been defined similar to the MISR\_MASK WDR, to allow DRAM vendors to share hardware resources for both WDRs.

[Figure 97](#) illustrates the interaction between SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR instructions and the associated registers. It is pointed out that the actual I/O lane remapping is derived from the content of the lane repair shadow register.

#### CaptureWR

When either SOFT\_LANE\_REPAIR or HARD\_LANE\_REPAIR is the current instruction, the CaptureWR event will load the lane remapping data from the lane repair shadow register into the shift stage of the WDR. This internal lane repair shadow register is pre-loaded with the repair data from a preceding HARD\_LANE\_REPAIR operation upon HBM device initialization (RESET\_n pulled Low). The memory controller may use these data to configure the lane repair accordingly at the host; it may also use these data as a seed value for subsequent lane repair operations.

#### UpdateWR

When SOFT\_LANE\_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the lane repair shadow register and force the I/O lanes to be remapped accordingly. This remapping is non-persistent; it will be lost when RESET\_n is pulled low or the device loses power. Pulling WRST\_n low does not reset the lane repair shadow register.

When HARD\_LANE\_REPAIR is the current instruction, the UpdateWR event will load the lane remapping data from the shift stage of the WDR into the hard lane repair register. The controller must wait  $t_{HLREP}$  to allow the device to complete this operation and permanently store the repair vector.

Only a single broken lane can be repaired at a time, in order to limit the current constraint of the associated circuits. If multiple lanes are to be repaired, it is required to shift in the repair vectors for each broken lane sequentially, with all other lane repair setting = Fh, and initiate each actual lane repair with a separate UpdateWR event.

The UpdateWR event itself does not lead to an actual re-mapping of the I/O lanes. For such re-mapping to get effective it is required to initiate an HBM chip reset by pulling RESET\_n LOW, which copies the repair vector from the hard lane repair register into the lane repair shadow register as shown in [Figure 97](#).

### 13.2.3.19 SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR (cont'd)

**Table 103 — LANE\_REPAIR Wrapper Data Register**

Bit Position	Bit Field	Type	Description
[71:56]	DWORD3[15:0]	R/W	Lane remapping applied to DWORD 3. Encoding shown in DWORD0 description.
[55:40]	DWORD2[15:0]	R/W	Lane remapping applied to DWORD 2. Encoding shown in DWORD0 description.
[39:36]	AWORD_RA[3:0]	R/W	Lane remapping applied to AWORD. 0h - 6h: R0 - R6 7h - Eh: Reserved Fh: No lane remapping. Default.
[35:32]	AWORD_CA[3:0]	R/W	Lane remapping applied to AWORD. 0h - 8h: C0 - C8 9h - Eh: Reserved Fh: No lane remapping. Default.
[31:16]	DWORD1[15:0]	R/W	Lane remapping applied to DWORD 1. Encoding shown in DWORD0 description.
[15:12]	DWORD0_BYT3[3:0]	R/W	Lane remapping applied to DWORD 0 byte 3. Encoding shown in DWORD0_BYT0 description.
[11:8]	DWORD0_BYT2[3:0]	R/W	Lane remapping applied to DWORD 0 byte 2. Encoding shown in DWORD0_BYT0 description.
[7:4]	DWORD0_BYT1[3:0]	R/W	Lane remapping applied to DWORD 0 byte 1. Encoding shown in DWORD0_BYT0 description.
[3:0]	DWORD0_BYT0[3:0]	R/W	Lane remapping applied to DWORD 0 Byte 0. 0h: DM0 1h - 8h: DQ0 - DQ7 9h: DBI for lane remapping using Mode 2. Reserved for lane remapping using Mode 1. Ah - Dh: Reserved Eh: Reserved for lane repair using Mode 1. Enables/disables RD pin with lane repair in other byte using Mode 2. Fh: No lane remapping. Default.

### 13.2.3.19 SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR (cont'd)

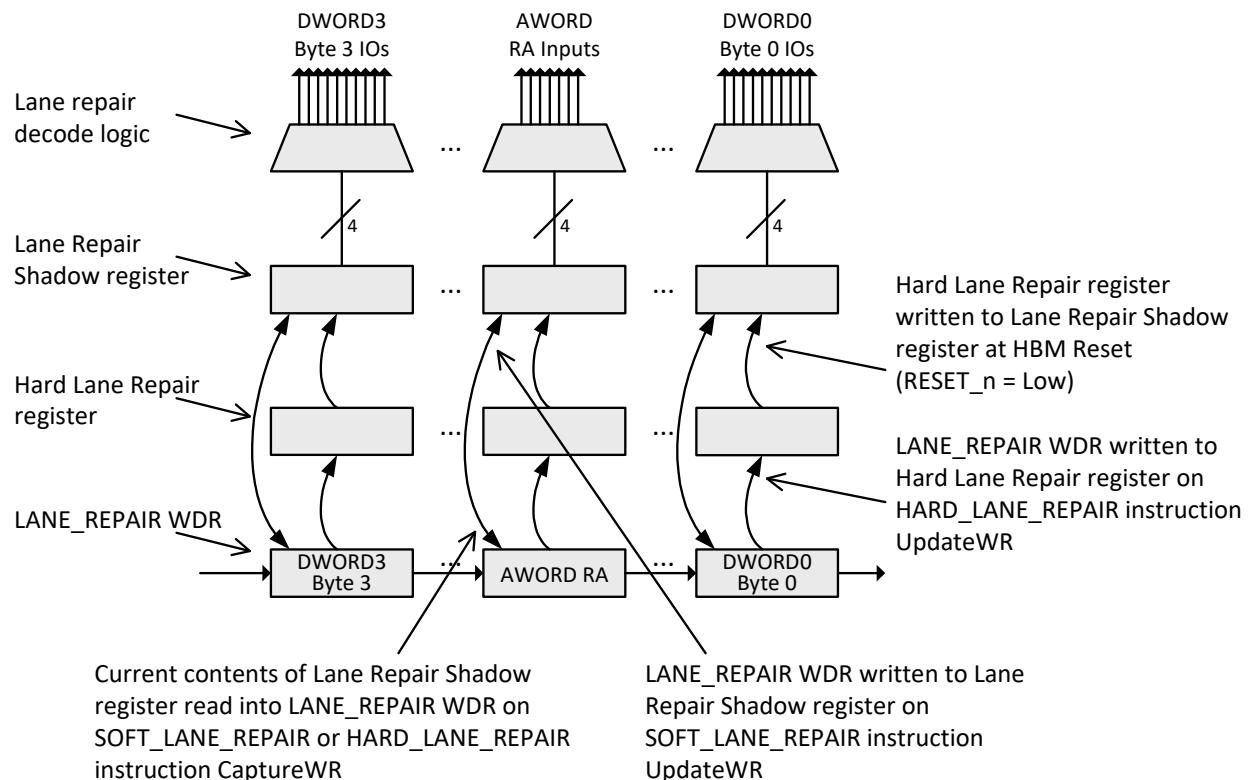


Figure 97 — Registers associated with Lane Repair Instructions

### 13.2.4 Interaction with Mission Mode Operation

[Table 104](#) defines the interaction of the various IEEE 1500 port instructions with mission mode operation, and any instruction exit requirements (see also [Table 84](#) for all IEEE1500 instructions).

**Table 104 — IEEE1500 Port Instruction Interactions**

Instruction	Interaction with Mission Mode	Post Instruction Requirements
BYPASS DWORD_MISR (1) AWORD_MISR (1) MISR_MASK (1) READ_LFSR_COMPARE_STICKY (1) DEVICE_ID TEMPERATURE MODE_REGISTER_DUMP_SET (dump)	Instructions may be used at any time. Core memory content is retained if refresh specifications are met.	None
SOFT_REPAIR (2) SOFT_LANE_REPAIR (2) MODE_REGISTER_DUMP_SET (set) AWORD_MISR_CONFIG (3)	Core memory content is retained if refresh specifications are met.	Meet IEEE1500 Port AC Timings (see <a href="#">Table 105</a> )
EXTEST_RX, EXTEST_TX INTEST_RX, INTEST_TX MBIST CHANNEL_ID HARD_REPAIR (4) HARD_LANE_REPAIR (4)	HBM interface state and core memory content is not defined.	Reset
NOTE 1 While accessing these MISR-related registers has no interaction with mission mode, operating the AWORD and DWORD MISR modes may result in memory content loss unless the channel is put into self refresh mode. See <a href="#">HBM Loopback Test Modes</a> .		
NOTE 2 Soft memory array and lane repairs imply that memory content is at least partially incorrect. While the HBM device imposes no restrictions on the interface state and memory content, the host should consider the health of the memory content based on the repair(s) being applied.		
NOTE 3 See <a href="#">HBM Loopback Test Modes</a> for proper sequencing of the AWORD MISR test modes.		
NOTE 4 Hard memory array and lane repairs involve blowing fuses. Normal operation on any channel is not supported when the hard repair operations are used. A reset is required after hard repair operations before returning the HBM to normal operation.		

### 13.2.5 IEEE1500 Port AC Timing Parameters

Table 105 — IEEE1500 Port AC Timings 1,2

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
<b>IEEE1500 Port I/O Timings</b>					
WRCK clock period	$t_{CKTP}$	20	—	ns	
WRCK clock high pulse width	$t_{CKTPH}$	0.45	—	$t_{CKTP}$	
WRCK clock low pulse width	$t_{CKTPL}$	0.45	—	$t_{CKTP}$	
WRST_n pulse width low	$t_{WRSTL}$	100	—	ns	
IEEE1500 port operation after WRST_n deassertion	$t_{WINIT1}$	3	—	$t_{CKTP}$	
Rising WRST_n edge to WRCK setup time	$t_{SWRST}$		—	ns	
WSP input setup time to WRCK rising edge	$t_{SR}$		—	ns	3
WSP input hold time from WRCK rising edge	$t_{HR}$		—	ns	3
WSP input setup time to WRCK falling edge	$t_{SF}$		—	ns	4
WSP input hold time from WRCK falling edge	$t_{HF}$		—	ns	4
WSO output valid time from WRCK falling edge	$t_{OVWSO}$	—		ns	5
<b>EXTEST_RX Instruction Related Timings</b>					
Input setup time to WRCK rising edge	$t_{SEXT}$		—	ns	6
Input hold time from WRCK rising edge	$t_{HEXT}$		—	ns	6
<b>EXTEST_TX Instruction Related Timing</b>					
Output valid time from WRCK falling edge	$t_{OVEXT}$	—		ns	7
<b>HBM_RESET Instruction Related Timing</b>					
HBM_RESET instruction minimum active time	$t_{RES}$	$t_{PW\_RESET}$	—	ns	8
<b>SOFT_REPAIR and HARD_REPAIR Instruction Related Timings</b>					
SOFT_REPAIR minimum waiting time	$t_{SREP}$		—	ns or $\mu$ s	9
HARD_REPAIR minimum waiting time	$t_{HREP}$		—	ns or $\mu$ s	10
<b>DWORD_MISR and AWORD_MISR Instruction Related Timing</b>					
DWORD and AWORD MISR data capture to WDR data capture delay	$t_{SMISR}$		—	ns	11
<b>CHANNEL_ID Instruction Related Timings</b>					
Output high time from WRCK falling edge	$t_{OVCHN}$	—		ns	12
Output return to default state delay	$t_{OZCHN}$	—		ns	13
<b>MODE_REGISTER_DUMP_SET Instruction Related Timings</b>					
WDR update to Mode Register valid delay	$t_{UPDMRS}$		—	ns	14
MRS command to WDR data capture delay	$t_{MRSS}$	$t_{MOD}$	—	nCK	15
<b>AWORD_MISR_CONFIG and MISR_MASK Instruction Related Timings</b>					
AWORD MISR config. or AWORD Mask config. to MISR operation delay	$t_{CMISR}$		—	ns	16
<b>SOFT_LANE_REPAIR and HARD_LANE_REPAIR Instruction Related Timings</b>					
SOFT_LANE_REPAIR minimum waiting time	$t_{SLREP}$		—	ns or $\mu$ s	17
HARD_LANE_REPAIR minimum waiting time	$t_{HLREP}$		—	ns or $\mu$ s	18

**Table 105 — IEEE1500 Port AC Timings 1,2 (cont'd)**

<b>PARAMETER</b>	<b>SYMBOL</b>	<b>VALUES</b>		<b>UNIT</b>	<b>NOTES</b>
		<b>MIN</b>	<b>MAX</b>		
NOTE 1					AC timing parameters apply to each channel of the HBM device independently except for timings related to IEEE1500 input pins that are common to all channels. No timing parameters are specified across channels, and all channels operate independently of each other.
NOTE 2					All parameters assume proper device initialization.
NOTE 3					Parameter applies to WSI, SelectWIR, ShiftWR and CaptureWR inputs.
NOTE 4					Parameter applies to UpdateWR input.
NOTE 5					Parameter applies to WSO output changes resulting from Wrapper Instruction Register (WIR), Wrapper Bypass Register (WBY) or any Wrapper Data Register (WDR) shift operation.
NOTE 6					Parameter applies to all HBM inputs and bidirectional IOs in the CaptureWR cycle when the active instruction is EXTEST_RX.
NOTE 7					Parameter applies to all HBM outputs and bidirectional IOs in the UpdateWR cycle when the active instruction is EXTEST_TX.
NOTE 8					Parameter applies when the active instruction is HBM_RESET; it is measured from either the falling WRCK edge that loads the HBM_RESET instruction in the UpdateWIR cycle (in case no WDR is associated with the instruction) or the falling WRCK edge that sets the WDR bit to '1' in the UpdateWR cycle (in case a WDR is associated with the instruction) until either the HBM_RESET instruction is invalidated or the WDR bit is set back to '0'. The minimum value equals the RESET_n minimum low time with stable power ( $t_{PW\_RESET}$ ).
NOTE 9					Parameter applies when the active instruction is SOFT_REPAIR; it describes the minimum time for the HBM device to perform the internal soft repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.
NOTE 10					Parameter applies when the active instruction is HARD_REPAIR; it describes the minimum time for the HBM device to perform the internal hard repair; it is measured from the falling WRCK edge that loads the repair vector and repair start bit in the UpdateWR cycle until the instruction is invalidated.
NOTE 11					Parameter applies when the active instruction is DWORD_MISR or AWORD_MISR; it is measured from the last CK clock that updates the data in the respective MISR until the rising WRCK edge associated with the CaptureWR cycle that copies the MISR data into the WDR shift register.
NOTE 12					Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets the CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '1' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs drive a High.
NOTE 13					Parameter applies when the active instruction is CHANNEL_ID; it describes the maximum duration from either the falling WRCK edge that sets any instruction other than CHANNEL_ID instruction in the UpdateWIR cycle (when no WDR is associated with the instruction) or the falling WRCK edge in the UpdateWR cycle that sets the enable bit in the WDR to '0' (when a WDR is associated with the instruction) until the outputs and bidirectional IOs return to their default state.
NOTE 14					Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the Mode Registers from the WDR shift register until any valid command other than RNOP and CNOP can be issued at the command interface.
NOTE 15					Parameter applies when the active instruction is MODE_REGISTER_DUMP_SET; it describes the minimum required delay between the last MRS command that loads any Mode Register and the rising WRCK edge in the CaptureWR cycle that copies the Mode Register content into the WDR shift register.
NOTE 16					Parameter applies when the active instruction is AWORD_MISR_CONFIG or MISR_MASK; it describes the minimum required delay between the falling WRCK edge in the UpdateWR cycle that loads the AWord MISR configuration or MISR mask data until the MISR configuration is valid for any subsequent AWORD or DWORD MISR operation in the CK clock domain.
NOTE 17					Parameter applies when the active instruction is SOFT_LANE_REPAIR; it describes the minimum time for the HBM device to perform the internal soft lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.
NOTE 18					Parameter applies when the active instruction is HARD_LANE_REPAIR; it describes the minimum time for the HBM device to perform the internal hard lane repair; it is measured from the falling WRCK edge that loads the repair vector in the UpdateWR cycle until the instruction is invalidated.

### 13.2.4 IEEE1500 Port AC Timing Parameters (cont'd)

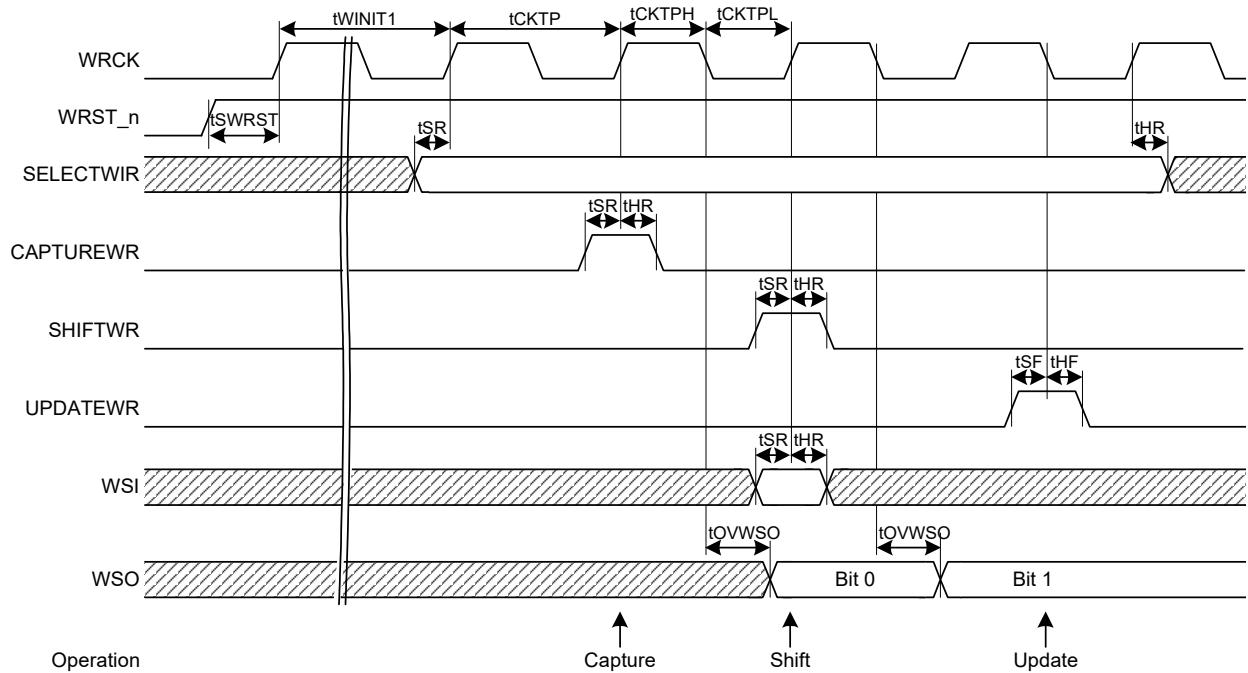


Figure 98 — IEEE1500 Port Input and Output Timings

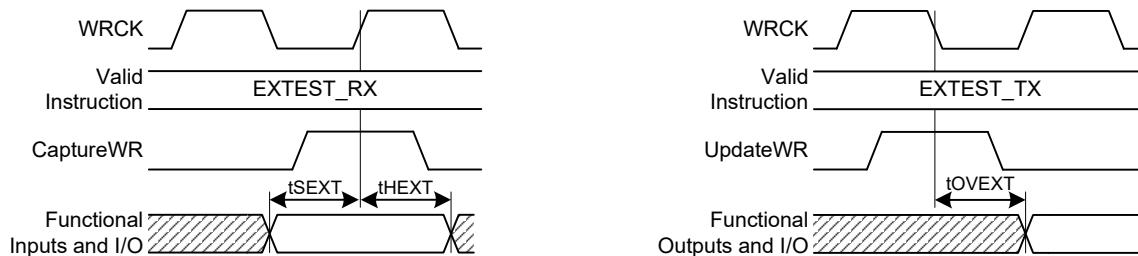


Figure 99 — IEEE1500 EXTEST\_RX and EXTEST\_TX Instruction Related Timings

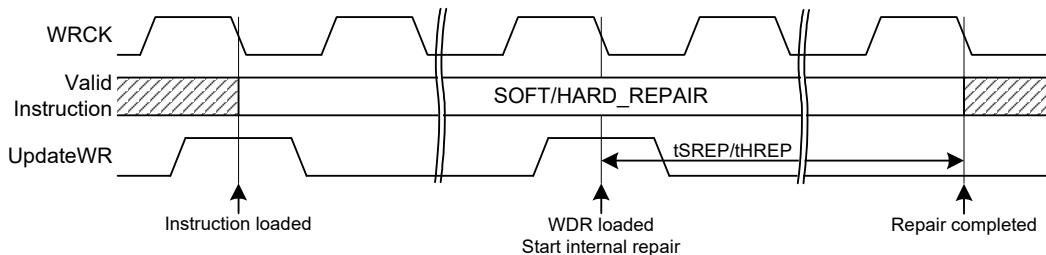
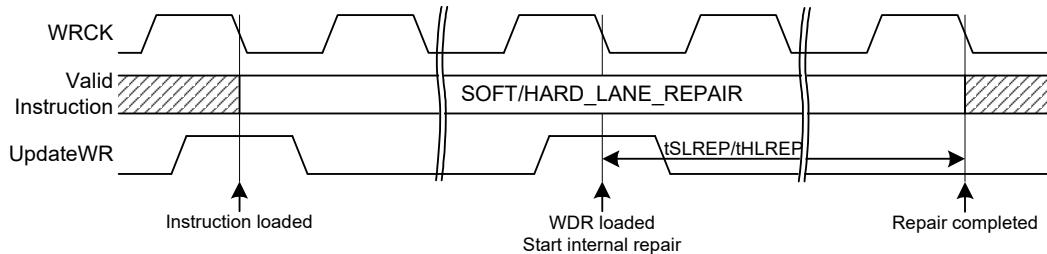
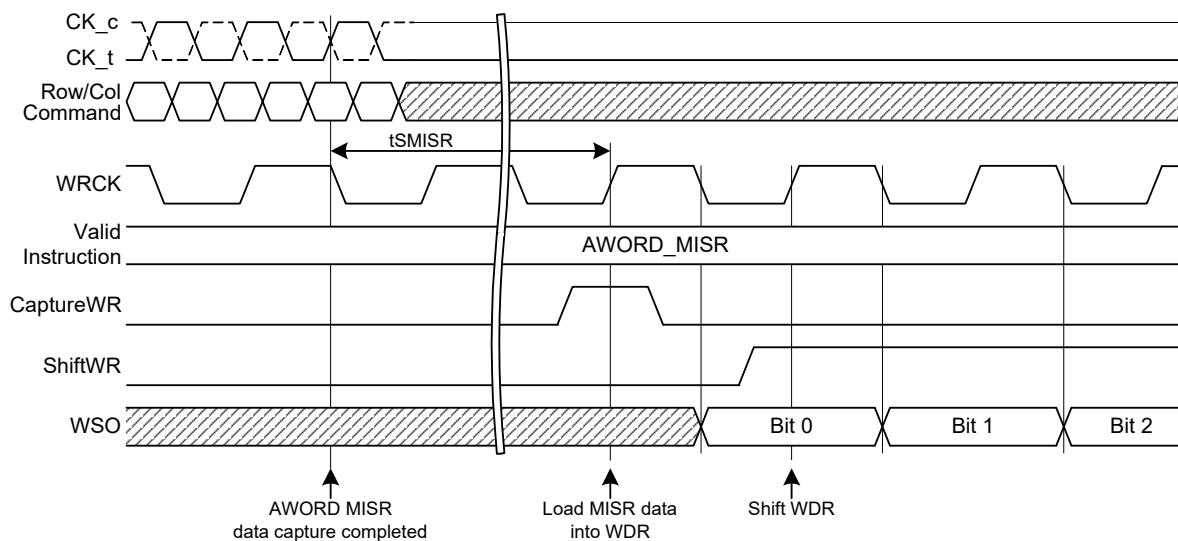


Figure 100 — IEEE1500 SOFT\_REPAIR and HARD\_REPAIR Instruction Related Timings

### 13.2.4 IEEE1500 Port AC Timing Parameters (cont'd)

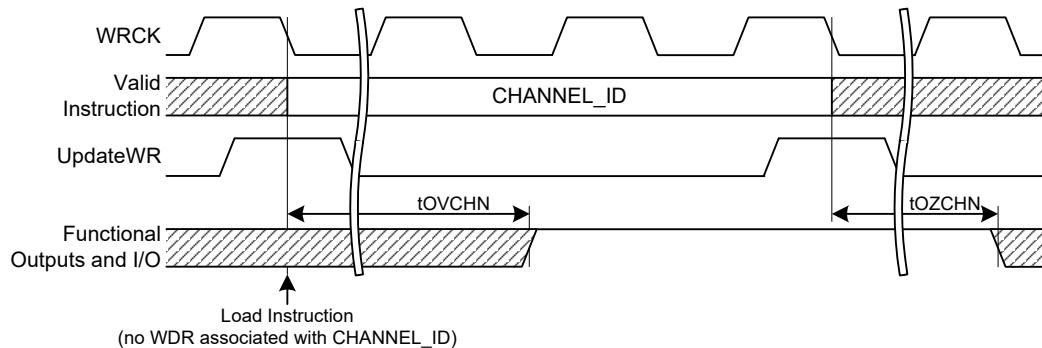


**Figure 101 — IEEE1500 SOFT\_LANE\_REPAIR and HARD\_LANE\_REPAIR Instruction Related Timings**



Note 1: Same timings for data inputs and DWORD MISR with DWORD\_MISR instruction.  
Note 2:  $t_{OVWSO} = 0$  for illustration purpose.

**Figure 102 — IEEE1500 DWORD\_MISR / AWORD\_MISR Instruction Related Timings**



Note:  $t_{OVCHN}$  and  $t_{OZCHN}$  refer to set/reset of Enable bit in WDR if optional WDR is implemented with CHANNEL\_ID instruction.

**Figure 103 — IEEE1500 CHANNEL\_ID Instruction Related Timings**

### 13.2.4 IEEE1500 Port AC Timing Parameters (cont'd)

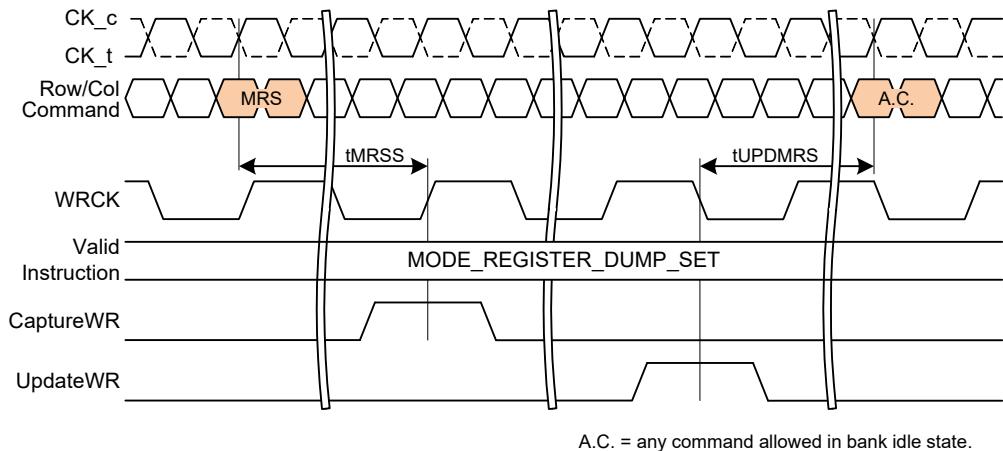


Figure 104 — IEEE1500 MODE\_REGISTER\_DUMP\_SET Instruction Related Timings

### 13.3 Boundary Scan

The HBM DRAM implements a boundary scan chain per channel via the IEEE 1500 port. The boundary scan operation is associated with IEEE1500 port instructions [EXTEST\\_RX](#) and [EXTEST\\_TX](#).

Scan data is shifted in through WSI and out through the respective WSO, based on the active channel selections in the WIR (see [Table 83](#)). All functional pins are included in the boundary scan chains. [Table 86](#) lists the micro-bump boundary scan chain order. Bit position 0 is the first bit shifted in on WSI and out on the WSOs.

Four pins in the mid-stack area are routed to the channel a and b scan chains: TEMP[2:0] are associated with channel a, and CATTRIP is associated with channel b. The boundary scan chain length for all channels is 215 or 217 bits, depending on device density (see [Table 86](#)), with dummy WDR bit padding as needed on the MSB end of the chains. Matched length boundary scan chains allows all channel chains to be loaded with matching data with one shift operation when WIR[11:8] = Fh.

Specific bits within the boundary scan chains are input-only, output-only or input/output (bidirectional), consistent with the micro-bump functional definitions. For example, the row and column command signals are functional inputs, and are defined as input-only (EXTEST\_RX only) in the boundary scan chains. The state captured on EXTEST\_RX for output pins is undefined.

While EXTEST\_RX is the current instruction, all functional pins of the selected channel(s) enter a Hi-Z state, including the output-only pins AERR, DERR, RDQS\_t/RDQS\_c, TEMP[2:0] and CATTRIP.

Optionally (vendor specific), the input-only and output-only pins may be implemented as bi-directionals to aid in SIP package level testing and fault isolation. If an HBM implementation supports bidirectional boundary scan, then all pins will support both EXTEST\_RX and EXTEST\_TX operations. During EXTEST\_RX, all pins will float and capture, including pins that are functional outputs (AERR, DERR, RDQS\_t/RDQS\_c, TEMP[2:0] and CATTRIP). Similarly, during EXTEST\_TX, all pins will output the boundary scan chain states, including the input-only pins (the AWORD signals and WDQS\_t/WDQS\_c).

Note that a host design should consider possible contention if the HBM device should support driving of signals that are normally inputs during EXTEST\_TX.

Scan mode entry may be asserted at any time after device initialization and during normal memory operation including when the HBM memory device is in power-down or self refresh mode. All I/O buffers are enabled when either EXTEST\_RX or EXTEST\_TX is the current instruction. Upon exiting the scan mode, the states of the HBM memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required before returning to normal operation.

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## Annex A (informative) Differences between JESD235D and JESD235C

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This table briefly describes the changes made to this standard, JESD235D, compared to its predecessor, JESD235C.

### Annex A (informative) Differences between JESD235D and JESD235C

Page	Description of Change
107-108	10, AC Timings, Part 1 (Table 67): speed bin 3.6 Gb/s added; $t_{IS2}$ , $t_{IH2}$ , $t_{DS2}$ and $t_{DH2}$ values changed for 3.2 Gb/s speed bin

## Annex A.1 (informative) Differences between JESD235C and JESD235B

This table briefly describes most of the changes made to this standard, JESD235C, compared to its predecessor, JESD235B. Minor editorial changes, parameter value changes and format updates of figures and tables are not included.

### Annex A1 (informative) Differences between JESD235C and JESD235B

Page	Description of Change
--	Table of Contents added
47, 49-51, 54-56, 71-72	Bit index for buses in Figures 36, 40 - 43, 46 - 51, 76 and 77 changed to bus notation
8	3.2.1, Bank Groups: 12-H configuration with 48 banks added in Table 5; $t_{CCDR}$ parameter added in Table 6
9	3.3, Simplified State Diagram: new section
30-31	6.3.1, Command Truth Tables (Tables 30 and 31): editorial updates: bits could be V, SID, SID0, SID1, depending on density; footnotes adapted accordingly
42	6.3.2.6, REFSB Command: 12-H configuration with 48 banks added to text
45	6.3.3.2, Read Command: added clarification for driver enabled state and link to DBIac States section for bus pre-conditioning
46	6.3.3.2.2, Read Data Strobe and Data Out Timings: added note 4 in Figure 35
47-51	6.3.3.2.3, Read Operation: added notes to Figures 36 to 43 about RDBI states and related mode register bits
53	6.3.3.3.2, Write Data Strobe and Data In Timings: added note 4 in Figure 45
54-58	6.3.3.3.3, Write Operation: added notes to Figures 46 to 53 about WDBI states and related mode register bits; added clarification to text related to Fig. 52 that the bus is not preconditioned when RDBI is disabled.
69-72	6.4.2, Data Parity: added notes to Figures 72 to 77 about RDBI and WDBI states and related mode register bits
97	8.2, Capacitance (Table 52): reference to “TBD” measurement method in note 1 deleted
107-108	10, AC Timings, Part 1 (Table 67): speed bins 2.8 and 3.2 Gb/s added; “TBD” for $t_{DQSCK}$ and 1.0 Gb/s speed bin deleted
109-111	10, AC Timings, Part 2 (Table 68): reference to footnotes corrected for parameters $t_{RTPS}$ , $t_{CCDR}$ and $t_{REFI}$ ; clarification “/ channel” added for parameter $t_{REFISB}$
116	11.3, HBM Stack Height: “TBD” for 12-High configurations deleted (value is vendor specific)
198	13.3.3, Boundary Scan: scan chain length corrected

**Annex A.2 (informative) Differences between JESD235B and JESD235A**

This table briefly describes most of the changes made to this standard, JESD235B, compared to its predecessor, JESD235A. Minor editorial changes, parameter value changes and format updates of figures and tables are not included.

**Annex A.2 (informative) Differences between JESD235B and JESD235A**

Page	Description of Change
--	Added abbreviations “HBM1” and “HBM2” to cover page
--	Revised text and tables for consistent use of bus notation (e.g., DQ[127:0], OP[3:0] and scalar notation (e.g., DA28, OP7)
1	Corrected density range, bank count and page size in Features list
3	Added optional input pins R6 and C8 to Table 1 (Single Channel Signal Count)
4 - 5	Added abbreviations “HBM1” and “HBM2” to descriptions of Legacy Mode and Pseudo Channel Mode, respectively; text edited for consistency regarding “prefetch per memory read / write access”; Fig. 2 and text updated for abbreviations “PC0” and “PC1”
4ff	Graphically updated Figures 2-5, 17, 30, 35-42, 45-52, 56, 67-76 and 80 to consistently show command and address inputs non-shaded during idle (NOP) cycles
11 - 13, 31,35,38, 40,43 - 44,51,58 - 59,64	Added optional input pins R6 and C8 to Figures 3-5, 15-16, 24-25, 29, 32-33, 43, 53, 55 and 66
6 - 7	Added larger densities to Table 4 (HBM Channel Addressing); table re-formatted and notes adapted
9	Updated Table 6 (Command Sequences affected by Bank Groups): deleted parameter $t_{RTPS}$ from middle column
10 - 12	Updated the HBM Power-up and Initialization Sequence and Initialization with Stable Power sections regarding CATTRIP pin (text, Table 7, Figures 3 and 4); added sentence on the use of HBM_RESET instruction as an alternate way for re-initialization
15	Typos corrected in Mode Registers section; Table 8 (Mode Register Overview) header edited and ERL, EWL bits added
17	Removed support for RL=2 and added higher RL and WL values in Table 11 (MR2)
18	Added ERL and EWL bits and merged DM and ECC fields in Table 15 (MR4)
22	Added definitions for rising and falling clock and data strobe edges in clocking section. Related edits throughout the document
24 - 25	Reworded text in data mask, DBI and ECC section for improved readability; added truth tables for write data mask (Table 28) and DM pin function (Table 29)
30 - 31	Updated Tables 30 and 31 (Row and Column Command Truth Tables) including footnotes: removed RA15 and CA6; added SID1; moved RA14 to R6 pin
33	Updated Figure 17 (Bank and Row Activation Command Cycle) regarding $t_{XP}$ and $t_{XS}$ timings
34	Updated note 2 in Figure 18 (Multiple Bank Activations)
34	Deleted redundant paragraphs in ACTIVATE w/ imPRE section
38	Updated Table 37 (Precharge and Auto Precharge Timings)
61	Updated Figure 56 (Power-Down Entry and Exit) to show $t_{CPDED} = 2 \text{ nCK}$
66	Updated Figure 67 (Self Refresh Entry and Exit) to show $t_{CPDED} = 2 \text{ nCK}$
--	Deleted “Data Integrity” section
67 - 69	Updated Figures 68 to 70 (note 2) and related text regarding parity function disable; updated Table 36 (Parity Function Table) and related text regarding optional R6 and C8 pin
68 - 73	Updated Figures 71 and 72 (note 6), Figures 77 to 79 (note 2) and related text regarding parity function disable
77	Changed refresh rate in Table 38 (Temperature Compensated Refresh Trip Points) from “TBD” to “vendor specific”

**Annex A.2 (informative) Differences between JESD235B and JESD235A (cont'd)**

<b>Page</b>	<b>Description of Change</b>
77	Added reference to initialization sequence added in Catastrophic Temperature Sensor section
78 - 79	Updated Tables 39 to 42 in AWORD Remapping section for optional R6 and C8 input pins
84	Updated Figure 82 (HBM Loopback Test Modes) and text for optional R6 and C8 input pins
85	Added 34-bit MISR polynomial in AWORD MISR Polynomial section
90	Added clarification n) in General Loopback Modes Features and Behavior section
92	Added clarification added regarding the use of PL in Test Method for DWORD Write Register Mode
97	Updated Table 51 (Input Leakage Current) for optional R6 and C8 input pins
97	Added $V_{IHR}$ and $V_{ILR}$ parameters and edited related footnotes in Table 53 (Input Receiver Voltage Level Specification)
99	Updated Table 56 (Overshoot/Undershoot Specification) for optional R6 and C8 input pins
100ff	Changed term IDDP to IPP; deleted address bits RA15 and CA6 from IDD Measurement Loop Pattern
102 - 105	Updated Table 58 (Timings used for IDD Measurement-Loop Pattern) for 8 Gb and 16 Gb densities; updated Tables 59 to 64 (IDDO, $I_{DD4R}$ and $I_{DD4W}$ measurement-loop pattern): - changed bank sequence from “0 - 5 - 2 - 7 - 4 - 1 - 6 - 3” to “0 - 5 - 2 - 7 - 1 - 6 - 3 - 4”; - adapted row address and column address pattern to match the address range defined in the addressing section
107 - 108	Updated AC Timings Part 1 (Table 67): - added 2.4 Gbps/pin speed bin - changed $t_{IS}$ , $t_{IH}$ , $t_{DS}$ , $t_{DH}$ , $t_{DQSS}$ and $t_{DQSQ}$ values - added parameters $t_{IS2}$ , $t_{IH2}$ , $t_{DS2}$ and $t_{DH2}$ and related Table 69
109 - 112	Updated AC Timings Part 2 (Table 68): - changed $t_{CCDL}$ , $t_{RFC}$ and $t_{RFCSB}$ values - edited $t_{RRDL}$ , $t_{RRDS}$ and $t_{RREFD}$ parameter description for consistency with REFSB command description - updated note 23 for $t_{RTW}$ parameter - updated $t_{REFI}$ and $t_{REFISB}$ parameters and related footnotes for additional device configurations
113	Updated Table 70 (I/O Signal Description) for optional R6 and C8 input pins
115	Added a second micro bump matrix (“Footprint 2”) in MicroBump Positions section;
116	Added entry for 12-High in Table 72 (Stack Height)
116 - 158	Renamed original bump matrix to “Footprint A” and added new “Footprint 2” matrix in HBM Ballout section
166	Corrected MISR_MASK reset state from “cleared to all 0s” to “cleared to all 1s” in WDR Reset State section
169	Added optional R6 and C8 input pins to Table 86 (EXTEST_RX and EXTEST_TX WDR)
171 - 172	Changed bit positions in Table 87 (INTEST_RX WDR) and Table 88 (INTEST_RX WDR) from “TBD” to “vendor specific”
173	Added clarifications including new Figure 95 regarding the relationship between RESET_n pin and HBM_RESET instruction in HBM_RESET section
174 - 175	Changed bit positions in Table 92 (SOFT_REPAIR WDR) and Table 93 (HARD_REPAIR WDR) from “TBD” to “vendor specific”
177-178	Updated Table 95 (AWORD_MISR WDR) and text to cover both 30-bit and 34-bit MISR polynomials
181	Updated Table 97 (MISR_MASK WDR) to cover both 30-bit and 34-bit MISR polynomials for optional R6 and C8 input pins
182	Added the optional POLYNOMIAL_SELECT bit to Table 98 (AWORD_MISR_CONFIG WDR)
183	Updated the DENSITY field in Table 99 (DEVICE_ID WDR) to cover all HBM device configurations
187 - 188	Updated Table 102 (READ_LFSR_COMPARE_STICKY WDR) for optional R6 and C8 input pins
190	Updated Table 103 (LANE_REPAIR WDR) for R6 and C8 input pins
193 - 195	Added $t_{WINIT1}$ parameter to Table 105 and Figure 97 in the IEEE1500 Port AC Timing Parameters section

**Annex A.3 (informative) Differences between JESD235A and JESD235**

This table briefly describes most of the changes made to this standard, JESD235A, compared to its predecessor, JESD235. Minor editorial changes, parameter value changes and format updates of figures and tables are not included.

**Annex A.3 (informative) Differences between JESD235A and JESD235**

Page	Description of Change
1	Added Pseudo Channel Mode concept for feature list
3	Added redundant data, row and column pins, and global signals RESET_n, TEMP[2:0] and CATTRIP to signal count tables
4	Added chapter on Legacy Mode and Pseudo Channel Mode
5	Updated Addressing table to reflect Legacy Mode and Pseudo Channel Mode; also added 8 Gb per channel configurations
6	Added 8 Gb, 8-High configuration with 32 banks to Bank Groups table; added table with timing parameters associated with BG
7 - 10	Updated power-up initialization and initialization with stable power sequences and related timings; added chapter on initialization sequence for use of limited IEEE 1500 instruction including lane repairs
11 - 16	Added bits for TRR mode, Implicit Precharge, CATTRIP, LFSR Compare mode and DA28 lockout to Mode Registers
20 - 21	Changed DBIac scheme for Reads to include the DBI pin; updated all timing diagrams associated with DBI operation
25 - 26	Added Stack ID (SID) bit to command truth tables
29 - 31	Added bank activation with implicit precharge (ImPRE) function
35 - 37	Updated conditions for REFSB command; added table on REF and REFSB command scheduling requirements
54 - 55	Added clarification on signal states and parity calculation to Power-Down section
58 - 59	Added clarification on signal states and parity calculation to Self Refresh section
69	Removed ECC bits from data parity calculation
70 - 71	Added Target Row Refresh (TRR) mode section
71 - 72	Added Temperature Compensated Refresh reporting section
73 - 78	Added Interconnect Redundancy Remapping section
79 - 90	Added section on HBM loopback test modes
94	Added Overshoot/Undershoot values
98 - 100	Added IDD measurement loop pattern for pseudo-channel mode
102 - 107	Added example speed bins to AC timing parameters; updated several timing parameters; added t <sub>RREFD</sub> , t <sub>CCDR</sub> , t <sub>RF-CSB</sub> , t <sub>IMPREPDE</sub> , t <sub>MAW</sub> parameters
108 - 109	Added redundant data, row and column pins and CATTRIP to I/O signal description
109 - 130	Added clarification regarding center aligned micro bump matrix; added 8 columns of mechanical bumps to the left of the bump matrix, thus changing the total number of columns from 60 to 68
133	Added clarifications and DA28 lockout function to test ports section
135-136	Updated the WIR channel select logic diagram and associated description
137	Added READ_LFSR_COMPARE_STICKY, SOFT_LANE_REPAIR and HARD_LANE_REPAIR instructions to WIR instruction table; added fixed WDR length to several instructions
138 - 154	Updated description of WDR reset state; split global WDR table into a single WDR table per IEEE1500 instruction; updated table content for several IEEE1500 instructions
154 - 158	Added READ_LFSR_COMPARE_STICKY, SOFT_LANE_REPAIR and HARD_LANE_REPAIR instruction sections

**Annex A.3 (informative) Differences between JESD235A and JESD235 (cont'd)**

Page	Description of Change
159	Added section on interaction with mission mode operation
160 - 164	Updated IEEE1500 Port AC Timings table and related timing diagrams
165	Added Boundary Scan section



## Standard Improvement Form

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The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

Requirement, clause number \_\_\_\_\_

Test method number      Clause number

The referenced clause number has proven to be:

Unclear    Too Rigid    In Error

Other \_\_\_\_\_

- ## 2. Recommendations for correction:

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- ### 3. Other suggestions for document improvement:

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