Safety-Related Known Issues for the TetraMAX II ADV Automotive ATPG N-2017.09 Release

This document lists the safety-related issues for TetraMAX II ADV Automotive ATPG for Safety N-2017.09.
Note that a number of these issues are found during our product testing and hence are internally reported.

ID	Summary	CHANGE
9001013841	**Title**: TetraMAX incorrectly classifies lockup latch enable as DI **How to Identify**: stuck-at classification for lockup latch enable is DI **How to Avoid**: currently how the tool classifies the enable pin of lockup-latch. After the latches are identified – write the fault list and search for the latches. This is a coverage issue than a safety issue.	
9000985650	**Title**: AN fault sites connected to UO/UU and UB fault sites should come under UD **How to Identify**: If you have UB (undetectable blocked) faults, then trace backwards for the presence of UU (undetectable unused) faults. **How to Avoid**: is not to use the option, set_build -nodelete	
9000841570	**Title**: Wrong DI status for latches not on scan chain This is unsafe because the DI status means that any scan operation will detect the fault, but that is untrue so it should be added to the faults list as NC. Then the DI status prevents ATPG from targeting the fault. **How to Identify**: transparent latch with clock_on gives higher optimistic coverage. Need to identify the latch – we need to write and supply a perl script to do this search. **How to avoid**: After the latches are identified – write the fault list and search for the latches.	
9000723596	**Title**: Program error: No faults found for equivalence [& no atpg patterns] **How to Identify**: If there is a program error like: Program error: No faults found for equivalence class search of flt=1331707/0/2 **How to Avoid**: Send testcase to Synopsys	
9000657628	**Title**: test coverage of scandata pipelines **How to Identify**: faults are created on every pin of the 2 stages of head/tail pipelines: 1332 faults. ATPG is unable to generate any patterns for the scandata pipelines. This only affects test related logic and not functional logic. **How to Avoid**: Cannot avoid; reported coverage will be slightly lower and not much coverage impact for very large designs.	
9001175430	**Title:** Sync OCC with LOES: fault sim doesn't credit DS faults from ATPG **How to Identify:** In the sync OCC flow with LOES, when read back external patterns; the readback will falsely classify the fault as NO (versus DS). On readback the timing sequence is not restored correctly; yielding pessimistic results **How to Avoid:** In the sync OCC flow with LOES, do not read back external patterns	

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9001143145	**Title:** False AU faults when -nomulti_fanout_di_faults is used **How to Identify:** The flip-flop Q output loops around through logic back to the same flip-flop's D input, and also into the next scan flip-flop in the scan chain. With set_faults -nomulti_fanout_di_faults, both sa0 and sa1 on the Q pin declared AN. **How to Avoid:** modify circuitry, or use 'run_fault_sim -sequential' for credit or use TetraMAX II instead of TetraMAX See SolvNet - Sequential Loop Causes Register Q Pin to be Classified as an AN Fault class TetraMAX **2574517** 2574517.html	
9001128383	**Title:** UR fault classification changes related to chain test usage **How to Identify:** If you have chain tests and see large UR count then turn off chain tests and compare the UR count is different by 2X or more. **How to Avoid:** use TetraMAX II instead of TetraMAX; or can turn chain tests off	
9000973465	**Title:** Option to generate at least 10 patterns for a potentially detected fault **How to Identify:** The Automotive Electronics Council AEC - Q100-007 Rev-B says in section 5.2 "Potentially Detected Faults" detected at least 10 times can be considered a detected fault. The request is for an option or switch for the set_atpg command to generate at least 10 patterns for all potentially detected (PT) faults that are found during the ATPG. A more user intensive flow is to write out the PT faults after the ATPG and then using the n-detect feature on these faults in a subsequent run – not user desirable. **How to Avoid:** This is an enhancement feature request; nothing to avoid.	
9000644260	**Title:** sequential fault grading classifies flop clock pin as NP **How to Identify:** non-scan functional faultsim. NP is not a fault class for nonscan full sequential **How to Avoid:** Use the ZOIX functional fault grading tool	
9000624347	**Title:** Faults declared AX for hold-only exceptions **How to Identify:** The analysis for AX faults currently considers only those effects produced by setup exceptions. But when a hold exception is read, the AX analysis is done on it as if it were a setup exception. **How to Avoid:** You can avoid having the bug affect the reported test coverage by keeping ax_credit at 0. But then the wrong AX analysis will prevent ATPG from targeting the falsely-identified faults.	