Synthesis

O-2018.06 Implementation and Signoff Documentation

SYNOPSYS

Power Compiler™

- Power Compiler User Guide, version O-2018.06

Design Compiler®

- Design Compiler User Guide, version O-2018.06

DC Explorer

- DC Explorer User Guide, version O-2018.06

Design Vision™

- Design Vision User Guide, version M-2016.12

HDL Compiler™

- HDL Compiler for VHDL User Guide, version O-2018.06
- HDL Compiler for Verilog User Guide, version O-2018.06
- HDL Compiler for SystemVerilog User Guide, version O-2018.06

Other

- Synopsys Multivoltage Flow User Guide, version O-2018.06
- Using the Synopsys Design Constraints Format Application Note, version 2.1
- Synopsys Timing Constraints and Optimization User Guide, version O-2018.06
- Using Tcl With Synopsys Tools, version O-2018.06
- Design Compiler Automated Test Case Packaging Application Note, version G-2012.06
- Milkyway Database Application Note,version J-2014.09
- Multibit Register Synthesis and Physical Implementation Application Note, version O-2018.06

ISO 26262 Documents

- Design Compiler Functional Safety Manual

Synthesis Man Pages, version O-2018.06

- Tool Invocation Commands
- Tool Commands
- Variables and Attributes
- Error Messages

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