NanoTime
Error Messages

Version O-2018.06, June 2018

SYNOPSYS®

Copyright Notice and Proprietary Information

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the reader's responsibility to determine the applicable regulations and to comply with them.

Disclaimer

SYNOPSYS, INC., AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Trademarks

Synopsys and certain Synopsys product names are trademarks of Synopsys, as set forth at http://www.synopsys.com/Company/Pages/Trademarks.aspx.
All other product or company names may be trademarks of their respective owners.

Free and Open-Source Licensing Notices

If applicable, Free and Open-Source Software (FOSS) licensing notices are available in the product installation.

Third-Party Links

Any links to third-party websites included in this document are for your convenience only. Synopsys does not endorse and is not responsible for such websites and their practices, including privacy practices, availability, and content.

Synopsys, Inc.
690 E. Middlefield Road
Mountain View, CA 94043
www.synopsys.com

Copyright Notice for the Command-Line Editing Feature

Copyright Notice for the Line-Editing Library

Contents

CHPP Error Messages

CHPP-001

CHPP-001 (Error) Internal error, unable to execute command %s.

DESCRIPTION

The command failed due to an internal error while performing actions related to the command.

WHAT NEXT

Report the error to Synopsys.

CHPP-002

CHPP-002 (Error) Cannot execute %s command in a %s.

DESCRIPTION

The command failed due to incorrect usage. **run_parallel** command cannot be run in a worker instance.

WHAT NEXT

Update the script file and re-run.

CHPP-003

CHPP-003 (Error) Cannot access the script file from %s command line.

DESCRIPTION

Unable to access the script file that is expected on the tool command line.

WHAT NEXT

Ensure that a script file with adequate permissions is provided on the tool command line.

CHPP-004

CHPP-004 (Error) Instance name %s contains one or more illegal characters defined in the string '%s'.

DESCRIPTION

Some characters are not allowed in an instance name.

WHAT NEXT

Remove illegal characters from the instance name.

CHPP-005

CHPP-005 (Error) Duplicate %s %s found in argument list.

DESCRIPTION

Duplicate entries are not allowed in the argument list.

WHAT NEXT

Remove duplicate entries from the argument list.

CHPP-006

CHPP-006 (Error) Cannot access the specified %s %s.

DESCRIPTION

Unable to access the script file specified in the command.

WHAT NEXT

Ensure that the script file exists and has adequate permissions.

CHPP-007

CHPP-007 (Error) A host definition file is needed to use the -exclude_master option.

DESCRIPTION

A host definition file is needed to identify compute resources other than the localhost.

WHAT NEXT

Specify a host definition file using the variable **distributed_processing_host_file** that describes the list of host machines for distributed processing.

CHPP-008

CHPP-008 (Error) Multiple use of script file %s detected.

DESCRIPTION

A script file can be used only once within a hierarchy of parallel instances.

WHAT NEXT

Check the arguments of **-files** option of **run_parallel** commands in the hierarchy.

CHPP-009

CHPP-009 (Error) Multiple use of script file %s and instance name %s detected.

DESCRIPTION

The combination of script file and instance name can be used only once within a hierarchy of parallel instances.

WHAT NEXT

Check the arguments of **-files** and **-instance_names** options of **run_parallel** commands in the hierarchy.

CHPP-010

CHPP-010 (Error) Illegal use of -directories option without using -files option.

DESCRIPTION

The **-directories** option can be used only if **-files** option is used.

WHAT NEXT

Check the arguments of **run_parallel** command.

CHPP-011

CHPP-011 (Error) Unequal number of directories and files.

DESCRIPTION

The number of directories specified must be equal to the number of files specified.

WHAT NEXT

Check the arguments of **run_parallel** command.

CHPP-012

CHPP-012 (Error) Cannot access the specified %s %s.

DESCRIPTION

Unable to access a run directory specified in the **run_parallel** command.

WHAT NEXT

Ensure that all run directories exist and have adequate permissions.

CHPP-013

CHPP-013 (Warning) Host definition file not specified.

DESCRIPTION

A host definition file is needed to identify compute resources.

WHAT NEXT

Specify a host definition file using the variable **distributed_processing_host_file** that describes the list of host machines for distributed processing.

CHPP-014

CHPP-014 (Error) Host definition file %s is not readable.

DESCRIPTION

An accessible host definition file is needed to identify compute resources.

WHAT NEXT

Specify a host definition file with proper permissions using the variable **distributed_processing_host_file** that describes the list of host machines for distributed processing.

CHPP-015

CHPP-015 (Error) Unable to reacquire the licenses held prior to run_parallel.

DESCRIPTION

The tool needs to reacquire all the licenses it had checked-out prior to executing **run_parallel** command to continue.

WHAT NEXT

Ensure that the license manager is accessible and there are enough licenses.

CHPP-016

CHPP-016 (Warning) Setting max instance count to %d based on number of processor cores on localhost %s.

DESCRIPTION

The number of tool instances is limited by the number of processor cores on the localhost.

WHAT NEXT

Ensure that there are adequate number of processors for the job.

CHPP-017

CHPP-017 (Information) %s

DESCRIPTION

This is only an informational trace message.

WHAT NEXT

Use the message to investigate any unexpected results.

CHPP-018

CHPP-018 (Error) %s

DESCRIPTION

An unexpected error has occurred.

WHAT NEXT

Use the message to investigate potential causes of the error.

CHPP-019

CHPP-019 (Error) Environment variable %s is not defined.

DESCRIPTION

A required environment variable could not be found.

WHAT NEXT

Consult user documentation on how to set the specified environment variable.

CHPP-020

CHPP-020 (Error) Executable for %s was not found.

DESCRIPTION

A required executable could not be found.

WHAT NEXT

Consult user documentation on how to set the PATH environment variable.

CMD Error Messages

CMD-001

CMD-001 (error) Cannot specify '%s' with '%s'.

DESCRIPTION

The listed command options are exclusive. Only one of them can be specified.

WHAT NEXT

Look at the manpage for this command for more information on command options.

CMD-002

CMD-002 (error) Value for '%s' cannot be negative

DESCRIPTION

The value for this option must be greater than or equal to zero.

WHAT NEXT

Enter the command again with a valid option value.

CMD-003

CMD-003 (error) Cannot specify %s without %s.

DESCRIPTION

One command option requires another.

WHAT NEXT

Refer to the manual page for this command for detailed information on valid options.

CMD-004

CMD-004 (error) Must specify one of these options: %s.

DESCRIPTION

This command requires that one of the options in the list is specified.

WHAT NEXT

Refer to the manual page for this command for detailed information on valid options.

CMD-005

CMD-005 (error) unknown command '%s'

DESCRIPTION

The command is not recognized.

WHAT NEXT

Look for a typographical error in the command. If it is correct, make sure that the program you are running supports the command, or you have the license to use the command.

CMD-006

CMD-006 (error) ambiguous command '%s' matched %d commands: (%s)

DESCRIPTION

The command does not have sufficient characters to distinguish it from other commands. The first three commands which match the abbreviation are listed. To see them all, use the help as follows: if the abbreviation is cmd, type 'help cmd*'. This lists all commands that begin with 'cmd'.

WHAT NEXT

Type enough characters so the command is unambiguous.

CMD-007

CMD-007 (error) Required argument '%s' was not found

DESCRIPTION

The listed argument to the command might not be omitted.

WHAT NEXT

Supply the required argument.

CMD-008

CMD-008 (error) value not specified for option '%s'

DESCRIPTION

The listed argument requires a value (that is, it is not a boolean option), and none were supplied.

WHAT NEXT

Supply a value for the argument.

CMD-009

CMD-009 (error) value '%s' for option '%s' not of type '%s'

DESCRIPTION

The value given for the listed argument is not the correct type. For example, if 'abc' is given for an integer option, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-010

CMD-010 (error) unknown option '%s'

DESCRIPTION

The option is not recognized.

WHAT NEXT

If this is not a simple mistake, retype the command with by the -help option. This lists all of the possible options.

CMD-011

CMD-011 (error) ambiguous option '%s'

DESCRIPTION

The option does not have sufficient characters to distinguish it from other options.

WHAT NEXT

Type enough characters so that the option is unambiguous.

CMD-012

CMD-012 (error) extra positional option '%s'

DESCRIPTION

The command expects some positional arguments and has already received enough. It might also be the case that this was intended as a dash option and is misspelled.

WHAT NEXT

Verify that the option given is not a misspelled dash option. If a list is provided directly instead of as a

variable, ensure it is enclosed by curly braces or double quotation marks. Use -help with the command to verify which arguments are already given.

CMD-013

CMD-013 (error) %s Use error_info for more info.

DESCRIPTION

A script or complex command failed and there is a stack trace for the failure. The trace points out the source files and loops where the error occurred. The error_info command is used to display this stack.

WHAT NEXT

Fix the error indicated by error_info.

CMD-014

CMD-014 (error) Invalid %s value '%s' in list.

DESCRIPTION

A list argument is expected to be a common type (like integer or float) and one or more elements cannot be converted to that format.

WHAT NEXT

Fix the offending list element.

CMD-015

CMD-015 (error) could not open %s file \"%s\"

DESCRIPTION

A script or an output redirect file cannot be opened.

WHAT NEXT

Verify that the file exists or that you have write access to the directory. Write access depends on the file type.

CMD-016

CMD-016 (error) could not close %s file \"%s\"

DESCRIPTION

A script or an output redirect file cannot be closed.

WHAT NEXT

CMD-017

CMD-017 (warning) duplicate option '%s' ignored.

DESCRIPTION

The given option is already issued. This command uses the first value of the option, and subsequent values are ignored.

WHAT NEXT

Make sure this is the option you want to use. If so, decide which value you want and verify that you get the correct one.

CMD-018

CMD-018 (warning) duplicate option '%s' overrides previous value.

DESCRIPTION

The given option has already been issued. This command uses the last value of the option, and previous values are ignored.

WHAT NEXT

Make sure that this is the option you want to use. If so, decide which value you want and make sure that

you get the correct one.

CMD-019

CMD-019 (error) value '%s' for option '%s' not in range (%s).

DESCRIPTION

The value given for the listed argument is not in the allowable range. For example, if 4 is given for an integer option, which has a range of 1 to 3, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-020

CMD-020 (error) unknown OR extra positional option '%s'

DESCRIPTION

The dash option is not recognized. Further, all positional arguments have already been received. This is most likely a misspelled dash option.

WHAT NEXT

Check to see if the option is misspelled. Look at the entire command, as other options may have misled the interpreter.

CMD-021

CMD-021 (warning) invoked %s outside of a loop

DESCRIPTION

The listed control command (break or continue) was used outside of the context of control structure (such as foreach, while, and so on).

WHAT NEXT

Look for a loop that ends prematurely or for a misspelled control word.

CMD-022

CMD-022 (warning) Can't create alias named '%s' - %s%s.

DESCRIPTION

An attempt was create an alias with an invalid name. Invalid names include those which match an existing command or procedure, and those which can be converted to a decimal, hexadecimal, or octal number.

WHAT NEXT

Choose another name. Use 'help' and 'alias' (with no arguments) to see what names are in use.

CMD-023

CMD-023 (error) Alias loop: %s

DESCRIPTION

You have aliases that refer to one another.

WHAT NEXT

Use the alias command to look at the aliases listed in the diagnostic. Remove the loop and re-execute the command.

CMD-024

CMD-024 (error) can't %s "%s": %s

DESCRIPTION

You attempted an operation on a variable which failed. You may have tried to read a non-existent variable (set var). Or, you may have tried to unset a non-existent or application-owned variable. The text of the message will indicate which operation failed.

WHAT NEXT

Verify that the variable exists with the printvar command. If it's not a user variable, you cannot remove (unset) it.

CMD-025

CMD-025 (error) No manual entry for '%s'

DESCRIPTION

The topic for which you requested man pages does not exist.

WHAT NEXT

Verify that the topic is spelled correctly.

CMD-026

CMD-026 (error) %s required for the '%s' argument.

DESCRIPTION

The command is incomplete as entered. The specified argument requires a valid object or list of objects.

WHAT NEXT

Enter the command with valid values for all arguments.

CMD-027

CMD-027 (error) couldn't change working directory to '%s'

DESCRIPTION

The directory which you specified to the cd command is not valid.

WHAT NEXT

Verify that the directory is spelled correctly.

CMD-028

CMD-028 (error) couldn't get working directory name

DESCRIPTION

The pwd command was unable to access the current directory. It is most likely the case that the directory which you are in no longer exists,

WHAT NEXT

Use the cd command to get into an existing directory.

CMD-029

CMD-029 (warning) no aliases matched '%s'

DESCRIPTION

You specified a pattern to the unalias command, and there are no aliases which match that pattern.

WHAT NEXT

There is no adverse effect of this action. However, check the spelling of the arguments to unalias to ensure that you removed all of the aliases which you wanted to remove.

CMD-030

CMD-030 (warning) File '%s' was not found in search path.

DESCRIPTION

The 'which' command evaluated an filename argument and the file was not found.

WHAT NEXT

No adverse effect on the result of the command, but check spelling, etc.

CMD-031

CMD-031 (error) value '%s' for option '%s' is not valid. Specify one of: %s

DESCRIPTION

The value given for the listed argument is not one of the limited allowable strings. This messages lists all of the appropriate values.

WHAT NEXT

Supply a compatible value for the argument.

CMD-032

CMD-032 (warning) command '%s' requires some options.

DESCRIPTION

No options were given for the command, yet some are required.

WHAT NEXT

Supply appropriate arguments.

CMD-033

CMD-033 (error) cannot source the current log file.

DESCRIPTION

An attempt to source the log file of the currently running interpreter is not allowed. It would cause the tool to infinitely loop.

WHAT NEXT

Copy the part of the log to be a source for another file, then source that file instead.

CMD-035

CMD-035 (error) Value for %s cannot be larger than the %s value.

DESCRIPTION

Some commands work in pairs, specifying a maximum and minimum value. The minimum value should be less than the maximum value. For example, never specify a **min_capacitance** which is larger than the **max_capacitance** for the same design or port.

WHAT NEXT

Remove the old value or use a different value.

CMD-036

CMD-036 (error) Value for list '%s' must have %s elements.

DESCRIPTION

The value given for the list argument does not have the correct number of elements. Some commands have list arguments which require either a specific number or an even number of elements. The message will indicate which it is.

WHAT NEXT

Supply a correct number of elements in the list. If the list is provided directly instead of as a variable, ensure it is enclosed by curly races or double quotation marks.

CMD-037

CMD-037 (error) value '%s' for option '%s' is invalid: must be %s.

DESCRIPTION

The value given for the listed argument is greater than or less than the allowable limit. For example, if 4 is given for an integer option, which is required to be less than or equal to 3, this error occurs.

WHAT NEXT

Supply a compatible value for the argument.

CMD-038

CMD-038 (information) The '%s' option for %s is unsupported.%s

DESCRIPTION

The option which you specified is not currently supported.

WHAT NEXT

CMD-039

CMD-039 (information) The '%s' variable is unsupported.%s

DESCRIPTION

The variable which you specified is not supported.

WHAT NEXT

If a replacement variable is specified, use it instead of this one.

CMD-040

CMD-040 (information) No %s matched '%s'.

DESCRIPTION

In command or variable search functions (help and printvar), you specified a pattern that did not match any variables or commands.

Note that printvar cannot find a specific array element; it can only find the entire array by name.

WHAT NEXT

Try using more wildcards (* or ?) in your search pattern.

CMD-041

CMD-041 (information) Defining new variable '%s'.

DESCRIPTION

This message is issued when a variable is set for the first time.

When combined with the **printvar** command, this message can be used to isolate spelling errors in system (application) variables. However, like many debugging features, this has significant CPU cost. Therefore, the feature should only be used interactively or when developing scripts.

This feature is enabled by setting the **sh_new_variable_message** variable to true. When combined with a true value for variables **sh_new_variable_message_in_script** or **sh_new_variable_message_in_proc**, this setting causes a warning message (CMD-042) to be issued, which indicates that the performance of scripts (or Tcl procedures) will be adversely affected. To enable the feature in Tcl procedures, set the **sh_new_variable_message_in_proc** variable to true. To enable the feature in Tcl scripts, set the **sh_new_variable_message_in_script** variable to true.

In the following example, the user has misspelled the variable **sh_continue_on_error** by making it plural. With this feature, debugging is simplified.

```
prompt> set sh_continue_on_errors true
Information: Defining new variable 'sh_continue_on_errors' (CMD-041)
true
prompt> printvar sh*
sh_arch              = "sparcOS5"
sh_continue_on_error = "false"
sh_continue_on_errors = "true"
sh_enable_page_mode  = "false"
sh_new_variable_message = "true"
sh_new_variable_message_in_proc = "false"
sh_product_version   = ""
sh_source_uses_search_path = "false"
prompt> unset sh_continue_on_errors
prompt> set sh_continue_on_error true
true

Application variables are always defined, so if this message appears,
a new user-defined variable has been created.
```

WHAT NEXT

If attempting to set an application variable, use **printvar** with wildcards to get the correct spelling for the variable.

SEE ALSO

printvar(2)
sh_new_variable_message(3)
sh_new_variable_message_in_proc(3)
sh_new_variable_message_in_script(3)
CMD-042(n)

CMD-042

CMD-042 (warning) Enabled new variable message tracing - Tcl scripting optimization disabled.

DESCRIPTION

This message is issued when you enable new variable tracing for Tcl scripts or procedures. That occurs when you set the variable **sh_new_variable_message** to TRUE, and when you set the variables **sh_new_variable_message_in_proc** or **sh_new_variable_message_in_script** to TRUE. It warns you that the performance of the application will be negatively mpacted because this feature is costly in CPU time when enabled.

This feature is intended for debugging, and should only be used interactively or when developing scripts. It should not be used in a main flow.

WHAT NEXT

Set one or more of the variables to FALSE unless you are debugging a script.

SEE ALSO

sh_new_variable_message(3)
sh_new_variable_message_in_proc(3)
sh_new_variable_message_in_script(3)

CMD-050

CMD-050 (error) Unknown procedure '%s'.

DESCRIPTION

The procedure name argument to **define_proc_attributes** is not a procedure.

WHAT NEXT

Verify that the argument is correct.

CMD-051

CMD-051 (error) Procedure '%s' cannot be modified.

DESCRIPTION

The procedure that you passed to **define_proc_attributes** is a permanent procedure that cannot be modified.

WHAT NEXT

The procedure might be part of the application, in which case it was correctly defined with *-permanent*. If it is not part of the application, it is possible that it was erroneously defined with *-permanent*.

CMD-052

CMD-052 (error) Unknown command group '%s'

DESCRIPTION

The command group referenced does not exist. For example, using the *-command_group* option with the **define_proc_attributes** command, and passing in a non-existent command group will raise this error.

WHAT NEXT

Verify that the correct command group name is being used.

CMD-053

CMD-053 (warning) The body of procedure '%s' is protected

DESCRIPTION

You attempted to examine the body of a procedure using **info body**. That procedure was protected by the writer so that it's body cannot be displayed.

WHAT NEXT

No action required.

CMD-060

CMD-060 (error) Syntax error in argument definition %d for proc '%s'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, there is some kind of syntax error, for example, an improperly formatted list.

WHAT NEXT

Use **error_info** to narrow the problem, then reenter the command.

CMD-061

CMD-061 (error) Need at least 2 fields in argument definition %d for proc '%s'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, an argument definition had insufficient arguments. At least 2 are required: the argument name and the option help text.

WHAT NEXT

Reenter the argument definition with the correct number of fields.

CMD-062

CMD-062 (error) Unknown %s '%s' in argument definition %d (%s) for proc '%s'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, either a data type or attribute is invalid.

The allowable data types are string, boolean, int, float, and list. The allowable attributes are required and optional.

WHAT NEXT

Correct the invalid data and reenter the command.

CMD-063

CMD-063 (error) Illegal name '%s' for Boolean argument definition %d for proc '%s': must begin with '-'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, you attempted to create a Boolean argument with a name not preceded by a '-'. Boolean arguments require a leading '-'.

WHAT NEXT

Correct the argument name and reenter the command.

CMD-064

CMD-064 (warning) Value help ignored for Boolean option %s in argument definition %d for proc '%s'.

DESCRIPTION

Using the *-define_args* option for **define_proc_attributes**, you tried to add value help for a Boolean argument. Boolean arguments cannot have the value help.

WHAT NEXT

Remove the value help field for boolean arguments and reenter the command.

CMD-065

CMD-065 (error) Can't specify both 'optional' and 'required' in argument definition %d (%s) for procedure '%s'

DESCRIPTION

This message indicates an attempt to specify conflicting flag values as part of the definition of a procedure argument within the **define_proc_attributes** command.

WHAT NEXT

Decide whether the argument is optional or required, and remove the opposite flag.

CMD-066

CMD-066 (error) Must specify a value for attribute 'values' when using '%s'option type as in option %d (%s) for procedure '%s'

DESCRIPTION

This message is issued by the **define_proc_attributes** command when you attempt to define an argument whose value must be one of a set of pre-defined strings (the one_of_string data type), without specifying the set of valid strings.

WHAT NEXT

If the value type really needs to be one_of_string, pass the values in as a list within the attributes list (i.e. {values {a b c}}).

CMD-067

CMD-067 (error) Invalid attribute specification for attribute '%s' (%s) in option %d (%s) for procedure '%s'

DESCRIPTION

This message is issued by the **define_proc_attributes** command. It indicates an incorrect attempt at specifying an attribute for a procedure argument. The reason for the error is included in the message.

WHAT NEXT

Fix the syntax of the command and try again.

CMD-068

CMD-068 (error) Could not find procedure '%s'. Arguments can't be parsed.

DESCRIPTION

This message indicates an attempt to use the parse_proc_arguments command from within a procedure which has not been defined using define_proc_attributes.

WHAT NEXT

Define the procedure's arguments using define_proc_attributes and try again.

CMD-069

CMD-069 (error) Could not set '%s(%s)' while parsing arguments in '%s'.

DESCRIPTION

This message indicates that the **parse_proc_arguments** command was not able to set the specified Tcl array variable to hold the value of a command option.

WHAT NEXT

This typically indicates that the variable was read-only. Use a different variable and try again.

CMD-070

CMD-070 (error) %s can only be called from within a procedure

DESCRIPTION

This message indicates an attempt to use the given command from the interpreter command line. Calls to this command are only supported from within a Tcl procedure.

WHAT NEXT

Create a procedure and call the command from within the scope of the procedure body.

CMD-080

CMD-080 (error) Command '%s' is disabled.

DESCRIPTION

Although part of the application, the listed command is not currently enabled.

WHAT NEXT

Look at the user documentation to determine how various commands are enabled and disabled.

CMD-081

CMD-081 (information) script '%s' stopped at line %d due to %s.

DESCRIPTION

The execution of a script was terminated. This message tells you which script stopped, the line number where it stopped, and why it stopped.

If the **sh_continue_on_error** variable is false (the default), any Tcl error, either syntax or semantic, stops the script. If **sh_continue_on_error** is false and the **sh_script_stop_severity** variable is W or E, messages of that severity or higher stop the script.

If the **sh_continue_on_error** variable is true, the **sh_script_stop_severity** variable is ignored and the script continues even if there are errors or warnings.

WHAT NEXT

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

SEE ALSO

sh_continue_on_error(3)
sh_script_stop_severity(3)

CMD-082

CMD-082 (information) %s occurred at or before line %d in script '%s'.

DESCRIPTION

You receive this message if an error or warning occurs while a script is executing, and the variable **sh_source_emits_line_numbers** is set to E or W. A setting of E causes this message to be issued only if an error occurs, while for a setting of W, this message is issued for both warnings and errors. This message tells you the error or warning and the line and script in which it occurred.

The setting of the **sh_script_stop_severity** variable affects the output of the CMD-082 message. If **sh_script_stop_severity** is set to E, the script stops executing if an error occurs; for a setting of W, the script stops executing if a warning or error occurs. In both cases, message CMD-081 is issued, and takes precedence over CMD-082.

WHAT NEXT

Use the information in this message to identify and correct the source of errors and warnings. Then reexecute the script.

SEE ALSO

sh_script_stop_severity(3)
sh_source_emits_line_numbers(3)
CMD-081(n)

CMD-085

CMD-085 (warning) Renaming %s %s cause %s commands which use it to fail.

DESCRIPTION

You receive this message if you rename a command which is not a user-defined Tcl procedure. Renaming commands can be dangerous. Parts of the application are written in Tcl, and if you rename a command that the application is using, it is possible that those parts of the application will not function.

The only true use for **rename** is to wrap a command. For example:

```
shell> rename command1 command1_orig
shell>  \
  proc command1 {args} {
    # ...
    eval command1_orig $args
    # ...
  }
```

If you use **rename** in this way, it is more likely that application will continue to function correctly. Still, use **rename** with extreme care and at your own risk.

WHAT NEXT

Consider using **alias**, Tcl procedures, or a private namespace before using **rename**.

SEE ALSO

rename(2)

CMD-086

CMD-086 (error) Could not find command '%s'.

DESCRIPTION

This message indicates that the command name entered does not exist and therefore operation on associated command mode could not be performed.

WHAT NEXT

Check to make sure command name is typed correctly.

CMD-087

CMD-087 (error) The command requires either a command name or a command mode name.

DESCRIPTION

This command requires either a command name or a command mode name to be specified.

WHAT NEXT

Enter **set_current_command_mode** with the **-command** option flag followed by a command name or the **-mode** option flag followed by a command mode name. These options are mutually exclusive.

CMD-088

CMD-088 (error) Could not find command mode '%s'.

DESCRIPTION

This message indicates that the command mode name entered does not exist and therefore could not be set as the current mode.

WHAT NEXT

Check to make sure command mode name is typed correctly. **get_command_modes -all** lists all defined command mode names.

CMD-089

CMD-089 (error) Initialization of command '%s' failed.

DESCRIPTION

This message indicates that a failure occurred during initialization and the specified command could not be evaluated.

CMD-090

CMD-090 (error) Initialization of command mode '%s' failed.

DESCRIPTION

This message indicates that a failure occurred during initialization of the command mode and the specified command mode could not be made current.

CMD-100

CMD-100 (warning) Detected use of obsolete/unsupported feature. The following will not be available in a future release of the application: %s. Use %s instead

DESCRIPTION

You have used a feature which is no longer supported by the application, and the feature is planned to be removed at some future date. The supported method is given in the message.

WHAT NEXT

Update your command usage as indicated.

CMD-101

CMD-101 (error) Failed to set value of option %s for command %s.

DESCRIPTION

A run of a command such as set_command_option_value failed to set the default or current value of an option. The command option may not have been enabled for value-tracking or a conversion error may have occurred when attempting to set the option value.

WHAT NEXT

It may be necessary to enable the option for value-tracking.

CMD-102

CMD-102 (error) No such positional option %d for command %s.

DESCRIPTION

An attempt was made to find the positional option of the command at the given position. No such positional option was found. Either the given command has no positional options, or the given position is "out of range". Note that positional options are numbered 0, 1, 2, ... (N-1) where N is the number of postional options of the command.

WHAT NEXT

Retry the operation using a positional option position that is "in range" for the command.

CMD-103

CMD-103 (error) A Severe error has occurred. To ensure that the script does not continue, the value of sh_continue_on_error has been overridden to be false. Your script is being interrupted. To see the Tcl call stack for the part of your script which generated the Severe error use the error_info command.

DESCRIPTION

A Severe error has occurred during a command execution. To ensure that the script does not continue, the value of sh_continue_on_error has been overridden to be false. Your script is being interrupted. To see the Tcl call stack for the part of your script which generated the Severe error use the error_info command.

WHAT NEXT

For details on the Severe error please look in your log file. You can also run man on the Severe error id to learn more about the error. Study the Severe error and try to fix the error in your script.

CMD-104

CMD-104 (error) Variable '%s' is not an application variable. Using Tcl global variable.

DESCRIPTION

The specified variable is not declared as an application variable (not returned by get_app_var -list). This

message is only generated when the application variable sh_allow_tcl_with_set_app_var is true.

Please see the manpages for get_app_var and set_app_var for additional details.

WHAT NEXT

Make sure you are using the correct variable name.

CMD-105

CMD-105 (warning) Option '%s' is deprecated, use '%s' instead.

DESCRIPTION

This option is deprecated, you should use a different option for this command feature. The code has automatically used a compatible option setting, but in the future the old option may be removed, so you should update your scripts.

WHAT NEXT

Update your script to use the new option.

CMD-106

CMD-106 (warning) Option '%s' for command '%s' is obsolete. See the command's man page for alternatives.

DESCRIPTION

This option is no longer supported, specifying it has no effect.

WHAT NEXT

Update your script

CMD-107

CMD-107 (error) Not enough values specified for option '%s', requires %d values found %d.

DESCRIPTION

The listed option requires that the specified number of values and not enough values were supplied.

WHAT NEXT

Supply all the required values for the option.

CMD-108

CMD-108 (warning) Command %s is obsolete. See the command's man page for alternatives.

DESCRIPTION

This command is obsolete. Calling it has no effect. Please see product documentation for alternatives.

WHAT NEXT

Update your script as needed.

CMD-109

CMD-109 (warning) Command %s is deprecated. See the command's man page for alternatives.

DESCRIPTION

This command is deprecated. Please see product documentation for alternatives.

WHAT NEXT

Update your script as needed.

CMD-110

CMD-110 (warning) Option '%s' for command '%s' is deprecated. See the command's man page for alternatives.

DESCRIPTION

This option is deprecated, you should use a different option for this command feature.

WHAT NEXT

Update your script to use the new option.

CMD-999

CMD-999 (severe) A Severe error has occurred during testing.

DESCRIPTION

A Severe error has occurred during testing. This should never happen in production.

WHAT NEXT

CMDS Error Messages

CMDS-001

CMDS-001 (error) Cannot read file '%s'.

DESCRIPTION

The file you specified either does not exist or you do not have read access to that file.

WHAT NEXT

Check the search path or use the **file** command to verify the existence of the file and its attributes.

CMDS-002

CMDS-002 (error) Pin %s is not a transistor pin.

DESCRIPTION

The clock pin must be a transistor pin.

WHAT NEXT

Remove all non-transistor pins from clock pins.

CMDS-003

CMDS-003 (Error) %s is not a transistor.

DESCRIPTION

The specified element is not a transistor. Certain commands or actions can only take transistors as arguments.

WHAT NEXT

Use the **is_transistor** cell attribute to determine whether the element is a transistor.

CMDS-004

CMDS-004 (Error) Invalid value %s for variable %s. Valid values are %s.

DESCRIPTION

The entered value for this variable is incorrect.

WHAT NEXT

Make sure that the value is an acceptable one.

CMDS-005

CMDS-005 (error) Cannot run command '%s'. Use '%s' to move forward to the next phase.

DESCRIPTION

The command cannot be executed because some required commands have not yet been executed.

WHAT NEXT

Use the command noted in the error message to move the tool forward to the next phase, then re-try the original command.

CMDS-006

CMDS-006 (error) Cannot run command '%s'. Use '%s' to move backward to a previous phase.

DESCRIPTION

The command cannot be executed because it would result in the loss of information which may be time-consuming to recalculate.

WHAT NEXT

Use the command noted in the error message to move the tool back to the desired phase, then re-try the original command.

CMDS-007

CMDS-007 (Error) Clock %s already exists.

DESCRIPTION

An attempt was made to define a clock that already exists.

WHAT NEXT

Either delete the existing clock or choose a different name for the new clock to avoid conflict.

CMDS-008

CMDS-008 (Error) Syntax problem while defining a clock: %s

DESCRIPTION

An illegal syntax combination was attempted during definition of a clock.

WHAT NEXT

Check for legal syntax from clock definition commands.

CMDS-009

CMDS-009 (Warning) Converting propagated clock at '%s' to ideal clock.

DESCRIPTION

The clock was originally a propagated clock. Adding network latency implies an ideal clock, so this clock is being converted to ideal.

WHAT NEXT

Make sure that this clock is intended to be ideal. If not, change the latency added to -source instead of -

network.

CMDS-010

CMDS-010 (warning) Virtual clock '%s' cannot be made propagated.

DESCRIPTION

A virtual clock does not have any pins and therefore can not be made propagated.

WHAT NEXT

Check to see if this clock should have pins defined.

CMDS-011

CMDS-011 (warning) Could not match an existing timing check.

DESCRIPTION

An attempt was made to change a timing check but no timing check in the current design matched the specified input.

WHAT NEXT

Check the netlist names specified when trying to match a timing check.

CMDS-012

CMDS-012 (error) Cannot open output file '%s'.

DESCRIPTION

The file you specified either cannot be created or you do not have write access to that file.

WHAT NEXT

Check the search path or use the **file** command to verify the existence of the output file or directory and its attributes.

CMDS-013

CMDS-013 (error) %s is not yet implemented.

DESCRIPTION

The command or option is not yet implemented.

WHAT NEXT

This option or feature will be implemented in a later version of NanoTime. Limit testing to features supported in this version of NanoTime.

CMDS-014

CMDS-014 (error) Incorrect value for global variable '%s':'%s'; must be one of {%s}.

DESCRIPTION

The value you specified is not one of the expected strings, so the first item in the list of allowed values was used.

WHAT NEXT

Check the list of allowed values and choose one of them.

CMDS-015

CMDS-015 (error) Can't set min library to %s.

DESCRIPTION

You receive this message if the min library you passed to **set_min_library** is invalid. The library might be the same as the max library, or might have already been used as the max library in a **set_min_library** command. The max and min libraries must be different.

WHAT NEXT

Execute **set_min_library** again and specify a valid min library.

CMDS-016

CMDS-016 (information) '%s' already has '%s' as its min library.

DESCRIPTION

The min library you passed to **set_min_library** has already been related to the max library using **set_min_library**.

WHAT NEXT

This is an informational message only; no action is required. However, if you intended to change the relationship of the max library to a different min library, check the spelling of the min library argument.

CMDS-017

CMDS-017 (warning) Cannot create max/min library cell relationship for '%s': %s.

DESCRIPTION

The **set_min_library** command found a library cell in the min library that matches the library cell in the max library. However, some aspect of the two library cells is different. For example, one might have more pins than the other; the pins might be in a different order; or the timing arcs might be different. The text of the message states the most serious difference. To create a max/min library cell relationship, both cells must have the same timing arcs and the same pins, with the same order and direction.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the **set_min_library** command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should read the message text to determine why the cells are different, and ensure that the max and min libraries are compatible.

CMDS-018

CMDS-018 (warning) No match for %s/%s in library '%s'.

DESCRIPTION

The **set_min_library** command could not find a library cell in the min library that matches the specified library cell in the max library. Therefore, a max/min library cell relationship cannot be created for that cell.

For cells where the max/min relationship fails, as in the current situation, the command uses a minimum condition delay calculation based on the max library. If even one of the library cell pairs matches and compares correctly, the **set_min_library** command continues executing and succeeds.

WHAT NEXT

This is a warning message; no action is required on your part. However, you should determine why there is not a match for the specified cell, and ensure that the max and min libraries are compatible.

CMDS-019

CMDS-019 (warning) The %s was not matched.

DESCRIPTION

There were no matches for the given subcircuit or pattern.

WHAT NEXT

Check the spelling and case of the subcircuit name, the applicability of the pattern, etc.

CMDS-020

CMDS-020 (warning) Could not match any existing timing constraints %s the specified pin(s).

DESCRIPTION

An attempt was made to change a timing check but no timing check in the current design matched the specified input.

WHAT NEXT

Check the netlist names specified when trying to match a timing check.

CMDS-021

CMDS-021 (error) Incompletely specified '%s' command.

DESCRIPTION

For the set_timing_check_attributes command, either the -of_objects option or at least one of the -to options or -target options must be specified. It is possible to specify both. However, if only the -to pin is specified, then it is assumed to be the same as the -target pin, as long as -to_not_target is not used. If -to_not_target is used, all the existing timing constraints are searched for a match of their checked pin with the given -to pin. Otherwise, only those that are associated with the given target pin are searched for a match with the -to pin. Also, the -trigger option cannot be used unless the -target option is also used for both set_timing_check_attributes and get_timing_checks.

WHAT NEXT

Check the command and add the appropriate option(s).

CMDS-022

CMDS-022 (Error) samples should be in range [5,100]

DESCRIPTION

The set_nonlinear_waveform command requires the number of samples to be a number between 5 and 100, inclusive.

WHAT NEXT

Enter the command again using -samples set to a number between 5 and 100.

CMDS-023

CMDS-023 (Error) Nonlinear ratio should be in the range of [0.01,100.0].

DESCRIPTION

The set_nonlinear_waveform command requires the -threshold option to be set a value between 0.01 and 100, inclusive.

WHAT NEXT

Enter the command again using -threshold set to a number between 0.01 and 100.

CMDS-024

CMDS-024 (Error) Invalid nonlinear waveform mode

DESCRIPTION

The set_nonlinear_waveform command requires the -mode option to be set to one of the following strings: accurate, efficient, detect_only, or fast.

WHAT NEXT

Enter the command again using -mode set to the string accurate, efficient, detect_only, or fast.

CMDS-025

CMDS-025 (Error) Invalid set_si_delay_analysis or remove_si_delay_analysis options combination '%s' and '%s'

DESCRIPTION

Only one option of (-exclude, -reselect, -ignore_arrival) is accepted by the set_si_delay_analysis and remove_si_delay_analysis command. -exclude option can be combined with -min, -max, -fall and -rise.

WHAT NEXT

Enter the command again using only one option of (-exclude, -reselect, -ignore_arrival)

CMDS-026

CMDS-026 (Error) '%s' should be combined with '%s' for set_si_delay_analysis or remove_si_delay_analysis

DESCRIPTION

Only one option of (-exclude, -reselect, -ignore_arrival) is accepted by the set_si_delay_analysis and

remove_si_delay_analysis command. -exclude option can be combined with -min, -max, -fall and -rise.

WHAT NEXT

Enter the command again using only one option of (-exclude, -reselect, -ignore_arrival)

CMDS-027

CMDS-027 (warning) %s can not be used without a NanoTime-ultra license.

DESCRIPTION

This feature is part of the NanoTime-ultra licensing package and must have a NanoTime-ultra license available for use.

WHAT NEXT

Check your license server and the status of any NanoTime-ultra licenses available.

CMDS-028

CMDS-028 (error) Incorrectly specified tabular value for set_timing_check_attributes command: %s

DESCRIPTION

For the **set_timing_check_attributes** command, the **-rise_from_transition**, **-fall_from_transition**, **-rise_target_transition**, and **-fall_target_transition** options are applicable only when the check value is tabular. The table must be complete so that the number of triplets equals the product of unique number of values for reference and checked transitions. The table must of be of the form {{T11 T21 V11} ..... {T1n T2m Vnm}} where T1 represents the rail-rail transition at the 'from' pin, T2 represents the rail-rail transition at the 'to' (target) pin, and V represents the check value.

WHAT NEXT

Check the command and add the appropriate options.

CMDS-029

CMDS-029 (error) The command %s can not be used on generated clock: %s

DESCRIPTION

The commands set_clock_period and set_clock_waveform can not be used on generated clocks. To modify the waveform of a generated clock change the master clock for this generated clock.

WHAT NEXT

Look up the master clock which is the source for this generated clock.

CMDS-030

CMDS-030 (error) New clock period %g is less than current rise %g or fall %g

DESCRIPTION

A clock period can not be reduced to a value less than the value of the current rise or fall edge of the clock waveform. If this is the desired period then change the clock waveform prior to changing the clock period.

WHAT NEXT

Use set_clock_waveform to change the clock waveform to allow for the new period.

CMDS-031

CMDS-031 (error) The proposed clock waveform {%g %g} has a pulsewidth or value which is greater than the current clock period %g

DESCRIPTION

A new waveform for a clock can not have a rise or fall value outside the range of the current clock period. The pulse width of the new waveform must also be smaller than the current clock period. If this waveform is desired then make the current clock period larger with the set_clock_period command.

WHAT NEXT

Use set_clock_period to change the clock period to allow for the new waveform.

CMDS-032

CMDS-032 (error) Cannot run set_soi_parameters command in non-SOI mode.

DESCRIPTION

SOI analysis mode must be enabled before set_soi_parameters can be run. To enable SOI mode, set the variable **soi_enable_analysis** to true. Special product licensing may apply.

WHAT NEXT

Check the value of the **variable** soi_enable_analysis.

CMDS-033

CMDS-033 (error) Must specify max, min and rail reference voltages.

DESCRIPTION

When providing SOI parameters for a transistor model, all three parameters must be specified.

WHAT NEXT

Check the arguments of the **set_soi_parameters** command.

CMDS-034

CMDS-034 (error) Cannot run set_soi_transistor_type command in non-SOI mode.

DESCRIPTION

SOI analysis mode must be enabled before set_soi_transistor_type can be run. To enable SOI mode, set the variable **soi_enable_analysis** to true. Special product licensing may apply.

WHAT NEXT

Check the value of the **variable** soi_enable_analysis.

CMDS-035

CMDS-035 (error) Must specify a valid list of transistors.

DESCRIPTION

This command accepts only a list of transistors.

WHAT NEXT

Check the arguments of the **set_soi_transistor_type** command.

CMDS-036

CMDS-036 (error) The min SOI body voltage must not be higher than the max body voltage for either PMOS or NMOS transistors types.

DESCRIPTION

The numerical value of the **max** option must not be smaller than that of the **min** option of the **set_soi_parameters** command.

WHAT NEXT

Check the arguments of the **set_soi_parameters** command.

CMDS-037

CMDS-037 (warning) '%s' cannot be set after '%s'.

DESCRIPTION

The user variable can only be set or unset before the referenced command, such as link_design or check_design.

WHAT NEXT

Move this user variable setting before the referenced command.

CMDS-038

CMDS-038 (Error) The '%s' command has failed while updating internal data.

DESCRIPTION

The command has failed while performing actions related to the command. This message is simply clarifying that previous errors have caused a failure of the command.

WHAT NEXT

Look for error messages in the log that occurred before this one and fix those errors.

CMDS-039

CMDS-039 (warning) %s is not turned on to enable SI analysis. Coupling capacitors (if there is any) will be split to ground.

DESCRIPTION

%s should be turned on for SI analysis.

WHAT NEXT

set %s to true.

CMDS-040

CMDS-040 (warning) The command or option %s can only be run during SI analysis.

DESCRIPTION

Some features are only valid during SI analysis.

WHAT NEXT

Set the variable si_enable_analysis TRUE.

CMDS-041

CMDS-041 (Warning) The %s path sense between start pin %s and generated clock target pin %s is inconsistent with generated clock definition sense for clock %s.

DESCRIPTION

When you use the **-divide_by** and **-multiply_by** options with the **create_generated_clock** command, the inversions along the clock path from path start to the targets must match the **-invert** option.

WHAT NEXT

If the generated clock was specified with the **-invert** option, consider removing it. If not, add the **-invert** option to the **create_generated_clock** command.

CMDS-042

CMDS-042 (warning) The -si_cluster option is unset by -si_aggressors option

DESCRIPTION

-si_cluster cannot be combined with -si_aggressors option, -si_aggressors option will disable -si_cluster option

WHAT NEXT

unset the option -si_aggressors

CMDS-043

CMDS-043 (warning) Net %s is not a clock net.

DESCRIPTION

The command report_clock_arrivals will only report on nets that are part of the clock network. The net in the warning is not currently a clock net.

WHAT NEXT

If the net should be in the clock network then check your clock definitions and other commands used to facilitate propagating the clock signals.

CMDS-044

CMDS-044 (warning) Invalid check specified, command %s can not remove a check of type %s.

DESCRIPTION

The commands remove_timing_check, remove_gated_clock_check, and remove_data_check each operate on mutually exclusive types of checks. Only the matching check can be used with each command.

WHAT NEXT

Use the appropriate remove command for the type of check indicated.

CMDS-045

CMDS-045 (error) '%s' cannot be used without '%s'.

DESCRIPTION

The first feature cannot be used without the second feature.

WHAT NEXT

Modify the command to include both the features.

CMDS-046

CMDS-046 (Error) The combination of delay/slew thresholds is invalid or out of range.

DESCRIPTION

The value specified is not within the bounds of the allowed delay and/or slew thresholds.

WHAT NEXT

Check the threshold values for consistency with other related thresholds.

CMDS-048

CMDS-048 (Error) Port %s is not an input or inout port.

DESCRIPTION

The set_driving_cell and remove_driving_cell commands apply only to input or inout ports.

WHAT NEXT

Specify the correct list of input or inout ports.

CMDS-049

CMDS-049 (Error) The command %s cannot be invoked without setting the variable "si_enable_noise_analysis" to true and reading in coupled parasitic capacitors.

DESCRIPTION

The commands related to signal integrity noise analysis can be invoked only if the **si_enable_noise_analysis** variable is set to **true**. Use the **-keep_capacitive_coupling** option with the **read_parasitics** or **link_design** command to preserve coupled devices.

WHAT NEXT

Set the **si_enable_noise_analysis** variable to **true** before invoking this command.

CMDS-050

CMDS-050 (Error) The -si_noise option can not be combined with -si_cluster or -si_aggressors options

DESCRIPTION

-si_noise is for SI noise analysis, while -si_cluster and -si_aggressors are options for SI delay analysis

WHAT NEXT

choose -si_noise for noise analysis or -si_cluster/-si_aggressors for SI-delay analysis

---

CMDS-051

CMDS-051 (warning) SI Noise analysis of type %s is not performed on net %s.

DESCRIPTION

Only nets with appropriate driver or holding resistance are considered for noise analysis.

WHAT NEXT

Check the netlist and specify driver or holding resistance for this net.

CMDS-052

CMDS-052 (Error) The command %s cannot be invoked without setting the variable "si_enable_noise_fanout_analysis" in addition to setting si_enable_noise_analysis to true.

DESCRIPTION

The commands related to SI Noise fanout analysis can be invoked only if the variable "si_enable_noise_fanout_analysis" is set to true in addition to si_enable_noise_analysis. Also use the -keep_capacitive_coupling option with read_parasitics or link_design to preserve coupled devices within NanoTime.

WHAT NEXT

Please set the variable "si_enable_noise_fanout_analysis" to true before invoking this command.

CMDS-053

CMDS-053 (Error) This command takes only 2 transistors as its arguments.

DESCRIPTION

This command works only with an argument list that has 2 transistors in it.

WHAT NEXT

Specify only 2 transistors on the command line.

CMDS-054

CMDS-054 (Error) %s and %s do not form a cross-coupled pmos topology.

DESCRIPTION

The specified transistors do not form a cross-coupled pmos pullup topology.

WHAT NEXT

Ensure that the devices are pulling up to power-supply and their gates are cross-coupled to the respective source/drain terminals.

CMDS-055

CMDS-055 (Warning) The write_spice noise (%s) requested on net %s does not exist%s.

DESCRIPTION

The noise requested by the **write_spice** command does not exist. Some possible causes are as follows: the specified net might not be active for noise analysis, the net might not have any coupling capacitances, the specific type of noise might not have been computed, or the fanout net (if specified) might not be correct for the victim net.

WHAT NEXT

Use the **report_noise** and **report_fanout_noise** commands to verify the existence of noise values on the requested nets. Use the **set_noise_parameters -include_beyond_rails** command if above_high or below_low noise values are needed.

CMDS-056

CMDS-056 (Warning) User-based multi-input switching and automatic multi-input switching modes are incompatible.

DESCRIPTION

The automatic multi-input switching mode of NanoTime cannot be used concurrently with the **set_conservative_min_delay** or **set_conservative_max_delay** commands. This might produce unpredictable results.

WHAT NEXT

Make sure that the global automatic multi-input switching mode (enabled with the **timing_enable_multi_input_switching** variable) is not turned on when using the **set_conservative_min_delay** or **set_conservative_max_delay** commands.

CMDS-057

CMDS-057 (Error) Command %s cannot be run after %s when DCS is enabled.

DESCRIPTION

There are restrictions on when certain commands can be run if DCS is enabled.

WHAT NEXT

Change the order of commands or invoke additional commands to reset the state.

CMDS-058

CMDS-058 (Error) The option %s for command %s cannot be used unless the variable %s is set to true.

DESCRIPTION

The **set_miller_direction_check** variable must be set in order to invoke direction-based Miller calculations.

WHAT NEXT

Set the **set_miller_direction_check** variable to **true**.

CMDS-059

CMDS-059 (Warning) Net %s and %s are not coupled.

DESCRIPTION

The two nets specified are not coupled.

WHAT NEXT

Check if the net name is correct.

CMDS-060

CMDS-060 (Warning) Net %s is not aggressor of any net.

DESCRIPTION

This net is not coupled to other nets.

WHAT NEXT

Check if the net name is correct.

CMDS-061

CMDS-061 (Error) Pin %s is not a generated clock start pin.

DESCRIPTION

The set_input_transition and set_model_input_transition_indexes commands can only be used with ports or pins which are generated clock starting points.

WHAT NEXT

Check the pin name and the generated clock definitions.

CMDS-062

CMDS-062 (Error) Can not create clock %s because it is dangling.

DESCRIPTION

The specified clock is not associated with any net and it is dangling.

WHAT NEXT

Check clock name or pin name specified and make sure it is correct.

CMDS-063

CMDS-063 (Error) Enable pin '%s' is not a %s pin of a transistor.

DESCRIPTION

The specified enable pin should be the appropriate pin of a transistor.

WHAT NEXT

Check the -enable argument and make sure it is the appropriate pin of the enable transistor.

CMDS-064

CMDS-064 (Error) Net '%s' is not connected to any specified transistor.

DESCRIPTION

The specified net should be connected to at least one transistor specified by the command.

WHAT NEXT

Check the -input and -output arguments and make sure nets are connected to the elements specified by the command.

CMDS-065

CMDS-065 (error) The -hspice_timing option cannot be enabled for designs using technology files.

DESCRIPTION

HSPICE does not support tech files. The recalibration needs spice models to run HSPICE.

WHAT NEXT

use spice models for simulation.

CMDS-066

CMDS-066 (error) The '%s' option for the command '%s' can only be used after running '%s'.

DESCRIPTION

This option requires a valid timing graph and can not be used without one.

WHAT NEXT

Run check_design before using this option or remove the option.

CMDS-067

CMDS-067 (error) The command '%s' failed due to requirements caused by the option '%s'.

DESCRIPTION

The command issued has additional requirements associated with some options. These requirements were not met, causing the command to fail. These options are typically related to command sequencing and/or the current state.

WHAT NEXT

Either remove the option causing the problem or run the commands needed to get to the needed state.

CMDS-068

CMDS-068 (Error) The variable sim_miller_use_active_load_min cannot be set to true unless the variable sim_miller_use_active_load is set to true.

DESCRIPTION

The variable sim_miller_use_active_load must be set in order to invoke active miller on min paths.

WHAT NEXT

Set the variable sim_miller_use_active_load to true.

CMDS-069

CMDS-069 (Error) No delay arcs matching the trigger pin and direction were found to the target point.

DESCRIPTION

When the set_timing_check -trigger/-rise_trigger/-fall_trigger option is used there must be at least one delay arc from the specified trigger to the target point. If none exist then the command will fail.

WHAT NEXT

Check the netlist and see if the trigger pin and direction have been specified correctly.

CMDS-070

CMDS-070 (Error) CCS Noise models cannot be generated unless the variable si_enable_noise_analysis is set to true.

DESCRIPTION

The variable si_enable_noise_analysis must be set to true before requesting the generation of CCS noise models.

WHAT NEXT

Set the variable si_enable_noise_analysis to true.

CMDS-071

CMDS-071 (warning) Executing command '%s' at this phase may result in a loss of previous work. Command '%s' must now be run again to move forward.

DESCRIPTION

It may be more efficient to execute the command at an earlier phase, so that phase transition commands do not need to be run more than once.

WHAT NEXT

Check and make sure this command is executed at the right phase.

CMDS-072

CMDS-072 (error) '%s' cannot be used with '%s'.

DESCRIPTION

The first feature cannot be used with the second feature.

WHAT NEXT

Modify the command to include only one of the features.

CMDS-073

CMDS-073 (warning) The PBSA override value of %2.4f for options %s may lead to excessively %s path.

DESCRIPTION

The supplied override value will be used for path-based slack adjustment on the given path. A very large or very small value should be used with great caution.

WHAT NEXT

Verify that the override value is correct.

CMDS-074

CMDS-074 (warning) %s cannot be used without a NanoTime for memories license.

DESCRIPTION

This feature is part of the NanoTime for memories licensing package and must have a NanoTime for memories license available for use.

WHAT NEXT

Check your license server and the status of any NanoTime for memories licenses available.

CMDS-075

CMDS-075 (warning) set_dcs_input is used without setting dcs_enable_analysis to true.

DESCRIPTION

The **set_dcs_input** command has an effect only if the **dcs_enable_analysis** variable is set to **true**.

WHAT NEXT

To enable dynamic clock simulation, set the **dcs_enable_analysis** variable to **true**.

CMDS-076

CMDS-076 (error) %s cannot be used without the appropriate licenses.

DESCRIPTION

This feature is part of the NanoTime memory feature and must have the appropriate licenses available for use.

WHAT NEXT

Check your license server to ensure there are sufficient licenses available.

CMDS-077

CMDS-077 (error) Generated clock source pins connected to different nets '%s' and '%s' have been defined.

DESCRIPTION

If multiple source pins are defined for a generated clock, they must all be connected to the same net or its differential complement net. Generated clocks cannot be created as a function of more than one input waveform together with its differential complement if it exists or one clock definition.

WHAT NEXT

Check your generated clock definition and adjust your source pin definitions so that they are all connected to the same net or its differential complement.

CMDS-078

CMDS-078 (warning) Nothing matched when trying to remove a '%s' type timing exception.

DESCRIPTION

The syntax used to match a user-defined type of timing exception did not match anything currently defined.

WHAT NEXT

Use the **report_exceptions** or **report_find_path** command to see what exceptions currently exist.

CMDS-079

CMDS-079 (Error) Syntax problem while defining input noise: %s

DESCRIPTION

An illegal syntax was attempted during definition of input noise.

WHAT NEXT

Check the legal syntax for defining input noise.

CMDS-080

CMDS-080 (Warning) Port %s is a supply net; NanoTime cannot set input transition.

DESCRIPTION

The set_input_transition and set_model_input_transition_indexes commands can only be used with input ports that are not power supply or ground.

WHAT NEXT

When running these commands ensure that supply or ground ports are not included in the port list.

CMDS-081

CMDS-081 (warning) SI delay or SI noise analysis is enabled without -keep_capacitive_coupling option

with %s command. Coupling capacitors (if there are any) will be split to ground.

DESCRIPTION

-keep_capacitive_coupling option should be used with %s command for SI delay or SI noise analysis.

WHAT NEXT

Use -keep_capacitive_coupling option with %s command.

CMDS-082

CMDS-082 (Error) parasitics_coupling_cap_variation_min should be in the range of [0.0, 1.0).

DESCRIPTION

The value of parasitics_coupling_cap_variation_min should be greater than or equal to 0 and less than 1.

WHAT NEXT

Set the value again within the range [0.0, 1.0), or the default value of 0 will be used.

CMDS-083

CMDS-083 (Error) parasitics_coupling_cap_variation_max should be greater than or equal to 0.

DESCRIPTION

The value of parasitics_coupling_cap_variation_max should be greater than or equal to 0.

WHAT NEXT

Set the value again within the acceptable range, or the default value of 0 will be used.

CMDS-084

CMDS-084 (Error) The skew between the reference net %s and the complement net %s in the differential pair is not specified correctly.

DESCRIPTION

The skew between two nets in a differential pair must be non-negative floating point values. The maximum skew must be larger than minimum skew.

WHAT NEXT

Change the negative skew value to non-negative.

CMDS-085

CMDS-085 (Error) The %s %s already belongs to a differential pair.

DESCRIPTION

An object cannot belong to multiple differential pairs.

WHAT NEXT

Check if the object in the differential pair was already defined as part of a differential pair.

CMDS-086

CMDS-086 (Error) The reference %s %s in the differential pair is neither a defined clock %s nor a master clock source of a generated clock.

DESCRIPTION

The **set_differential** command requires an argument that is a list or collection of exactly two objects of the same type.

The reference pin or port must be either (1) A clock leaf pin or port defined by the **create_clock** or **create_generated_clock** command, or (2) A leaf pin of a master clock source defined by a **create_generated_clock** command.

WHAT NEXT

Check if the reference pin or port in the differential pair satisfies either constraint (1) or (2).

CMDS-087

CMDS-087 (Error) Specifying skew between two clock %s in a differential pair is not allowed.

DESCRIPTION

Specifying the **skew_max** and **-skew_min** options in the **set_differential** command is valid only with net objects.

WHAT NEXT

Use the **set_differential** command with net objects to specify skew between them. To specify skew between differential clock ports or pins, use the **set_clock_latency** command.

CMDS-088

CMDS-088 (Error) Option -same_cycle is inconsistent with the other specified arguments of command %s.

DESCRIPTION

The **-same_cycle** option only applies to timing checks between the same edges of a clock.

WHAT NEXT

Change one or more of the other specified arguments of the command or do not use the **-same_cycle** option.

CMDS-089

CMDS-089 (Information) The %s path sense between start pin %s and generated clock target pin %s is inconsistent with generated clock definition sense for clock %s, pruning path search.

DESCRIPTION

When you use the **-divide_by** and **-multiply_by** options with the **create_generated_clock** command, the inversions along the clock path from path start to the targets must match the **-invert** option.

WHAT NEXT

Check the usage of the **-invert** option of the **create_generated_clock** command.

CMDS-090

CMDS-090 (Error) Cannot create clock %s because pin %s is a differential complement pin for another clock.

DESCRIPTION

The specified pin is already part of another clock.

WHAT NEXT

Check pin name specified and make sure it is correct.

CMDS-091

CMDS-091 (Error) Cannot create generated clock with source pins on more than two nets.

DESCRIPTION

Differential generated clocks can be created with source pins on two nets, otherwise they must be on one net.

WHAT NEXT

Check pin names specified and make sure they are correct.

CMDS-092

CMDS-092 (Error) Clock %s was already created on pin %s.

DESCRIPTION

Only one clock can be created on a pin.

WHAT NEXT

Check pin names specified and make sure they are correct.

CMDS-093

CMDS-093 (Warning) The %s %s is not set as a differential pair.

DESCRIPTION

The object specified by user is not set as a differential pair.

WHAT NEXT

Check if the object belongs to a differential pair or was removed by **remove_differential** command.

CMDS-094

CMDS-094 (Warning) Clock pin %s is not a leaf pin.

DESCRIPTION

Hierarchical clock pins create ambiguity during timing analysis.

WHAT NEXT

Check pin names specified and make sure they are correct.

CMDS-095

CMDS-095 (Warning) Detected use of obsolete/unsupported feature. The following will not be available in a future release: %s.

DESCRIPTION

You have used a feature which is no longer supported, and the feature is planned to be removed at some future date.

WHAT NEXT

Update your command usage as indicated.

CMDS-096

CMDS-096 (Error) The objects in the differential pair are not of the same type.

DESCRIPTION

The list or collection in the argument of the **set_differential** command must contain two objects of the same type (nets, pins, or ports).

WHAT NEXT

Check if there are exactly two items in the list and make sure that they are of the same type (nets, pins, or ports).

CMDS-097

CMDS-097 (Error) Pin %s in the differential pair is not a leaf pin.

DESCRIPTION

The object list or collection in the argument of **set_differential** command must contain exactly two objects of the same type (nets, pins, or ports). If the objects are pins, they must be leaf pins.

WHAT NEXT

Check if the pins in the list are leaf pins.

CMDS-098

CMDS-098 (Error) The complement %s %s in the differential pair is already defined as a clock %s.

DESCRIPTION

The **set_differential** command requires an argument that is a list or collection of exactly two objects of the same type. The first object is the reference pin or port and the second object is the complement pin or port. The complement pin or port must be a leaf pin or port which is not defined as a clock.

WHAT NEXT

Check if the complement pin or port has already been defined as a clock pin or port.

CMDS-099

CMDS-099 (Error) The number of objects in the list of differential pair is not exactly two.

DESCRIPTION

The list or collection in the argument of **set_differential** command must contain exactly two objects of the same type (nets, pins, or ports). The first object in the list must be the reference object and the second object must be the complement object of the differential pair.

WHAT NEXT

Check if there are exactly two items in the list and make sure that they are of the same type (nets, pins, or ports).

CMDS-100

CMDS-100 (Error) An illegal combination of options was used for set_variation_parameters.

DESCRIPTION

The command set_variation_parameters supports several values for -type. If "nmos" or "pmos" has been chosen, the option -width must be also included. Also, the options -length, -voltage, -transistor_model_type, -series2, -series3, and -series4 may be specified.

If the value for -type is set to "dds", "dcs", "libcell", or default, the options -length, -voltage, -transistor_model_type, -series2, -series3, and -series4 may not be specified.

WHAT NEXT

Change the combination of options being used for this command.

CMDS-101

CMDS-101 (Error) The reference %s %s and the complement %s %s of a differential pair are improperly on the same logical net.

DESCRIPTION

The reference and complement pins of a differential pair must have an inverse relationship. Therefore, they cannot be on the same logical net.

WHAT NEXT

Make sure that the reference and complement pins are on different logical nets that have an inverse relationship.

CMDS-102

CMDS-102 (Error) Found existing differential synchronizer defined on transistor %s which is connected to net %s.

DESCRIPTION

The **set_differential** command must be used to mark all related differential nets before a differential synchronizer is manually marked or automatically recognized.

WHAT NEXT

Ensure that all relevant differential nets are defined with the **set_differential** command before marking a differential synchronizer manually with the **mark_differential_synchronizer** command.

If you want NanoTime to automatically recognize differential synchronizers, mark all related differential nets with the **set_differential** command before you invoke the **match_topology** command.

CMDS-104

CMDS-104 (Error) Unable to declare a new differential %s pair at the current command phase.

DESCRIPTION

After **check_topology** the **set_differential** command can only be used to change the attributes of an existing differential pair.

WHAT NEXT

Check the arguments of the **set_differential** command.

CMDS-105

CMDS-105 (Error) Cannot declare differential property on the %s %s since it is connected to rail.

DESCRIPTION

Differential property cannot be declared on nets, pins or ports that are connected to rail.

WHAT NEXT

Check the arguments of the **set_differential** command.

CMDS-106

CMDS-106 (Error) Command '%s' is not supported with TMI2 SPICE models.

DESCRIPTION

This command or option cannot be used with TMI2 SPICE models.

WHAT NEXT

Check for alternate commands or options.

CMDS-107

CMDS-107 (Warning) Redefining the type of an existing supply net %s: previously defined as %s, now setting to %s.

DESCRIPTION

The net specified has existing supply type defined that is inconsistent with the new type.

WHAT NEXT

Check that net names and supply types are specified correctly. Also check that the command options -gnd and -virtual are specified appropriately.

CMDS-108

CMDS-108 (Warning) Net %s is not a top-level design net.

DESCRIPTION

Creating a port for a net, which is not in the top hierarchy, can lead to errors in reporting, model generation, etc.

WHAT NEXT

Check net names specified and make sure they are top-level design nets.

CMDS-109

CMDS-109 (Warning) No delay arcs matching the trigger pin ('%s') and direction were found to the target pin ('%s').

DESCRIPTION

When **set_timing_check** command is used with **-trigger**, **-rise_trigger**, or **-fall_trigger** options there should be at least one delay arc from the specified trigger to target. If multiple trigger and target pairs exist with corresponding delay arcs, constraints will be generated as requested. If no delay arcs exist across all trigger and target pairs then the command will fail.

WHAT NEXT

Check the netlist and see if the trigger pin and direction have been specified correctly.

CMDS-110

CMDS-110 (Error) Found differential net pair (%s, %s) in a %s region.

DESCRIPTION

NanoTime currently does not support differential analysis in DDS/DCS. Having a differential net pair in a dynamic simulation region can lead to erroneous result or undefined behavior.

WHAT NEXT

Check that a dynamic simulation region does not contain differential net pairs.

CMDS-111

CMDS-111 (Warning) Ignoring '%s' option for the '%s' command. The option can only be used after running '%s'.

DESCRIPTION

This option is available only after certain commands have been run. The option will be ignored.

WHAT NEXT

Run the specified command before using this option to get the intended results.

CMDS-112

CMDS-112 (Error) Found inconsistent supply voltage %g at pin %s (previously set %g by command %s).

DESCRIPTION

This error occurred because a different rail voltage has already been set on this pin, either in set_input_transition or set_model_input_transition_indexes.

WHAT NEXT

Check rail voltages value specified in set_input_transition and set_model_input_transition_indexes.

CMDS-113

CMDS-113 (warning) The command %s can only be run during multi-input switching analysis.

DESCRIPTION

Some features are only valid during multi-input switching analysis.

WHAT NEXT

Set the variable timing_enable_multi_input_switching to TRUE.

CMDS-114

CMDS-114 (Error) The set_delay_coefficients command must have either <trigger_objects> or -target <target_objects> specified.

DESCRIPTION

The **set_delay_coefficients** command must have either the trigger or target objects specified.

WHAT NEXT

Add one or both of the needed options to the command.

CMDS-115

CMDS-115 (Error) %s must be a list of nets connected to inputs, transistor gate pins, output ports, or model inputs.

DESCRIPTION

The **set_delay_coefficients** command can only be specified on trigger and target pins which are transistor inputs, model input pins, output ports, or nets that are connected to these inputs.

WHAT NEXT

Modify the syntax of the specified objects so that they only contain input pins or nets that are connected to input pins or output ports.

CMDS-116

CMDS-116 (Warning) No gate pins, output ports, or model input pins were found for net %s"

DESCRIPTION

When using nets as objects to the **set_delay_coefficients** command, only nets that are connected to transistor inputs, output ports, or model input pins are allowed.

WHAT NEXT

Modify the syntax of the specified objects to use only nets that are connected to transistor input pins, output ports, or model inputs.

CMDS-117

CMDS-117 (Warning) The number of transistors at register file net %s specified with the -transistors option %d is greater than %d.

DESCRIPTION

When marking a register file topology, only the transistors needed to simulate that specific topology should be included in the topology definition. The current number specified could lead to long simulation times and have a negative runtime impact.

WHAT NEXT

The attribute "transistors" can be accessed from the register file topology in order to see which devices have been included with the -transistors option. Look at this list and try to remove any devices not appropriate for this register file.

CMDS-118

CMDS-118 (Warning) The generated write_spice deck may not be accurate when the option -si_aggressors is omitted for the write_spice command and SI analysis is enabled.

DESCRIPTION

Some options to the command write_spice are required to ensure the accuracy of SI analysis results.

WHAT NEXT

Set the option -si_aggressors to the write_spice command.

DO NOT USE message relates to the deprecated option -si_aggressors

---

CMDS-119

CMDS-119 (Warning) The generated SPICE deck may not be accurate when the -no_si_aggressors option is used with the write_spice command and SI analysis is enabled.

DESCRIPTION

When SI analysis is enabled, a SPICE deck generated by the write_spice command includes any cross-coupling capacitors to nets within the scope of the specified objects, along with a driver on the aggressor side of each capacitor to represent the aggressor waveform. When the -no_si_aggressors option is used these aggressors are no longer represented in the SPICE deck and the subsequent simulated delay result for this deck may not correlate with the NanoTime result.

WHAT NEXT

Remove the -no_si_aggressors option to the write_spice command.

CMDS-120

CMDS-120 (Warning) %s will be made obsolete and removed from future releases of NanoTime starting with the %s release.

DESCRIPTION

The specified command, option or variable is in the process of being obsoleted and will not be supported in future releases of NanoTime.

WHAT NEXT

Check the command or variable man pages, product manuals, or release notes for more details about the obsolescence and to find out whether there are alternative approaches or replacements for this feature.

CMDS-121

CMDS-121 (Warning) Negative offset vector delays for a DDS stage were converted to zero or modified to post-switch values for the path being simulated.

DESCRIPTION

The simulation of DDS subckt stages is started at the trigger pin of that stage. If the DDS vectors for this stage have timing with earlier arrivals at other inputs, these arrivals cannot be simulated properly due to spice simulator limitations. If the side inputs are determined to have switched early enough, these side inputs are modified to be set to their fixed logic post-switch state. If not, offsets that should have been negative will be converted to zero.

WHAT NEXT

Look for warning messages within the write_spice output file. The VCVS statements in the file can be manually converted into a different waveform if necessary to resolve vector issues and improve accuracy.

CMDS-122

CMDS-122 (Error) Found %s rail voltage values associated with input transition settings at pin %s.

DESCRIPTION

This error occurred because there is an explicit setting of rail voltage value for either rise or fall input transitions through command set_input_transition that is either missing or incompatible with another one.

WHAT NEXT

Check rail voltage values specified in set_input_transition for either extra, missing, or incompatible options relative to one of the transitions (rise or fall).

CMDS-123

CMDS-123 (Error) Option %s must be accompanied by option %s.

DESCRIPTION

Differential override pin(s) must be specified for both clear and preset of a cross coupled differential net.

WHAT NEXT

Add the missing option and its value.

CMDS-124

CMDS-124 (Warning) When overriding differential behavior of net %s by switching at pin %s: %s; ignoring pin.

DESCRIPTION

The condition specified in the warning was not met for the given pin to be considered for overriding the differential behavior of the given net. The pin was therefore ignored.

WHAT NEXT

Resolve the failing condition.

CMDS-125

CMDS-125 (Error) When overriding differential behavior of net %s: %s.

DESCRIPTION

The condition specified in the error was not met for the given net to be considered for overriding its differential behavior.

WHAT NEXT

Resolve the failing condition.

CMDS-126

CMDS-126 (Warning) When erasing differential override pin %s for net %s: %s; ignoring pin.

DESCRIPTION

The condition specified in the warning was not met for the pin to be erased.

WHAT NEXT

Resolve the failing condition.

CMDS-127

CMDS-127 (Error) Options %s and %s must be accompanied by one of %s or %s.

DESCRIPTION

When differential override pins are specified, the clamp state must also be specified for the overridden differential net.

WHAT NEXT

Add the missing option.

CMDS-128

CMDS-128 (Error) Option %s or %s must be accompanied by options %s and %s.

DESCRIPTION

When differential clamp state is specified, differential override pins must also be specified for the differential net.

WHAT NEXT

Add the missing options.

CMDS-129

CMDS-129 (Error) When overriding differential behavior of net %s by switching at pin %s: %s.

DESCRIPTION

The condition specified in the error was not met for the given pin to be considered for overriding the differential behavior of the given net.

WHAT NEXT

Resolve the failing condition.

CMDS-130

CMDS-130 (Warning) When overriding differential behavior of net %s by switching at pin %s: %s.

DESCRIPTION

The condition specified in the warning is not common and needs to be checked.

WHAT NEXT

Check that the reported condition will not cause an issue.

CMDS-131

CMDS-131 (Error) Can't find installation of Library Compiler.

DESCRIPTION

When NanoTime reads a .lib file, NanoTime needs to invoke Synopsys Library Compiler. The Library Compiler executable is installed separately. This error indicates that NanoTime is unable to locate your Library Compiler installation.

WHAT NEXT

Set the SYNOPSYS_LC_ROOT environment variable to point to the directory where Library Compiler is installed. For example, if you set

```
setenv SYNOPSYS_LC_ROOT /remote/depot/lc
```

then NanoTime expects to find a Library Compiler shell script at /remote/depot/lc/bin/lc_shell. It also expects to find an executable under a machine-specific directory. For example, if you are using linux64, you should see this executable:

```
/remote/depot/lc/linux64/lc/lc_shell_exec
```

If you do not see this executable, check your installation.

CMDS-132

CMDS-132 (Error) At least two unique nets must be named.

DESCRIPTION

The set_lvs_equivalent_nets command requires at least two unique nets to be named.

WHAT NEXT

Modify the command to name pairs of nets to be made equivalent.

CMDS-133

CMDS-133 (Error) set_lvs_equivalent_nets command is incompatible with link_enable_wrapper_subckt_parasitics set to true.

DESCRIPTION

If the gvar link_enable_wrapper_subckt_parasitics is true, NanoTime processes parasitics when executing the link_design command. The set_lvs_equivalent_nets command must be issued after link_design but before any parasitics have been read in. The two modes of use are incompatible.

WHAT NEXT

Change the value of the gvar link_enable_wrapper_subckt_parasitics to false, or else eliminate the set_lvs_equivalent_nets command.

CMDS-134

CMDS-134 (Error) Design '%s' does not match the current design '%s'.

DESCRIPTION

A design named in the command did not match the design currently read into memory.

WHAT NEXT

Check the spelling of the design in the command. Check that the current design contains this design.

CMDS-135

CMDS-135 (Warning) Back-annotated RC parasitics skew is disabled on net %s, since an external simulator is used on this net.

DESCRIPTION

The back-annotated RC parasitics skew analysis, which is enabled by the set_enable_input_spf_skew command, is not supported by the external simulator.

WHAT NEXT

Remove the specific net from the set_enable_input_spf_skew command, or remove the spcific net from the set_simulator commnad.

CMDS-136

CMDS-136 (Warning) Command '%s' does not apply to %s '%s'.

DESCRIPTION

NanoTime could not apply the referenced command to the object named. This could occur because the command tried to remove an attribute from a group of nets, some of which did not have the attribute.

WHAT NEXT

As long as the object named was not expected to work with the referenced command, no action is required.

CMDS-137

CMDS-137 (Warning) Unable to find net '%s' or '%s' to create alias.

DESCRIPTION

NanoTime expects exactly one of the net names to exist in the design, so that the other name can be set up as an alias.

WHAT NEXT

Check if any back annotation errors refer to the reported net names, and modify the net combined report as needed.

CMDS-138

CMDS-138 (Warning) Unable to create alias because nets '%s' and '%s' were both found in the design.

DESCRIPTION

NanoTime expects exactly one of the net names to exist in the design, so that the other name can be set up as an alias. This net name pair will be ignored.

WHAT NEXT

Check if any back annotation errors refer to the reported net names, and modify the net combined report as needed.

CMDS-139

CMDS-139 (Warning) Unable to create alias because nets '%s' and '%s' have different hierarchical paths.

DESCRIPTION

NanoTime can only create an alias within a given subckt. This net name pair will be ignored.

WHAT NEXT

Check if any back annotation errors refer to the reported net names, and modify the net combined report as needed.

CMDS-140

CMDS-140 (Warning) The net combined report file uses a fixed '/' hierarchy separator, which differs from this NanoTime session setting. Some mappings may not be successful.

DESCRIPTION

The Calibre net combined report file has a hard-coded hierarhical separator of '/'. The current hierarchical separator for this session is different, so SPICE net or instance names that contain '/' will not be resolved correctly.

WHAT NEXT

Consider using 'set_hierarchy_separator "/"'

CMDS-141

CMDS-141 (Information) Found multiple declarations of a differential %s pair.

DESCRIPTION

NanoTime found multiple declarations of a differential pair. Arguments from the last declaration will be used.

WHAT NEXT

Check the arguments of the **set_differential** command.

CMDS-142

CMDS-142 (Error) Cannot use pin name %s since this conflicts with variable %s.

DESCRIPTION

NanoTime found one of the pin names conflicts with a pin name in another pin name list.

WHAT NEXT

Ensure the pin name lists are non-overlapping.

CMDS-143

CMDS-143 (Error) The pin list must contain exactly 2 pins.

DESCRIPTION

The pin list must contain exactly 2 pins.

WHAT NEXT

Confirm that the list contains 2 pins.

CMDS-144

CMDS-144 (Error) %s

DESCRIPTION

When timing_enable_slew_variation is set, variations, input_slopes, and transition_variations must be set, with equal length lists. The input_slopes values must be monotonically increasing positive values. The values for variations and transition_variations must be positive.

If timing_enable_slew_variation is not set, then only one variation value should be specified, and input_slopes and transition_variations are not allowed.

WHAT NEXT

Check the value of timing_enable_slew_variation and the options used for the set_variation_parameters command.

CMDS-145

CMDS-145 (Warning) Installing a %s timing check on a %s pin %s from pin %s.

DESCRIPTION

NanoTime provides the command **create_gate_clock_timing_check** to install intrace timing checks on gated clock circuits. This warning indicates that either this command was used on a non-gated clock circuit or **create_timing_check** was used on a gated clock circuit.

WHAT NEXT

Ensure that the command used matches the type of cricuit on which the timing check is installed.

CMDS-146

CMDS-146 (Warning) Transistor %s is not turned off by gate connection to a real rail.

DESCRIPTION

When marking a transistor to be excluded from clock propagation and topology recognition, it is expected that the transistor will be turned off by a netlist connection of its gate pin to an appropriate real rail.

WHAT NEXT

Check the connectivity of the transistor identified for the marking.

CMDS-147

CMDS-147 (Error) id %s is expected to have only %d levels..

DESCRIPTION

When using the **report_stage** command, there is a set depth of ID hierarchy.

WHAT NEXT

Make sure you select the right arc number. Check your report_paths -show_stage_id output and make sure you don't have too many slashes.

CMDS-148

CMDS-148 (Error) id %s should take the following form [DNI]\N+/\N+.

DESCRIPTION

When using the **report_stage** command, a stage ID has a prefix D, N or I indicating delay, noise or debug info, respectively. The suffix is followed by a numerical path to the relevant data, delimited by forward-slash. Example: D1/3 is the 4th stage of path ID 1.

WHAT NEXT

Check your reporting command with -show_stage_id .

CMDS-149

CMDS-149 (Error) Arc %d and/or path %d do not exist or missing data.

DESCRIPTION

When using the **report_stage** command, both path ID and arc ID need to point to existing data.

WHAT NEXT

A stage ID is of the following format: D<path ID>/<arc ID>. Check your report_paths -show_stage_id output.

DCS Error Messages

DCS-001

DCS-001 (warning) Waveform generated for undefined side input %s, which may have performance impact and/or result in incorrect output waveforms.

DESCRIPTION

DCS will generated waveform for undefined side input to the clock network, which will cover different states of the side input. This will make the simulation time longer and may result in incorrect output waveforms due to the possible invalid states of the side inputs.

WHAT NEXT

Check to see that the clocks are being propagated correctly and all clock gating structures are marked.

DCS-002

DCS-002 (warning) Found a ccb of clock net %s together with a non-clock net %s, please make sure all clocks are propagated correctly.

DESCRIPTION

A ccb inside the clock network should have all the nets marked as clocks in most cases, if not, it may result in inaccurate simulation.

WHAT NEXT

Check to see that the clocks are being propagated correctly.

DCS-003

DCS-003 (warning) No clock arrival on clock node %s.

DESCRIPTION

There is no clock arrival (delay & slope) coming out from simulation for the clock node.

WHAT NEXT

Check to see if the clock network are built up correctly.

DCS-004

DCS-004 (warning) A generated clock is specified on a pin of net %s, however not on all gate pins of this net, which may cause incorrect clock waveforms.

DESCRIPTION

A generated clock should be propagated through all gate pins of a net. If some of the gate pins are not marked, path tracing may not be able to propagate clock waveforms through the unmarked gate pins.

WHAT NEXT

Check to see if all gate pins of the generated clock net are specified in the create_generated_clock command.

DCS-005

DCS-005 (error) Cannot identify the ground node for DCS/DDS simulation. Please make sure ground node is defined in the netlist. Exiting...

DESCRIPTION

Cannot identify the ground node for DCS/DDS simulation.

WHAT NEXT

Make sure ground node is defined in the netlist.

DCS-006

DCS-006 (error) DCS cannot be used in the presence of ideal clocks.

DESCRIPTION

Ideal clocks specify waveforms at the clock end-points.

WHAT NEXT

To use DCS, make sure that ideal clocks are not specified.

DCS-007

DCS-007 (error) Source pin %s for generated clock %s can not be within a DCS region.

DESCRIPTION

Generated clock source pins must be pins which become timing points of the timing graph. Internal pins within a DCS region should not be used.

WHAT NEXT

Modify the generated clock definition such that the source pin is also a start pin of a non-generated clock definition.

DCS-009

DCS-009 (warning) DCS clock transitions %g (rise) %g (fall) are too slow for clockwave form high pulse =%g low pulse =%g, resetting

DESCRIPTION

When using DCS simulation for a clock waveform the transition times must be fast enough to allow complete switching before the end of a high and low clock pulse.

WHAT NEXT

Reset the clock input transition points to smaller values using the command set_model_input_transition_indexes or the variable model_default_input_transition_indexes.

DCS-010

DCS-010 (error) The number of side inputs exceeds the maximum of 10 for a DCS region.

DESCRIPTION

Dynamic clock simulation generates a waveform for undefined side inputs to the clock network, which covers different states of the side input.

This error message occurs when the number of side inputs is large, causing excessive simulation time and memory usage.

WHAT NEXT

Verify that the clocks are being propagated correctly and that all clock-gating structures are marked. For example,

- If these side inputs drive some channel-connected blocks (CCBs), check if these CCBs should be clock-gate structures. If yes, verify that the clock-gate structures are correctly marked or automatically recognized.
- If these side inputs should be clock nets, verify that they are recognized as clock nets. If not, find out why clock propagation does not reach the net.
- Check if there are **mark_clock_network -force_propagation** commands that incorrectly force some nets be clock nets.

SEE ALSO

`dcs_enable_analysis(3)`

DCS-011

DCS-011 (Error) Found no input for the DCS region.

DESCRIPTION

NanoTime cannot identify the input for the DCS region.

WHAT NEXT

Check the port directions to see if the clock ports get correct direction settings. Use **report_port** to check the port direction. Use **set_port_direction** to set the port direction.

DCS-012

DCS-012 (warning) Case analysis setting %s conflicts with DCS side input logic settings: use case

analysis setting %s on net %s for DCS simulation.

DESCRIPTION

Conflict logic states have been set by "set_dcs_input" and "set_case_analysis". The value set by "set_case_analysis" wins.

WHAT NEXT

First check whether "set_dcs_input" and "set_case_analysis" commands are correctly set. Then check to see if clocks are being propagated correctly.

DCS-013

DCS-013 (error) DCS side input logic setting %s conflicts with previous DCS side input logic setting : unable to set net %s to DCS logic %s.

DESCRIPTION

Conflict logic states have been set by multiple "set_dcs_input", the one that comes first succeeds and the later ones fail.

WHAT NEXT

Firstly, remove unwanted logic values by using "remove_dcs_input". Secondly, check to see if clocks are being propagated correctly.

DCS-014

DCS-014 (error) Net %s cannot be marked as a synchronized data net.

DESCRIPTION

A synchronized data input is a non-clock signal that feeds into a channel-connected block (CCB) whose output is a clock signal. It is also a side input signal of the DCS region. The current definition contains a pin connected to a clock net and is therefore an error.

WHAT NEXT

Check the clock definitions. Check the pin(s) selected for use as synchronized data inputs.

DCS-015

DCS-015 (error) The synchronized data input at pin %s cannot have equal rise and fall arrival times of %g.

DESCRIPTION

A synchronized data input is a non-clock signal that defines a side input signal of the DCS region. The arrival times of this input must be periodic i.e. defined as relative to a defined clock. The rise and fall arrival times must also define a clock-like waveform that has a non-zero pulsewidth. If the arrival times occur after the first clock cycle completes then they will be cycle adjusted back until they occur within the first clock cycle. In this case either the original rise and fall times are equal or the cycle adjusted rise and fall times are equal and do not define a valid clock-like waveform.

WHAT NEXT

Look at the incoming paths to the synchronized data points. If they come from an input port then look at the input delays defined at that port and make sure that the rise and fall values define a valid clock-like waveform.

DCS-016

DCS-016 (error) The synchronized data input at pin %s does not have valid periodic arrival times.

DESCRIPTION

A synchronized data input is a non-clock signal that defines a side input signal of the DCS region. The arrival times of this input must be periodic i.e. defined as relative to a defined clock. The arrival times at this input are not relative to a clock definition and cannot be used as a synchronized data input.

WHAT NEXT

Look at the incoming paths to the synchronized data points. If they come from an input port then make sure that the input definitions are defined as a function of a clock.

DCS-017

DCS-017 (error) Net %s is not an input to the DCS region and therefore cannot be a synchronized data net.

DESCRIPTION

A synchronized data input is a non-clock signal that feeds into a channel-connected block (CCB) whose output is a clock signal. It must be a side input to the DCS region. The net specified is not an input to the DCS region. This could be caused by limiting the DCS region with the mark_instance -exclude_from_dcs or mark_clock_network -end_dcs commands.

WHAT NEXT

Check for commands limiting the DCS region. Also, check to see if the set_dcs_input -synchronized_data command is specified correctly.

DCS-018

DCS-018 (warning) There is no simulatable element in the clock network.

DESCRIPTION

The dynamic clock simulation region has no simulatable element. Dynamic clock simulation is disabled for the clock simulation.

WHAT NEXT

Check if the clock network is correctly configured.

DCS-019

DCS-019 (warning) Incompatible settings: dcs_enable_internal_coupling_caps false for si_enable_analysis true together with dcs_enable_si_analysis true.

DESCRIPTION

For accurate SI delay analysis of the DCS region, coupling caps internal to the DCS region must be retained. Setting dcs_enable_internal_coupling_caps to true.

WHAT NEXT

Check the tcl setup file for incorrect setting of dcs_enable_internal_coupling_caps.

DCS-020

DCS-020 (warning) Detected multiple logic constraints for side input '%s'. Only one logic constraint will be honored featuring this side input, which may lead to pessimistic results.

DESCRIPTION

When variable **dcs_honor_side_input_logic_constraints** is set true, DCS will detect when enable conditions cannot be met due to logic constraints among the side inputs. If a side input is detected in more than one group of logic constraints, this warning will be issued because only one logic constraint group featuring this side input will be honored. This limitation is needed to keep the run time of DCS reasonable.

WHAT NEXT

Use **set_dcs_input -logic <0,1>** command, if feasible, to force the logic on the multi-constrained side input and release it from consideration among the multiple logic constraints.

DCS-021

DCS-021 (warning) Some logic constraints among DCS side input enables have been ignored to reasonably bound the simulation duration.

DESCRIPTION

Dynamic clock simulation (DCS) generates pulse waveforms for logically constrained side input enables that respect the logic relationships among constrained side inputs. This warning occurs when the number of constraints is likely to extend the simulation period beyond a reasonable limit, causing excessive simulation time and memory usage. The extended simulation period upper bound is based on the limit (10 by default) to the number of undefined side inputs tolerated for which waveforms are generated.

Since some logic constraints are ignored, the DCS simulation might yield pessimistic results due to infeasible combinations of side input enables.

WHAT NEXT

Verify that the logic constraints among side input enables are being set correctly using the **report_logic_constraint** command. If the settings look correct, use the **set_dcs_input -logic <0,1>** command, if feasible, to force the logic on side inputs and reduce the number of constraints considered with the **dcs_honor_side_input_logic_constraints** variable.

SEE ALSO

```
set_dcs_input(2)
report_logic_constraint(2)
```

DCS-022

DCS-022 (error) Cell '%s' used by instance '%s' has no transistor model. DCS region cannot be simulated.

DESCRIPTION

Dynamic clock simulation (DCS) requires all cells to have a transistor-level view. This error happens when a cell inside the DCS region is associated with a library and not with a spice level representation. Without a spice model it is not possible to simulate the cell inside the DCS region.

WHAT NEXT

Verify that all cells have a transistor level in the input spice file. Certify that **link_prefer_model_port** is not forcing library models to take precedence over the spice model for cells inside the DCS region.

DDS Error Messages

DDS-001

DDS-001 (warning) The net \"%s\" in \"mark_simulation -force_group\" is not adjacent to CCBs of other nets in the command. CCB grouping ignored.

DESCRIPTION

"mark_simulation -force_group" is used to group CCBs into one DDS region, which requires all nets to be in adjacent CCBs. If any net is found to be not adjacent to CCBs of other nets in the command, such grouping will be ignored.

WHAT NEXT

Make sure the nets specified in the "mark_simulation -force_group" command are in adjacent CCBs.

DDS-002

DDS-002 (warning) Failed to get delay from pin %s (net %s) %s to net %s of DDS block using default vectors.

DESCRIPTION

Outputs fail to switch for specified input switching direction.

WHAT NEXT

Look at the DDS block between the two pins (nets) and see if it can achieve a full-rail transition. Use **report_cell** to look at the transistor models bound to the cells in this part of the design. Make sure the equivalent transistor models were bound to the cell. The NanoTime transistor matching function could be using an incorrect transistor model. For some DDS regions not all input to output combinations are possible. See the variables **tech_match_***.

DDS-003

DDS-003 (warning) Failed to get delay from pin %s (net %s) edge %s to net %s of DDS block using user defined vectors.

DESCRIPTION

Outputs fail to switch for specified input switching direction.

WHAT NEXT

Look at the DDS block between the two pins (nets) and see if it can achieve a full-rail transition. Use **report_cell** to look at the transistor models bound to the cells in this part of the design. Make sure the equivalent transistor models were bound to the cell. The NanoTime transistor matching function could be using an incorrect transistor model. For some DDS regions not all input to output combinations are possible. See the variables **tech_match_***.

DDS-004

DDS-004 (Error) Found %d non-contiguous sub-regions.

DESCRIPTION

The nets used to define the dynamic delay simulation (DDS) region enumerate a set of channel-connected regions that are not contiguous.

WHAT NEXT

Check the nets which are being used and either (1) add additional nets to include enough channel-connected regions to make them all contiguous, or (2) change the original set of nets being used.

DDS-005

DDS-005 (Error) Net %s is already part of DDS region %d.

DESCRIPTION

A net can only be part of one dynamic delay simulation (DDS) region. The specified net is already included in a previously defined DDS region, therefore the new DDS definition is ignored.

WHAT NEXT

Look at previously defined regions using the **report_simulation -verbose** command to determine where the overlap occurs.

DDS-006

DDS-006 (Information) Created DDS region number %d from %d unique channel connected blocks.

DESCRIPTION

The dynamic delay simulation (DDS) region has been successfully created.

WHAT NEXT

Information only; no further action is needed.

DDS-007

DDS-007 (Warning) DDS region input net %s is the inversion of region input net %s.

DESCRIPTION

The listed nets are inverted logic signals but the channel connected block between them was not added to the region because that block had other inputs.

WHAT NEXT

The inverted signal could be added to the region definition. Vectors could be added to reflect the dependency between these two nets.

DDS-008

DDS-008 (Error) Number of side inputs %d exceeds maximum of %d for a mark_simulation region

DESCRIPTION

When using mark_simulation to create a region for simulation with DDS the defined region will have a number of non-controlling side inputs. These inputs must have vectors applied to them for each possible

combination of values. When the number of side inputs is large, the simulation time and memory usage can become excessive.

WHAT NEXT

The simulation region can be redefined in a way that has less side inputs or the option -max_inputs can be used to override the default limit. When using this override it is important to also use set_simulation_attributes to define a vector set of reasonable size for use when this region is simulated.

DDS-009

DDS-009 (Error) DDS region contains latch net %s

DESCRIPTION

DDS regions are not allowed to contain latch nets.

WHAT NEXT

Either redefined the DDS region or remove the latch topology.

DDS-010

DDS-010 (Warning) No vectors matched for DDS region.

DESCRIPTION

The vectors specified for the dynamic delay simulation (DDS) region must specify values for all inputs of the region and match at least one output.

WHAT NEXT

Use the **report_simulation -template** command to generate a default vector file and indicate all the needed inputs.

DDS-011

DDS-011 (Error) Options section specifying min/max is missing, vectors will be ignored.

DESCRIPTION

When specifying DDS vectors the options section must be used to specify if they are for min delays, max delays, or both.

WHAT NEXT

Use the **report_simulation -template** command to generate a default vector file that includes an options section for reference.

DDS-012

DDS-012 (Warning) Unknown keyword "%s" found in vector file.

DESCRIPTION

The DDS vector file has a predefined set of keywords that are recognized. The input file contains some unknown or illegal syntax.

WHAT NEXT

Use the **report_simulation -template** command to generate a default vector file that includes example syntax.

DDS-013

DDS-013 (Error) Found no input for a mark_simulation region.

DESCRIPTION

NanoTime cannot identify inputs for the dynamic delay simulation (DDS) region defined by the **mark_simulation** command.

WHAT NEXT

Check the port directions to see if the ports connecting to the DDS region have the correct direction settings. Use the **report_port** command to check the port direction. Use the **set_port_direction** command to set the port direction.

DDS-014

DDS-014 (Warning) Dangling input is found at following net: %s

DESCRIPTION

The dynamic delay simulation block has a dangling input net without a driver.

WHAT NEXT

SPICE simulation will run with that input dangling. Check the original design for that net, make sure there is driver for that net.

DDS-015

DDS-015 (Error) The total number of inputs %d exceeds the allowed maximum of %d for a mark_simulation region. The first excess input net is %s.

DESCRIPTION

When using mark_simulation to create a region for simulation with DDS the defined region will have a number of non-controlling side inputs. These inputs must have vectors applied to them for each possible combination of values. When the number of side inputs is large, the simulation time and memory usage can become excessive.

WHAT NEXT

The simulation region can be redefined in a way that has fewer side inputs.

DDS-016

DDS-016 (Error) The total number of non-constant inputs %d exceeds the allowed maximum of %d for a mark_simulation region. An excess non-constant input net is %s.

DESCRIPTION

When using mark_simulation to create a region for simulation with DDS the defined region will have a number of non-controlling side inputs. Non-constant inputs must have vectors applied to them for each possible combination of values. When the number of non-constant side inputs is large, the simulation time

and memory usage can become excessive.

WHAT NEXT

The simulation region can be redefined in a way that has fewer side inputs, or more of the side inputs can be forced to logical constants with set_case_analysis, or the DDS vectors can be overridden manually.

DDS-017

DDS-017 (warning) Failed to get DDS delay from pin '%s' (net '%s') %s with full transition time of %gps to net(s)%s, unable to trace further.

DESCRIPTION

The dynamic delay simulation (DDS) delay calculation does not have any switching outputs.

WHAT NEXT

Use the **report_simulation** command to examine the DDS simulation region configuration. Determine if this condition is expected or not.

Some edges of some inputs might not cause outputs to switch. Some vectors might not be used due to logic constraints or logic settings at the time of the simulation.

DDS-018

DDS-018 (Error) Could not find %s net "%s" while reading vector file.

DESCRIPTION

The DDS vector contains signal or output net names that are not recognized.

WHAT NEXT

Use the **report_simulation -template** command to generate a default vector file that includes the correct signal and output names for this simulation.

DDS-019

DDS-019 (Error) Ignoring vector "%s". Number of vector signals %d does not equal the number of defined signals %d.

DESCRIPTION

The number of logic values for a vector in the Vectors section of vector file does not match the number of signal nets defined earlier in the vector file.

WHAT NEXT

Confirm that the number of entries in each vector line matches the number of input signal nets. Use the **report_simulation -template** command to generate a default vector file to determine the correct names for signal and output nets.

DDS-020

DDS-020 (Warning) %s Initial Condition setting for net %s has inconsistent voltage %g, supply range for this net is %g to %g.

DESCRIPTION

The Initial Condition values for DDS vectors are typically set to the positive supply voltage value or zero. The current value does not meet this expectation.

WHAT NEXT

Check the Initial Condition setting value for this net to be sure it is the intended value. The Initial Condition values are not logic settings, they are voltage values.

DDS-021

DDS-021 (Error) Bad value '%s' for initial condition, this vector will be ignored.

DESCRIPTION

The Initial Condition values for DDS vectors must be floating point values or the names of supply nets. Any other value will be ignored and the initial condition set containing the bad value will be ignored.

WHAT NEXT

Check the Initial Condition syntax in the user defined vector file. Check the values of the variables link_vdd_alias and link_gnd_alias for correct supply names.

DELC Error Messages

DELC-001

DELC-001 (warning) A transistor stack of more than %d transistors at element %s will be ignored for the purpose of finding stage delay arcs.

DESCRIPTION

A limit has been placed on the number of transistors through which the tool will search when trying to find a path from power or ground to a signal node. The given design contains one or more series of channel-connected transistors that contain more transistors than this limit.

WHAT NEXT

Check the transistor direction settings for possible false paths. The limit can be set to a different value by setting the **transistor_stack_height_limit** variable.

DELC-002

DELC-002 (Error) Stack with %d or more transistors with unresolved directions has been found (element %s stack %s). Use strict transistor direction checking flow to correctly analyze the circuit.

DESCRIPTION

A limit has been placed upon the number of transistors with unresolved directions through which the tool will search when trying to find a path from power or ground to a signal node. The given design contains one or more series of channel-connected transistors that contain more transistors with unresolved directions than this limit.

WHAT NEXT

Check the transistor direction settings for possible false paths. The limit can be set to a different value by setting the **transistor_stack_bidirectional_limit** variable.

DELC-003

DELC-003 (warning) Failed to get delay from pin %s (net %s) edge %s to pin %s (net %s) edge %s, unable to trace further.

DESCRIPTION

NanoTime was unable to calculate the delay between the two pins.

WHAT NEXT

Look at the design between the two pins (nets) and see if it can achieve a full-rail transition. Use **report_cell** to look at the transistor models bound to the cells in this part of the design. Make sure the equivalent transistor models were bound to the cell. The NanoTime transistor matching function could be using an incorrect transistor model. See the variables **tech_match_***.

DELC-004

DELC-004 (warning) Simulator Warning: Net %s failed to switch.

DESCRIPTION

NanoTime found that the net did not switch correctly during simulation.

WHAT NEXT

Check the circuit for glitch conditions and for sufficient drive strength on the net.

DELC-005

DELC-005 (warning) Simulator Warning: Net %s has nonlinear waveform.

DESCRIPTION

NanoTime found that the transition waveform is not a linear ramp.

WHAT NEXT

Setting nonlinear waveform analysis for this net using the **set_nonlinear_waveform** command will improve the simulation accuracy.

DELC-006

DELC-006 (Error) Dynamic clock simulation failed to create %s delays.

DESCRIPTION

The dynamic clock simulation did not produce the required information.

WHAT NEXT

Look for other associated error messages to help diagnose the problem.

DELC-007

DELC-007 (warning) Simulator Warning: A transition on net %s failed to switch rail-to-rail.

DESCRIPTION

NanoTime found that the net did not switch from rail to rail during simulation.

WHAT NEXT

Check the circuit for glitch conditions and for sufficient drive strength on the net. Consider the possibility that more than one transition might occur on a net during a simulation.

DELC-008

DELC-008 (warning) Simulator Warning: Watch net %s logic state cannot be determined.

DESCRIPTION

NanoTime found that based on the current topology configuration, the watch net's logic state could not be determined. This net is no longer considered a watch net for further analysis.

WHAT NEXT

Check the topology associated with the net and make sure it is valid.

DELC-009

DELC-009 (warning) Feedforward device %s controlled by net %s can not be turned off.

DESCRIPTION

Due to case analysis settings or logic constraints, the listed device is forced to be on and will be on during simulation of the stage that includes it.

WHAT NEXT

Verify that the logic settings or case analysis statements are correct and that this device should always be turned on.

DELC-010

DELC-010 (warning) Using %s single corner simulation for multi-corner path %u due to device model encryption.

DESCRIPTION

Due to the presence of encrypted device models, multi-corner paths will be simulated using its dominant technology corner.

WHAT NEXT

Verify that the technology corners encountered by the path are correct.

DELC-011

DELC-011 (error) %s as the %s simulator does not support the tech file flow.

DESCRIPTION

Not all simulators support DCS/DDS flows with tech files.

WHAT NEXT

Check if NanoSim can be used instead.

DELC-012

DELC-012 (error) %s as the %s simulator requires a spice header file to be specified when using TMI2 spice models.

DESCRIPTION

Some simulators require the user to specify a spice header file when TMI2 spice models are used.

WHAT NEXT

Specify a spice header file.

DELC-013

DELC-013 (error) %s as the %s simulator does not support encrypted device models.

DESCRIPTION

Not all simulators currently support encrypted netlists or device models.

WHAT NEXT

Provide unencrypted device models.

DELC-100

DELC-100 (Error) External simulator setup: %s

DESCRIPTION

An error occurred while setting up the files needed to run an external simulator.

WHAT NEXT

Check if the external simulator path exists.

Based on the information in the message, check for error conditions such as a lack of write permission in the directory or a full disk.

DELC-101

DELC-101 (Information) Launching external simulator with command line '%s'

DESCRIPTION

An external simulator has been launched with the shown command line.

WHAT NEXT

No action is required by the user.

DELC-102

DELC-102 (Error) External simulator results: %s

DESCRIPTION

An error occurred while reading back results from an external simulator.

WHAT NEXT

The external simulator might have failed due to bad setup (e.g., licensing), bad input, or bad configuration commands. Check the log file and error files generated by the external simulator in the run directory indicated in the message.

DELC-103

DELC-103 (warning) Simulator Warning: Net %s final voltage %f is not within 5%% of rail (supply voltage %f).

DESCRIPTION

NanoTime found that the net did not switch from rail to rail during simulation.

WHAT NEXT

Check the circuit for glitch conditions and for sufficient drive strength on the net.

DELC-104

DELC-104 (warning) The ratio %.1f of full transition time %.3f ps at pin %s (net %s) to the delay %.3f ps to net %s exceeds the user specified ratio %.1f.

DESCRIPTION

A large transition time to delay ratio could indicate incorrect port settings or design issues. The units for the transition time and delay are picoseconds, not user time units. This is a customizable design rule check that will be useful to ensure that input transitions keep pace with process migrations.

WHAT NEXT

Check the port settings or other issues that can create large transition times.

DELC-105

DELC-105 (warning) The ratio %.1f of full transition time %.3f ps at pin %s to the default transition time %.3f ps exceeds the user specified ratio %.1f.

DESCRIPTION

A large transition time could indicate incorrect port settings or design issues. The units for the transition times are picoseconds, not user time units.

WHAT NEXT

Check the port settings or other issues that can create large transition times.

DELC-106

DELC-106 (Warning) Allowing %d or more bidirectional transistors in a stack %s may cause false paths and increased runtime.

DESCRIPTION

The tool has searched through two or more bidirectional transistors when it tries to find a path from power or ground to a signal node.

WHAT NEXT

Check the transistor direction settings for possible false paths.

DELC-107

DELC-107 (Warning) Path %d can not be simulated using HSPICE. It will not be recalibrated.

DESCRIPTION

The path might contain timing model, clock network, or other types of arcs that cannot be simulated.

WHAT NEXT

Check the path SPICE deck for more details.

DELC-108

DELC-108 (Information) Total number of HSPICE runs %d, completed %d, running %d, pending %d.

DESCRIPTION

This message report the status of parallel HSPICE runs.

WHAT NEXT

No action is required by the user.

DELC-109

DELC-109 (Warning) Timing model index out of range for cell %s at instance %s for %s :%s.

DESCRIPTION

When an index is outside the characterization range of input slope and/or output load for a model instance, it can adversely impact the accuracy of timing analysis. If SI analysis is enabled, the max effective load driven by the model instance should include 3x the coupling capacitance expected on the driven net. The min effective load should include -1x the expected coupling capacitance with a floor of zero for the total capacitance.

WHAT NEXT

First, check that the units are correct. Then, check if the cell is correctly instantiated in the design.

Another option is to re-generate the timing model with modified slope and/or load ranges.

DELC-110

DELC-110 (warning) The difference between the rail voltage %g of the trigger transition at pin %s and the voltage %g of the model library is larger than %g.

DESCRIPTION

NanoTime does not support scaling the delay when the library has a different voltage than the rail voltage used for the trigger transition.

WHAT NEXT

Check the voltage settings and modify them if they are incorrect. Use the **lib_voltage_mismatch_tolerance** variable to waive this warning.

DELC-111

DELC-111 (Error) Simulator does not support this type of analysis: %s.

DESCRIPTION

Simulator does not support the given type of analysis.

WHAT NEXT

This analysis type is not supported by the selected simulator, change simulator or remove this analysis from the input.

DELC-112

DELC-112 (Error) No technology setup for external simulation using %s.

DESCRIPTION

External simulation SPICE decks require that the **set_technology** command be used to define the technology header files.

WHAT NEXT

Use the **read_spice_model** and **set_technology** commands to define the technology header files.

DELC-113

DELC-113 (Warning) Fanout glitch not due to injection noise (at net %s) detected for fanout net %s.

DESCRIPTION

A spurious fanout glitch was detected before the injection noise was applied.

WHAT NEXT

Use **write_spice** with **-fanout -fanout_net** to investigate the fanout stage.

DELC-114

DELC-114 (Information) %s simulation failed to get delay; %s %s simulation deck to file %s.

DESCRIPTION

Simulation failures can arise from incorrect tool configuration or circuit design. It could also be normal circuit response to the applied stimulus.

WHAT NEXT

Inspect and verify the written simulation deck.

DELC-115

DELC-115 (Information) %s simulation(s) failed to get delay; %s %s simulation deck to file %s.

DESCRIPTION

Simulation failures can arise from incorrect tool configuration or circuit design. It could also be normal circuit response to the applied stimulus. Some of the simulations may involve the use of data sweeps. In these scenarios the simulation deck will only capture the stimulus from one of the sweeps.

WHAT NEXT

Inspect and verify the written simulation deck.

DELC-116

DELC-116 (Information) %s simulation(s) failed to get delay; maximum simulation deck write count exceeded.

DESCRIPTION

Simulation failures can arise from incorrect tool configuration or circuit design. It could also be normal circuit response to the applied stimulus.

WHAT NEXT

Check the tool setup and correctness of data provided.

DELC-117

DELC-117 (Error) Invalid value '%s' for variable %s.

DESCRIPTION

The user variables dcs_simulator and dds_simulator can accept only one of the following values: 'nanosim', 'finesim'.

WHAT NEXT

Check the value set for the variable.

DELC-118

DELC-118 (warning) Discarding incomplete %s output waveform; simulation time %g ns.

DESCRIPTION

Output waveform did not switch from rail to rail. This could be due to insufficient simulation time.

WHAT NEXT

Try increasing the simulation time.

DELC-119

DELC-119 (Information) %s DDS %s simulation deck to file %s.

DESCRIPTION

Informational message to indicate that a simulation deck was (not) saved for inspection.

Some of the simulations may involve the use of data sweeps. In these scenarios the simulation deck will only capture the stimulus from one of the sweeps.

WHAT NEXT

Inspect and verify the simulation deck if written.

DELC-120

DELC-120 (Information) %s DCS %s simulation deck to file %s.

DESCRIPTION

Informational message to indicate that a simulation deck was (not) saved for inspection.

WHAT NEXT

Inspect and verify the simulation deck if written.

DELC-121

DELC-121 (Warning) Multi-voltage clock network is not well-suited for the current capabilities of DCS.

DESCRIPTION

NanoTime detected multiple supply voltages within the clock network. The results might be affected if the boundary nets of the clock network do not have the same voltage or detailed path reporting is enabled.

WHAT NEXT

Select an appropriate delay calculation approach.

DELC-122

DELC-122 (Error) %s simulator has encountered an error: %s.

DESCRIPTION

This message indicates that an unexpected error occurred during simulation. This could be due to tool setup issues or problems in the data provided.

WHAT NEXT

Check the tool setup and correctness of data provided.

DELC-123

DELC-123 (Warning) %s is not marked %s.

DESCRIPTION

This operation attempts to unset a victim or aggressor net status that has not been previously set.

WHAT NEXT

Check your scripts for the appropriate **set_si_delay_analysis** and **remove_si_delay_analysis** command settings.

DELC-125

DELC-125 (Information) Found %d floating transistor bulk connections.

DESCRIPTION

This message indicates that NanoTime found one or more transistors with floating bulk connections. Such connections can affect the accuracy of simulation results.

WHAT NEXT

Check the tool setup and correctness of data provided.

DELC-126

DELC-126 (Warning) Could not compute %s fanout noise at net %s due to injection noise at net %s

DESCRIPTION

NanoTime internal noise validation failed for the computed fanout noise.

WHAT NEXT

Check the circuit topology and user set_case_analysis commands impacting the fanout cluster.

DELC-127

DELC-127 (Warning) Net %s driven by timing model also has channel connection to transistor %s.

DESCRIPTION

NanoTime does not support channel connected transistors on nets driven by timing models. The hybrid net may have other channel connected transistors than the one reported.

WHAT NEXT

Remove channel connected transistors from any net driven by a timing model.

DELC-129

DELC-129 (Error) Could not simulate delay from pin '%s' %s (net '%s'). Stage side input '%s' has unknown logic state.

DESCRIPTION

NanoTime was unable to calculate the delay due to missing side input logic settings.

WHAT NEXT

Look at the design related to this stage input and ensure its logic is set properly.

DELC-130

DELC-130 (Error) Could not compute noise at net '%s'. Stage side input '%s' has unknown logic state.

DESCRIPTION

NanoTime was unable to calculate the noise due to missing side input logic settings.

WHAT NEXT

Look at the design related to this stage input and ensure its logic is set properly.

DELC-131

DELC-131 (Information) Embedded FineSim will be used as default simulator, since the design uses MOS level 76 technologies.

DESCRIPTION

This design has transistors with level 76 models. NanoTime automaticlly selects FineSim as its default simulator.

WHAT NEXT

No action is required by the user.

DELC-132

DELC-132 (Warning) No technology setup for external simulation using %s. Simulation speed will be affected.

DESCRIPTION

In order to simulate the SPICE decks efficiently, external simulation SPICE decks require that the **read_spice_model** and **set_technology** command be used to define the technology header files.

If the **set_technology** command is not used, the technology files may end up loaded multiple times while

simulating SPICE decks with external simulators.

WHAT NEXT

Use the **read_spice_model** and **set_technology** commands to define the technology header files.

DELC-133

DELC-133 (Warning) Could not compute %s injected noise at net %s due to absence of %s %s drive resistance.

DESCRIPTION

NanoTime internal noise validation failed to compute injected noise.

WHAT NEXT

Use command **set_drive_resistance** to specify the driving resistance for the net.

DELC-135

DELC-135 (Information) Using FineSim Embedded for net %s.

DESCRIPTION

FineSim Embedded simulator is used for analysis of the given net.

WHAT NEXT

No action is required by the user.

DELC-136

DELC-136 (Information) Using threshold voltage %g volts for turn off delay of transistor %s.

DESCRIPTION

Reports the threshold voltage used for turn off delay of a given transistor.

WHAT NEXT

No action is required by the user.

DELC-137

DELC-137 (Warning) Unable to configure differential cross coupled output nets %s and %s for variation analysis.

DESCRIPTION

NanoTime could not create the simulation unit necessary for accurate variation analysis of the differential cross coupled circuit.

WHAT NEXT

Check the markings of the differential cross coupled output nets.

DISP Error Messages

DISP-001

DISP-001 (Information) Starting distributed processing pre-testing.

DESCRIPTION

NanoTime performs pre-testing for distributed processing when a host file is specified.

WHAT NEXT

If the pre-testing fails, check error messages and fix user settings and the distributed processing host file.

DISP-002

DISP-002 (Information) Distributed processing pre-testing finished successfully.

DESCRIPTION

NanoTime performs pre-testing for distributed processing and it is successful.

WHAT NEXT

No action is required by the user.

DISP-003

DISP-003 (Error) Distributed processing pre-testing failed. Check the message from your farm: %s

DESCRIPTION

NanoTime performs pre-testing for distributed processing and it failed.

WHAT NEXT

Check error messages and fix user settings and distributed processing host file.

DISP-004

DISP-004 (Error) Distributed processing failed: %s.

DESCRIPTION

NanoTime distributed processing failed due to unexpected errors.

WHAT NEXT

Check distributed processing log file and fix the error.

DISP-005

DISP-005 (Information) Total number of runs %d, completed %d, running %d, pending %d.

DESCRIPTION

Reports the status of external runs.

WHAT NEXT

No action is required by the user.

DISP-006

DISP-006 (Warning) Total number of job submissions reached the maximum %d.

DESCRIPTION

The total number of job submissions reached the maximum value. The remaining submissions will be ignored.

WHAT NEXT

Check the maximum allowed number of runs defined by write_spice_sim_max**.**

DISP-007

DISP-007 (Information) There are %d external runs.

DESCRIPTION

Reports the number of external runs.

WHAT NEXT

No action is required by the user.

DISP-008

DISP-008 (Warning) No external command is defined for distributed processing.

DESCRIPTION

When you execute the **write_spice -simulate** command, NanoTime checks the **write_spice_sim_cmd**, **write_spice_sim_pre_processing**, and **write_spice_sim_post_processing** variables. NanoTime issues this warning message when all three variables are empty. If all three variables are empty, the **-simulate** option of the **write_spice** command has no effect.

WHAT NEXT

Check the **write_spice_sim_cmd**, **write_spice_sim_pre_processing**, and **write_spice_sim_post_processing** variables.

DISP-009

DISP-009 (Error) External environment: %s

DESCRIPTION

An error occurred while setting up the files needed to run an external command.

WHAT NEXT

Check if the external command path exists.

Based on the information in the message, check for error conditions such as a lack of write permission in the directory or a full disk.

DISP-010

DISP-010 (Information) Launching external command '%s'

DESCRIPTION

An external command has been launched.

WHAT NEXT

No action is required by the user.

DISP-011

DISP-011 (Warning) Failed to obtain the status of task %d in the past %d minutes. %s.

DESCRIPTION

The status of the task could not be obtained within a given time.

WHAT NEXT

Verify your distributed processing settings.

DISP-012

DISP-012 (Warning) Unable to validate results of task %d. %s

DESCRIPTION

The return value of the validation command defined by the variable **write_spice_sim_validate** is non-zero when the task is done.

WHAT NEXT

Check the preprocessing, postprocessing , and/or simulation command.

DISP-013

DISP-013 (Warning) Worker timeout is overwritten by maximum life span for each task.

DESCRIPTION

The worker timeout value is smaller than the maximum life span for each task. In order to have the work alive long enough to finish the task, the worker timeout value is overwritten.

DISP-014

DISP-014 (Warning) Worker maximum life span is overwritten by the worker timeout.

DESCRIPTION

The value of maxmum life span of the worker should be greater than or equal to the worker timeout value.

DISP-015

DISP-015 (Information) Worker %u will be terminated once the current task finishes due to its timeout %ds has been reached.

DESCRIPTION

The worker timeout has been reached. Once the current task finishes, the worker will be terminated.

DISP-016

DISP-016 (Information) Worker %u is terminated due to its maximum life span %ds has been reached.

DESCRIPTION

The worker is terminated due to its maximum life span has been reached.

DISP-017

DISP-017 (Information) Worker %u is terminated due to its maximum idle time %ds has been reached.

DESCRIPTION

The worker is terminated due to its maximum idle time has been reached.

DISP-018

DISP-018 (Information) Inifinite number of HSPICE licenses can be consumed for parallel processing.

DESCRIPTION

The **distributed_processing_number_hspice_license** variable is set to 0. This will cause the largest possible number of HSPICE licenses to be consumed by the parallel processing depending on your farm status.

LICS Error Messages

LICS-001

LICS-001 (fatal) %s is not enabled.

DESCRIPTION

The application tried to reserve the specified license, but it was not available.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

LICS-002

LICS-002 (Error) Failed to checkout any complete license set from these possible sets: %s.

DESCRIPTION

NanoTime tried to checkout licenses from the shown set. It was not able to get all the licenses of any set, so the license operation failed.

WHAT NEXT

Verify that the key file is up to date and that sufficient licenses are available.

LICS-003

LICS-003 (information) Successfully checked out feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable

SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LICS-004

LICS-004 (information) Started queuing for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LICS-005

LICS-005 (information) Still waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LICS-006

LICS-006 (information) Timeout while waiting for feature '%s'.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in nt_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LICS-007

LICS-007 (information) License queuing is enabled.

DESCRIPTION

You receive this message because you have enabled licensing queuing.

The license queuing is enabled by setenv SNPSLMD_QUEUE TRUE

When enabled the following timeouts can be adjusted:

Timeout for the initial license: setenv SNPS_MAX_WAITTIME <number of seconds>

Timeout for all subsequent licenses: setenv SNPS_MAX_QUEUETIME <number of seconds>

Defaults are equivalent to setenv SNPS_MAX_WAITTIME 259200 setenv SNPS_MAX_QUEUETIME 28800

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-008

LICS-008 (Error) License '%s' does not exist.

DESCRIPTION

The application checked for the presence of the license, but it was not present.

WHAT NEXT

Verify that the key file is up to date and that the license exists in the key file.

LICS-009

LICS-009 (information) Maximum number of licenses allowed for user has been reached.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in nt_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LICS-010

LICS-010 (information) All licenses are checked out.

DESCRIPTION

You receive this message because you have enabled licensing queuing by setting environment variable SNPSLMD_QUEUE to TRUE in nt_shell.

WHAT NEXT

This is an informational message only. No action is required on your part.

SEE ALSO

LICS-007(n)

LOGC Error Messages

LOGC-001

LOGC-001 (error) Must have exactly two objects for the command 'remove_logic_constraint -invert'.

DESCRIPTION

The command **remove_logic_constraint -invert** needs exactly two objects.

WHAT NEXT

Make sure that two objects are specified.

LOGC-002

LOGC-002 (warning) Constraint not found.

DESCRIPTION

The constraint specified in the **remove_logic_constraint** command did not match any previously defined constraint.

WHAT NEXT

Make sure that the constraint you are specifying in the **remove_logic_constraint** command has been set previously with the **set_logic_constraint** command.

LOGC-003

LOGC-003 (error) Must have exactly two objects for the 'set_logic_constraint -invert' command.

DESCRIPTION

The command **set_logic_constraint -invert** needs exactly two objects.

WHAT NEXT

Make sure that two objects are specified.

LOGC-004

LOGC-004 (error) Cannot add %s constraint between nets/pins {%s} because the constraint conflicts with previous constraints or existing logic values.

DESCRIPTION

The constraint specified in the set_logic_constraint command conflicts with previous constraints or existing logic values. The new constraint will be ignored.

WHAT NEXT

Use **report_logic_state** on the nets/pins to check existing logic values. Use **report_logic_constraint** on the nets/pins to check existing logic constraints. The **-related** option shows all logic constraints that might affect the nets/pins.

LOGC-005

LOGC-005 (error) Case analysis setting conflicts with the logic state of other nets: unable to set net %s to logic state %s because of net %s already in logic state %s.

DESCRIPTION

The case analysis value specified in the **set_case_analysis** command conflicts with the logic state of other nets. NanoTime propagates the case analysis value through transistors and combinational cell functions. If the logic state propagated from the case analysis value conflicts with an existing logic state on a net, the case analysis value is ignored.

WHAT NEXT

Use the **report_logic_constraint -conflicts** to report nets with constraint conflicts. The **-related** option shows all the constraints that affect a pin or net.

LOGC-006

LOGC-006 (error) Must have more than one object for the 'set_logic_constraint -[one_hot|one_off|at_most_one_hot|at_most_one_off]' option.

DESCRIPTION

The command option needs more than one object for the specified logic condition.

WHAT NEXT

Make sure that a set of multiple objects is specified in the command.

LOGC-007

LOGC-007 (error) The options -enable_trace_from and -exclude_from_when cannot be used since object "%s" is not an input port.

DESCRIPTION

The options -enable_trace_from and -exclude_from_when for the **set_case_analysis** command can only be used with input ports.

WHAT NEXT

Check the list of objects specified.

LOGC-008

LOGC-008 (error) Cannot remove invert logic constraint between two nets that form a differential pair.

DESCRIPTION

The command **remove_logic_constraint -invert** cannot be applied to a differential net pair.

WHAT NEXT

Removing the differential marking will also remove the invert logic constraint.

LOGC-009

LOGC-009 (information) Logic constraints ignored during generation of the CCS Noise model for pin %s.

DESCRIPTION

Logic constraints were ignored during construction of circuit simulations that were used for generating a CCS Noise model for a particular pin.

WHAT NEXT

Check logic constraints.

LOGC-010

LOGC-010 (Error) Differential nets %s, %s have incompatible logic settings: %s, %s.

DESCRIPTION

NanoTime expects user defined logic states on nets to be consistent with their differential marking. This applies to propagated logic states as well.

WHAT NEXT

Check the **set_differential** commands to ensure that only the correct nets are included. Use **report_case_analysis** to investigate nets with conflicts.

LOGC-011

LOGC-011 (Information) Partially differential nets %s, %s may have incompatible logic settings: %s, %s.

DESCRIPTION

NanoTime expects user defined logic states on nets to be consistent with related structural markings. This applies to propagated logic states as well.

WHAT NEXT

Check the **set_differential** commands to ensure that only the correct nets are included. Use

report_case_analysis to investigate nets with potential conflicts.

LOGC-012

LOGC-012 (Information) No logic constraint found from net %s to net %s driving a differential cross coupled circuit.

DESCRIPTION

Logic constraints can be helpful to the construction of simulation units for differential cross coupled circuits.

WHAT NEXT

Use the **set_logic_constraint** command to specify logic constraints between the two specified nets.

LOGC-013

LOGC-013 (Warning) The option -crosstalk_force will be ignored when it is used with -equal, -nand or -nor options.

DESCRIPTION

Invert and mutex constraints can be used with -crosstalk_force option to control the priorities among logic constraints between aggressors during SI delay (not noise) analysis. Equal, nand, or nor logic constraints are not considered in pessimism reduction during neither SI delay nor noise analysis. Therefore, -crosstalk_force option will be ignored for theose constraints.

WHAT NEXT

No action is necessary.

MXTR Error Messages

MXTR-001

MXTR-001 (error) Could not extract a successful model due to previously reported errors or warnings.

DESCRIPTION

The **extract_model** command did not succeed due to errors such as simulation failures. A .lib model file may have been generated for debug purposes.

WHAT NEXT

Review and fix previously reported errors and warnings.

MXTR-002

MXTR-002 (error) Incorrect command line arguments for **extract_model**.

DESCRIPTION

The **extract_model** command did not succeed due to conflicting or incomplete command line arguments. Note that the options **-ignore_boundary_parasitics** and **-extract_boundary_parasitics** are mutually exclusive and are valid only with the **-name** option.

WHAT NEXT

See the man page for **extract_model** for more information.

MXTR-003

MXTR-003 (error) Incorrect setting of global variables for extract_model.

DESCRIPTION

The **extract_model** command did not succeed due to incompatible settings for certain global variables. The **-extract_boundary_parasitics** option requires **timing_save_wire_delay** to be set to true prior to **check_design** and RC reduction to be disabled by setting either **rc_reduction_max_net_delta_delay** to zero or **rc_reduction_exclude_boundary_nets** to true prior to **read_parasitics**.

WHAT NEXT

Check the man page for **extract_model** for more information.

MXTR-004

MXTR-004 (error) Could not merge models due to errors.

DESCRIPTION

The **merge_models** command did not succeed due to errors.

WHAT NEXT

Consult the **merge_models** man page for details.

MXTR-005

MXTR-005 (warning) Unable to extract parasitics on %s boundary net %s due to the presence of pass transistors, models or DCS.

DESCRIPTION

The timing effect of the parasitics on this boundary net is included in the core cell model. The parasitics will not appear in the extracted SPEF file.

WHAT NEXT

Adding a buffer at the affected port is suggested as a possible workaround for pass transistors or models.

MXTR-006

MXTR-006 (information) No parasitics found on %s boundary net %s.

DESCRIPTION

Unable to extract parasitics for this net since it did not have any.

WHAT NEXT

This is an informational message only; no action is required if the net is not supposed to have any parasitics.

MXTR-007

MXTR-007 (warning) CCS receiver model for input port %s (which has multiple fanouts but no parasitics on its net %s) will only include capacitance from one of the fanouts.

DESCRIPTION

NanoTime requires parasitics on input nets with multiple fanouts for correct CCS receiver model extraction if hierarchical interface parasitics extraction is not enabled.

WHAT NEXT

Use hierarchical interface parasitics extraction or add parasitics to the net.

MXTR-008

MXTR-008 (warning) CCS driver model for output port %s will not include the effects of any parasitics on the net %s.

DESCRIPTION

NanoTime requires no parasitics on output nets driven by cell models for correct CCS driver model extraction if hierarchical interface parasitics extraction is not enabled.

WHAT NEXT

Use hierarchical interface parasitics extraction or remove parasitics from the net.

MXTR-009

MXTR-009 (warning) CCS driver for the timing model driving output port %s is missing.

DESCRIPTION

NanoTime requires CCS driver model for timing models driving output ports when CCS model generation is enabled.

WHAT NEXT

Check the cell library.

MXTR-010

MXTR-010 (warning) -ignore_ports and -extract_boundary_parasitics are supported together only when the ignored ports do not have parasitics.

DESCRIPTION

Only ports that do not have parasitics can be ignored when **-extract_boundary_parasitics\FP option is enabled.**

WHAT NEXT

See the man page for **extract_model** for more information.

MXTR-011

MXTR-011 (error) Clock %s defined on internal pin %s does not have a source defined.

DESCRIPTION

All internal generated clock pins must have timing paths to them from source pins.

WHAT NEXT

Check the create_generated_clock commands.

MXTR-012

MXTR-012 (error) Incorrect use of option -nominal for clock port %s.

DESCRIPTION

The **set_model_input_transition_indexes** command does not accept the option **-nominal** for clock ports if DCS is enabled. Instead, use **set_input_transition** to specify the nominal value for clock ports.

WHAT NEXT

See the man pages for **set_model_input_transition_indexes** and **set_input_transition** for more information.

MXTR-013

MXTR-013 (information) Setting model mode to '%s'.

DESCRIPTION

NanoTime inferred the mode for the generated model based on the recognized topologies in the design.

WHAT NEXT

This is an informational message only; no action is required if the mode is appropriate. Otherwise, use -mode option of extract_model command to set the desired mode.

MXTR-014

MXTR-014 (warning) CCS driver model of output port %s cannot be extracted for path %u because it %s.

DESCRIPTION

NanoTime does not support the generation of CCS driver models for output ports that are driven by DDS or DCS regions.

WHAT NEXT

Check if DDS or DCS can be disabled.

MXTR-015

MXTR-015 (warning) Duplicated look-up table to make %s model arc %s full-unate.

DESCRIPTION

NanoTime defaults to creating timing models with full-unate arcs.

WHAT NEXT

Use the option **-enable_arc_segmentation** to prevent duplication of look-up table.

MXTR-016

MXTR-016 (information) Moved arc boundary from pin %s to pin %s for path %u to make a %s model arc full-unate.

DESCRIPTION

NanoTime defaults to creating timing models with full-unate arcs.

WHAT NEXT

Use the option **-enable_arc_segmentation** to prevent duplication of look-up table.

MXTR-017

MXTR-017 (error) Could not find any path to an internal register from input %s for clock domain %s %s.

DESCRIPTION

It is incorrect to have one or more paths from the given input to outputs but none to internal registers.

WHAT NEXT

Using **trace_paths** verify that paths to internal registers exist from the given input for the specified clock domain.

MXTR-018

MXTR-018 (warning) Could not find a sub-path of %s path %u from pin %s %s to a boundary transparent device pin %s %s that is checked against pin %s %s.

DESCRIPTION

It is incorrect to have no path to a boundary transparent device from an input when one or more paths exist to non-boundary registers reachable from the same input.

WHAT NEXT

Using **trace_paths** verify that a path to the boundary transparent device exist from the given input. Check to ensure that necessary timing checks have not been removed.

MXTR-019

MXTR-019 (error) Could not find any path from a clock to output %s.

DESCRIPTION

It is incorrect to have one or more paths to the given output from inputs but none from a clock.

WHAT NEXT

Using **trace_paths** verify the existence of one or more paths from a clock to the given output.

MXTR-020

MXTR-020 (warning) Removed unconnected output pin %s from model and added its capacitance (%gff) to the extracted boundary parasitics.

DESCRIPTION

Unconnected output pins in a model can result in extra runtime and memory requirements when the model is consumed.

WHAT NEXT

Use the option **-enable_arc_segmentation** to retain unconnected output pins in the model.

MXTR-021

MXTR-021 (warning) Could not create pin-based noise model for %s port %s.

DESCRIPTION

The **extract_model** command was unable to create CCS Noise library information for a particular port.

WHAT NEXT

See the man page for **extract_model** for more information.

MXTR-022

MXTR-022 (warning) %s must be %s %g; replacing %g with %g.

DESCRIPTION

The model load and transition indexes must meet certain criteria to ensure the correctness of delay and noise calculations.

One source of error might be inappropriate design units. Using a large design unit might cause small values to lose precision. For example, a current value of 0.23759 mA would become 237.59 uA if the current unit specified in the **lib_current_unit** variable is set to **1uA**. In this case, no information is lost. However, if the current unit is set to **1A**, the value becomes 0.000238 A, losing some digits of precision.

This issue is especially important if you are creating composite current source (CCS) models. You must verify that your **lib_current_unit** variable setting does not have an adverse effect on the accuracy of current values stored in the model. For best results, use a value of **1uA** for the **lib_current_unit** variable when you are creating CCS models.

WHAT NEXT

See the man page for the **extract_model** command and the *NanoTime User Guide*.

MXTR-023

MXTR-023 (warning) No pin-based noise model for %s port %s due to the absence of timing information.

DESCRIPTION

The **extract_model** command did not create CCS Noise library information for a particular port.

WHAT NEXT

See the man page for **extract_model** for more information.

MXTR-024

MXTR-024 (error) Could not find parasitics in the design.

DESCRIPTION

The **-extract_boundary_parasitics** option require the design to have parasitics.

WHAT NEXT

See the man page for **read_parasitics** for more information.

MXTR-025

MXTR-025 (warning) Latch error recovery variable setting incompatible with latch transparency depth limit.

DESCRIPTION

When the latch transparency depth limit is greater than zero, latch error recovery must be enabled if transparent devices exist in the design.

WHAT NEXT

See the man page for the **trace_latch_error_recovery** variable for more information.

MXTR-026

MXTR-026 (warning) No logic conditions found for timing arc %s in the model.

DESCRIPTION

If no logic conditions are found, enabling **when** option will not produce a 'when' condition.

WHAT NEXT

See the man page for **set_case_analysis** for more information.

MXTR-027

MXTR-027 (error) Unable to create CCS driver model for pin %s %s due to negative reference time or current time step.

DESCRIPTION

CCS timing model requires reference time and the current waveform time steps to be positive numbers. This error can be caused by simulation issues.

WHAT NEXT

Check that the design is correctly configured and the characterization ranges for input slope and output load match the capabilities of the design.

MXTR-028

MXTR-028 (warning) Port %s is not well-suited for context independent characterization due to the presence of pass transistor(s).

DESCRIPTION

Presence of pass transistors at inputs can impact the accuracy of the generated NLDM and CCS models when they are used broadly.

WHAT NEXT

Eliminate pass transistors from input ports through buffering or circuit repartitioning.

MXTR-029

MXTR-029 (warning) Path %u may not be well-suited for representation as a combinational arc in the timing model.

DESCRIPTION

Paths that go through boundary transparent devices clocked by different clock domains may not be represented accurately as combinational arcs in a generated timing model. The multi-cycle count provided in the SDC file for such paths may not be accurate.

WHAT NEXT

Generate a transparent timing model, partition the design or change the clock domain.

MXTR-030

MXTR-030 (information) Offsetting LER adjustment of %g ns in model delay arc representing path %u.

DESCRIPTION

LER delay adjustment on a max clock to output path has been excluded from the delay arc in the model that represents the path.

WHAT NEXT

Fix timing violations in the design and regenerate the model.

MXTR-031

MXTR-031 (Warning) Found %s timing violation of %g ns at pin %s.

DESCRIPTION

NanoTime issues this warning message during **extract_model** when it encounters a timing violation while path tracing from a clock.

You should be aware that an extracted timing model generated in the presence of timing violations cannot represent the design correctly. A timing model represents the boundary of the design and does not provide details about timing violations inside the design.

During iterative analysis such as signal integrity, differential skew, and multi-input switching analysis, MXTR-031 warning messages are issued for the worst-case timing violation at a pin only after all the iterations. For an error-free design, there should not be any MXTR-031 warnings.

If you set the **timing_save_violating_internal_model_paths** variable to **true**, additional timing paths are saved during model path tracing to provide detailed contexts for these messages. For each warning message at a pin, there will be one or more saved timing paths, depending on the number of clock start points from which the pin can be reached.

Timing violations from non-clock inputs are not covered by this message. Note that this message is based on the nominal input transitions and output loads used for **extract_model** and comprehensive timing analysis is the purview of the **trace_paths** command.

WHAT NEXT

You should fix all timing violations before creating an extracted timing model. A model created in the presence of timing violations might not represent the design correctly.

MXTR-032

MXTR-032 (warning) Unable to use path %u for modeling due to missing transparency information.

DESCRIPTION

The path with the given id failed certain validity checks possibly due to internal errors.

WHAT NEXT

Check for errors or warnings and resolve them.

MXTR-033

MXTR-033 (information) Starting context-dependent %s model trace from pin %s %s.

DESCRIPTION

Context-dependent modeling uses input arrival times specified with set_input_delay commands. To generate a robust timing model it is important that the specified arrival times cover the range of arrival times that can be expected at all the instances where the model will be used.

WHAT NEXT

Check specified input arrival times.

MXTR-034

MXTR-034 (warning) Unable to perform context-dependent %s model trace from pin %s %s.

DESCRIPTION

Context-dependent modeling requires input arrival times to be specified with set_input_delay commands; none were found. To generate a robust timing model it is important that the specified arrival times cover the range of arrival times that can be expected at all the instances where the model will be used.

WHAT NEXT

Check specified input arrival times.

MXTR-035

MXTR-035 (error) Found %s %s.

DESCRIPTION

Model merging cannot handle duplicate model file names or models created by other tools.

WHAT NEXT

Check the models specified.

MXTR-036

MXTR-036 (warning) Deleted duplicate arc %s in merged model.

DESCRIPTION

Timing models are not expected to contain duplicate arcs with the same 'when' logic condition.

WHAT NEXT

Ensure that the paths traced for each mode of operation of the design is required for that mode.

MXTR-037

MXTR-037 (warning) Unable to find restored characterization data for path %u.

DESCRIPTION

Characterization data is required for critical paths when invoking modeling commands in a restored session.

WHAT NEXT

Ensure that the variable **model_save_path_characterization_data** is set to true before **extract_model** and that a model was generated prior to **save_session**.

MXTR-038

MXTR-038 (error) Incompatible command line arguments: %s

DESCRIPTION

The **extract_model** command did not succeed due to conflicting or incomplete command line arguments. Note the following restrictions: (1) options **-ignore_boundary_parasitics** and **-extract_boundary_parasitics** are mutually exclusive and are valid only with the **-name** option, (2) option -keep_paths_within cannot be used without -pbsa or -npaths > 1, and (3) option -npaths > 1 cannot be used without -extend_inputs or -extend_outputs.

WHAT NEXT

See the man page for **extract_model** for more information.

MXTR-039

MXTR-039 (warning) Moved arc boundary from port %s to internal pin %s for %s path %u.

DESCRIPTION

Extraction of boundary parasitics necessitated the replacement of a model arc end-point from a design port to an internal pin.

WHAT NEXT

Check for timing constraints on ports and move them to internal pins.

MXTR-041

MXTR-041 (warning) Enabling moded model extraction due to zero path count.

DESCRIPTION

Since there will be no timing arcs due to zero path count, 'when' logic condition will be added to the mode definition in the generated model.

WHAT NEXT

Check if zero path count after model tracing is to be expected.

MXTR-042

MXTR-042 (warning) Disabling CCS model extraction due to zero path count.

DESCRIPTION

CCS receiver and driver model generation requires paths.

WHAT NEXT

Check if zero path count after model tracing is to be expected.

MXTR-043

MXTR-043 (warning) Applied exhaustive completion for bus arc %s.

DESCRIPTION

An exhaustive bus completion is when all 'from' pins are connected to all 'to' pins. Such a bus completion can result in redundant arcs for model pins that need completion.

WHAT NEXT

Ensure that all expected timing paths are present.

MXTR-044

MXTR-044 (warning) Changed start %s %s of path %u that generates clock %s at pin %s to %s.

DESCRIPTION

The context for this message is a single-ended generated clock with differential clock source pins. In this scenario the ETM will not have a generated clock definition for the original start port/pin of the path. Change of the start port/pin will be accompanied by a corresponding change in start transition direction.

WHAT NEXT

Check the correctness of generated clock definitions.

MXTR-045

MXTR-045 (warning) Definition of differential generated clock %s in the ETM may not be possible without specifying edges.

DESCRIPTION

Edge specifications are needed to accurately represent a differential generated clock in the extracted timing model.

WHAT NEXT

Define generated clocks using edge specifications.

MXTR-046

MXTR-046 (warning) Feedthrough path %u will not be characterized.

DESCRIPTION

Feedthrough paths are represented by the extracted boundary parasitics and the Verilog wrapper. They will not be represented in the core cell timing model as part of either delay or constraint arcs.

WHAT NEXT

Ensure that the reported path is a feedthrough path.

MXTR-047

MXTR-047 (warning) Generated clock %s defined on internal pin %s does not have a path to it.

DESCRIPTION

All internal generated clock pins must have timing paths to them from/through source pins.

WHAT NEXT

Check the create_generated_clock commands.

MXTR-048

MXTR-048 (information) Could not find any characterizable path %s port %s.

DESCRIPTION

Characterizable paths are needed to measure port capacitances when Hspice timing is enabled, and for creating CCS receiver and driver models.

WHAT NEXT

Ensure that the ports in the design are defined correctly.

MXTR-049

MXTR-049 (warning) Option %s is not recommended when %s.

DESCRIPTION

This message is issued when an option of **extract_model** that is incompatible with the current settings is used.

WHAT NEXT

Check the command line options.

MXTR-050

MXTR-050 (warning) Path start or end pin %s is neither a port nor a generated clock.

DESCRIPTION

NanoTime could not create a model pin.

WHAT NEXT

Check port and generated clock definitions.

MXTR-051

MXTR-051 (warning) Unable to obtain voltage value for rail net %s, using default voltage %g.

DESCRIPTION

Since the specified rail net does not have a voltage value associated with it, the default voltage value was used instead during model generation.

WHAT NEXT

Check to ensure that voltage values are specified for all rail nets.

MXTR-052

MXTR-052 (error) %s is not a valid file prefix.

DESCRIPTION

NanoTime expects the **-name** option to have a valid file name prefix with which to create the output file(s).

WHAT NEXT

Check to ensure that the command line arguments are correct.

MXTR-053

MXTR-053 (error) extract_model is not compatible with set_driving_cell command found on input port %s.

DESCRIPTION

The **extract_model** command cannot be used in conjunction with the **set_driving_cell** command.

WHAT NEXT

Remove the set_driving_cell with **remove_driving_cell** command. You will need to run **check_design** and subsequent commands again prior to **extract_model**.

MXTR-054

MXTR-054 (warning) Detected exclusion of clock uncertainty from transparent ETM.

DESCRIPTION

It is recommended that clock uncertainties be included in the ETM when **extract_model** command is used to generate a transparent timing model.

WHAT NEXT

Check the value of **model_exclude_clock_uncertainty** variable.

MXTR-055

MXTR-055 (warning) Detected the use of inter-clock uncertainty when extracting a transparent ETM.

DESCRIPTION

It is recommended that inter-clock uncertainties be not enabled when **extract_model** command is used to generate a transparent timing model.

WHAT NEXT

Check the value of **timing_propagate_interclock_uncertainty** variable.

MXTR-056

MXTR-056 (warning) Nonlinear waveform analysis is not set on all nets in the design. The generated CCS model may be inaccurate or even ill-conditioned.

DESCRIPTION

When **ccs_timing** and/or **ccs_noise** are used in model extraction, it is recommended that **set_nonlinear_waveform** command be applied on all nets in the design.

WHAT NEXT

Use **set_nonlinear_waveform** command with necessary accuracy setting.

MXTR-057

MXTR-057 (warning) Unable to create min_capacitance and max_capacitance attributes for model pin %s; ensure that max load is more than %f.

DESCRIPTION

NanoTime can create min_capacitance and max_capacitance attributes only when the max_capacitance attribute is greater than the min_capacitance attribute when the intrinsic load of the pin is accounted for. Intrinsic load is always included in the min_capacitance but only included in the max_capacitance when **model_exclude_self_load_for_ccs** is set to false.

WHAT NEXT

Check the characterization load range specified for the pin.

MXTR-058

MXTR-058 (warning) Updated clock waveforms will not be generated from the transparent clock gate at net '%s' during model generation.

DESCRIPTION

By default NanoTime considers all data signals as context independent during model generation. This implies using maximally early start times for min path tracing and maximally late start times for max path tracing while creating paths for **extract_model**. This is not conducive to getting correct wave shaping updates at transparent clock gate outputs and therefore wave shaping is suppressed.

WHAT NEXT

Review whether the clock gate can be marked as non-transparent.

MXTR-059

MXTR-059 (Warning) Adjusting model constraint based on violating path %u from %g to %g.

DESCRIPTION

NanoTime issues this warning message during **extract_model** when a violating path to an internal timing check is adjusted based on the transparency window of the boundary transparent device on the path. Such paths are identified with an '*' in the debug paths file.

WHAT NEXT

You should fix all timing violations before creating an extracted timing model. A model created in the presence of timing violations might not represent the design correctly. To avoid the adjustment set the variable **model_enable_transparent_constraint_adjustment** to false.

MXTR-060

MXTR-060 (Warning) Found %s timing error of %g ns at pin %s.

DESCRIPTION

NanoTime issues this warning message during extract_model when it encounters a timing error at a pin while path tracing from a clock and a delay adjustment to recover from the error may be applied to continue tracing. Since the error is a negative quantity (it represents a timing check violation) a setup error is subtractive to path delay while a hold error is additive in absolute terms.

You should be aware that an extracted timing model generated in the presence of timing violations cannot represent the design correctly. A timing model represents the boundary of the design and does not provide details about timing violations inside the design.

During iterative analysis such as signal integrity, differential skew, and multi-input switching analysis, MXTR-060 warning messages are issued for the worst-case timing errors at a pin only after all the iterations. For an error-free design, there should not be any MXTR-060 warnings.

If you set the **timing_save_violating_internal_model_paths** variable to **true**, additional timing paths are saved during model path tracing to provide detailed contexts for these messages. For each warning message at a pin, there will be one or more saved timing paths, depending on the number of clock start points from which the pin can be reached.

Timing violations from non-clock inputs are not covered by this message. Note that this message is based on the nominal input transitions and output loads used for **extract_model** and comprehensive timing analysis is the purview of the **trace_paths** command.

WHAT NEXT

You should fix all timing violations before creating an extracted timing model. A model created in the presence of timing violations might not represent the design correctly.

NLNK Error Messages

NLNK-001

NLNK-001 (error) Netlist contains no elements, perhaps due to an empty top level.

DESCRIPTION

The netlist contains no elements.

WHAT NEXT

Check the input netlist for a top level and specify the top-level name in the **link_design** command.

NLNK-002

NLNK-002 (error) Compiling netlist failed.

DESCRIPTION

There were errors in the netlist that prevented a good compilation.

WHAT NEXT

Check the input netlist(s) for syntax or link errors.

NLNK-003

NLNK-003 (error) Unable to load db in: %s

DESCRIPTION

The library cannot be loaded because it contains one or more errors.

WHAT NEXT

Check your database file for errors and then regenerate.

NLNK-004

NLNK-004 (error) There are no netlist files registered to be read in.

DESCRIPTION

Before the **link_design** command can be executed, the netlist files must be registered to be read in.

WHAT NEXT

Use the **register_netlist** command to register the netlist files to be read in. Use the **list_netlists** command to see which files have been registered.

NLNK-005

NLNK-005 (Information) Assigning a new name '%s' to the top module.

DESCRIPTION

The top-level subcircuit does not have a name. Flat-netlist designs do not have top-level names.

WHAT NEXT

Set variable **default_top_name** to assign a top module name. The default value is "top".

NLNK-006

NLNK-006 (error) Inconsistencies detected in the netlist after linking. Please check the instance %s.

DESCRIPTION

Inconsistencies were detected in the netlist after the link phase.

WHAT NEXT

Check for inconsistent model names before the **link_design** command.

NLNK-007

NLNK-007 (Information) Created parasitic annotations containing %d resistors, %d capacitors and %d cross-coupled capacitors.

DESCRIPTION

This message describes the number of parasitic elements that were created from the input netlist.

WHAT NEXT

No action is necessary. The parasitic annotations created during **link_design** behave just like those create by **read_parasitics**, and can be manipulated in the same way.

NLNK-008

NLNK-008 (Information) Created %d lumped net capacitances.

DESCRIPTION

This message describes the number of nets for which lumped capacitor annotations have been created. This value is accessible via a net object's netlist_capacitance attribute.

WHAT NEXT

No action is necessary. To prevent the conversion of netlist capacitors into lumped capacitances, use **link_design -disable_lumped_capacitance**.

NLNK-009

NLNK-009 (Information) Representing %g Ohm parameterized resistor '%s' as %s-circuit.

DESCRIPTION

This message describes the representation chosen for the parameterized resistor, which is represented by either an open-circuit or short-circuit subckt instance.

WHAT NEXT

No action is necessary. To cause parameterized resistors to be represented as parasitics, set the **link_switch_resistors_as_switch_subckts** variable to **false**.

NLNK-010

NLNK-010 (Warning) Resistor '%s' in subckt '%s' has instances with resistance in both the switch range (e.g. '%s' with %g Ohms) and the parasitic range (e.g. '%s' with %g Ohms). Treating as parasitic.

DESCRIPTION

The resistance of the resistor evaluates into be the parasitic and switch ranges. NanoTime requires that for a resistor to be treated as a switch, all instances must evaluate to the switch range. Therefore this resistor is treated as parasitic. In the case where the some instances of the resistor have a very high resistance, this may not be what is desired.

WHAT NEXT

Use a resistance greater than 1e6 or less than 1e-6 Ohms for switch resistors, or turn off this feature using **set link_switch_resistors_as_switch_subckts false**.

NLNK-011

NLNK-011 (information) Design '%s' was not successfully linked.

DESCRIPTION

A summary message indicating that the link process failed for your design.

WHAT NEXT

See previous error messages for more details.

NLNK-012

NLNK-012 (error) Power net '%s' is shorted with ground net '%s' at pin '%s'.

DESCRIPTION

There are shorted power and ground nets.

WHAT NEXT

Check variables link_vdd_alias and link_gnd_alias to get power and ground net names. Check the net connections.

NLNK-013

NLNK-013 (Warning) Could not find %s.

DESCRIPTION

An object in the netlist database could not be located. This might be due to a mismatch between the non-flattened and flattened views of the netlist data.

WHAT NEXT

This issue might be caused by netlist control options or degenerate netlist constructs. No actions is necessary if the condition is acceptable.

To resolve such issues, try eliminating related netlist control options from the NanoTime input script as well as from the netlist files themselves. Also, consider removing shorted resistors or other unusual netlist constructs.

NLNK-014

NLNK-014 (Error) Netlist contains inconsistent SPICE model data.

DESCRIPTION

There were problems reading the SPICE model data during the **link_design** command.

WHAT NEXT

Look for previous errors or warnings regarding SPICE models. This problem may be caused by reading multiple models with the same name.

NLNK-015

NLNK-015 (Information) Created design containing %d transistors, %d timing model cells, and %d hierarchical cells.

DESCRIPTION

This message describes the number of cells that were created from the input netlist.

WHAT NEXT

No action is necessary.

NLNK-016

NLNK-016 (Information) Ignoring embedded RC parasitics in subckt '%s'.

DESCRIPTION

The parasitics in the named subckt have been ignored. This can be due to setting the user variable **link_enable_wrapper_subckt_parasitics** to false.

WHAT NEXT

No action is necessary.

NLNK-017

NLNK-017 (Warning) Ignoring embedded RC parasitics in wrapper subckt '%s'.

DESCRIPTION

The parasitics in the named wrapper subckt have been ignored. This can occur when the **link_enable_wrapper_subckt_parasitics** variable is set to **false** and the wrapper subckt contains multiple levels of hierarchy between the top-level wrapper and the wrapper transistor element.

WHAT NEXT

This warning indicates that the transistor model technology is not compatible with the corner-specific wrapper subckt parasitics flow. Because the parasitics are ignored, there are likely to be accuracy problems in the delay calculations involving these subckt instances. Setting the **link_enable_wrapper_subckt_parasitics** variable to **true** is recommended in this case.

NTL Error Messages

NTL-001

NTL-001 (error) In subckt '%s', coupling capacitor named '%s' is not supported. Skipped creating it.

DESCRIPTION

Coupling capacitors are not supported in the netlist.

WHAT NEXT

Remove the coupling capacitors from the netlist. Declare any coupling capacitors in the parasitics files.

NTL-002

NTL-002 (error) In subckt '%s', unsupported element '%s' in the netlist. Skipped creating it.

DESCRIPTION

Unsupported element type in the netlist.

WHAT NEXT

Remove the unsupported elements from the netlist.

NTL-003

NTL-003 (Warning) Positive net (%s) of DC source (%s) not found

DESCRIPTION

The netlister cannot find the positive net of the DC source in the netlist database.

WHAT NEXT

Check the net name and make sure that the net is defined in the netlist. A '0' net is not valid.

NTL-004

NTL-004 (Warning) Negative net (%s) of DC source (%s) not found

DESCRIPTION

The netlister cannot find the negative net of the DC source in the netlist database.

WHAT NEXT

Check the net name and make sure that the net is defined in the netlist.

NTL-005

NTL-005 (Warning) Voltage source %s does not connect to any ground nets (%s %s)

DESCRIPTION

The voltage source defined does not connect to any ground nets. A voltage source must have one of its terminals connected to ground.

WHAT NEXT

Modify the voltage source definition and make sure one of the terminals is connected to a ground net.

NTL-006

NTL-006 (error) Port %s cannot be created because there is already a port with the same name in the top-level design.

DESCRIPTION

The top-level design cannot have multiple ports with the same name.

WHAT NEXT

Use the **current_design** and **get_ports** commands to find out what ports exist in the top-level design.

NTL-007

NTL-007 (error) Unable to remove file %s from the netlist registry.

DESCRIPTION

Only a netlist that has been registered by the **register_netlist** command can be removed from the registry.

WHAT NEXT

Use the **list_netlists** command to find out if the file you are trying to remove is in the netlist registry. To remove a netlist file, specify only the file name, without the full path.

NTL-008

NTL-008 (Error) File %s is not of type db.

DESCRIPTION

The file specified in the **link_path** variable is not a database (.db) file. Auto load can only work with .db files.

WHAT NEXT

Change the **link_path** variable to point to only .db files.

NTL-009

NTL-009 (Warning) Failed to infer bus '%s' (%d:%d) for design '%s': %s

DESCRIPTION

The netlist reader cannot infer the specified bus with bus inferencing enabled through the **bus_notation** variable. Some ports matched the bus inferencing style, but either had different directions or did not have contiguous indexes. The reason is given in the message.

WHAT NEXT

If this condition is as you expected, no action is required on your part. Otherwise, examine the netlist and correct it if necessary.

NTL-010

NTL-010 (Error) No bulk pin connection for transistor '%s' in subckt '%s'.

DESCRIPTION

NanoTime could not determine the bulk pin connection for the transistor. If this connection is not given in the netlist, NanoTime will try to choose a reasonable default net from the subckt containing the transistor. NanoTime uses the names given by the **link_vdd_alias** and **link_gnd_alias** variables as candidate net names. If there is exactly one net that matches the criteria, NanoTime connects it to the bulk pin. Otherwise, you receive this message.

WHAT NEXT

Add the bulk pin connection to the transistor instance in the netlist.

NTL-011

NTL-011 (error) Unable to create net group '%s'.

DESCRIPTION

NanoTime was unable to create the net group because there is already a net group with the same name.

WHAT NEXT

Try creating a net group with another name.

NTL-012

NTL-012 (warning) Unable to add net '%s' to group '%s' because it already exists in group '%s'.

DESCRIPTION

NanoTime is unable to add a particular net to a group because the net already belongs to another group. A net can belong to no more than one group at a time.

WHAT NEXT

You can remove the group that the net belongs to by using the **remove_net_group** command.

NTL-013

NTL-013 (warning) Unable to add any nets to group '%s'.

DESCRIPTION

Unable to add any nets to a group. This occurs if all the specified nets already belong to other groups. A net can belong to no more than one group at a time.

WHAT NEXT

You can remove the groups that the nets belong to by using the **remove_net_group** command.

NTL-014

NTL-014 (error) Net group '%s' does not exist.

DESCRIPTION

The specified net group does not exist.

WHAT NEXT

Existing net groups can be listed with the **list_net_groups** command.

NTL-015

NTL-015 (Warning) Net names "%s" partially match known %s nets but are not marked as %s

DESCRIPTION

Not marking power and ground nets can lead to long run times and incorrect results.

WHAT NEXT

If the nets in question are indeed power or ground nets, then mark them with 'set link_vdd_alias' or 'set link_gnd_alias'.

NTL-016

NTL-016 (error) A floating point exception occurred during netlist parsing.

DESCRIPTION

A fatal floating-point exception occurred while reading the netlist. This might be due to errors in the netlist or a problem in the netlist-reading code. Fixing any errors or warnings from the netlist parser might resolve this problem.

WHAT NEXT

Look at the messages that precede this one. Look for issues such as parameters not found. If possible, fix the netlist to ensure that these warnings or errors no longer occur.

NTL-017

NTL-017 (Warning) Signal net %s is dependent on multiple supply sources; using net %s and ignoring net %s.

DESCRIPTION

A signal net reachable from multiple supply sources can lead to DC currents.

WHAT NEXT

Check if the circuit can be correctly analyzed by considering only one of the supply sources.

NTL-018

NTL-018 (Error) Parameter %s = %f for cell %s is out of range.

DESCRIPTION

The value of the specified parameter is out of its allowable range.

WHAT NEXT

Check if the parameter value is defined correctly. If the value is zero, it might not have been defined or it might have been overwritten by global parameters.

NTL-019

NTL-019 (Warning) In subckt '%s', unsupported behavior capacitor '%s' in the netlist. Skipped creating it.

DESCRIPTION

Unsupported element type in the netlist.

WHAT NEXT

Remove the unsupported elements from the netlist.

NTL-020

NTL-020 (error) Behavioral voltage source (BVS) '%s' is not supported. %s.

DESCRIPTION

The only behavioral voltage source (or voltage-controlled voltage source) supported by NanoTime is a BVS controlled by the source/drain voltage in the MOS macro model.

WHAT NEXT

Check if the netlist contains behavioral voltage sources other than those supported by NanoTime.

NTL-021

NTL-021 (Warning) The set_input_transition -rail_voltage value %g on input port %s does not match the voltage %g of the dependent supply net for corner %s.

DESCRIPTION

NanoTime detects inconsistent rail voltage settings.

To specify the voltage values of the power supply nets, use the **set_voltage** command. If no power supply voltage is specified, NanoTime uses the value of the **oc_global_voltage** variable as the rail voltage. The set_input_transition command with the -rail_voltage option overrides these settings for individual input waveforms.

WHAT NEXT

Confirm if the set_input_transition -rail_voltage values set are correct.

NTL-022

NTL-022 (Error) Found unsupported data encryption.

DESCRIPTION

NanoTime supports encryption of only wrapper sub-circuits and Spice model cards.

WHAT NEXT

Check whether netlist data is encrypted.

NTL-023

NTL-023 (Error) Command '%s' is currently unsupported with encrypted data.

DESCRIPTION

Certain commands and options are currently not supported with encrypted data due to disclosure of sensitive information.

WHAT NEXT

Check for alternate commands and options.

NTL-024

NTL-024 (information) Encountered encrypted Spice file(s) containing neither encrypted device models

nor encrypted and instantiated macro models.

DESCRIPTION

NanoTime prevents the disclosure of only those entities that are encrypted. Elaborations of encrypted entities are not subject to disclosure constraints.

WHAT NEXT

Ensure that all entities to be protected are encrypted.

NTL-025

NTL-025 (Warning) Supply net '%s' is driven by a Liberty model output or Liberty model bidi pin with incompatible voltage value (%.3fV). The voltage value from the Liberty file will be ignored.

DESCRIPTION

A supply net is driven by an instance whose linked Liberty file shows an incompatible voltage value.

WHAT NEXT

Check if supply voltage settings are correct in the NanoTime setup, or if the input Liberty file should be generated using a matching voltage value for the driving pin.

NTL-026

NTL-026 (Warning) Unable to confirm that net '%s' and '%s' are equivalent. Failed to mark them as equivalent nets.

DESCRIPTION

Nets specified by the **set_lvs_equivalent_nets** command are not marked as equivalent because they do not seem to be equivalent.

WHAT NEXT

Check netlist topology and make sure that nets are at identical depth on parallel stacks in the same channel-connected block and the pullup and pulldown paths have identical gate controls. Use **-force** option if it is needed.

NTL-027

NTL-027 (Information) Marking net '%s' and '%s' as equivalent nets. Net '%s' will represent the other net.

DESCRIPTION

Nets specified by the **set_lvs_equivalent_nets** command are merged into one net.

WHAT NEXT

No action is necessary.

NTL-028

NTL-028 (Warning) Net '%s' and '%s' are already marked as equivalent.

DESCRIPTION

Nets specified by the **set_lvs_equivalent_nets** command are already marked as equivalent.

WHAT NEXT

Check if the nets are already marked as equivalent using **set_lvs_equivalent_nets** command.

NTL-029

NTL-029 (Warning) Net '%s' has annotated parasitic resistors. Cannot mark it as an equivalent net.

DESCRIPTION

A net specified by the **set_lvs_equivalent_nets** command already has back-annotated parasitic resistors that can cause inconsistent resistor connection after **read_parasitics**.

WHAT NEXT

Remove annotated parasitics using the **remove_annotated_parasitics** command if the net is needed to be marked as an equivalent net.

NTL-030

NTL-030 (Warning) Unable to confirm that net '%s' and '%s' are equivalent. But because of "-force" option, marking them as equivalent nets.

DESCRIPTION

Nets specified by the **set_lvs_equivalent_nets** command do not seem to be equivalent. However, because the **-force** option is specified, NanoTime tool forces them as equivalent nets.

WHAT NEXT

Check netlist topology and make sure that nets are equivalent. Also, make sure that there are swapped transistor connections on the nets in parasitics files.

NTL-031

NTL-031 (Error) Cell '%s' may only have one pair of swapped pins.

DESCRIPTION

The **set_allow_pin_swap** command may only allow a single pair of swapped pins per cell.

WHAT NEXT

Please use the **remove_allow_pin_swap** command to remove the existing pin pair and retry.

NTM Error Messages

NTM-001

NTM-001 (Error) The clock (%s) for the %s %s arrival at pin '%s' does not match the clock (%s) for the %s %s arrival at pin '%s'.

DESCRIPTION

The simulation of a memory column is done by using clock arrivals at all inputs to the column. These inputs must originate from the same clock.

WHAT NEXT

Analyze the clock network to the column input and to other inputs of the column.

NTM-002

NTM-002 (Error) The clock arrival at memory column input pin %s is missing.

DESCRIPTION

The simulation of a memory column is done by using clock arrivals at all inputs to the column. These inputs must originate from the same clock and same edge of that clock.

WHAT NEXT

Review the clock network definition, timing exceptions, case analysis statements, clock gating definitions, and netlisting issues to determine why the clock did not propagate to this pin.

NTM-003

NTM-003 (Error) %s for %s '%s'.

DESCRIPTION

The topology was not found for the related topology or net.

WHAT NEXT

Review the markings of related topologies, such as muxes, sense-amps and memory write circuits.

NTM-004

NTM-004 (Error) Bitline '%s' is cross-coupled to net '%s', not to net '%s'.

DESCRIPTION

Cross-coupled PMOS transistors were found, but they are cross-coupled between nets that are not complementary bitlines.

WHAT NEXT

Review the markings of cross-coupled PMOS devices.

NTM-005

NTM-005 (Warning) Using name-based ordering for %s net '%s' because %s.

DESCRIPTION

Delay-based ordering was not possible for this net because there is no parasitic back-annotation, the back-annotation has fewer than 3 nodes, or there is a problem with the annotation, so name-based ordering was used instead. Name-based ordering may cause the critical path to be missed in a post-layout design.

WHAT NEXT

If this is a pre-layout design, then this condition is expected, so no action is necessary. If this is a post-layout design, check the back-annotated parasitics on the net for problems.

NTM-006

NTM-006 (Error) Could not simulate delay from pin '%s' %s (net '%s'). The vectors are missing skew

annotations.

DESCRIPTION

The simulation of a memory column is done by using clock arrivals at all inputs to the column. The arrivals were not found so this simulation could not be performed.

WHAT NEXT

The source of the problem is described in **NTM-001** messages. Look for those messages preceding this message and fix the problem which caused the **NTM-001** messages.

NTM-007

NTM-007 (Warning) Not automatically marking bit mux on net %s because %s.

DESCRIPTION

During the check topology phase NanoTime marks bit-column muxes and demuxes identified automatically by an algorithm. Certain mux-like structures may not be automatically marked due to the above reported reason.

WHAT NEXT

The source of the problem is described in **NTM-007** messages. Look for those messages preceding this message and fix the problem which caused the **NTM-007** messages.

NTM-008

NTM-008 (Error) The memory wordline net '%s' is not a clock net.

DESCRIPTION

In order to properly analyze memory bitcells and simulate a memory bit column, the wordline must be a clock net. The indicated net is not currently marked as a clock net.

WHAT NEXT

Look at the clock network circuitry and clock related commands to determine why clock propagation cannot reach the indicated net. The report_clock_arrivals and report_clock_network commands may be used for this analysis.

NTM-009

NTM-009 (Error) Auto-recognized port type '%s' for bit-line '%s' does not exist in user specified port type list.

DESCRIPTION

NanoTime recognized a memory port type in the design that does not match a user specified port type.

WHAT NEXT

Check that all memory related topologies are properly recognized or marked. Also check that all memory port types are specified with the create_memory command.

NTM-010

NTM-010 (Error) User specified port type '%s' was not found in the design.

DESCRIPTION

NanoTime cannot find a port type specified with the **create_memory** command.

WHAT NEXT

Check that all memory-related topologies are properly recognized or marked. Also, check that port types are specified correctly with the **create_memory** command.

NTM-011

NTM-011 (Warning) Found mismatch in port type for bitcells connected to the same bitline: '%s'.

DESCRIPTION

A bitcell has a port type inconsistent with other bitcell ports connected to the same bitlines.

WHAT NEXT

Check that all bitcells connected to the same bitline have the same port type.

NTM-012

NTM-012 (Error) User specified %d nmos_bidi port(s), but NanoTime found %d nmos_bidi port(s).

DESCRIPTION

The number of nmos_bidi ports found is not consistent with the number specified in the **create_memory** command.

WHAT NEXT

Check that all memory-related topologies are properly recognized or marked. Also, check that port types are specified correctly with the **create_memory** command.

NTM-013

NTM-013 (Error) Memory bitcells cannot have more than 2 ports, %d ports are currently specified .

DESCRIPTION

NanoTime supports single port and dual port SRAM configurations. More than two ports are not allowed.

WHAT NEXT

Check the arguments to the -bitcell_ports option and see if more than 2 ports have been defined.

NTM-014

NTM-014 (Error) Memory bitcell port type '%s' is not supported.

DESCRIPTION

NanoTime supports single port and dual port SRAM configurations. The legal bitcell port types are: "nmos_read", "nmos_write", "nmos_bidi", "single_ended_nmos_read", "single_ended_nmos_read_differential_write", "two_nmos_read" and "single_ended_two_nmos_read".

WHAT NEXT

Check the arguments to the -bitcell_ports option and see if the correct port type(s) have been specified.

NTM-015

NTM-015 (Warning) No memory bitcell port type(s) have been defined, defaulting to a single 'nmos_bidi' configuration.

DESCRIPTION

The create_memory command allows for the definition of the ports used by the bitcell in the memory array. If no ports are specified then a default configuration of a single nmos, bidirectional port configuration will be assumed.

WHAT NEXT

Use the -bitcell_ports option to the create_memory command to specify the type of ports used by the memory array bitcell.

NTM-016

NTM-016 (Error) No bitcell port with type %s has been defined.

DESCRIPTION

The create_memory command allows for the definition of the ports used by the bitcell in the memory array. There must be at least one port that can read from the bitcell and one port that can write into the bitcell.

WHAT NEXT

Check the arguments used in the create_memory option -bitcell_ports and make sure they are correct.

NTM-017

NTM-017 (Error) Found incorrect or unsupported memory port configurations: %s (bitline %s).

DESCRIPTION

NanoTime identified incorrect or unsupported memory port configurations in the design. In the current version, NanoTime only supports the following single port and dual port SRAM configurations: "nmos_read", "nmos_write", "nmos_bidi", "single_ended_nmos_read", "single_ended_nmos_read_differential_write", "two_nmos_read" and "single_ended_two_nmos_read".

WHAT NEXT

Check if the memory port type is supported by NanoTime. Also check if the supporting circuit structures (such as write driver circuit, sense amp, memory precharge, cross-coupled pmos, and etc.) are correctly recognized or marked.

NTM-018

NTM-018 (Error) "%d port devices found, only %d allowed at bitcell net "%s"

DESCRIPTION

NanoTime identified incorrect or unsupported memory port configurations in the design. The number of devices connected to a bitcell net is greater than the number required for the bitcell ports defined for this memory.

WHAT NEXT

Check the bitcell port definitions for this memory and verify that none are missing. Also check if the bitcell referenced is incorrectly included in this memory topology. Check if the cell containing the memory core has been properly specified with the **create_memory** command.

NTM-019

NTM-019 (Error) No write control was found for write block associated with bitline %s

DESCRIPTION

NanoTime could not find any write control for the specified memory write block. Such write control can be a write mux enable pin or a write drive circuit enable pin.

WHAT NEXT

Verify topology recognition or topology marking is correct. Check enable pins for the write mux or write driver circuit are identified correctly in topology report.

NTM-020

NTM-020 (Error) Bitline pairs not specified in the skip_array mode analysis of %s.

DESCRIPTION

Memory bitcells are black-boxed in the **skip_array** mode analysis, so Nanotime cannot recognize bitline pairs automatically. Therefore, the user must specify bitline pairs manually.

WHAT NEXT

Specify memory bitline pairs with the **mark_memory_bitline** command.

NTM-021

NTM-021 (Error) Differential high/low voltages for sense-amp %s not declared in the skip_array mode analysis of memory %s.

DESCRIPTION

Memory bitcells are black-boxed in the **skip_array mode analysis, so the user must specify the differential high/low voltages of the sense-amps.**

WHAT NEXT

Specify the differential high/low voltages of the sense-amps with the **-diff_high and -diff_low options in the mark_sense_amp command.**

NTM-022

NTM-022 (Error) The skip_array mode analysis supports only a single nmos_bidi port type.

DESCRIPTION

A single **nmos_bidi** is the only memory bitcell port type supported in the memory **skip_array** mode analysis.

WHAT NEXT

Check the memory bitcell port type. If it is not a single **nmos_bidi** port, change the memory mode of operation to **read** or **write** in the **create_memory** command.

NTM-023

NTM-023 (Warning) Ignoring the %s command in the memory %s mode analysis.

DESCRIPTION

The **mark_memory_bitline** and **erase_memory_bitline** commands can be executed only in the memory **skip_array** mode analysis. Nanotime ignores these commands in a different mode of operation.

WHAT NEXT

Check the memory mode of operation to be analyzed. If the argument to the **-mode** option in the **create_memory** command was set correctly, delete the **mark_memory_bitline** and **erase_memory_bitline** commands.

NTSR Error Messages

NTSR-001

NTSR-001 (Information) %s session %s.

DESCRIPTION

Saving or restoring the indicated type of data has begun.

WHAT NEXT

This is an informational message only; no action is required.

NTSR-002

NTSR-002 (Error) Data inconsistency encountered during save_session.

DESCRIPTION

An inconsistency was discovered in the session data during a **save_session** command. The saved session data may be incomplete.

WHAT NEXT

It should be possible to restore this session data as normal, however some data is likely missing. A bug report should be filed.

OPCD Error Messages

OPCD-001

OPCD-001 (warning) Voltage not set for supply '%s', using default value of %.3f volts.

DESCRIPTION

A supply net was found in the design, but its voltage was not defined.

WHAT NEXT

Use the **set_voltage** command to set the voltage for the net.

OPCD-002

OPCD-002 (warning) Design contains no %ssupply nets.

DESCRIPTION

The current design has no supply nets. This could negatively impact the performance of NanoTime during topology identification.

WHAT NEXT

Check the input netlist for supply nets, or use the **set_supply_net** command to indicate that a net is a supply.

OPCD-003

OPCD-003 (warning) Design contains no %sground nets.

DESCRIPTION

The current design contains no ground nets. This could negatively impact the performance of NanoTime during topology identification.

WHAT NEXT

Check the input netlist for ground nets, or use the **set_supply_net** command to indicate a net is ground.

OPCD-004

OPCD-004 (Error) Unable to find operating condition %s

DESCRIPTION

NanoTime was not able to find the requested operating condition.

WHAT NEXT

Use the **list_operating_conditions** command to see what operating conditions are available. Use the **create_operating_condition** command to create new operating conditions.

OPCD-005

OPCD-005 (error) Unable to set a supply voltage of %g on a non-supply net, %s

DESCRIPTION

Only supply nets can have a supply voltage applied to them.

WHAT NEXT

Use the **set_supply_net** command to define supply nets before applying a voltage value to them.

OPCD-006

OPCD-006 (Error) Unable to use link_default_operating_conditions variable.

DESCRIPTION

NanoTime is not able to interpret the value stored in the **link_default_operating_conditions** variable,

therefore it is ignored.

WHAT NEXT

Set the **link_default_operating_conditions** to a valid value.

OPCD-007

OPCD-007 (error) A value for default supply voltage is not set in the variable oc_global_voltage.

DESCRIPTION

A default value for supply voltage was not set.

WHAT NEXT

Set a value for the variable **oc_global_voltage**.

OPCD-008

OPCD-008 (warning) Specified default supply voltage of %.3fV is outside the range (%.3fV, %.3fV) of supply voltages found in the design.

DESCRIPTION

The default value for supply voltage was determined to be outside the range of supply voltages in the design.

WHAT NEXT

Ensure that the value set for the variable **oc_global_voltage** is correct.

OPCD-009

OPCD-009 (warning) Setting the default supply voltage variable oc_global_voltage to the only supply voltage %.3fV found in the %s.

DESCRIPTION

The default value for supply voltage was set automatically.

WHAT NEXT

Ensure that the value set for the variable **oc_global_voltage** is correct.

OPCD-010

OPCD-010 (error) A value for default supply voltage is not set in the variable oc_global_voltage; found supply voltages in the range (%.3fV, %.3fV).

DESCRIPTION

A default value for supply voltage was not set.

WHAT NEXT

Set a value for the variable **oc_global_voltage**.

OPCD-011

OPCD-011 (Error) Specified default supply voltage of %.3fV is <= 0.0.

DESCRIPTION

The default value for supply voltage was determined to be invalid.

WHAT NEXT

Ensure that the value set for the variable **oc_global_voltage** is greater than 0.0.

OPCD-012

OPCD-012 (Error) Specified value for the -rail_voltage option of the set_input_transition command of %.3fV is <= 0.0.

DESCRIPTION

The value of the rail voltage must be greater than 0.0.

WHAT NEXT

Ensure that the value used with the -rail_voltage option is greater than 0.0.

PARS Error Messages

PARS-001

PARS-001 (warning) User-specified load capacitance will be ignored for net with SPF (net %s)

DESCRIPTION

A net has both user-specified load capacitance and SPF annotation. Delay calculations will use the SPF annotation and not the user-specified load capacitance.

WHAT NEXT

To avoid this warning message, do not specify a load capacitance where SPF has been annotated.

PARS-002

PARS-002 (Error) The %s net of transistor %s is not connected to net %s.

DESCRIPTION

The specified net connection of the transistor is incorrect. NanoTime cannot proceed with the wrong information.

WHAT NEXT

Check the transistor connection in the netlist.

PARS-003

PARS-003 (Error) The %s pin of transistor %s is not connected to pin %s.

DESCRIPTION

The specified pin connection of the transistor is incorrect. NanoTime cannot proceed with the wrong information.

WHAT NEXT

Check the transistor connection in the netlist.

PARS-004

PARS-004 (Error) DPF parse error on line %d.

DESCRIPTION

NanoTime encountered a parsing error at the specified line of the DPF file.

Failure to read or interpret parasitic data correctly might lead to other errors such as PARA-040 and PARA-044 messages.

WHAT NEXT

Check the line in the file for syntax errors or insufficient arguments.

PARS-005

PARS-005 (Warning) Unrecognized parameter %s in DPF section on line %d. This parameter will be ignored.

DESCRIPTION

NanoTime cannot read in the specified parameter because it doesn't recognize the parameter.

WHAT NEXT

Check to see if it is a supported transistor parameter.

PARS-006

PARS-006 (Error) Unable to find element %s.

DESCRIPTION

NanoTime cannot find the element in the netlist.

WHAT NEXT

Check the netlist to see if the specified element exists.

PARS-007

PARS-007 (Error) Cannot find fingered or layout-only device %s for physical pin %s on net %s. The RC parasitics on this net will be ignored.

DESCRIPTION

A physical pin was referenced in the parasitics, but NanoTime is unable to find the declaration of the fingered or layout-only device for this pin.

WHAT NEXT

Use **read_device_parameters** to read in fingered or layout-only devices so that the physical pins can be linked, or check your parasitics file to ensure that the declarations of fingered or layout-only devices use the correct names.

PARS-008

PARS-008 (Warning) Fingered devices detected on transistor %s. Deleting parasitics on nets %s as well.

DESCRIPTION

A **remove_annotated_device_parameters** command was issued on a transistor with fingered devices. Parasitics on nets connected to the fingered devices are being deleted.

WHAT NEXT

Make sure that removal of parasitics from the listed nets is correct.

PARS-009

PARS-009 (Error) Cannot find a connection to the %s pin of back-annotated device '%s' of netlist device '%s'.

DESCRIPTION

A fingered device was declared, but NanoTime is unable to find a connection to a pin of the fingered device in any net parasitics.

WHAT NEXT

Use **read_device_parameters** to read in fingered devices so that the physical pins can be linked, or check your parasitics file to ensure that the declarations of fingered devices use the correct names.

PARS-010

PARS-010 (Warning) Found fingered net '%s', but the read_parasitics -increment option was not used.

DESCRIPTION

A fingered net was found in the parasitics file, but the **-increment** option was not used when reading the parasitics file. To correctly read parasitics files with fingered nets, the **-increment** option is required.

WHAT NEXT

Use the **read_parasitics -increment** command to read in the parasitics. If necessary, use the **remove_annotated_parasitics** command before the **read_parasitics -increment** command.

PARS-011

PARS-011 (Information) Connecting pin '%s' to pin '%s' with a large parasitic resistor.

DESCRIPTION

Direct support is not provided for fingered nets. Instead, one combined parasitic RC network is used for all fingers of the fingered nets, but the parasitics for each fingered net are stored intact as part of the larger annotation. To satisfy RC network consistency checking, the separate parts of the annotation are then joined by adding large resistors to the RC network.

WHAT NEXT

Information only; no action is necessary. This message provides information about fingered net support.

PARS-012

PARS-012 (Error) For back-annotated device %s, cannot change wrapper subckt from '%s' in the netlist to '%s' in the DPF.

DESCRIPTION

A DPF statement using a wrapper subckt is referencing a different wrapper subckt than was given in the netlist. NanoTime does not support this.

WHAT NEXT

Update either the netlist or the DPF file so that the wrapper subckt names match.

PARS-013

PARS-013 (Error) Unable to parse DPF statements in enhanced mode due to %s.

DESCRIPTION

NanoTime extracted DPF statements from the input parasitics file and wrote them to a SPICE deck for further processing. There were errors parsing this extracted SPICE deck. The DPF statements are ignored in this case.

WHAT NEXT

Look for error messages from the netlist parser preceding this message. Also, make sure that a correct SPICE header file was given to bring in the SPICE model and subckt definitions.

PARS-014

PARS-014 (Error) Unable to access element %d of the DPF SPICE deck in enhanced mode.

DESCRIPTION

NanoTime extracted DPF statements from the input parasitics file and wrote them to a SPICE deck for further processing. Some elements found after parsing the SPICE deck were not transistors. These elements are ignored.

WHAT NEXT

Look for error messages from the netlist parser preceding this message. Also, make sure that a correct SPICE header file is given to bring in SPICE model and subckt definitions.

PARS-015

PARS-015 (Information) The RC annotation or completion for net '%s' has more than 10K near-zero elements.

DESCRIPTION

NanoTime detects that the RC annotation for a net has more than 10K near-zero elements. A resistor with value less than or equal to 0.01 ohm is considered near-zero. A capacitor with value less than or equal to the value defined by the variable **parasitics_min_capacitance** is considered near-zero.

Near-zero resistor elements might occur during parasitic completion. Near-zero capacitor elements might occur in an annotation of resistors that are specified without capacitors at the resistors' nodes. In this case, NanoTime automatically creates capacitors with the value defined by the variable **parasitics_min_capacitance**.

WHAT NEXT

No action is necessary.

PARS-016

PARS-016 (Error) Cannot determine orientation of instance %s with swap-allowed pin on net %s.

DESCRIPTION

This instance does not have correct connectivity, whether swap-allowed pins are swapped or not.

If **parasitics_enable_source_drain_swap** is true, transistor drain and source pins are allowed to be swapped. Other primitives may have swap-allowed pins defined by the **set_allow_pin_swap** command.

Sometimes this message can be caused by an ambiguous mapping of physical device names to the logical netlist. This can be controlled using the variable **parasitics_device_name_mapping_method**.

WHAT NEXT

Check the drain/source connections if the instance is a transistor. Consider modifying the variable **parasitics_device_name_mapping_method**. Use **report_allow_pin_swap** to see allowed pin swaps.

PARS-017

PARS-017 (Warning) Instance %s is not a transistor.

DESCRIPTION

The specified element is being ignored since it is not a transistor.

WHAT NEXT

This message can be considered informational if the specified element is not intended to be a transistor.

PARS-018

PARS-018 (Warning) Design has incomplete RC annotations. Use "report_annotated_parasitics -check" to see which nets have incomplete RC annotations and run "complete_net_parasitics" command to complete parasitics of the nets. Otherwise incomplete RC annotations will be ignored.

DESCRIPTION

The **check_design** command found that the design has incomplete RC annotations. NanoTime will ignore the incomplete RC annotations if they are not successfully completed by using the **complete_net_parasitics** command.

WHAT NEXT

Use the **report_annotated_parasitics -check** command to identify the nets with incomplete RC annotations and run the **complete_net_parasitics** command to complete the parasitics of the nets.

PARS-019

PARS-019 (Warning) Duplicated back-annotation for %s is found. The previous one is ignored.

DESCRIPTION

In DPF or DSPF file, multiple entries of back-annotation for the same device are found. NanoTime removes the previous annotation.

WHAT NEXT

Check the devices in DPF or DSPF file.

PARS-020

PARS-020 (Warning) Removing back-annotated parasitics on floating net '%s'

DESCRIPTION

A net that is not connected to any leaf-level cell pins was found to have back-annotated parasitics. The back-annotated parasitics are removed to avoid spurious error reporting.

WHAT NEXT

Check that the net is intended to be floating. Otherwise, no action is necessary.

PARS-021

PARS-021 (Error) The floating net '%s' has cross-coupled capacitances.

DESCRIPTION

A net that is not connected to any leaf-level cell pins was found to have back-annotated parasitics which include cross-coupled capacitances. This is not supported at this time.

WHAT NEXT

Check that the net is intended to be floating.

PARS-022

PARS-022 (Warning) Net %s has a parasitic network with %d RC elements. Having more than %d RC elements on a single net might cause a long runtime.

DESCRIPTION

This message is shown if NanoTime detects that a net has a parasitic network with a large number of RC elements. Having too many RC elements on a single net might cause a long runtime.

WHAT NEXT

If RC reduction is not being used, try using it. If RC reduction is being used, try using a larger error tolerance for the RC reduction.

SEE ALSO

```
parasitics_rc_count_per_net_warning_threshold(3)
rc_reduction_min_net_delta_delay(3)
rc_reduction_max_net_delta_delay(3)
```

PARS-023

PARS-023 (Warning) Ignoring %d non-minimum and %d minimum resistors on rail net %s.

DESCRIPTION

NanoTime may not utilize all rail net parasitic resistors when variable parasitics_extract_rail_contact_resistance is set to true. Incompatible layout extraction can lead to parasitics that may contain resistors which are not contact resistances of transistor pins. This may result in inaccurate path delays.

WHAT NEXT

Re-extract the parasitic file so that it contains only contact resistances on rail nets by using proper commands and options of your layout extraction tool.

PARS-024

PARS-024 (Warning) Net "%s" has a parasitic network with %d RC elements and a min RC reduction delta delay of %g ps. A minimum delta delay value of %g ps will be used.

DESCRIPTION

This message is shown if NanoTime detects that a net has a parasitic network with a large number of RC elements that will not be reduced sufficiently. In order to prevent long runtimes and/or simulation problems a default min delta delay value will be enforced.

WHAT NEXT

If RC reduction is not being used, try using it. If RC reduction is being used, try using a larger error tolerance for the RC reduction.

SEE ALSO

```
parasitics_rc_count_per_net_warning_threshold(3)
rc_reduction_min_net_delta_delay(3)
rc_reduction_max_net_delta_delay(3)
```

PARS-025

PARS-025 (Warning) Parasitics completion of net %s may cause stack overflow because it has more than %d R elements.

DESCRIPTION

This message is shown if NanoTime detects that a net has a parasitic network with a large number of R elements. Having too many R elements on a single net might cause a stack overflow during parasitics completion.

WHAT NEXT

Double-check that RC extraction of the net looks reasonable. If a stack overflow occurs during **complete_net_parasitics**, **read_parasitics -complete_with zero**, or **check_design -complete_with zero**, try increasing the stack size on the machine. But be forewarned: Similar to **PARS-022**, having too many R elements on a single net might cause a long runtime.

SEE ALSO

```
parasitics_completion_r_count_per_net_warning_threshold(3)
complete_net_parasitics(2)
read_parasitics(2)
check_design(2)
PARS-022(n)
```

PARS-100

PARS-100 (Error) Could not find %s.

DESCRIPTION

An object in the netlist database could not be located. This is usually due to a mismatch between the non-flattened and flattened views of the netlist data.

WHAT NEXT

This may be caused by netlist control options. Try eliminating those from the NanoTime input script as well as from the netlist files themselves.

PARS-101

PARS-101 (Warning) Self-coupling capacitor '%s' is ignored.

DESCRIPTION

The **link_design** command found a capacitor which couples from a net to itself. NanoTime does not support self-coupling, so this coupling is discarded.

WHAT NEXT

No action is necessary.

PARS-102

PARS-102 (Information) Rail to rail capacitor '%s' is ignored.

DESCRIPTION

The **link_design** command found a capacitor which couples between two rail nets. NanoTime does not support self-coupling, so this coupling is discarded.

WHAT NEXT

No action is necessary.

PARS-103

PARS-103 (Warning) Capacitor '%s' is ignored because its nets could not be found.

DESCRIPTION

The **link_design** command has discarded this capacitor because one or both of the nets to which it is connected could not be found. This error might related to subckt port nets for which no connection was made at the level above.

WHAT NEXT

Information only; no action is necessary.

PARS-104

PARS-104 (Warning) %s may cause the loss of netlist parasitics.

DESCRIPTION

This is warning that the current command may modify the annotated parasitics such that some or all parasitics are removed. However some or all of the annotated parasitics in the current design came in through the netlist and were created during the **link_design** command. If such parasitics are removed, they can only be restored by re-running the **link_design** command.

WHAT NEXT

Verify that the final parasitics are accurate.

SEE ALSO

link_design(2)
read_parasitics(2)
remove_annotated_parasitics(2)

PARS-105

PARS-105 (Warning) Behavioral resistor '%s' is ignored.

DESCRIPTION

The **link_design** command found a behavioral resistor whose resistance value could not be statically determined. This resistance value, therefore, could not be annotated onto the net.

WHAT NEXT

No action is necessary.

PARS-106

PARS-106 (Warning) Could not find resistor %s.

DESCRIPTION

A resistor in the netlist database could not be located. This is usually due to a mismatch between the non-flattened and flattened views of the netlist data or the 2 terminals of the resistor are connected together.

WHAT NEXT

Check the resistor connection in the netlist

PARS-107

PARS-107 (Information) Converted inductor '%s' into %g ohm resistor.

DESCRIPTION

An inductor in the input netlist has been converted into a resistor and annotated onto a net as part of the net's annotated parasitics.

WHAT NEXT

No action is necessary

SEE ALSO

link_inductors_as_resistors(3)

PARS-108

PARS-108 (Information) Converted polynomial capacitor '%s' into %g fF capacitor.

DESCRIPTION

A polynomial capacitor in the input netlist has been converted into a constant capacitor and annotated onto a net as part of the net's annotated parasitics.

WHAT NEXT

No action is necessary

SEE ALSO

link_polynomial_capacitors_as_capacitors(3)

PARS-109

PARS-109 (Error) Could not determine value for '%s': %s.

DESCRIPTION

The **link_design** command could not determine a value for the element. This error happens while the **link_design** command is processing parasitic elements in the netlist.

WHAT NEXT

This might be an unsupported element type. If so, remove it from the netlist or replace it with elements which are supported.

If the element is a polynomial capacitor, make sure that the **oc_global_voltage** variable is set to the correct value so that the polynomial equation can be evaluated.

SEE ALSO

`link_polynomial_capacitors_as_capacitors(3)`
`oc_global_voltage(3)`

PARS-110

PARS-110 (warning) Cannot find DPF diode %s in the SPICE netlist. Skipping back-annotation for this instance.

DESCRIPTION

The target DPF diode instance does not have a matching diode element in the SPICE netlist. Back-annotation cannot be performed for this DPF instance.

WHAT NEXT

Double-check the spelling of the specified DPF diode instance name.

PARS-111

PARS-111 (Error) Design %s has diodes but -disable_lumped_capacitance is not specified in link_design. RC annotation to diode pins will be discarded.

DESCRIPTION

NanoTime cannot back-annotate RC parasitics to diode pins when the design has diodes and the **-disable_lumped_capacitance** option is not specified for the **link_design** command.

WHAT NEXT

Specify the **-disable_lumped_capacitance** option for the **link_design** command.

PARS-112

PARS-112 (Information) Representing layout-only resistor '%s' of %g ohms as open circuit.

DESCRIPTION

A resistor from a back-annotated layout-only device has been converted to an open circuit.

WHAT NEXT

Check that the resistance of the resistor is high.

PARS-113

PARS-113 (Warning) Layout-only resistor '%s' is ignored because %s.

DESCRIPTION

A resistor from a back-annotated layout-only device has been ignored.

WHAT NEXT

Check that the two terminals of the resistor are connected to valid nets or net subnodes. Also, make sure that the two terminals are not connected together.

PARS-114

PARS-114 (Error) The lumped capacitance on fingered net %s will be discarded because there is no corresponding fingered device.

DESCRIPTION

A parasitic capacitance appears to be fingered. It should have a corresponding fingered device in the netlist. Without a corresponding device, NanoTime is unable to attach the capacitance to the network.

WHAT NEXT

Investigate the device in question in parasitic file and netlist.

PARS-115

PARS-115 (Warning) Instance %s of type %s is not supported.

DESCRIPTION

The specified element is ignored because it is not a supported object type.

WHAT NEXT

This message can be considered informational if the specified element is not intended as a known object type.

PARS-116

PARS-116 (Warning) Capacitor '%s' between two layout only nets is ignored.

DESCRIPTION

NanoTime found a capacitor that couples between two layout only nets. NanoTime does not support coupling capacitances between layout only nets, so this coupling is discarded.

WHAT NEXT

No action is necessary.

PARS-117

PARS-117 (Warning) Capacitor '%s' between a layout only net and a rail net is ignored.

DESCRIPTION

NanoTime found a capacitor that couples between a layout only net and a rail net. NanoTime does not support such coupling capacitances, so this coupling is discarded.

WHAT NEXT

No action is necessary.

PARS-118

PARS-118 (Warning) Cannot annotate diode '%s' on the net connected to pin '%s'.

DESCRIPTION

NanoTime could not annotate the diode. This is usually due to mismatched diode models or sub-circuits between **link_design** and **check_design**. Layout only diodes can cause this message as well.

WHAT NEXT

Check netlist, model, and parasitic files which describe the diode.

PARS-119

PARS-119 (Warning) Pin '%s' in '%s' does not appear in subckt definition of '%s'.

DESCRIPTION

The **read_parasitics** command found a pin name in the parasitics file that is not defined in the subckt model file.

For example, a warning message is displayed as follows, Warning: Pin 'a' in 'badi_x8/a' does not appear in subckt definition of 'parancap'. (PARS-119)

The pin with full name 'badi_x8/a' is used in .spef file, *NAME_MAP *1 in ... *130 BADI_X8 ...

*CAP 1 *130:A *1:1116 0.00034476427 2 *130:A *1:1436 0.017395578 3 *130:A *1:1439 0.030271478 4 *130:A *1:1241 0.00044815813 5 *130:A *1:1473 0.017390778 6 *130:A *1:1426 0.00045561971 7 *130:A 0.041689169 *END

The device 'BADI_X8' is an instance of 'parancap' defined in .dpf file as follows: XBADI_X8 BADN_X_77 BADN_X_471 gndl parancap ...

And 'parancap' in library file parancap.inc is defined as follows: .subckt parancap in nd sx

The warning is raised because pin 'a' in 'badi_x8/a' does not appear in the definition of 'parancap'.

WHAT NEXT

Check parasitic files and device model files. Try to use exact pin names in RC extraction.

PARS-120

PARS-120 (Error) Cannot find the source of rail net '%s'. Ignoring the incomplete RC annotation.

DESCRIPTION

During the parasitic completion of a rail net, NanoTime could not find the source pin of the rail net. In this case, NanoTime cannot finish the parasitic completion of the net and the rail net parasitics are ignored in path delay estimation.

WHAT NEXT

Check parasitic files to make sure the source of rail net exists. If it is a virtual rail net, try **report_topology -structure_type power_switch** command to see power switch transistors exist. If there is no power switch transistor, use the **mark_power_switch** command to mark a transistor as a power switch transistor.

SEE ALSO

read_parasitics(2)
complete_net_parasitics(2)
set_supply_net(2)
report_topology(2)
mark_power_switch(2)

PARS-121

PARS-121 (Error) Cannot find parasitic %s '%s' in design '%s'; the object exists only in a timing model or a discarded subcircuit '%s'.

DESCRIPTION

NanoTime found a parasitic net or pin that does not exist in top-level netlist database. But the missing parasitic object is inside a black-box (timing model or discarded subcircuit).

WHAT NEXT

Remove the parasitic object from the parasitics file, or avoid the use of timing models or discarded subcircuits.

PARS-122

PARS-122 (Information) Enabling "-increment" option because %s.

DESCRIPTION

The **read_parasitics** command is applied without **-increment** option. But because of some conditions that require the option, NanoTime tool enables the option automatically. The condition includes equivalent net groups created by the **set_lvs_equivalent_nets** command.

WHAT NEXT

No action is necessary.

SEE ALSO

`read_parasitics(2)`
`set_lvs_equivalent_nets(2)`

PATH Error Messages

PATH-001

PATH-001 (warning) Loop found in clock network at pin %s.

DESCRIPTION

A combinational loop was detected in the clock tree at the named pin.

WHAT NEXT

Look at the design around the pin to see if a clock gating structure should be defined with the **mark_clock_gate** command.

PATH-002

PATH-002 (warning) Result of post-trace constraint evaluation could not be saved for constraint '%s' due to missing '%s' arrival record at the checked pin '%s'.

DESCRIPTION

A post-trace evaluated timing check such as a data-to-data check could not be evaluated properly. One of the timing check endpoints did not have a path saved during evaluation.

WHAT NEXT

Check all data-to-data and pulse width timing checks and see if they are defined properly. Check to see if any false path exceptions or other blocking mechanisms might be preventing a path from being found at one of the timing check endpoints. This warning can be ignored at a transparent latch node that misses the transparency open check.

PATH-003

PATH-003 (error) Generated clock pin %s is not found in fanout of reference clock pin %s.

DESCRIPTION

A generated clock defined as coming from a specific pin of a reference clock must be within the fanout of that reference pin.

WHAT NEXT

Check the definition of the generated clock and be sure that the generated clock pin is within the fanout of the reference clock.

PATH-004

PATH-004 (warning) Maximum depth of %d exceeded during path search.

DESCRIPTION

The path search algorithm has a maximum search depth limit to prevent excessive tracing in the event of an incorrect design build. When the limit is reached, the search algorithm will not search any further from that point.

WHAT NEXT

Check the value of the variable **trace_search_depth_limit**.

PATH-005

PATH-005 (Information) The port %s has fixed logic and will not be used to start a search.

DESCRIPTION

If a port is set to a fixed logic value, it cannot be used as a startpoint for path tracing. A fixed logic value could be the result of a user-defined setting at that point or some other logic constraint.

WHAT NEXT

If you expect path tracing to start from the port, check for logic settings or logic constraints that might involve that point (**report_case_analysis**, **report_logic_constraint**).

PATH-006

PATH-006 (warning) Generated clock tracing for clock %s at pin %s cannot start because this generated clock has no source pin defined.

DESCRIPTION

Generated clocks defined without a source pin can only be propagated from their own pin list. The pin list should not be found or propagated from the fanout of some other clock.

WHAT NEXT

Check the generated clock definition.

PATH-007

PATH-007 (warning) A turnoff %s transition was converted to a regular %s transition during generated clock tracing for clock %s at pin %s.

DESCRIPTION

A turnoff transition was encountered during clock trace. This may indicate a problem with clock network recognition or user annotations.

WHAT NEXT

Check the generated clock definition or turnoff markings.

PATH-008

PATH-008 (warning) Min and Max tracing must be on during SI analysis, forcing the %s path tracing.

DESCRIPTION

During signal integrity analysis, minimum delay and maximum delay arrival values are needed to generate timing windows so that the overlaps can be determined.

WHAT NEXT

Do not execute the **trace_paths** command with the **-min_only** or **-max_only** option when signal integrity analysis is enabled.

PATH-009

PATH-009 (error) Re-simulation failed for new input slope %g ns, new output load %g ff for arc %d of path id %d

DESCRIPTION

A resimulation failed to complete during characterization of a path found earlier. In the case of dynamic delay simulation, this failure might be due to insufficient simulation time, which can be fixed with the **set_simulation_attributes -time** command.

WHAT NEXT

Check the input slope and output load values used for model characterization.

PATH-010

PATH-010 (Information) Searching from %s vertex %s %s %s

DESCRIPTION

Depth first path tracing is starting at the indicated timing point.

WHAT NEXT

This is an informational message only; no action is required.

PATH-011

PATH-011 (Information) Stages traversed = %ld total stages traversed = %ld total paths considered = %d

DESCRIPTION

The number of arcs traversed during the depth first search is shown.

WHAT NEXT

This is an informational message only; no action is required.

PATH-012

PATH-012 (Warning) Find path exception only matched %d levels of %d total

DESCRIPTION

A user defined find path sequence of pins could not be traversed completely. This path sequence may not be valid or could be blocked by another exception or logic setting.

WHAT NEXT

Look at the sequence of nodes listed and verify that they are within the transitive fanin/fanout of each other. The specific level of the exception that can not be reached is listed in the warning message.

PATH-013

PATH-013 (Error) set_find_path exceptions can not be used during model generation without the option -use_find_path or -find_path_only.

DESCRIPTION

By default model tracing will do full path tracing using all user defined inputs, clocks, and outputs. Exceptions defined with set_find_path are not allowed.

WHAT NEXT

Either remove the set_find_path statements or invoke extract_model with the option "-use_find_path" or "-find_path_only".

PATH-014

PATH-014 (Warning) Using set_find_path exceptions will restrict generation of timing windows and change the impact of crosstalk effects.

DESCRIPTION

In order to properly model crosstalk effects a valid timing window is needed on each aggressor and victim net. When set_find_path exceptions have been defined it restricts the search space during path tracing and may prevent some nets from getting valid timing windows. A net without a timing window is assumed to have an infinite window and uses the default aggressor slope.

WHAT NEXT

Either remove the set_find_path statements, use set_si_delay_analysis to exclude unwanted aggressors, and/or set new default aggressor slopes with the variables si_aggressor_transition_default_fall and si_aggressor_transition_default_rise.

PATH-015

PATH-015 (warning) The %s input arrival needs to be specified for input %s to generate correct results during SI and/or MIS analysis.

DESCRIPTION

During SI analysis min and max arrival values are needed to generate windows so that overlaps can be determined. When min or max arrivals are missing only one edge of a timing window can be determined. The missing edge must be assumed to be infinite, leading to overly pessimistic results.

WHAT NEXT

Check your set_input_delay definitions and make changes to include min and max values for each input.

PATH-017

PATH-017 (warning) Path characterization for input slope %g ns, output load %g ff for arc %d of path id %u has triggered some simulation warnings above.

DESCRIPTION

Simulation run for an arc of a path with a certain input slope and output load has triggered some simulation warnings such as DELC-007.

WHAT NEXT

Check the input slope and output load values being used for model characterization.

PATH-018

PATH-018 (warning) Found multiple matching %s exceptions at %s. Using the last one that matched.

DESCRIPTION

If multiple exceptions are used for the path then the last one is used.

WHAT NEXT

PATH-019

PATH-019 (warning) Can not generate clock waveform for synchronized data %s, ignoring this synchronized data point.

DESCRIPTION

Either rise or fall delay is missing at this synchronized data point.

WHAT NEXT

Make sure both rise and fall delay are present at this synchronized data point.

PATH-020

PATH-020 (Error) Detailed DCS path from %s(%s) to %s(%s) could not be mapped to the timing graph.

DESCRIPTION

The specified delay path will be missing from the analysis. A bug report should be filed.

WHAT NEXT

The detailed path reporting feature for DCS can be disabled by setting **dcs_enable_detailed_path_reporting** to false.

PATH-021

PATH-021 (Error) No set_find_path exceptions were found.

DESCRIPTION

To generate a model using paths created by set_find_path exceptions, one or more set_find_path exceptions must be defined prior to invoking extract_model.

WHAT NEXT

Either add set_find_path commands or invoke extract_model without the option "-find_path_only".

PATH-022

PATH-022 (Error) The timing point "%s" is contained in more than one correlated region.

DESCRIPTION

When the command mark_correlated_region is issued it defines a region between the inputs and outputs. If the command is used more than once then the regions defined must not overlap. If an overlap is detected then the second region defined at an overlapping point will not be used.

WHAT NEXT

Examine the mark_correlated_region commands and determine if the regions defined can be modified so that they do not overlap.

PATH-023

PATH-023 (Information) Executing iteration %d of path search in differential mode.

DESCRIPTION

NanoTime can perform path tracing iterations to improve the skew values between differential net pairs. The feature must be enabled by setting the **timing_differential_iteration_count** variable to a value greater than 1. If iterations are performed, the **PATH-023** message shows the iteration count.

Multiple path searches might be necessary to achieve convergence of differential skews. The tool does not analyze convergence; you must set an appropriate number of iterations to achieve the desired accuracy.

WHAT NEXT

This is an informational message only; no action is required.

SEE ALSO

`timing_differential_iteration_count(3)`

PATH-024

PATH-024 (Information) Applying differential skew %g and transition slope %g at pin %s when tracing through pin %s.

DESCRIPTION

NanoTime can perform path tracing iterations to improve the skew values between differential net pairs. The feature must be enabled by setting the **timing_differential_iteration_count** variable to a value greater than 1.

The **PATH-024** message shows the skew and slope being applied at a pin during the current iteration. These are the worst-case values from the previous path trace iteration, determined by evaluating all arrivals at this pin.

WHAT NEXT

This is an informational message only; no action is required.

SEE ALSO

`timing_differential_iteration_count(3)`

PATH-025

PATH-025 (Information) Extending differential path search to iteration %d.

DESCRIPTION

When other features such as SI or MIS require more iterations than the specified differential iteration count, those additional iterations must use differential skew and slope from the previous path search.

WHAT NEXT

This is an informational message only; no action is required.

SEE ALSO

`timing_differential_iteration_count(3)`

PATH-026

PATH-026 (Warning) PBSA/POCV analysis will be computed without the removal of the common path SI delta delays for non-zero cycle paths. Results may be optimistic.

DESCRIPTION

By default all the SI delta delays for the data and clock A segments are included in the common mode adjustment. When the **pbsa_include_common_si_deltas** variable is set to **true**, the SI delta delays for the data and clock A segments will be considered common only for zero-cycle paths.

WHAT NEXT

Set pbsa_include_common_si_deltas to true to get a more accurate treatment of the SI deltas on the common path.

PATH-027

PATH-027 (Warning) PBSA/POCV analysis will be computed without the consideration of same direction common path differences. Results may be optimistic.

DESCRIPTION

By default the difference between the data segment A delay and the clock A segment delay is credited back to the slack. When the **pbsa_common_net_use_same_direction_delays** variable is set to **true**, the minimum of the differences between the data-rise arrival time and the clock-rise arrival time and the data-fall arrival time and the clock-fall arrival time for the common segment will be credited back to the slack.

WHAT NEXT

Set pbsa_common_net_use_same_direction_delays to true to get a more conservative common mode adjustment.

PATH-028

PATH-028 (Warning) PBSA/POCV analysis will be computed without considering mismatched edges at a reconvergent common net. Results may be optimistic.

DESCRIPTION

When reconvergent nets exist among the clock and data paths, the **pbsa_allow_reconvergent_common_net** variable is set to **true**, and the **pbsa_same_common_switching_direction** variable is set to **false**, the common net can occur beyond the first divergent net. When the **pbsa_same_edge_reconvergence_only** variable is set to **true**, the reconvergent net must have matched edges.

WHAT NEXT

Set the **pbsa_same_edge_reconvergence_only** variable to **true** to get a more conservative common net selection.

PATH-029

PATH-029 (warning) Internal pin %s of generated clock %s was not searched from.

DESCRIPTION

At least one of the pins where a generated clock is defined was not searched from. Possible causes are logic blocking of paths, false paths exceptions blocking the path to the generated clock, or an incorrect marking of the -master_clock from the create_generated_clock command.

WHAT NEXT

Check the generated clock definition.

PATH-030

PATH-030 (Warning) PBSA/POCV analysis will be computed without considering mismatched edges at a reconvergent common net for zero cycle paths. Results may be optimistic.

DESCRIPTION

When reconvergent nets exist among the clock and data paths, the **pbsa_allow_reconvergent_common_net** variable is set to **true**, and the **pbsa_same_common_switching_direction** variable is set to **false**, the common net can occur beyond the first divergent net. When the **pbsa_same_edge_reconvergence_only** variable is set to **true**, the reconvergent net must have matched edges. Further, if the **pbsa_same_edge_zero_cycle_reconvergence_only** is set to **true**, reconvergence is only allowed for zero cycle paths where it is not possible to physically have the data and clock paths take different paths.

WHAT NEXT

Set the **pbsa_same_edge_zero_cycle_reconvergence_only** variable to **true** to get a more conservative common net selection.

PATH-031

PATH-031 (Warning) The **pbsa_same_edge_zero_cycle_reconvergence_only** variable is set to **true** without the **pbsa_allow_reconvergent_common_net** variable and the **pbsa_same_edge_reconvergence_only** variable set to **true**. The functionality enforced by the **pbsa_same_edge_zero_cycle_reconvergence_only** variable will not be in effect.

DESCRIPTION

When reconvergent nets exist among the clock and data paths, setting the **pbsa_same_edge_zero_cycle_reconvergence_only** variable to **true**, will restrict reconvergence for zero cycle paths only. For the correct functionality, the **pbsa_same_edge_reconvergence_only** variable must be to **true** and the **pbsa_allow_reconvergent_common_net variable must also be set to true.**

WHAT NEXT

Check the settings of the **pbsa_same_edge_reconvergence_only** variable and the **pbsa_allow_reconvergent_common_net** variable.

PATH-032

PATH-032 (Error) The variable %s must have a value between -1.0 and 1.0.

DESCRIPTION

The pbsa scaling variables pbsa_K[A,B,C,D]max and pbsa_K[A,B,C,D]min variables must have a value between -1.0 and 1.0.

WHAT NEXT

Change the setting of the variable to have a value between -1.0 and 1.0.

PATH-033

PATH-033 (Warning) The value %g for variable %s may cause optimistic results.

DESCRIPTION

The pbsa scaling variables pbsa_K[A,B,C,D]max typically have a value between 0.0 and 1.0, increasing the delay of max paths. A negative value for one of these variables could lead to optimistic results.

The pbsa scaling variables pbsa_K[A,B,C,D]min typically have a value between -1.0 and 0.0, decreasing the delay of min paths. A positive value for one of these variables could lead to optimistic results.

WHAT NEXT

Verify the value of the pbsa variable setting to see if it is consistent with the scaling desired.

PATH-034

PATH-034 (warning) Vertex %s of a '%s' exception cannot reside in DCS region.

DESCRIPTION

The common_through/exclude_reference_through vertex of this exception cannot reside in a DCS (dynamic clock simulation) region. The exception will be ignored.

WHAT NEXT

Stop the DCS network before the common_through/exclude_reference_through point. Either use **mark_instance -exclude_from_dcs** (prior to check_topology) or **mark_clock_network -end_dcs** (prior to match_topology).

PATH-035

PATH-035 (warning) Multiple '%s' exceptions detected in single path trace at through vertices %s and %s - these exceptions will no longer apply.

DESCRIPTION

Multiple exceptions triggered in a single path trace are not supported. All through matches are ignored at this point and subsequently will not apply.

WHAT NEXT

Tighten the restrictions of each offending exception by adding more nets or pins to the -from/-through/-to options.

PATH-036

PATH-036 (Warning) Missing prefix path of generated clock (%s) path (ID=%d) starting from vertex %s.

DESCRIPTION

The prefix path leading to the generated clock starting vertex is missing from the path database. This may lead to pessimism in PBSA if the common-mode net shared by launch and capture paths is in the prefix path.

WHAT NEXT

Check the generated clock definition. If multiple clocks feed into the generated clock, see if it can be redefined to use one master clock.

PEXE Error Messages

PEXE-001

PEXE-001 (Information) Spawned process %ld has not %s yet.

DESCRIPTION

A process spawned by the main NanoTime process has either not yet started or has not yet finished. If the main process terminates for any reason while one or more spawned processes are still running they will be terminated.

WHAT NEXT

Give more time for the spawned process to finish.

PEXE-002

PEXE-002 (Error) Unable to %s file %s: %s.

DESCRIPTION

NanoTime has encountered a file I/O error.

WHAT NEXT

Ensure adequate access for the file.

PEXE-003

PEXE-003 (Information) Spawning process %ld by process %ld at time %s to execute '%s'.

DESCRIPTION

NanoTime has launched a separate process to execute a command.

WHAT NEXT

Ensure that the spawnded process completes before exiting the parent process.

PEXE-004

PEXE-004 (Information) At time %s process %d was finished with the command%s%s (Tcl return code: %d).

DESCRIPTION

Spawned child process has evaluated the command.

WHAT NEXT

Check log file for results.

PEXE-005

PEXE-005 (Information) Launching separate process %ld at time %s to execute command '%s'; check process file %s for more info.

DESCRIPTION

NanoTime is about to launch a separate process to improve overall performance by reducing elapsed time.

WHAT NEXT

Check process file for information about the process.

PEXE-006

PEXE-006 (Warning) For command '%s' unable to spawn a separate process: %s.

DESCRIPTION

NanoTime was unable to launch a separate process to execute the command.

WHAT NEXT

The command will be executed inline.

PEXE-007

PEXE-007 (Error) Unable to create more than %d concurrent child processes for parallel command execution.

DESCRIPTION

NanoTime was unable to launch a separate process to execute the command.

WHAT NEXT

The command will be executed inline.

PEXE-008

PEXE-008 (Information) Separate process %ld finished.

DESCRIPTION

NanoTime has detected the completion of one of the separate processes it launched to execute a command in parallel with the main process.

WHAT NEXT

Check the results in the associated log file.

PEXE-009

PEXE-009 (Error) Spawned process %ld was terminated at time %s.

DESCRIPTION

A spawned process was terminated before completion. This could be due to the termination of the parent process.

WHAT NEXT

Check the log of the parent process.

PEXE-010

PEXE-010 (Information) Spawned process %ld exited at time %s.

DESCRIPTION

A spawned process exited by executing either the **exit** or the **quit** command.

WHAT NEXT

Check the log for results.

PEXE-011

PEXE-011 (Error) Incorrect specification of parallel_execute: %s.

DESCRIPTION

The parallel_execute command could not be parsed due to errors.

WHAT NEXT

Correct the arguments to the command.

PTTR Error Messages

PTTR-001

PTTR-001 (error) Pattern file contains top-level circuit.

DESCRIPTION

The pattern file contains one or more subcircuit definitions. Top-level circuits are not allowed.

WHAT NEXT

Remove the top-level elements from the pattern file.

PTTR-002

PTTR-002 (error) Cannot find pattern '%s'.

DESCRIPTION

The pattern you specified does not exist in the pattern database.

WHAT NEXT

Check the name of the pattern and make sure it is correct. Use **read_pattern** to read patterns into NanoTime and **list_patterns** to list patterns that have been read in.

PTTR-003

PTTR-003 (error) Pattern '%s' already exists.

DESCRIPTION

The pattern already exists in the pattern database. The old pattern is preserved.

WHAT NEXT

Check the name of the pattern and make sure it is correct. Use the **remove_pattern** command to remove the old pattern if necessary.

PTTR-004

PTTR-004 (error) Cannot run pattern matching within a pattern match command.

DESCRIPTION

A pattern matching command was run from within the **-command** parameter of a pattern matching command. The matching of patterns inside patterns is not supported.

WHAT NEXT

Within the pattern match command string, directly reference the objects in the pattern instead of searching for them using pattern matching.

PTTR-005

PTTR-005 (information) Transistors %s were found parallel. Transistor %s will represent all the other parallel transistors.

DESCRIPTION

A group of transistors have been found to be parallel. The first transistor in the group is chosen as the representative transistor. The non-representative parallel transistors will be ignored for pattern matching if the **pattern_merge_parallel_transistors** variable is set to **true**.

WHAT NEXT

This is an informational message only; no action is required.

PTTR-006

PTTR-006 (warning) Invalid pattern '%s'. The port list of the pattern is empty or only contains rail nets.

DESCRIPTION

Pattern matching fails if the port list of the pattern is empty or only contains rail nets.

WHAT NEXT

Decide port nets for the pattern and add them to the port list.

PTTR-007

PTTR-007 (warning) Invalid pattern. Subckt '%s' is nested. Pattern netlist does not support nested subckts.

DESCRIPTION

Pattern netlist does not support nested subckts.

WHAT NEXT

Flatten the pattern netlist.

SAVR Error Messages

SAVR-001

SAVR-001 (error) Analysis data in file %s is incompatible with the current data structures.

DESCRIPTION

The version number in the data provided to the **restore_analysis_data** command has indicated that the data is incompatible with the version of the program being run.

WHAT NEXT

Regenerate and save new analysis data with the command **save_analysis_data**.

SAVR-002

SAVR-002 (error) Unable to %s file %s to %s analysis data.

DESCRIPTION

The analysis data operation did not succeed due to possible problems with the given directory path.

WHAT NEXT

Check to ensure that the data directory path is valid.

SAVR-003

SAVR-003 (information) Wrote %d simulation units to disk.

DESCRIPTION

The **save_analysis_data** command successfully persisted analysis data to file.

WHAT NEXT

The persisted data can be read with **restore_analysis_data** command.

SAVR-004

SAVR-004 (information) Read %d simulation units from disk.

DESCRIPTION

The **restore_analysis_data** command successfully read analysis data from file.

WHAT NEXT

Updated analysis data can be written back to disk with the **save_analysis_data** command.

TECH Error Messages

TECH-001

TECH-001 (error) found no transistor models.

DESCRIPTION

No transistors in the design have models. Delays through transistor circuitry cannot be computed without transistor models.

WHAT NEXT

Transistor models can come from BSIM3/BSIM4 models when the design is linked or when the models are read explicitly with the **read_spice_model** command, or from externally generated techfiles read with the **read_techfile** command.

TECH-002

TECH-002 (Warning) %d out of %d transistors do not have transistor models linked to them.

DESCRIPTION

This message occurs after the transistor models are linked if not all the transistors have valid models. Delays through transistor circuitry cannot be computed without transistor models.

WHAT NEXT

Use the **list_technology** and **report_technology** commands to see what transistors models are being used. Transistor models can come from BSIM3/BSIM4 models when the design is linked or when the models are read explicitly with the **read_spice_model** command, or from externally generated techfiles read with the **read_techfile** command.

TECH-003

TECH-003 (Information) %d out of %d transistors have transistor models linked to them.

DESCRIPTION

After the transistor models are linked, this message tells you how many transistors have valid transistor models.

WHAT NEXT

Use the **list_technology** and **report_technology commands to see what transistors models are being used.**

TECH-004

TECH-004 (Error) Parameter %s cannot be changed on transistor %s.

DESCRIPTION

A specific transistor parameter cannot be modified. In order to change transistor parameters, they must be defined in the netlist.

WHAT NEXT

Check to see if the parameter that needs to be changed is defined in the netlist.

TECH-005

TECH-005 (Warning) Unable to find %s transistor model for transistor %s.

DESCRIPTION

NanoTime was unable to find a suitable transistor model for this particular transistor.

WHAT NEXT

Use the **list_technology** and **report_technology** commands to find out whether the required transistor models have been read in. Check to see if the sizes of the transistor models are available for the transistors.

TECH-006

TECH-006 (Warning) Invalid technology file command %s. This command will be skipped.

DESCRIPTION

NanoTime was not able to recognize a command in the technology file.

WHAT NEXT

Check the technology file for incorrect commands or commands that are not supported.

TECH-007

TECH-007 (error) Unable to read technology file in: %s

DESCRIPTION

The technology file cannot be read because it contains one or more errors.

WHAT NEXT

Check your technology files for errors and then regenerate.

TECH-008

TECH-008 (Warning) Model %s is not of type PMOS or NMOS. This model will be ignored.

DESCRIPTION

NanoTime can only read NMOS and PMOS type transistor models.

WHAT NEXT

Check your model file to see that only PMOS and NMOS type transistor models are being used.

TECH-009

TECH-009 (Error) No transistor models found in file %s.

DESCRIPTION

NanoTime cannot find valid transistor models specified in the file.

WHAT NEXT

Check your modelcard file to see if all transistor models are declared correctly.

TECH-010

TECH-010 (Error) Unable to determine transistor type (PMOS/NMOS) for transistor %s with a transistor model name of %s%s.

DESCRIPTION

NanoTime cannot find a PMOS/NMOS type for this transistor. It must know the transistor cell type before the transistor can be added to netlist.

WHAT NEXT

Check and set the variables **pmos_alias** and **nmos_alias** to recognize transistor types by name.

TECH-011

TECH-011 (Warning) Removing transistor model %s (Length = %gum, Width = %gum) that is being used.

DESCRIPTION

This transistor model has been linked to a transistor in the netlist. Removing the transistor model information will require the transistor model to be re-linked by **check_design** command. The design will not be built if any transistor fails to link to a model.

WHAT NEXT

Use the **list_technology** and **report_technology** commands to see what transistor models are available for the design. Load additional transistor models with the **read_spice_model** command or from externally generated techfiles read with the **read_techfile** command to make sure there is an acceptable

replacement for the removed model.

TECH-012

TECH-012 (Error) Missing %s in transistor model %s. This transistor model will be removed.

DESCRIPTION

The transistor model is not complete and is missing information.

WHAT NEXT

Check to see if the transistor model has errors, either in the technology file or the SPICE modelcard.

TECH-013

TECH-013 (Information) No transistor models found.

DESCRIPTION

NanoTime has not loaded any transistor models into memory. Transistor models are required for each transistor when simulation occurs.

WHAT NEXT

Transistor models can come from BSIM3/BSIM4 models when the design is linked or when the models are read explicitly with the **read_spice_model** command, or from externally generated techfiles read with the **read_techfile** command.

TECH-014

TECH-014 (Error) %s (%.4f) must be greater than %s (%.4f).

DESCRIPTION

The model generation parameters are not consistent.

WHAT NEXT

Check the *nanosim tech directives in the technology files, which may be read in during **link_design** or **read_spice_model**.

TECH-015

TECH-015 (Warning) *nanosim tech directive %s not set, using default values (%.4f) instead. Inappropriate values can cause simulation error.

DESCRIPTION

The model generation parameters are set to default values.

WHAT NEXT

Add the *nanosim tech directives in the technology files, which may be read in during **link_design** or **read_spice_model**.

TECH-016

TECH-016 (Error) Model %s not found or instance %s width or length does not fit into the wmax/wmin or lmax/lmin range of model. The channel width= %.3e and length= %.3e .

DESCRIPTION

The transistor size is out of the range of model card.

WHAT NEXT

Check if correct model cards are included.

TECH-017

TECH-017 (Information) Creating corner-specific technology data for technology named '%s'.

DESCRIPTION

NanoTime is calculating corner-specific SPICE model data. This is required when the **set_technology** is used with wrapper subckt SPICE models (also called macro model).

WHAT NEXT

No action is necessary.

TECH-018

TECH-018 (Warning) %d transistors were identified, but only %d were annotated with corner-specific technology data.

DESCRIPTION

Not all transistors were annotated with corner-specific SPICE models.

WHAT NEXT

There might have been a problem writing the corner-specific flat netlist or reading it back in. Use the **sim_transistor_wrapper_subckts** variable to identify the correct subckt names for your model library. Use the **set_technology** command to identify the correct technology SPICE file.

TECH-019

TECH-019 (Error) Could not parse the files for technology '%s'.

DESCRIPTION

The file or files given to **read_spice_model** had errors during parsing.

WHAT NEXT

Review the parsing error messages above this message and correct the problem.

SEE ALSO

```
read_spice_model(2)
set_technology(2)
```

TECH-020

TECH-020 (Error) Instance %s width or length is zero. The channel width= %.3e and length= %.3e.

DESCRIPTION

The transistor size is zero.

WHAT NEXT

(1) Check the case sensitivity and case mode to be used by the netlist reader and linker. (2) Check if the value is not defined or overwritten by global parameters.

TECH-021

TECH-021 (Error) Skipping element named '%s'%s. Not a MOSFET.

DESCRIPTION

An error occurred during multi-corner macro-model processing. The element in the corner-specific SPICE deck is not an instance of a wrapper subckt defined in the technology file specified in the **read_spice_model** command.

WHAT NEXT

Use the **sim_transistor_wrapper_subckts** variable to limit the wrapper transistor identification to instances of subckts which are defined in the technology file specified in the **read_spice_model** command. Alternatively, include a definition of the missing subckt in your technology file.

SEE ALSO

```
read_spice_model(2)
set_technology(2)
sim_transistor_wrapper_subckts(3)
```

TECH-022

TECH-022 (Information) Created parasitic annotations containing %d resistors, %d capacitors and %d cross-coupled capacitors.

DESCRIPTION

This message describes the number of parasitic elements that were created from the corner-specific wrapper subckts.

WHAT NEXT

No action is necessary. The parasitic annotations created during **check_design** behave just like those

create by **read_parasitics**, and can be manipulated in the same way.

TECH-023

TECH-023 (Information) Created %d lumped net capacitances.

DESCRIPTION

This message describes the number of nets for which lumped capacitor annotations have been created during **check_design**. This value is accessible via a net object's netlist_capacitance attribute.

WHAT NEXT

No action is necessary. To prevent the conversion of netlist capacitors into lumped capacitances, use **link_design -disable_lumped_capacitance**.

TECH-024

TECH-024 (Information) Wrapper subckt parasitics will use the corner technology file specified by parasitics_wrapper_subckt_technology.

DESCRIPTION

NanoTime maintains only 1 parasitic database, rather than a different database for each technology corner. In a multi-corner flow, if **link_enable_wrapper_subckt_parasitics** is true, then parasitics_wrapper_subckt_technology must be set. This variable tells NanoTime which technology file to use when instantiating parasitics found in wrapper subckts after back-annotation with DPF or SPF.

WHAT NEXT

Ensure the **parasitics_wrapper_subckt_technology** variable identifies the preferred parasitic corner for wrapper subckt parasitics. Alternatively, you can set **link_enable_wrapper_subckt_parasitics** to true, which will evaluate wrapper subckt parasitic values based on pre-layout device parameters.

TECH-025

TECH-025 (ERROR) SOI model: %s will not be linked. SOI analysis is not enabled.

DESCRIPTION

This message is generated when the **check_design** command attempts to bind an SOI SPICE model (level=57, 70 or 69) to a transistor without SOI analysis enabled.

WHAT NEXT

Set the **soi_enable_analysis** variable to **true** before running the **check_design** command. This feature requires a NanoTime Ultra license.

TECH-026

TECH-026 (ERROR) Attempting to use an incompletely specified mos model (name= %s): type= %s

DESCRIPTION

This message is generated when the **check_design** command attempts to use an incomplete transistor model that has missing information and cannot be used to create a DC model. This occurs when selection of a matching MOS model for a transistor fails or is disabled.

WHAT NEXT

This message is normally generated in conjunction with other TECH messages. Look for the model name in these other messages. Verify that the source files for this transistor model are compatible with the design process corner.

TECH-027

TECH-027 (Warning) Invalid voltage (%.4f) specified in NanoSim directives. This voltage will be skipped for device evaluation.

DESCRIPTION

NanoTime only accepts positive voltages for device evaluation.

WHAT NEXT

Check the NanoSim voltage directives definition.

TECH-028

TECH-028 (Warning) Incomplete voltage definition found in NanoSim directives, defaulting to %.4f.

DESCRIPTION

NanoTime only accepts positive voltages for device evaluation.

WHAT NEXT

Check the NanoSim voltage directives definition.

TECH-029

TECH-029 (Error) Model %s not found or instance %s nfin or length does not fit into the nfinmax/nfinmin or lmax/lmin range of model. The nfin= %f and the channel length= %.3e .

DESCRIPTION

The finfet transistor parameter nfin or l for bin selection is out of the range of model card.

WHAT NEXT

Check if correct model cards are included.

TECH-030

TECH-030 (Error) Must use single-corner mode for this technology.

DESCRIPTION

This message means that NanoTime does not currently support the transistor model technology used in this design in multi-corner mode.

WHAT NEXT

Use the **set_technology** command to specify a single corner.

TECH-031

TECH-031 (Error) TMI version %s is not supported.

DESCRIPTION

NanoTime supports TMI version up to 2.0.1.

WHAT NEXT

Check the TMI version in the model.

TECH-032

TECH-032 (Error) Incorrect parameter tolerance specification.

DESCRIPTION

Specified transistor instance parameter name is not valid or the tolerance value is below 0.

WHAT NEXT

Specify valid transistor instance parameter name and/or tolerance value.

TECH-033

TECH-033 (Warning) Voltage step scale factor for charge analysis is out of range (Min : %f, Max : %f). The value set by user will be ignored.

DESCRIPTION

The scale factor for charge analysis is not within the valid range. The value will be reset to default value.

WHAT NEXT

Check if the global variable **tech_charge_step_scale_factor** is correctly set.

TECH-034

TECH-034 (Information) Annotating paracap devices using '%s' technology.

DESCRIPTION

This message shows which technology is used for paracap device annotation. NanoTime does not support multi-corner parasitics. Because paracap devices are annotated as parasitic elements, NanoTime chooses one technology corner (max data corner) for paracap device annotation.

WHAT NEXT

No action is necessary.

TECH-035

TECH-035 (Warning) The number of bulk voltage samples for charge sampling, **mos_finfet_charge_table_bulk_samples**, was set too low. It was set to %d and must be at least %d if set by the user.

DESCRIPTION

The number of bulk voltage samples for charge sampling will be increased to bring it into the valid range.

WHAT NEXT

Check if the global variable **mos_finfet_charge_table_bulk_samples** is correctly set.

TECH-036

TECH-036 (Warning) The variable parasitics_wrapper_subckt_technology does not refer to any currently defined technology. The technology associated with max data tracing will be used.

DESCRIPTION

The variable **parasitics_wrapper_subckt_technology** determines which technology file should be used when wrapper subcircuit parasitics are back annotated from a DPF or SPF file. The current setting does not refer to any currently defined or used technology.

Technology files are configured using the **read_spice_model** and **set_technology** commands. The **parasitics_wrapper_subckt_technology** variable should agree with one of the names supplied with the **read_spice_model -name** option, and subsequently associated with a corner in the **set_technology** command.

WHAT NEXT

Use **report_technology** to report the currently defined technologies. Check if the global variable **parasitics_wrapper_subckt_technology** is correctly set.

TIMI Error Messages

TIMI-001

TIMI-001 (warning) Pin %s in timing exception is not a timing point.

DESCRIPTION

The pin must be a timing pin.

WHAT NEXT

Remove all non-timing pins from timing exception commands.

TIMI-002

TIMI-002 (Warning) More than one multicycle path exception found at pin %s.

DESCRIPTION

More than one multicycle path exception was found at the pin.

WHAT NEXT

Use **remove_multicycle_path** to remove the exceptions that should not be applied.

TIMI-003

TIMI-003 (Warning) More than one same_phase or no_same_phase exceptions found at pin %s.

DESCRIPTION

More than one same_phase or no_same phase path exception was found at the pin.

WHAT NEXT

Use **remove_same_phase_path** or **remove_no_same_phase_path** to remove the exceptions that should not be applied.

TIMI-004

TIMI-004 (Warning) Skipping redundant input definition at clock pin %s.

DESCRIPTION

The clock pin was declared more than once.

WHAT NEXT

Check your clock definitions using **report_clock**. Remove unwanted clock definitions using **remove_clock**.

TIMI-005

TIMI-005 (warning) problem evaluating post-trace %s constraint from reference pin %s edge %s to checked pin %s edge %s, likely caused by missing path to %s pin.

DESCRIPTION

NanoTime was unable to evaluate a timing constraint. This condition is usually caused by incomplete clock tree tracing.

WHAT NEXT

Check to see if there are issues in clock network identification and tracing. Use **report_clock_arrivals** to verify that all the clock edges arrived at the constraint's clock pin.

TIMI-006

TIMI-006 (error) Clock pin can only be on first or last pin of a timing exception.

DESCRIPTION

A clock pin was specified in a timing exception, and it was not the first or last pin in the exception.

WHAT NEXT

Check for an incorrect timing exception, or incorrect clock propagation.

TIMI-007

TIMI-007 (error) from option must be on first frame of timing exception.

DESCRIPTION

The from option of a timing exception must come first.

WHAT NEXT

Check for incorrect timing exception command.

TIMI-008

TIMI-008 (error) to option must be on last frame of timing exception.

DESCRIPTION

The to option of a timing exception must come last.

WHAT NEXT

Check for incorrect timing exception command.

TIMI-009

TIMI-009 (error) rise and fall are specified together in this timing exception.

DESCRIPTION

You can specify a pin in a timing exception to be either rise or fall, but not both.

WHAT NEXT

Check for incorrect timing exception command.

TIMI-010

TIMI-010 (warning) problem evaluating %s constraint "%s" between checked/related pin %s edge %s (net %s) and %s reference pin %s edge %s (net %s)%s.

DESCRIPTION

NanoTime was unable to evaluate a timing constraint at the given pin.

WHAT NEXT

Check clock propagation.

TIMI-011

TIMI-011 (warning) Found unknown constraint type at pin %s.

DESCRIPTION

NanoTime was unable to evaluate a timing constraint at the given pin because its type was unknown.

WHAT NEXT

Report this occurrence to Synopsys.

TIMI-012

TIMI-012 (warning) unable to evaluate latch timing at pin %s (edge %s).

DESCRIPTION

NanoTime was unable to evaluate a latch timing constraint at the given pin.

WHAT NEXT

Check clock propagation.

TIMI-013

TIMI-013 (error) Clock and non-clock elements cannot be mixed in a timing exception.

DESCRIPTION

Both clock and data pins have been specified in the same frame of a timing exception.

WHAT NEXT

Check clock propagation.

TIMI-014

TIMI-014 (warning) Pin %s %s is not a timing point.

DESCRIPTION

Not all pins in a netlist are available as timing points. The timing points must be pins in the timing graph. This restriction may be removed in a future release.

WHAT NEXT

Remove all non-timing pins from commands and try to find an equivalent pin which is part of the timing graph.

TIMI-015

TIMI-015 (error) Exceptions defined -to/-from a clock can not be defined -through other pins or nets.

DESCRIPTION

Timing exceptions going to or from a clock must not include any intermediate points. Clock-based exception syntax can not be mixed with pin-based syntax.

WHAT NEXT

Create a new exception that either uses pins instead of clocks or removes the -through qualifiers.

TIMI-016

TIMI-016 (warning) No leaf-level pins corresponded to %s %s.

DESCRIPTION

Timing exceptions are defined at leaf-level pins. Non-pin objects are expanded into a list of leaf-level gate pins or design ports. Some objects are not connected to any leaf-level pins, and therefore cannot be used for timing exception definitions.

WHAT NEXT

Look at the exception definition and change or remove the option with the object that is causing the warning.

TIMI-017

TIMI-017 (error) This timing exception contains an option which expands to zero pins and will be ignored.

DESCRIPTION

Each -to/-from/-through option for a timing exception definition must contain at least one leaf-level pin. If any option expands to no pins at all, the timing exception will have no effect and is therefore discarded.

WHAT NEXT

Look at the exception definition and change or remove the option with the object that is causing the warning.

TIMI-018

TIMI-018 (warning) A data-to-data check path was not saved at endpoint pin %s.

DESCRIPTION

The endpoint was a pin where there is a post-trace data-to-data timing check constraint. A path needed to properly evaluate this check was not saved.

WHAT NEXT

This could be caused by using a **set_find_path** constraint or by model generation not needing paths saved at some internal check points.

TIMI-019

TIMI-019 (warning) The expected switching edge %s was not found at pin %s when traversing to pin %s within a precharge/predischarge element.

DESCRIPTION

The expected switching direction was not found in the precharge/predischarge circuit.

WHAT NEXT

Look at the topology definitions at or near these pins and verify their correctness.

TIMI-020

TIMI-020 (Error) Port or pin (%s) must be clocked.

DESCRIPTION

Pin (or port) of the timing check is not clocked.

WHAT NEXT

Specify a clocked pin (or port) for the pin.

TIMI-021

TIMI-021 (Error) Port or pin (%s) must not be clocked.

DESCRIPTION

Pin (or port) of the timing check is clocked.

WHAT NEXT

Specify a non-clocked pin (or port) for the pin.

TIMI-023

TIMI-023 (Error) Port or pin (%s) must belong to a leaf element.

DESCRIPTION

Pin or port of the timing check is not at the leaf level.

WHAT NEXT

Specify a leaf pin or port for the timing check.

TIMI-024

TIMI-024 (warning) The ratio %.1f of transition time %.3f at pin %s to the default transition time %.3f exceeds the user specified ratio %.1f.

DESCRIPTION

A large transition time could indicate incorrect port settings.

WHAT NEXT

Check the port boundary settings.

TIMI-025

TIMI-025 (warning) The %s for selecting paths does not contain any valid timing points.

DESCRIPTION

When selecting paths the selection criteria must be at valid timing points. These are typically found at the boundary of channel connected regions. Paths are identified and reported at these boundary points and must be selected accordingly.

WHAT NEXT

Check your path selection criteria. Make adjustments to the selection criteria so that they all occur on the boundary of channel connected regions.

TIMI-027

TIMI-027 (error) Because %s, timing check associated cannot be created.

DESCRIPTION

When using the option -use_existing_timing_points while creating timing checks, the specified pins must be available as timing points in the timing graph and each timing point must have delay arcs to it with the required direction.

WHAT NEXT

Remove the option -use_existing_timing_points from the command when creating a new timing check. The check_design command will need to be run again and a timing graph with the pin will be created.

TIMI-028

TIMI-028 (warning) did not find transparency information at pin %s where %g ns error recovery was applied.

DESCRIPTION

Transparency information is expected at pins where latch error recovery is applied.

WHAT NEXT

Transparency depth limit can be used when non-transparent model generation is a workaround.

TIMI-029

TIMI-029 (error) System resources are not available: %s.

DESCRIPTION

The necessary system resources are not available. This message is usually caused by running out of virtual memory or not sufficient disk space.

WHAT NEXT

Check if there is sufficient amount of memory and disk space.

TIMI-030

TIMI-030 (error) NanoTime sub-process was killed by a signal.

DESCRIPTION

NanoTime subprocess was killed by a signal generated by either a user command or the operating system. Typically, the OS generates the signal in the case of insufficient system resources.

WHAT NEXT

Check if there is a sufficient amount of memory and disk space.

TIMI-031

TIMI-031 (Warning) Ambiguous hold timing check from reference pin %s %s to checked pin %s %s.

DESCRIPTION

NanoTime was unable to definitively pair a hold check with one of the setup checks at the specified pins. It assumes the existence of an equal number of setup and hold timing checks at a model pin.

WHAT NEXT

Use the command **set_no_same_phase_path** to tighten the phasing of the hold check if necessary.

TIMI-032

TIMI-032 (Warning) Adding si_timing_window_overlap_tolerance caused infinite windows on %d unfiltered coupled nets (%.2f%%).

DESCRIPTION

NanoTime sets infinite timing windows when adding the si_timing_window_overlap_tolerance to a net timing window results in the timing window exceeding the clock period.

WHAT NEXT

Consider lowering the value used for si_timing_window_overlap_tolerance.

TIMI-033

TIMI-033 (Error) Object %s of type %s does not match object %s of type %s.

DESCRIPTION

Inside a from/through/to clause, the objects must be of the same type prior to check_topology. After check_topology, objects may be of different types.

WHAT NEXT

Separate the command into multiple commands, or rewrite using the similar object types.

TIMI-034

TIMI-034 (error) Found timing constraint '%s' from fast launch clock %s to slow capture clock %s with non-integer period multiple %g at checked pin %s%s.

DESCRIPTION

NanoTime might not accurately evaluate a timing constraint when the capture clock is slower than the launch clock and the capture clock period is not an integer multiple of the launch clock period. If the launch or capture clocks are generated clocks, then the periods of these generated clocks are to be used in calculating the multiple. The multiple is not affected by the duty cycle of the respective clocks.

WHAT NEXT

Apply launch or capture cycle adjustments as needed.

TIMI-035

TIMI-035 (Warning) Coefficient values specified on both the trigger '%s' and target '%s' pins.

DESCRIPTION

Delay coefficient values can be specified on trigger pins, target pins, or trigger-target pairs. When more than one of these definitions exists then the order of precedence is trigger-target pair first, then target,

then trigger.

WHAT NEXT

Determine if the coefficients specified are correct. If not, remove or modify the commands that create the delay coefficients.

TIMI-036

TIMI-036 (Warning) The %s pulse width check to clock pin '%s' of untapped differential synchronizer not allowed on feedback pins and can cause incorrect clock width due to unadjusted arrivals. Please remove.

DESCRIPTION

Untapped differential synchronizers are feedback transistors that do not have delay arcs spanning them. Consequently, any arrival times at their gate endpoints remain unadjusted (for example, with respect to generated clock waveforms on corresponding nets) and lead to unrealistic pulse width waveforms.

WHAT NEXT

Filter the transistors on which the checks are applied by using the **is_differential_synchronizer** and **is_differential_synchronizer_tapped_transistor** cell attributes.

TIMI-037

TIMI-037 (Warning) Setting the variable timing_max_transparency_begin_margin %s can lead to %s.

DESCRIPTION

The variable timing_max_transparency_begin_margin should only be used for special circumstances. If it is set to a negative value, then paths that could not feasibly pass through a transparent latch may be found. If it is set to a positive value, then a critical path through a transparent latch may be suppressed.

WHAT NEXT

Leave this variable at the default value of zero unless there is a what-if scenario that needs to be explored.

TIMI-038

TIMI-038 (error) Exactly one level of '%s' option is required per '%s' exception.

DESCRIPTION

That option can only be specified once per exception.

WHAT NEXT

Make sure one and only one occurrence of that option is specified.

TIMI-039

TIMI-039 (Information) Non-pulse %sclock %s was found to have coincident base cycle rise and fall times of %g.

DESCRIPTION

Non-pulse clocks are expected to have distinct base cycle rise and fall times. The given clock does not meet this expectation.

WHAT NEXT

Ensure correct clock waveform definition.

TIMI-040

TIMI-040 (Warning) Edges used to define generated pulse clock %s are inconsistent with the waveform at the clock definition point in the design.

DESCRIPTION

NanoTime expects a generated pulse clock's waveform at the clock definition point in the design obtained by path tracing to be consistent with the clock edges specified as part of the generated clock's defnition. The given generated clock does not meet this expectation.

WHAT NEXT

Ensure that the edges chosen to define the pulse clock are consistent with the clock generation circuitry.

TIMI-041

TIMI-041 (Warning) Large duty cycle of %g%% found for %spulse clock %s.

DESCRIPTION

Pulse clocks are expected to have small duty cycles. The timing check clock phasing relationships are based on this expectation. The given pulse clock does not meet this expectation where it is defined.

WHAT NEXT

Remove the pulse property from the clock by applying **mark_clock_network -no_pulse**.

TIMI-042

TIMI-042 (warning) Timing constraint '%s' at checked pin %s matches a set_common_required_capture_path exception, but no capture path exists at reference pin %s that passes through the common required point.

DESCRIPTION

If NanoTime evaluates a timing check at a checked point matching a **set_common_required_capture_path** exception, capture paths exist, but none of the capture paths themselves pass through the common required point, then this warning is issued. The timing check is suppressed and will show up as untested in **report_analysis_coverage**.

WHAT NEXT

Make sure the **set_common_required_capture_path** exception is specified correctly and ensure that no other exception is blocking capture paths through the common point using **report_exceptions**.

TIMI-043

TIMI-043 (Warning) The variation value %f set by command 'set_libcell_variation_parameters' will override LVF table for library cell %s.

DESCRIPTION

The variation information for a cell can be specified in multiple ways. NanoTime tool can read LVF tables in

library files. **set_libcell_variation_parameters** can be used to set variation values for the library cell. When a library cell has LVF tables and user specifies variation values for the cell using the command, the value set by the command is used in analysis.

WHAT NEXT

Make sure the **set_libcell_variation_parameters** is used for correct library cells.

TIMI-044

TIMI-044 (warning) Timing constraint '%s' at checked pin %s matches a set_exclude_reference_path exception, but all capture paths have been excluded at reference pin %s.

DESCRIPTION

If NanoTime evaluates a timing check at a checked point matching a **set_exclude_reference_path** exception and all capture paths have been excluded, then this warning is issued. The timing check is suppressed and will show up as untested in **report_analysis_coverage**.

WHAT NEXT

Make sure the **set_exclude_reference_path** exception is specified correctly and ensure that no other exception is blocking capture paths through non-excluded through points using **report_exceptions**.

TIMI-045

TIMI-045 (Warning) The variation definition is within tolerance of a previous definition. The new definition will replace the previous definition.

DESCRIPTION

The following parameters are used to determine if a transistor is unique: tech_pocv_match_length_pct, tech_pocv_match_voltage_pct, tech_pocv_match_wrapper_parameter_pct.

If a new definition matches the length, voltage, and wrapper parameters within the specified margins, it will be considered the same. In this case the new definition will replace the existing definition.

WHAT NEXT

Check the definitions made by set_variation_parameters for correctness. Check the values of the variables tech_pocv_match_length_pct, tech_pocv_match_voltage_pct, tech_pocv_match_wrapper_parameter_pct and be sure they have the desired resolution.

TLIB Error Messages

TLIB-001

TLIB-001 (Error) Failed to read in lib_topology netlist named '%s' in a topology library.

DESCRIPTION

Failed to read in specified lib_topology netlist.

WHAT NEXT

The netlist must be a valid spice format file.

TLIB-002

TLIB-002 (Error) Cannot read topology library named '%s'. A library with this name already exists.

DESCRIPTION

The topology library cannot be read in because its name conflicts with a library which has already been read in. The name of each library must be unique. The topology library's name is the name of the directory which contains the library files.

WHAT NEXT

Determine if this is the same library being read in twice, or two different libraries. If the latter, one of the libraries must be renamed.

TLIB-003

TLIB-003 (Error) Could not read .libt file '%s'.

DESCRIPTION

The file could not be read. The file must include only one valid create_lib_topology command.

WHAT NEXT

Review the file and correct any syntax errors, remove any other commands, etc.

TLIB-004

TLIB-004 (Error) Could not read .ntlib file '%s'.

DESCRIPTION

The file could not be read. The file must include only one valid create_topology_library command.

WHAT NEXT

Review the file and correct any syntax errors, remove any other commands, etc.

TLIB-005

TLIB-005 (Warning) %s. Marked by %s. Ignore topology marked by %s.

DESCRIPTION

Ignore topology when the same type of topology detected. The topology marking follows the precedence order. If multiple topologies detected on the same net, the one with lower precedence order is ignored. The user marked topology always has higher precedence order than the NT algorithmic searched one. For user marked topologies, they are firstly sorted according to the user topology library they belong to. User need to explicitly set the library order in topo_library_order variable. Within a library, the default order is ascending alphanumerical order by lib_topology name. User can explicitly set the lib_topology order using -search_priority option in the lib_topology definition. The lib_topologies are sorted in ascending alphanumerical order by assigned search_priority value. Any lib_topology with an assigned search_priority has higher precedence order than regular lib_topologies.

WHAT NEXT

Check the precedence orders of the topology being detected and ignored. The topo_library_order and the -search_priority may change the default the precedence order.

TLIB-006

TLIB-006 (Error) Topology library named '%s' was not found.

DESCRIPTION

The specified topology library cannot be found. The library is either not read in or removed.

WHAT NEXT

The topology library may be specified in the **topo_library_order** variable or a command. If the library is specified in the variable, it needs to be read in before the **match_topology** command for library search.

TLIB-007

TLIB-007 (Warning) Topology library named '%s' missing from topo_library_order variable is NOT searched.

DESCRIPTION

Only topology libraries in the **topo_library_order** variable are searched. By default, only the common library is included in the variable.

WHAT NEXT

If the missing topology library needs to be searched, check the **topo_library_order** variable. If the variable is not set or does not include the missing topology library, set the variable to include the library.

TLIB-008

TLIB-008 (Error) Could not remove library named '%s'. lib_topology named '%s' in the library cannot be removed.

DESCRIPTION

There are topologies marked by the lib_topologies in the library.

WHAT NEXT

Check whether the topologies of the lib_topologies should be erased. If yes, erase the topologies before removing the library.

TLIB-009

TLIB-009 (Error) File '%s': line %d: %s.

DESCRIPTION

An error occurred while parsing a topology library file.

WHAT NEXT

Make sure all required topology libraries have been read in before running the **list_lib_topology** command.

TOPO Error Messages

TOPO-001

TOPO-001 (warning) No clock pin found for candidate latch net %s.

DESCRIPTION

No clock pin is controlling the latch on the specified net.

WHAT NEXT

Check to see that the clock is being propagated correctly to the latch.

TOPO-002

TOPO-002 (error) Transistor (%s) in this mark_inverter command is not an NMOS transistor.

DESCRIPTION

The transistor specified with the **-n_transistor** option of the **mark_inverter** command is not an NMOS transistor. The **mark_inverter** command will be ignored.

WHAT NEXT

Check that the name of the transistor is correct.

TOPO-003

TOPO-003 (error) Transistor (%s) in this mark_inverter command is not a PMOS transistor.

DESCRIPTION

The transistor specified with the **-p_transistor** option of the **mark_inverter** command is not a PMOS

transistor. The **mark_inverter** command will be ignored.

WHAT NEXT

Check that the name of the transistor is correct.

TOPO-004

TOPO-004 (error) The transistors (%s, %s) in this mark_inverter command do not drive the same output net.

DESCRIPTION

The two transistors specified in the **mark_inverter** command must drive the same output net.

WHAT NEXT

Check that the names of the transistors are correct.

TOPO-005

TOPO-005 (error) The transistors (%s) in this mark_inverter command are not connected to the same input net.

DESCRIPTION

The gate terminals of the transistors specified in the **mark_inverter** command must be connected to the same input net.

WHAT NEXT

Check that the names of the transistors are correct.

TOPO-006

TOPO-006 (error) The output of the transistors (%s, %s) in this mark_inverter command are connected to a power or ground net (%s).

DESCRIPTION

The output of the transistors specified in the **mark_inverter** command cannot be connected to a power or ground net. The **mark_inverter** command will be ignored.

WHAT NEXT

Check that the names of the transistors are correct.

TOPO-007

TOPO-007 (warning) No clock pin specified for this mark_latch command.

DESCRIPTION

A **mark_latch** command was found that did not specify a clock pin. If clock pins are not specified, NanoTime will attempt to locate them. If they cannot be located, no setup or hold checks will be done for the latch.

WHAT NEXT

Add a clock pin specification to the **mark_latch** command.

TOPO-008

TOPO-008 (warning) No feedforward devices were inferred for latch (Net %s is latch net).

DESCRIPTION

An output net was specified in this **mark_latch** command, but no feedforward devices were specified. NanoTime was not able to infer feedforward devices for this latch.

WHAT NEXT

Add a feedforward device specification to the **mark_latch** command.

TOPO-009

TOPO-009 (error) Feedforward devices were specified in this mark_latch command, but no output net was specified (Net %s is latch output).

DESCRIPTION

If feedforward devices are specified in a **mark_latch** command, an output net must be specified as well.

WHAT NEXT

Add an output net specification to the **mark_latch** command.

TOPO-010

TOPO-010 (error) Feedback devices were specified in this mark_latch command, but no output net was specified.

DESCRIPTION

If feedback devices are specified in a mark_latch command, an output net must be specified as well.

WHAT NEXT

Add an output net specification to this command.

TOPO-011

TOPO-011 (warning) An output net was specified in this mark_latch command, but no feed forward devices were specified. A feedforward network has been inferred.

DESCRIPTION

No feed forward devices were specified in the mark_latch command, and a feed forward network has been inferred.

WHAT NEXT

Add a feed forward device specification to the mark_latch command, or verify that the inferred feed forward devices are correct.

TOPO-012

TOPO-012 (warning) No feedforward devices were specified (Net %s is latch node).

DESCRIPTION

An output net was specified in the **mark_latch** command, but no feedforward devices were specified. If an output net is specified in a **mark_latch** command, then feedforward devices should be specified as well.

WHAT NEXT

Add a feedforward device specification to the **mark_latch** command.

TOPO-013

TOPO-013 (warning) No transistor gate pins found connected to latch output net '%s', net '%s' is latch net.

DESCRIPTION

A net was specified as the output net for a latch, and that net does not connect to any transistor gate pins. No "setup to latch output" will be done for the latch.

WHAT NEXT

Make sure the latch output was specified correctly.

TOPO-014

TOPO-014 (warning) Inferred clock pin for latch (Net %s is latch node, pin %s is clock pin)

DESCRIPTION

No clock pins were specified in the **mark_latch** command for this latch. NanoTime has inferred a clock pin.

WHAT NEXT

Use the **-clock** option of the **mark_latch** command to explicitly specify the clock pin for the latch.

TOPO-015

TOPO-015 (warning) No clock pins inferred for latch (Net %s is latch node)

DESCRIPTION

No clock pins were specified in the **mark_latch** command for this latch, and NanoTime could not find any clock pins.

WHAT NEXT

Use the **-clock** option of the **mark_latch** command to explicitly specify the clock pin for the latch.

TOPO-016

TOPO-016 (warning) Inferred clock pin for latch (latch net %s, clock pin %s)

DESCRIPTION

No clock pins were specified in the **mark_latch** command for this latch. NanoTime has inferred a clock pin.

WHAT NEXT

Use the **-clock** option of the **mark_latch** command to explicitly specify the clock pin for the latch.

TOPO-017

TOPO-017 (warning) No clock pins inferred for latch (Net %s is latch node)

DESCRIPTION

No clock pins were specified in the **mark_latch** command for this latch, and NanoTime could not find any clock pins.

WHAT NEXT

Use the **-clock** option of the **mark_latch** command to explicitly specify the clock pin for the latch.

TOPO-018

TOPO-018 (warning) Inferred feedforward transistor for latch (Net %s is latch node, element %s is transistor)

DESCRIPTION

An output net was specified for this **mark_latch** command, but no feedforward transistors were specified. NanoTime has inferred a feedforward device for the latch.

WHAT NEXT

Use the **-feedforward** option of the **mark_latch** command to explicitly specify the feedforward objects for the latch.

TOPO-019

TOPO-019 (error) Clock did not propagate to clock pin of latch (latch net %s, clock pin %s, clock pin connected to net %s)

DESCRIPTION

The clock pin specified in the **mark_latch** command for this latch is connected to a net that is not classified as a clock.

WHAT NEXT

Verify that the clock pins are specified correctly and check the clock propagation.

TOPO-020

TOPO-020 (error) No clock pins specified in mark_latch command.

DESCRIPTION

No clock pins were specified in the **mark_latch** command.

WHAT NEXT

Add clock pins to the **mark_latch** command.

SEE ALSO

topo_auto_find_latch_clock(3)

TOPO-021

TOPO-021 (error) Transistor (%s) in this mark_inverter has already been marked as a feedback.

DESCRIPTION

A transistor identified in a **mark_inverter** command has been marked as a feedback transistor. This command will be ignored.

WHAT NEXT

Check to see if a **mark_feedback** command was issued.

TOPO-022

TOPO-022 (error) Transistor (%s) in this mark_tgate command is not an NMOS transistor.

DESCRIPTION

The transistor specified in the **-n_transistor** option of a **mark_tgate** command is not an NMOS transistor. The command will be ignored.

WHAT NEXT

Check to be sure the name of the transistor is correct.

TOPO-023

TOPO-023 (error) Transistor (%s) in this mark_tgate command has already been marked as a feedback.

DESCRIPTION

A transistor identified in a **mark_tgate** command has been marked as a feedback transistor. This command will be ignored.

WHAT NEXT

Check to see if a **mark_feedback** command was issued.

TOPO-024

TOPO-024 (error) Transistor (%s) in this mark_tgate command is not a PMOS transistor.

DESCRIPTION

The transistor specified in the **-p_transistor** option of a **mark_tgate** command is not a PMOS transistor. This command will be ignored.

WHAT NEXT

Check to be sure the name of the transistor is correct.

TOPO-025

TOPO-025 (Information) Clock propagations from clock %s and clock %s intersect at net %s.

DESCRIPTION

Different clock domains intersect on the same net. NanoTime propagates both clocks forward.

WHAT NEXT

If the clock networks are correct, and if you want only one clock to propagate, use the **mark_clock_network -stop_propagation** command to stop propagating the undesired clock. If the clock intersection is caused by incorrect clock domain recognition, use the **topo_clock_propagation_strict_logic_check** variable to take case analysis and logic constraints into account during clock propagation.

TOPO-026

TOPO-026 (Warning) Topology specified does not have no_same_phase attribute.

DESCRIPTION

Only sequential topologies have the no_same_phase attribute.

WHAT NEXT

Check to see if the type of topology is correct.

TOPO-027

TOPO-027 (warning) Mixed keeper types for multiple output precharge gate, net %s has keeper type %s, net %s has keeper type %s.

DESCRIPTION

NanoTime does not support multiple keeper types on the same precharge gate.

WHAT NEXT

Use the **mark_precharge** command again, carefully specifying the keeper information.

TOPO-028

TOPO-028 (Warning) Topology specified does not have %s attribute.

DESCRIPTION

Only latch, precharge, gated clock, and register file topologies have the **non_transparent** attribute. The gated clock topology does not have the **edge_triggered** attribute.

WHAT NEXT

Check to see if the type of topology is correct.

TOPO-029

TOPO-029 (error) No clock pins specified for user-marked latch (Net %s is latch node)

DESCRIPTION

No clock pins were specified in the **mark_latch** command for this latch, and NanoTime could not find a clock pin. NanoTime cannot go beyond check_topology.

WHAT NEXT

Use the **-clock** option of the **mark_latch** command to explicitly specify the clock for the latch.

TOPO-030

TOPO-030 (Warning) User-marked precharge (net %s) not recognized.

DESCRIPTION

A net was marked as a precharge evaluation net, but NanoTime was not able to find a corresponding precharge gate.

WHAT NEXT

Check the **mark_precharge** command.

TOPO-031

TOPO-031 (warning) Inferred feedforward transistor is already a feedback transistor of the latch (Net %s is latch node, element %s is transistor). Inferred feedforward transistor is being ignored.

DESCRIPTION

An output net was specified for this **mark_latch** command, but no feedforward transistors were specified. NanoTime tried to infer a feedforward device for the latch, but the device found was already marked as a feedback device. This feedforward device is being dropped from the list.

WHAT NEXT

Use the **-feedforward** option of the **mark_latch** command to explicitly specify the feedforward device. Verify the functionality of the feedback device.

TOPO-032

TOPO-032 (Warning) Topology specified does not have '%s' attribute '%s'.

DESCRIPTION

Valid setup types for latch and flip_flop are input, latch_net and output. Valid setup types for precharge are input, evaluate_net and output. Valid hold types for latch and flip_flop are latch_net and input. Valid hold types for precharge are evaluate_net and input.

WHAT NEXT

Check to see if the type of topology matches the type of check.

TOPO-033

TOPO-033 (error) Unable to find output net for precharge topology at evaluate net '%s' having latch type '%s'.

DESCRIPTION

The output net needed for the setup_to output could not be found.

WHAT NEXT

Define a latch topology at the evaluate net using **mark_latch** and specify the output explicitly with the **-output** option.

TOPO-034

TOPO-034 (error) Incomplete latch definition for precharge topology at evaluate net '%s' having latch type '%s'.

DESCRIPTION

The output net corresponding to a precharge evaluate net is determined using a latch definition. The latch definition found at the evaluate net did not include the output net needed for the setup_to output.

WHAT NEXT

Define a latch topology at the evaluate net using **mark_latch** and specify the output explicitly with the **-output** option.

TOPO-035

TOPO-035 (error) Clock gate topology's transparency status can not be modified after %s.

DESCRIPTION

The transparency status of a gated clock topology must be set before **check_design** is executed. No modifications can take place after that without resetting the design to an earlier state.

WHAT NEXT

Modify your input script to set the transparency status before **check_design** or use the command **reset_design** to move to an earlier state.

TOPO-036

TOPO-036 (error) Cannot trace 'force clock propagation' net %s back to a clock.

DESCRIPTION

A net marked with as a 'force propagation' net with the backward option (**mark_clock_network -force_propagation -backward**) is required to trace back to a clock net. NanoTime was unable to do so.

WHAT NEXT

Check the net name and ensure that it traces back to a clock net.

TOPO-037

TOPO-037 (warning) Mux found at net %s without appropriate enable control logic.

DESCRIPTION

A mux structure that does not have the proper enable control logic has been identified.

WHAT NEXT

Provide the appropriate logic constraint relationship for the enable pins using the **set_logic_constraint** command.

TOPO-038

TOPO-038 (error) One of the evaluate nets (%s) specified in this mark_precharge command does not connect to the source or drain pin of any precharge clock transistor.

DESCRIPTION

One of the evaluate nets specified with the **-evaluate_net** option of the **mark_precharge** command is

not connected to any of the precharge clock transistors specified with the **-precharge_clock** option. The **mark_precharge** command will be ignored.

WHAT NEXT

Check that the names of the evaluate nets and precharge clock transistors match.

TOPO-039

TOPO-039 (warning) Unable to find %s clock arrival at pin %s.

DESCRIPTION

One of the timing checks stemming from the **-stop_propagation** option of the **mark_clock_network** command was impacted.

WHAT NEXT

Check that the clock gating circuit driving the marked net has complementary clock and data pins (as in the case of a nand or a nor clock gater).

TOPO-040

TOPO-040 (error) Unable to create clock stop propagation timing checks for net %s because %s.

DESCRIPTION

The timing checks stemming from the **-stop_propagation** option of the **mark_clock_network** command could not be installed.

WHAT NEXT

Check that the specified net is eligible for clock stop propagation.

TOPO-041

TOPO-041 (warning) Not marking possible mux like structure, due to the lack of appropriate enable control logic, found at net %s.

DESCRIPTION

A mux-like structure is detected that does not have the proper enable control logic. The structure has not been marked as a mux.

WHAT NEXT

Provide the appropriate logic constraint relationship for the enable pins using the **set_logic_constraint** command.

TOPO-042

TOPO-042 (error) Output net is same as evaluate net '%s' for precharge having latch type '%s'.

DESCRIPTION

The output net corresponding to a precharge evaluate net is determined using a latch definition. The latch definition found at the evaluate net declares the evaluate net itself as the output net.

WHAT NEXT

Define a latch topology at the evaluate net using **mark_latch** and specify the output explicitly with the **-output** option.

TOPO-043

TOPO-043 (Warning) Latch net (%s) for latch is identical to the latch output net.

DESCRIPTION

The latch net for a latch should be different from the output net of the latch.

WHAT NEXT

Check the **mark_latch** command to ensure that the latch net and output net are not the same.

TOPO-044

TOPO-044 (error) No keeper transistors specified for a precharge having latch type '%s'.

DESCRIPTION

Keeper transistors are required when the precharge latch type is other than **none**.

WHAT NEXT

Check the options for the **mark_precharge** command.

TOPO-045

TOPO-045 (Warning) Logic constraint conflict detected at mux net (%s) on the mux select nets. Removing mux marking.

DESCRIPTION

When applying automatic logic constraint, a conflict was found with already existing logic constraints.

TOPO-046

TOPO-046 (Warning) Logic constraint conflict detected at user defined mux net (%s) on the mux select nets. Disabling mux marking.

DESCRIPTION

When applying automatic logic constraint, a conflict was found with already existing logic constraints.

WHAT NEXT

Modify the **mark_mux** command to specify the appropriate logic constraint and constraint type.

TOPO-047

TOPO-047 (Warning) Removing feedback marking from transistor %s as it is marked as a feedforward device for latch net %s.

DESCRIPTION

A feedforward device, which is part of a latch, was also marked as a feedback. The feedback marking will now be removed as a transistor cannot be marked as a feedforward and a feedback.

WHAT NEXT

Examine the various topologies involved for correctness.

TOPO-049

TOPO-049 (Warning) Latch output net %s of latch net %s does not drive the feedback stack.

DESCRIPTION

The latch output is required to drive the feedback stack of a latch. Check the **mark_latch** command associated with this latch net and ensure that the latch output drives the feedback stack.

WHAT NEXT

Examine the **mark_latch** command for correctness.

TOPO-050

TOPO-050 (warning) No feedback transistors inferred for latch (Net %s is latch net)

DESCRIPTION

No feedback transistors were specified in the **mark_latch** command for this latch, and NanoTime could not find any feedback transistors.

WHAT NEXT

Use the **-feedback** option of the **mark_latch** command to explicitly specify the feedback transistors for the latch.

TOPO-051

TOPO-051 (information) Annotating %d MUX-based 2-input XORs.

DESCRIPTION

NanoTime has found MUX-based 2-input XOR circuits in the input, and it is updating the delay calculation information for these circuits in order to remove pessimism from the delay calculation.

A 'Mux-based 2-input XOR' is identified as two oppositely controlled tgates whose output's are connected to the same net, and whose inputs are connected by an inverter.

WHAT NEXT

No action is necessary.

To disable this processing, set **timing_enable_mux_xor_pessimism_removal** to false.

TOPO-052

TOPO-052 (information) Modifying delay calculation from pin %s(edge %s) to pin %s(edge %s) due to a MUX-based XOR circuit.

DESCRIPTION

NanoTime has found MUX-based 2-input XOR circuits in the input, and it is updating the delay calculation information for these circuits in order to remove pessimism from the delay calculation.

WHAT NEXT

No action is necessary.

To disable this processing, set **timing_enable_mux_xor_pessimism_removal** to false.

TOPO-053

TOPO-053 (Warning) A conflict exists between a user-defined latch and a user-forced clock at net %s. Latch is not marked. Latch feedback devices are automatically inferred as feedback devices.

DESCRIPTION

A user-defined latch should not be defined with the latch net as part of the clock network. A user-defined latch and a user-forced clock definition have been defined at the same net.

WHAT NEXT

Check the **mark_latch** and **mark_clock_network -force_propagation** commands that have been issued and resolve the conflict.

TOPO-054

TOPO-054 (Warning) Possible logic conflict may hinder setup check to latch output net %s due to clock gating; attaching setup check to latch net %s.

DESCRIPTION

A logic conflict between the clock of the latch and that of the feedforward gated clock device can cause a simulation failure.

WHAT NEXT

If the logic conflict will not occur, an additional user defined setup check at the latch output net can be created.

TOPO-055

TOPO-055 (Warning) Channel connected block has no output net; setting transistor %s as non-directional.

DESCRIPTION

The channel connected block has no output net. Cannot decide the signal propagation direction through the transistors because there is no output to drive.

WHAT NEXT

Check to see that the nets in the channel connected block get correct connections.

TOPO-056

TOPO-056 (Error) Clock propagation is not complete.

DESCRIPTION

Commands in lib_topology's post_clock_propagation and post_match_topology phase points change the clock network after the clock propagation. The clock network is incomplete.

WHAT NEXT

Move the commands to the pre_match_topology phase point.

TOPO-057

TOPO-057 (warning) Clock network and topology are reset by command '%s' in lib_topology '%s' at phase point '%s'.

DESCRIPTION

NanoTime repropagates the clock network and reruns topology recognition when executing the command listed in the error message. The command cannot be used in the lib_topology post_clock_propagation, post_match_topology, pre_check_topology, post_check_topology, pre_check_design, and post_check_design phase points.

WHAT NEXT

Move the command to the lib_topology pre_match_topology phase point.

TOPO-058

TOPO-058 (Warning) Because pin %s is a %s pin, fanout delay arcs from that pin and timing checks associated with them will be removed.

DESCRIPTION

Certain commands such as 'mark_instance -dont_search_through_gate' can have unintended consequences during the ensuing timing analysis if used incorrectly. These consequences due to incorrect usage can include loss of accuracy and incomplete timing checks.

WHAT NEXT

Check to see if there are alternative ways to accomplish the same results without unwanted side effects.

TOPO-059

TOPO-059 (Warning) Because transistor %s is a %s transistor, delay arcs and timing checks based on delay arcs through that transistor will be removed.

DESCRIPTION

Certain commands such as 'mark_instance -dont_search_through_channel' can have unintended consequences during the ensuing timing analysis if used incorrectly. These consequences can include loss of accuracy and incomplete timing checks.

WHAT NEXT

Check to see if there are alternative ways to accomplish the same result without unwanted side effects. Consult relevant Synopsys SolvNet articles.

TOPO-060

TOPO-060 (Warning) Gate input nets '%s' to bidirectional transistors '%s' in a register file (or ram cells) have no logic constraints.

DESCRIPTION

When a bidirectional pass transistor in a ram cell has no logic constraint, there could be unintended consequences like long run time during check_design phase.

WHAT NEXT

Assign logic constraints on the set of nets or set directions of the pass transistors.

TOPO-061

TOPO-061 (Warning) Found delay arc for %s latch topology structure (name %s, output net %s) from an input of its feedforward device back to the latch net.

DESCRIPTION

The feedforward and feedback transistors of a latch structure must not have any common transistor.

WHAT NEXT

Check the correctness of mark_latch commands.

TOPO-062

TOPO-062 (Warning) User specified transistor direction %s overwrites the existing direction %s on

transistor %s.

DESCRIPTION

A transistor direction has been overwritten by a user-specified direction. NanoTime accepts the user-specified direction as correct and uses the newly specified direction for all aspects of the analysis, including path tracing and delay calculation. You have the responsibility to ensure that the new direction is correct.

WHAT NEXT

Use the **report_transistor_direction** command to verify that the specified direction is correct.

TOPO-063

TOPO-063 (Information) Marked %d nets as clock nets.

DESCRIPTION

This message describes the number of nets that were marked as clock nets.

WHAT NEXT

No action is necessary.

TOPO-064

TOPO-064 (warning) Only one side of transmission gate is marked as clock (pin %s is specified as clock pin, pin %s is not specified) for user-marked latch (Net %s is latch node).

DESCRIPTION

If one side of transmission gate is marked as clock pin in the **mark_latch** command, NanoTime requires the other side also to be marked as clock pin.

WHAT NEXT

Check the **-clock** option of the **mark_latch** command to specify the complete clock pin list for the latch.

TOPO-065

TOPO-065 (warning) Latch feedback device %s is marked or auto-recognized as clock pin %s for user-marked latch (Net %s is latch node).

DESCRIPTION

Latch feedback devices are marked or auto-recognized as clock pin in the **mark_latch** command.

WHAT NEXT

Check the **-feedback** and **-clock** options of the **mark_latch** to correct the clock pin list for the latch. Check the variable **topo_auto_find_latch_feedback_clock**. The latch clock pin auto-recognition includes latch feedback devices when the **topo_auto_find_latch_feedback_clock** is true.

TOPO-066

TOPO-066 (error) The maximum number of inputs for a channel connected region %d was exceeded by a region with %d inputs.

DESCRIPTION

In order to facilitate correct timing graph construction and avoid excessive runtime NanoTime limits the maximum number of inputs to a channel connected region. Anything exceeding the limit will be ignored during analysis.

WHAT NEXT

Check the input netlist for errors. Make sure all power nets are defined. The variable topo_ccb_max_number_of_inputs can be reset to a higher value to allow the channel connected region to be processed.

TOPO-067

TOPO-067 (error) Channel connected region containing net %s has %d inputs which exceeds the maximum number of inputs %d.

DESCRIPTION

In order to facilitate correct timing graph construction and avoid excessive runtime NanoTime limits the maximum number of inputs to a channel connected region. Anything exceeding the limit will be ignored during analysis.

WHAT NEXT

Check the input netlist for errors. Make sure all power nets are defined. The variable topo_ccb_max_number_of_inputs can be reset to a higher value to allow the channel connected region to be processed.

TOPO-068

TOPO-068 (Warning) Overwriting user defined register file at net(s) %s and %s.

DESCRIPTION

Only one register file can be defined on a net. When multiple definitions overlap the most recent definition is the only one preserved.

WHAT NEXT

Check the mark_register_file commands and determine if they are correct. It may be possible to merge them together and define sets of clock transistors.

TOPO-069

TOPO-069 (warning) Maximum clock gate depth of %d exceeded at net %s during clock propagation.

DESCRIPTION

NanoTime limits the maximum number of clock gates the clock flag propagates through in order to avoid excessive clock propagation in the event of an incorrect design build. When the limit is reached, the clock flag does not propagate any further from the point.

WHAT NEXT

The variable topo_clock_gate_depth can be reset to a higher value to allow the clock flag to be propagated further.

TOPO-070

TOPO-070 (Error) %ld transistors with unresolved directions found.

DESCRIPTION

Transistors have unresolved directions.

WHAT NEXT

Report transistor directions and fix unresolved directions.

TOPO-071

TOPO-071 (Warning) %ld transistors with unresolved directions found. Use strict transistor direction checking flow to avoid missing paths, false paths, or increased runtime.

DESCRIPTION

Transistors have unresolved directions.

WHAT NEXT

Report transistor directions and fix unresolved directions.

TOPO-072

TOPO-072 (Error) Found storage nodes in error condition.

DESCRIPTION

Potential storage nodes are not marked as sequential topologies or do not connect to the clock network.

WHAT NEXT

Report storage nodes and fix the error.

TOPO-073

TOPO-073 (Error) Found the clock network in error condition.

DESCRIPTION

The clock network has invalid end points or there are nets which are required to be clock but are not part of the clock network.

WHAT NEXT

Report the clock network and fix the error.

TOPO-074

TOPO-074 (Error) Transistors specified in the topology marking command are insufficient for pattern matching.

DESCRIPTION

NanoTime needs sufficient transistors to build a pattern from the marked topology and recognize the topologies of the same pattern. If the transistors specified in the command do not formulate a valid pattern, the pattern matching cannot be performed.

WHAT NEXT

Include the transistors of the topology in the topology marking command.

TOPO-075

TOPO-075 (warning) Skip %s recognition for CCB at net %s. The number of transistors %d in the CCB is over the limit %d.

DESCRIPTION

The number of transistors in the CCB is over the transistor limit for a big CCB.

WHAT NEXT

Check the variable topo_big_ccb_transistors for the transistor limit of big channel-connected blocks.

TOPO-076

TOPO-076 (Error) A clock has been defined at pin "%s" which is not connected to a net.

DESCRIPTION

A clock definition must be at a pin connected to a valid net in the netlist in order to be propagated forward.

WHAT NEXT

Check the output for problems during link_design. Investigate the netlist for inconsistencies with .lib models or other similar type problems.

TOPO-077

TOPO-077 (Warning) User marked %s overwrites the existing %s on %s.

DESCRIPTION

NanoTime only keeps one topology of each type on the same net or transistor. If multiple user markings are issued, the last user-marked topology overwrites the previous markings.

WHAT NEXT

Check the topology and remove the redundant markings.

TOPO-078

TOPO-078 (Warning) Removing latch at net %s due to %s.

DESCRIPTION

A latch defined at the net is removed because of the errors found on the net.

WHAT NEXT

Examine the various topologies involved for correctness.

TOPO-079

TOPO-079 (Warning) Found %d potential storage nodes, %d are not marked as sequential topologies, %d do not connect to the clock network, and %d are neither marked as sequential topologies nor connect to the clock network.

DESCRIPTION

NanoTime found potential storage nodes which are not marked as sequential topologies or do not connect to the clock network. When the variable topo_check_storage_node is set to true, it will cause **check_topology** failure.

WHAT NEXT

Report storage nodes using **report_storage_node** and resolve the problems.

SEE ALSO

report_storage_node(2)
topo_check_storage_node(3)

TOPO-080

TOPO-080 (warning) Clock network and topology cannot be reset by command '%s' in lib_topology '%s' at phase point '%s'.

DESCRIPTION

NanoTime cannot repropagate the clock network and rerun the topology recognition when executing the command listed in the warning message if the **topo_match_topology_reset_clock_and_topology** variable is set to **false**. The command also cannot be used in the lib_topology post_clock_propagation, post_match_topology, pre_check_topology, post_check_topology, pre_check_design, and post_check_design phase points.

WHAT NEXT

Move the command to the lib_topology pre_match_topology phase point.

TOPO-081

TOPO-081 (Warning) Logic conflict detected at latch net %s when adding an equal constraint from net %s

DESCRIPTION

When applying automatic logic constraint, a conflict was found with already existing logic constraints.

WHAT NEXT

Check to ensure that logic constants and constraints are set correctly.

TOPO-082

TOPO-082 (Error) User defined Ram structure at node %s and node %s is not a supported Ram structure.

DESCRIPTION

While applying topology marking using the **mark_ram** command, NanoTime recognizes an unsupported form of RAM structure.

WHAT NEXT

Ensure that the **mark_ram** command correctly identifies the RAM structure of the supported form.

TOPO-083

TOPO-083 (error) Transistor '%s' has already been marked as part of a differential synchronizer%s.

DESCRIPTION

A transistor identified in a **mark_differential_synchronizer** command was already marked as part of a differential synchronizer. This command will be ignored.

WHAT NEXT

Check other **mark_differential_synchronizer** commands.

TOPO-084

TOPO-084 (Error) Expecting %spin %s of differential generated clock %s to be marked as differential.

DESCRIPTION

The generated clock was specified with pins on two different nets.

WHAT NEXT

Create the appropriate differential pin pairs with **set_differential** command.

TOPO-085

TOPO-085 (Error) Expecting differential %s of generated clock %s to be exclusively paired.

DESCRIPTION

The generated clock was specified with pins that have differential relationships with other pins.

WHAT NEXT

Create the appropriate differential pin pairs with **set_differential** command.

TOPO-086

TOPO-086 (Warning) Missing differential complementary path for path from net %s %s (pin %s) to net %s %s (pin %s).

DESCRIPTION

Could not find the differential complementary path for the path from the given start net to end net.

WHAT NEXT

Create the appropriate differential net pairs with **set_differential** command.

TOPO-087

TOPO-087 (Warning) Unable to find logic compatible complementary path for stage from net %s (%s) to net %s (%s).

DESCRIPTION

There is no logic-compatible complementary path for the stage from the given start net to the end net.

WHAT NEXT

Ensure that there is no logic conflict between the reference path and the differential path.

TOPO-088

TOPO-088 (Error) Too many transistors in one differential synchronizer, found %d transistors (max number of transistors allowed: %d)

DESCRIPTION

The number of transistors specified in this differential synchronizer is larger than the limit.

WHAT NEXT

Verify the transistors specified for this differential synchronizer.

TOPO-089

TOPO-089 (Error) Do not use the **-feedback**, **-tapped_feedback**, **-feedforward**, and **-output** options with the commands for differential latches that include a differential synchronizer (latch net %s, complement net %s).

DESCRIPTION

For differential latches which include a differential synchronizer, NanoTime automatically infers the feedback and feedforward transistors as well as the output net. Command options are disabled in this case.

WHAT NEXT

Let NanoTime handle the latch feedback, feedforward and output recognition and leave out the corresponding command options.

TOPO-090

TOPO-090 (Error) NanoTime cannot mark this differential synchronizer on net %s because other

differential synchronizers already exist on the same net.

DESCRIPTION

A net can be part of only one differential synchronizer definition. If a net is specified in more than one **mark_differential_synchronizer** command, the first definition is accepted and all subsequent definitions are ignored.

WHAT NEXT

Check that there is only one differential synchronizer associated with the given net.

TOPO-091

TOPO-091 (Information) Created delay arc from differential net %s %s to its complement net %s %s.

DESCRIPTION

Delay arcs between differential net pairs are not common.

WHAT NEXT

Ensure that the differential synchronizer topology markings are correct.

TOPO-092

TOPO-092 (Error) Can not define a differential synchronizer on the following transistors {%s} due to: %s.

DESCRIPTION

NanoTime could not mark this differential synchronizer due to the specified reason.

WHAT NEXT

Check that corresponding nets are marked as differential nets before marking a differential synchronizer. Also check that the transistors specified are correct.

TOPO-093

TOPO-093 (Error) Expecting source pin %s of generated clock %s to be marked differential.

DESCRIPTION

The generated clock was specified with multiple source pins on different nets.

WHAT NEXT

Create the appropriate differential pin pairs with **set_differential** command.

TOPO-094

TOPO-094 (Error) NanoTime cannot mark this latch on net %s because latch node drives feedback device %s.

DESCRIPTION

A latch node can not drive any devices listed with the -feedback option to **mark_latch** command.

WHAT NEXT

Examine the latch being defined by the mark_latch command involved for correct latch node and feedback devices.

TOPO-095

TOPO-095 (Warning) Too many differential reference nets found for synchronizer%s: %s

DESCRIPTION

NanoTime could not uniquely identify the differential nets for the differential synchronizer.

WHAT NEXT

Mark the synchronizer using **mark_differential_synchronizer** command and avoid feedback property on the subset of transistors needed to drive the tapped outputs using the **tapped_transistors** option before the **match_topology** command. Ensure that the non-tapped transistors have their directions set correctly. There must be at least one transistor each to drive the enclosing reference and complement nets of the synchronizer.

TOPO-096

TOPO-096 (Warning) Removing cross-coupled topology %sfound on a differential synchronizer net pair (%s, %s).

DESCRIPTION

NanoTime removes conflicting cross-coupled topologies that coincide with differential synchronizers.

WHAT NEXT

Check that the cross-coupled topologies are marked correctly and differential nets are specified at the correct places. Usually a differential synchronizer has more significance than cross-coupled structures in a differential design.

TOPO-097

TOPO-097 (Error) Expecting one tapped net driven by differential synchronizer net %s, found %d.

DESCRIPTION

NanoTime could not uniquely identify a tapped net for the differential synchronizer. The tapped net must have an invert switching relationship with the differential synchronizer net and must be driven by a transistor gate connected to the differential synchronizer net. If tapped transistors are specified there must exist two tapped nets that form a differential pair.

WHAT NEXT

Mark the synchronizer using **mark_differential_synchronizer** command and avoid feedback property on the subset of transistors needed to drive the tapped outputs using the **tapped_transistors** option before the **match_topology** command. Ensure that the non-tapped transistors have their directions set correctly.

TOPO-098

TOPO-098 (Information) Defined a differential synchronizer consisting of %d NMOS and %d PMOS transistors between net %s and net %s.

DESCRIPTION

This message provides the number of transistors in a user defined differential synchronizer. An odd number of transistors may indicate a problem with the marking. The transistors in a differential synchronizer must form two channel connected regions.

WHAT NEXT

Check the **mark_differential_synchronizer** command to ensure that only the correct transistors are included.

TOPO-099

TOPO-099 (Error) Found differential synchronizer defined on the following transistors {%s} which failed consistency check.

DESCRIPTION

NanoTime found invalid differential nets associated with this differential synchronizer. Usually there should be only one pair of differential nets for a differential synchronizer. If tapped transistors are specified, there should be two pairs of differential nets associated with such a differential synchronizer.

WHAT NEXT

Check any preceding TOPO-095 warning messages for more information. Make sure that all relevant differential nets are defined with the **set_differential** command before invoking the **match_topology** or **mark_differential_synchronizer** commands. Also ensure that tapped transistors are specified correctly using the **-tapped_transistors** option of the **mark_differential_synchronizer** command.

TOPO-100

TOPO-100 (Warning) Found declaration of a differential pin pair %s %s with incompatible timing arcs to differential synchronizer nets %s %s

DESCRIPTION

This message provides a warning when incompatible timing arcs are detected from pins that form a differential pair. This includes the scenario where there exists a timing arc from one of the pins to a differential synchronizer net while there is no timing arc from the other pin to the complement differential synchronizer net. The differential synchronizer net can be either an enclosing net or a tapped output net.

WHAT NEXT

Check the **set_differential** command to ensure that the pins are ordered correctly.

TOPO-101

TOPO-101 (Error) Found both reference and complement differential clock pins on net %s.

DESCRIPTION

It is incorrect to have both reference and complement differential clock pins on the same net. Source pins of generated clocks are not included in this check.

WHAT NEXT

Check the related **set_differential** commands to ensure that only the correct pins are included.

TOPO-102

TOPO-102 (Error) Found both reference and complement differential clock pins on net %s of %s pin %s.

DESCRIPTION

It is incorrect to have both reference and complement differential clock pins on the same net. Source pins of generated clocks are not included in this check.

WHAT NEXT

Check the related **set_differential** commands to ensure that the correct pins are included in the proper order.

TOPO-103

TOPO-103 (Error) Differential synchronizer transistor %s does not belong to the CCB of either enclosing net %s or net %s.

DESCRIPTION

All transistors of a differential synchronizer must form a two CCB (channel connected block) loop. Moreover, each CCB must drive one of the two enclosing nets of the synchronizer.

WHAT NEXT

Check the related **mark_differential_synchronizer** command to ensure that the correct transistors are

included.

TOPO-104

TOPO-104 (Error) Differential synchronizer with enclosing net %s and net %s does not satisfy the two CCB rule.

DESCRIPTION

All transistors of a differential synchronizer must form a two CCB (channel connected block) loop. Moreover, each CCB must drive one of the two enclosing nets of the synchronizer.

WHAT NEXT

Check the related **mark_differential_synchronizer** command to ensure that the correct transistors are included.

TOPO-105

TOPO-105 (Information) Recognized net %s as a weak CCB output.

DESCRIPTION

When certain cross-coupled transistors are marked as weak pullups or forming differential synchronizers, related nets will be recognized as weak CCB outputs.

WHAT NEXT

Check the related **mark_weak_pullup** or **mark_differential_synchronizer** command to ensure that the correct transistors are included.

TOPO-106

TOPO-106 (Warning) Expecting differential net %s also to be clocked since clock propagation reached the other net %s from clock source net %s.

DESCRIPTION

The two differential nets that form a pair are expected to be of the same type, i.e., data or clock. A net is

considered clocked if it has the clock property. The clock property is placed on nets reachable through clock propagation from ports and pins on which clocks are defined.

WHAT NEXT

Check the arguments of **set_differential** commands. Use **report_clock_network** to investigate why clock propagation reached only one of the nets in the differential pair.

TOPO-107

TOPO-107 (Warning) Clocked differential net pair %s, %s do not form a differential clock.

DESCRIPTION

A net is considered clocked if it has the clock property. The clock property is placed on nets reachable through clock propagation from ports and pins where clocks are defined. A differential clock is created only by pairing the clock pins specified in a **create_clock\FP or create_generated_clock command with corresponding complement pins using the set_differential command. NanoTime found a clocked differential net pair whose clock source nets do not have differential pins.**

WHAT NEXT

Check the **set_differential** commands to ensure that only the correct nets are included.

TOPO-108

TOPO-108 (Error) No valid path consisting of precharge transistors could be found that connects the precharge evaluate net "%s" to power net.

DESCRIPTION

NanoTime checks if the precharge transistors specified could form a path from precharge evaluate net to power net.

WHAT NEXT

Check that the precharge transistors and evaluate nets are specified correctly.

TOPO-109

TOPO-109 (Warning) User defined enable pin %s replaced by parallel reference pin %s.

DESCRIPTION

The enable pin specified in the mark_clock_gate command is not the reference pin. NanoTime finds the pin with the is_parallel_reference attribute for use in the analysis.

WHAT NEXT

No action is required. You can eliminate the warning message by changing the enable pin specification.

TOPO-110

TOPO-110 (Error) Found clock driven data input nets %s for %s on net %s.

DESCRIPTION

In a strict sequential topology input matching flow, NanoTime reports sequential topologies whose data inputs are driven by clock signals.

This might be either an error or an intentional part of the design. Use the **topo_sequential_structure_strict_input_matching** variable to enable or disable the strict flow.

WHAT NEXT

Check that the specified sequential topology is correctly marked or recognized.

TOPO-111

TOPO-111 (Warning) Found clock driven data input nets %s for %s on net %s.

DESCRIPTION

In a strict sequential topology input matching flow, NanoTime reports sequential topologies whose data inputs are driven by clock signals.

This might be either an error or an intentional part of the design. Use the **topo_sequential_structure_strict_input_matching** variable to enable or disable the strict flow.

WHAT NEXT

Check that the specified sequential topology is correctly marked or recognized.

TOPO-112

TOPO-112 (Warning) Input net %s is connected to rail for %s on net %s.

DESCRIPTION

NanoTime checks and warns about input nets of sequential topology that are connected to a rail.

WHAT NEXT

Check that the specified sequential topology is correctly marked or recognized.

TOPO-113

TOPO-113 (Information) Inferred input nets %s for %s on net %s.

DESCRIPTION

NanoTime infers data input nets for sequential topologies.

WHAT NEXT

Check that NanoTime inferred input nets are correct for the sequential topology.

TOPO-158

TOPO-158 (Information) Because pin %s is a %s pin, fanout delay arcs from that pin and timing checks associated with them will be removed.

DESCRIPTION

Certain pins in the design, such as feedback and non-proxy parallel transistor pins, will not have outgoing delay arcs or timing checks.

WHAT NEXT

No user action is expected for this message.

TOPO-159

TOPO-159 (Information) Because transistor %s is a %s transistor, delay arcs and timing checks based on delay arcs through that transistor will be removed.

DESCRIPTION

Certain transistors in the design, such as feedback and non-proxy parallel transistors, will not have delay arcs through them or associated timing checks.

WHAT NEXT

No user action is expected for this message.

TOPO-160

TOPO-160 (Information) Because %s, the clock gate driving net %s will not have non-controlling delay arcs disabled.

DESCRIPTION

The topo_clock_gate_timing_resolution variable enables timing resolution to use an internal algorithm to attempt to select the controlling pins on clock gating topologies. This message indicates that this algorithm has failed (possibly partially) on the clock gate driving the specified net. In this case, none of the clock delays arcs of the affected portion of this clock gate timing graph will be disabled, so they will all propagate their clock arrival times and the clock gate output arrival time will be the pessimistic combination of all of these propagated times.

WHAT NEXT

If certain delay arcs for this clock gate are manually known to be non-controlling, they can be disabled manually in tcl.

TOPO-161

TOPO-161 (Warning) The power-switch transistor %s is turned off.

DESCRIPTION

The power-switch transistor is off because of the fixed logic state on the gate net of the transistor.

WHAT NEXT

Check if there are any logic constraints or case-analysis that sets the fixed logic state on the net.

TOPO-162

TOPO-162 (Error) mark_memory_precharge device %s is not a transistor. Mark_memory_precharge command will be ignored.

DESCRIPTION

An element listed in the mark_memory_precharge command is not a transistor.

WHAT NEXT

Check the mark_memory_precharge command options.

TOPO-163

TOPO-163 (Error) Precharge devices must be controlled by the same net. The mark_memory_precharge command will be ignored.

DESCRIPTION

There are multiple control signals to memory precharge devices.

WHAT NEXT

Check your precharge module architecture.

TOPO-164

TOPO-164 (Error) Mark_memory_precharge command must have at least 1 and no more than 2 nets specified as evaluate nets. %d nets found.

DESCRIPTION

The number of nets listed in the **-evaluate_net** option of the **mark_memory_precharge** command is invalid. You must specify either one or two nets with this option.

WHAT NEXT

Modify the **-evaluate_net** option of the **mark_memory_precharge** command to specify either one or two nets.

TOPO-165

TOPO-165 (Warning) Found conflicting flip flop topologies, none will be accepted. Flip flop with master latch net %s, slave latch net %s is conflicting with flip flop with masterlatch net %s, slave latch net %s.

DESCRIPTION

NanoTime found conflicting flip flop topologies and can not decide which is the correct one. NanoTime does not allow one latch to be part of two different flip flops.

WHAT NEXT

First, make sure the latch topologies are correctly recognized, then use mark_flip_flop to resolve any ambiguity. A user-defined flip flop pattern can be used to facilitate the marking process.

TOPO-166

TOPO-166 (Warning) The -backward option to the mark_clock_network command has been deprecated.

DESCRIPTION

The -backward option to the mark_clock_network command has been deprecated and will be removed in a future release.

WHAT NEXT

Use the set_requires_clock command to indicate that a net requires a clock. Clock markings will automatically propagate backwards through inverters in any case.

TOPO-167

TOPO-167 (Warning) Because %s this clock gate will not have non-controlling delay arcs disabled.

DESCRIPTION

The command mark_clock_gate with options -min_rise_controlling_pin <pin> -max_rise_controlling_pin

<pin> -min_fall_controlling_pin <pin> -max_fall_controlling_pin <pin> enables users to specify how min and max path traversals occur through the clock gate during path tracing. The user must ensure that a single pin is defined for each option. The user must also ensure that the pins are part of the same clock gate and connect to the correct transistors that are used in the traversal. This message indicates that the current pin assignment specified does not adhere to one of the above criteria.

WHAT NEXT

Please recheck the pins assigned to each -min(max)_rise(fall)_controlling_pin option for correctness.

TOPO-168

TOPO-168 (Error) All the controlling pins of the clock gate driving net %s must be defined for the non-controlling delay arcs of the clock gate to be disabled.

DESCRIPTION

The command mark_clock_gate with options -min_rise_controlling_pin <pin> -max_rise_controlling_pin <pin> -min_fall_controlling_pin <pin> -max_fall_controlling_pin <pin> enables users to specify how min and max path traversals occur through the clock gate during path tracing. The user must ensure that all controlling pins are specified when the command is issued.

WHAT NEXT

Please ensure that all options -min_rise_controlling_pin, -min_fall_controlling_pin, -max_rise_controlling_pin and -max_fall_controlling_pin are defined with the mark_clock_gate command.

TOPO-169

TOPO-169 (Warning) The controlling pin %s %s on the clock gate driving net %s. Shaper resolution of this clock gater is incomplete.

DESCRIPTION

The command mark_clock_gate with options -min_rise_controlling_pin <pin> -max_rise_controlling_pin <pin> -min_fall_controlling_pin <pin> -max_fall_controlling_pin <pin> enables users to specify how min and max path traversals occur through the clock gate during path tracing. The user must ensure that all controlling pins are specified when the command is issued.

WHAT NEXT

Please ensure that pins defined by options -min_rise_controlling_pin, -min_fall_controlling_pin, -max_rise_controlling_pin and -max_fall_controlling_pin are part of the clock gate.

TOPO-170

TOPO-170 (Information) Net %s and net %s form a differential cross coupled circuit.

DESCRIPTION

NanoTime has recognized the cross coupling of the differential nets.

WHAT NEXT

Ensure that the automatic circuit recognition is congruent with the design intent.

TOPO-171

TOPO-171 (Warning) Differential net %s is not cross coupled and therefore cannot have override.

DESCRIPTION

Only cross coupled differential circuits can have differential override. Since the reported net was not found to be part of a cross coupled structure the override will not be applied.

WHAT NEXT

Check the differential net and override markings.

TOPO-172

TOPO-172 (Information) Net %s with %s clamp state, and net %s with %s clamp state form a differential cross coupled circuit.

DESCRIPTION

NanoTime has identified the cross coupling of the differential nets. The circuit will be further recognized as partially differential if the differential behavior of the nets is restricted by user declared override pins.

WHAT NEXT

Ensure that the circuit identification is congruent with the design intent.

TOPO-173

TOPO-173 (Information) Net %s does not have differential override while coupled net %s has differential override specified.

DESCRIPTION

NanoTime has recognized the cross coupling of the differential nets.

WHAT NEXT

Ensure that differential override specification is complete.

TOPO-174

TOPO-174 (Information) Clamping direction found for differential cross coupled net %s but no differential override specified.

DESCRIPTION

NanoTime has recognized the cross coupling of the differential nets.

WHAT NEXT

Ensure that differential override specification is complete.

TOPO-175

TOPO-175 (Warning) Clamping direction not found for differential cross coupled net %s but differential override was specified.

DESCRIPTION

NanoTime has recognized the cross coupling of the differential nets.

WHAT NEXT

Ensure that differential override specification is correct.

TOPO-176

TOPO-176 (Information) Connecting inverter between inputs of channel connected regions of differential net %s has other fanout on net %s.

DESCRIPTION

NanoTime will include such inverters in the simulation of the differential regions.

WHAT NEXT

Check the connectivity.

TOPO-178

TOPO-178 (Warning) Using the mark_net command with the -clock_gate_checking option after the match_topology command does not have an effect.

DESCRIPTION

The mark_net command with the -clock_gate_checking force_strict | non_strict <net> option, enables users to specify the type of checking that will be carried out for clock gates that drive this net. The mark_net command with the -clock_gate_checking force_strict | non_strict option must be issued before calling the match_topology command.

WHAT NEXT

Please ensure that the mark_net command is called before calling the match_topology command in your script.

TOPO-179

TOPO-179 (Error) Differential cross coupled property of net %s is not compatible with net %s that does not have the differential cross coupled property.

DESCRIPTION

NanoTime has detected either an incompatible or an incorrect marking of differential nets. A differential net pair can function as a differential cross coupled net pair only if both the nets are successfully marked as differential cross coupled nets individually.

WHAT NEXT

Ensure that differential cross coupled markings of the two nets in the differential pair are correct.

TOPO-180

TOPO-180 (Error) Could not detect cross coupling for the marked differential cross coupled net %s.

DESCRIPTION

NanoTime has detected an incompatible marking of differential cross coupled nets.

WHAT NEXT

Ensure that differential cross coupled marking is correct.

TOPO-181

TOPO-181 (Error) Inner cross coupled net %s for net %s should not be marked differential cross coupled.

DESCRIPTION

NanoTime has detected an incompatible marking of differential cross coupled nets.

WHAT NEXT

Ensure that differential cross coupled marking is correct.

TOPO-182

TOPO-182 (Warning) Missing power switch on virtual supply net %s.

DESCRIPTION

NanoTime has detected that a power switch topology is missing on the specified virtual supply net.

WHAT NEXT

Make sure a power switch topology is correctly identified by NanoTime or manually marked on all virtual

supply nets.

TOPO-183

TOPO-183 (Error) Cross coupled differential nets %s and %s must have the same override enable net.

DESCRIPTION

NanoTime has detected multiple enable nets for the differential net pair. They can have atmost one enable net. If there are two enable nets connected by an inverter for the override pins, select the override pins on the input of the inverter.

WHAT NEXT

Ensure that differential cross coupled marking is correct.

TOPO-184

TOPO-184 (Error) Unable to determine unique true cross coupled net for net %s with differentially paired net %s.

DESCRIPTION

NanoTime could not identify a unique true cross coupled net.

WHAT NEXT

Ensure that differential cross coupled marking is correct.

TOPO-185

TOPO-185 (Information) Cross coupled differential nets %s and %s do not have an override enable net.

DESCRIPTION

NanoTime has detected that an enable net may be needed for the differential net pair but none was specified.

WHAT NEXT

Ensure that differential cross coupled marking is correct.

TOPO-186

TOPO-186 (information) The CCB (containing representative net %s) which loads pin %s has %d schematic transistors, which exceeds the limit of %d fets set in the **sim_miller_use_extended_load_fet_limit** variable. A simplified model of this CCB will be used as a load.

DESCRIPTION

NanoTime has detected that a potential loading CCB is larger than the size limit set.

WHAT NEXT

If more accuracy is desired, increase the size limit.

TOPO-187

TOPO-187 (Error) The pins "%s" and "%s" have a differential marking. These two pins are on different clocks "%s" and "%s".

DESCRIPTION

Differential markings require that the items being marked are associated with the same clock. It is recommended that all clock definitions be completed before any differential markings are made.

WHAT NEXT

Check your usage of the set_differential command and the clocks defined by create_clock and create_generated_clock.

TOPO-188

TOPO-188 (Warning) Transistors "%s" and "%s" of a topology pattern "%s" were detected to be parallel.

DESCRIPTION

Topology patterns should not include parallel connected components. They are redundant for describing a

topology. Parallel components in the netlist are merged by default. Therefore, a pattern that contains parallel components will not be matched to any subcircuit, even tough they would be topologically equivalent.

WHAT NEXT

Leaving parallel transistors in a topology pattern is highly discouraged. The pattern will only match if pattern_merge_parallel_transistors is set to FALSE and the subcircuit contains the exact number of redundancies. In all other cases, the algorithm will fail to match the pattern.

TOPO-189

TOPO-189 (Warning) Clock pin "%s" of user-specified (mark_latch) latch net "%s" blocks the input(s) ("%s") during the transparency window.

DESCRIPTION

The clock pins of a mark_latch command need to capture the input (data or clock) that is latched for proper setup and hold timing checks. If the clock pin is determined to be on a transistor that blocks the input from reaching the latch net, this warning is issued since an incorrect capture edge (transparent latches) or opening edge (nontransparent latches) might be used for setup/hold timing checks, and path tracing may prematurely stop if the incorrect transparency window is missed.

WHAT NEXT

Double-check the clock pins specified in the mark_latch command. Make sure they turn on transistors that enable the input(s) to set the state of the latch net during the transparency window and subsequently be captured on the closing edge.

TOPO-190

TOPO-190 (Error) Error detected for differential cross coupled nets %s and %s: %s.

DESCRIPTION

NanoTime has detected an incorrect specification of the reported differential cross coupled nets.

WHAT NEXT

Ensure that the differential cross coupled net specification is correct.

TOPO-191

TOPO-191 (Error) %s-directional transistor %s connected to differential cross coupled output net %s.

DESCRIPTION

NanoTime expects either source-to-drain or drain-to-source direction for all transistors connected to a differential cross coupled output net.

WHAT NEXT

Ensure that the strict transistor direction checking is enabled.

TOPO-192

TOPO-192 (Information) Setting transistor %s direction away from differential cross coupled output net %s.

DESCRIPTION

NanoTime expects either source-to-drain or drain-to-source direction for all transistors connected to a differential cross coupled output net.

WHAT NEXT

Ensure that directions of transistors connected to a differential cross coupled output net are specified.

TOPO-193

TOPO-193 (Information) Setting clock property %s on net %s because its differental paired net %s has the same property.

DESCRIPTION

NanoTime expects clock nets that form a differential pair to have similar settings or properties.

WHAT NEXT

Check the value of **topo_copy_clock_property_from_differential_net** variable.

TOPO-194

TOPO-194 (Error) The argument is not a list or collection of exactly two objects.

DESCRIPTION

The argument of the **mark_memory_bitline** command must be a pair of a memory bitline and its complement.

WHAT NEXT

Specify a pair of a bitline and its complement.

TOPO-195

TOPO-195 (Error) Could not find memory %s.

DESCRIPTION

The **mark_memory_bitline** or **erase_memory_bitline** command could not find the memory specified in the **-memory** option.

WHAT NEXT

Check the argument to the **-memory** option and see if the named memory has been created with the **create_memory** command.

TOPO-196

TOPO-196 (Error) The differential high voltage %g must be higher than the differential low voltage %g.

DESCRIPTION

The argument to the **-diff_high** must be higher than the argument to the **-diff_low** option in the **mark_sense_amp** command.

WHAT NEXT

Set a higher voltage to the **-diff_high** option in the **mark_sense_amp** command.

TOPO-197

TOPO-197 (Error) Cannot set a negative value %g for the differential %s voltage.

DESCRIPTION

The arguments to the **-diff_high** and **-diff_low** options must be non-negative values in the **mark_sense_amp** command.

WHAT NEXT

Set non-negative values to the **-diff_high** and **-diff_low** options in the **mark_sense_amp** command.