REPORT

ON

AHB to APB BRIDGE DESIGN

Submitted by

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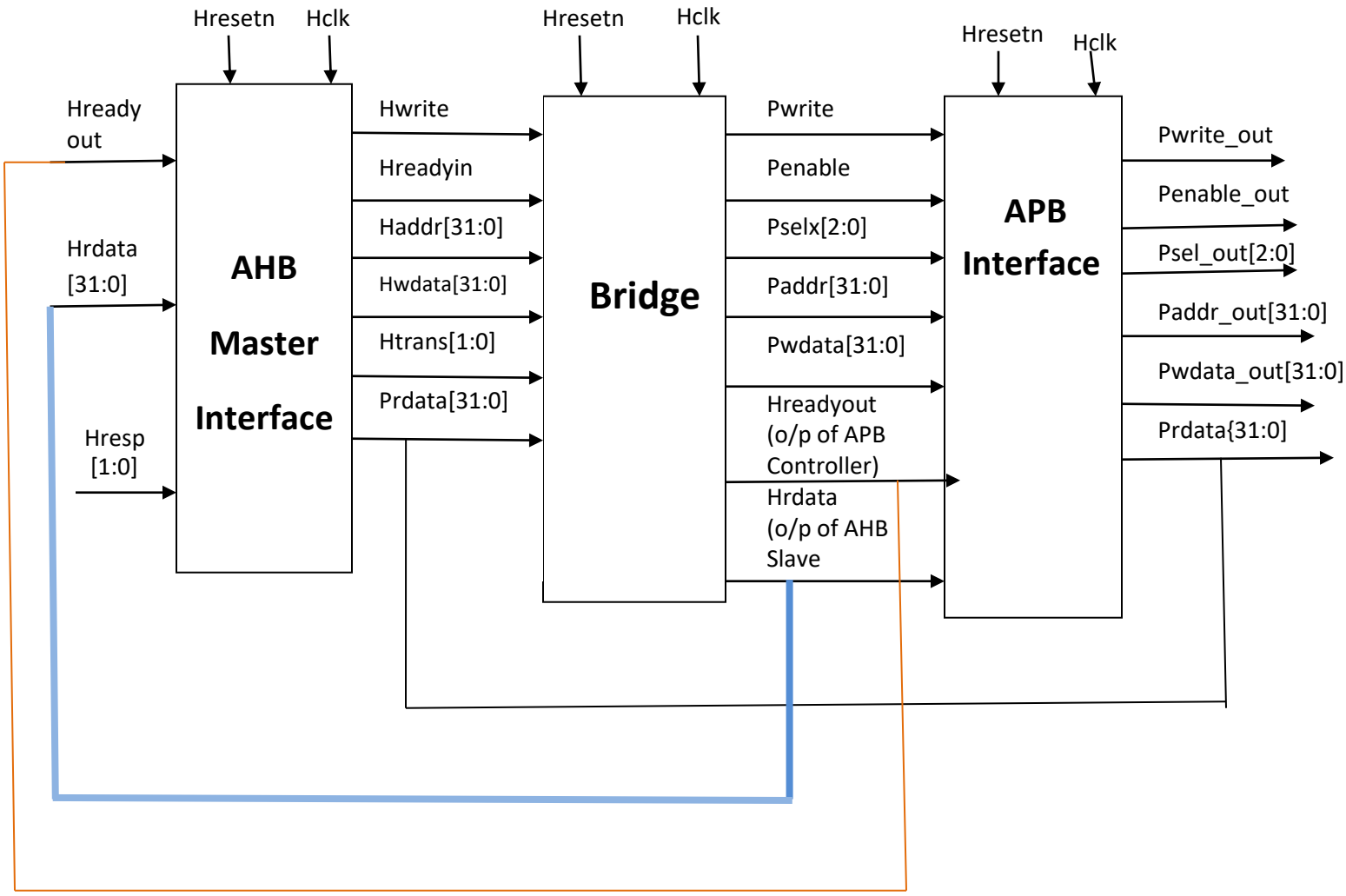
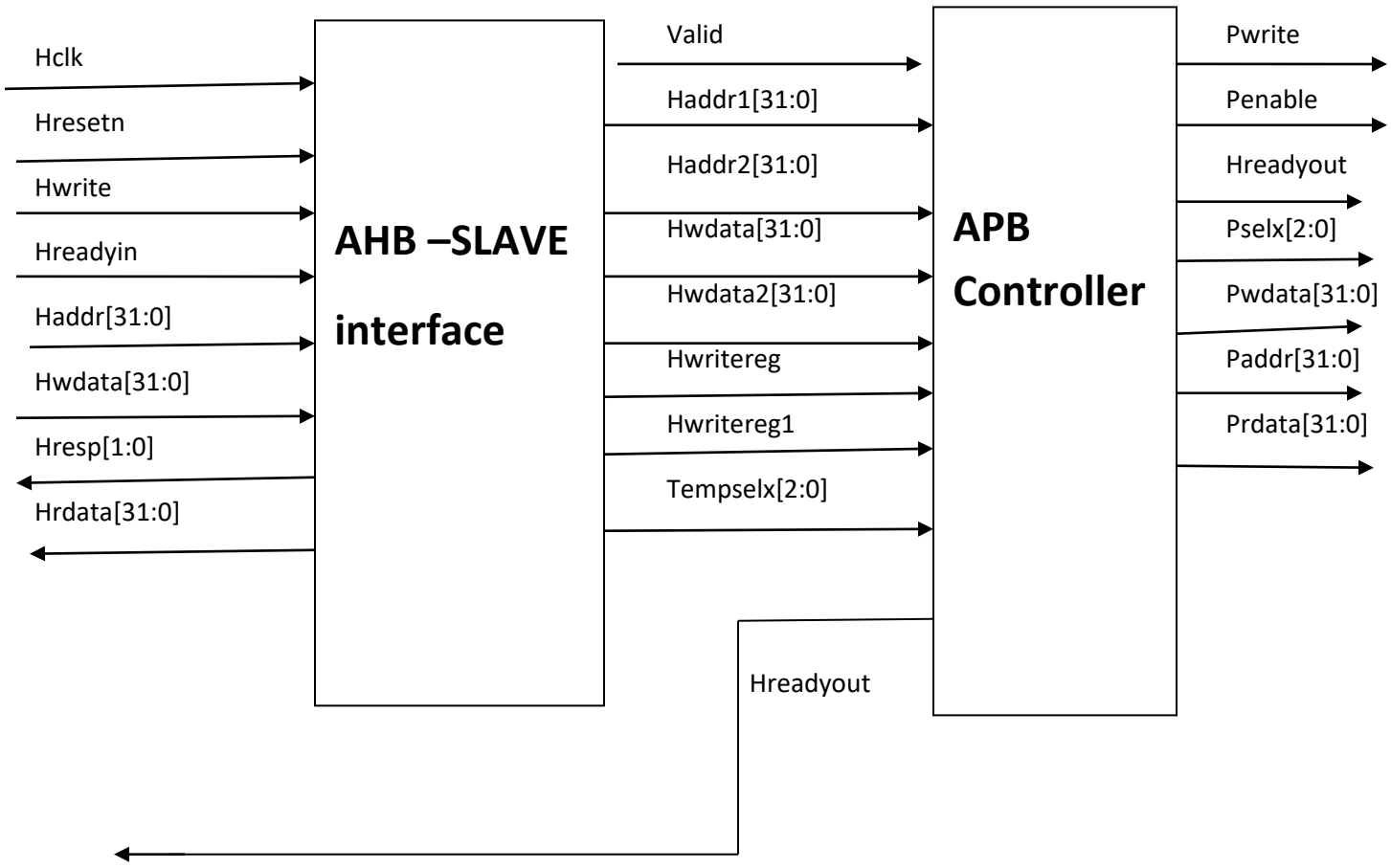
BATCH- DI 45

BRIDGE ARCHITECTURE: TOP MODULE



BRIDGE MODULE:



AMBA AHB Protocol

AMBA AHB (Advanced High-performance Bus) is a bus interface designed to support high-performance and synthesizable designs. It provides a standardized communication method between various components such as Masters (Managers), interconnects, and Slaves (Subordinates) in a system.

The AHB protocol is specifically tailored to meet the requirements of high-performance and high clock frequency systems. Key features of AHB include:

- Burst Transfers: Supports data bursts for efficient data movement.

- Single Clock-Edge Operation: Ensures synchronization of data transfer on a single clock edge.

- Non-Tristate Implementation: Simplifies the design by avoiding the use of tristate buffers.

- Configurable Data and Address Bus Widths: Allows customization of bus widths to suit system requirements.

In typical designs, the most common AHB Slaves are internal memory blocks, external memory interfaces, and high-bandwidth peripherals. Although low-bandwidth peripherals can also function as AHB Slaves, they are generally placed on the AMBA Advanced Peripheral Bus (APB) for performance reasons. An AHB Slave, known as an APB bridge, serves as the interface between the higher performance AHB and the APB.

In a typical single Master AHB system design, as depicted in the simplified diagram (Figure 1-1), the system consists of an AHB Master and multiple AHB Slaves. The interconnect logic includes an address decoder and a Slave-to-Master multiplexer. During the address phase of a transfer, the decoder monitors the address from the Master and selects the appropriate Slave during the data phase. The multiplexer then routes the selected Slave's output data back to the Master.

For systems with multiple Masters, AHB supports multi-Master configurations by utilizing an interconnect component that manages arbitration and routing signals between multiple Masters and their corresponding Slaves.

It is important to note that the simplified diagram (Figure 1-1) primarily illustrates the main address and data buses along with typical data routing. Not all signals are represented in this diagram.

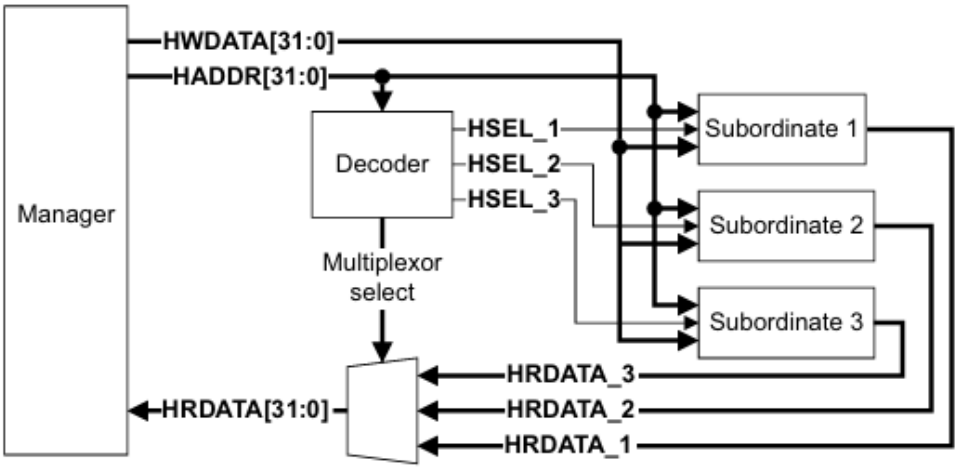


Fig.1-1

AHB master interface

It is master that gives signal for single_write, single_read, burst_4incr_write, burst_4incr_read to the AHB slave interface.

AHB slave interface

It is slave for master it's working is

1.) it generates pipelining for haddr, hwdata, hwrite.
2.) It generates valid signal for APB controller (FSM).
3.) And also generate tempselx for selecting peripheral according to address.

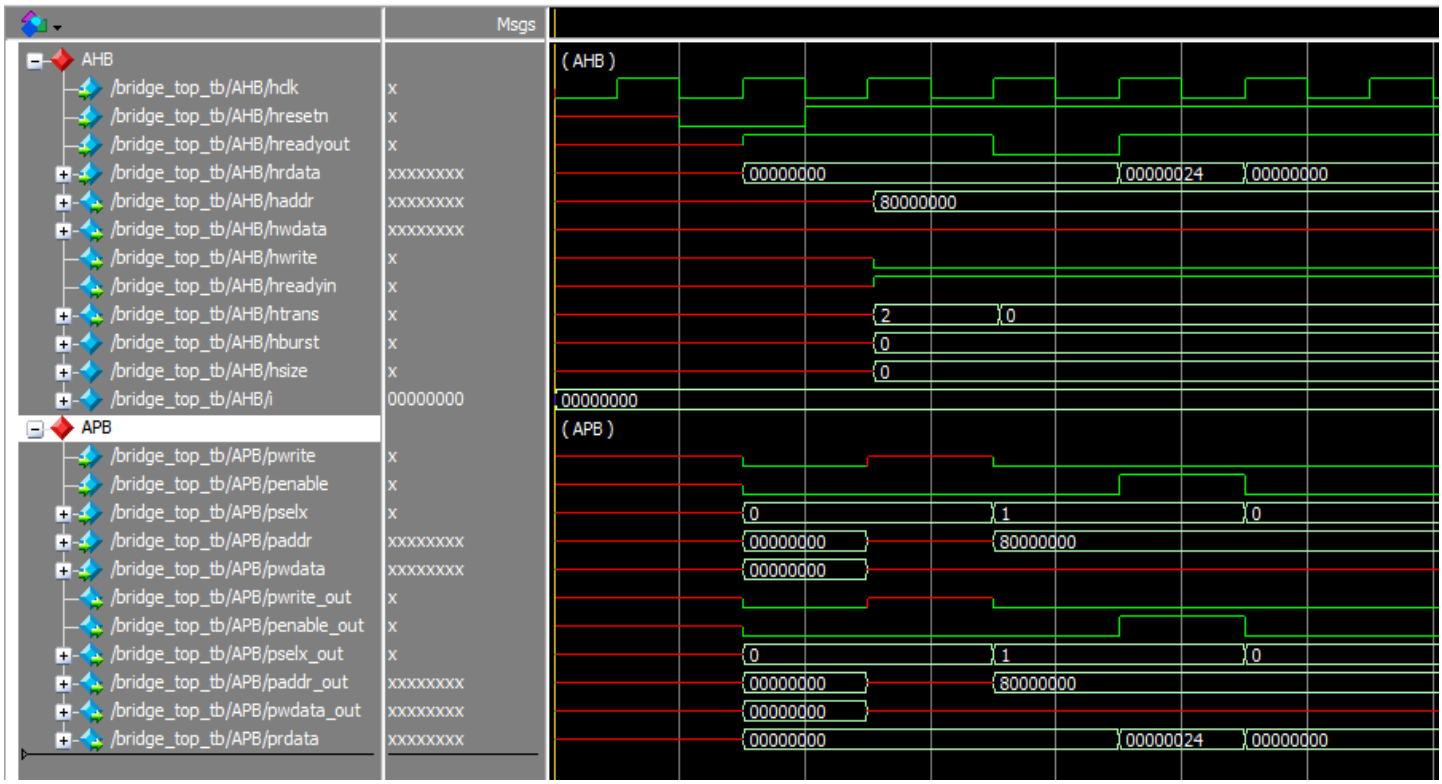
APB controller (FSM)

It is FSM that uses eight different states and by using these states it generates peripheral and hready_out signals.

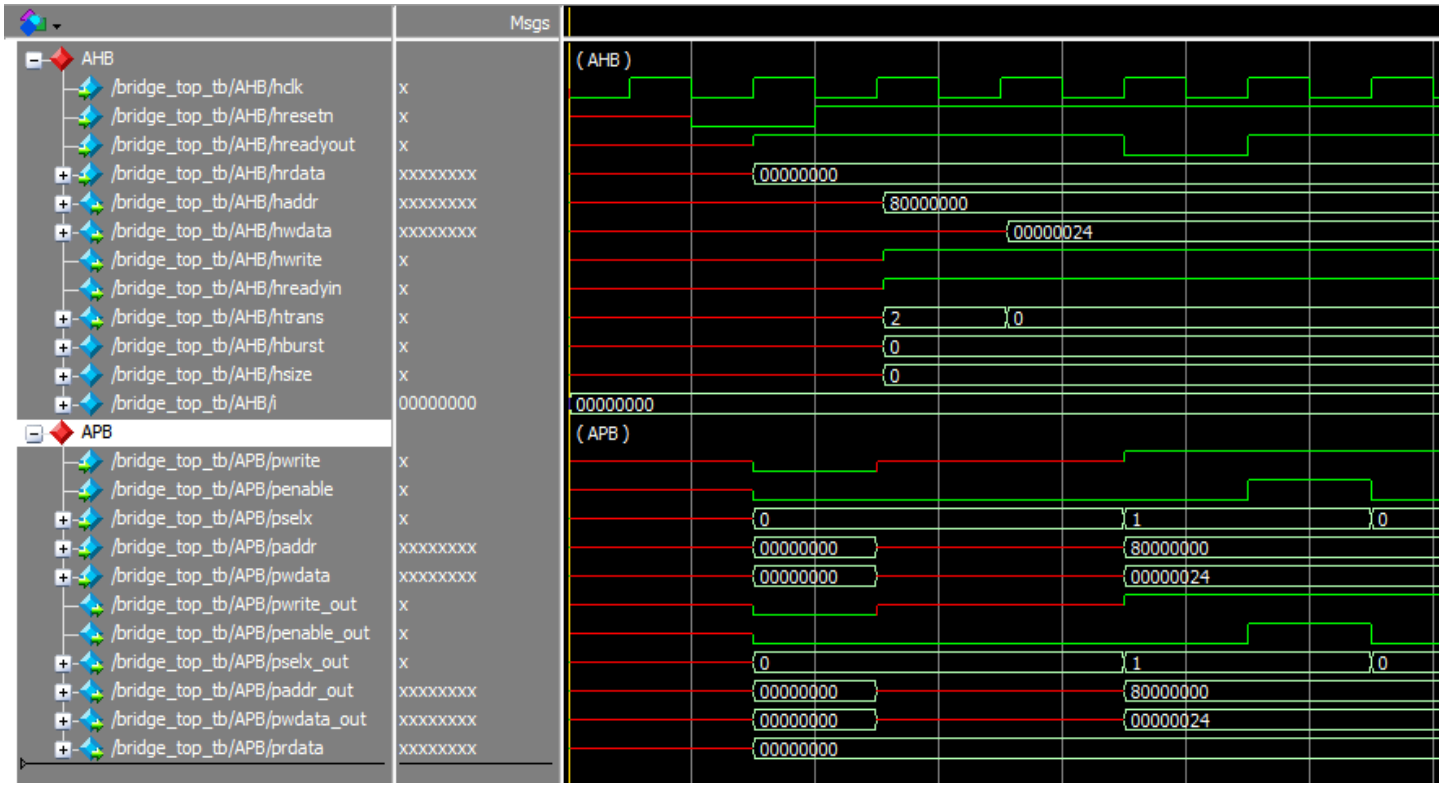
APB interface

We create this block for taking peripheral_out and pr_data signals.

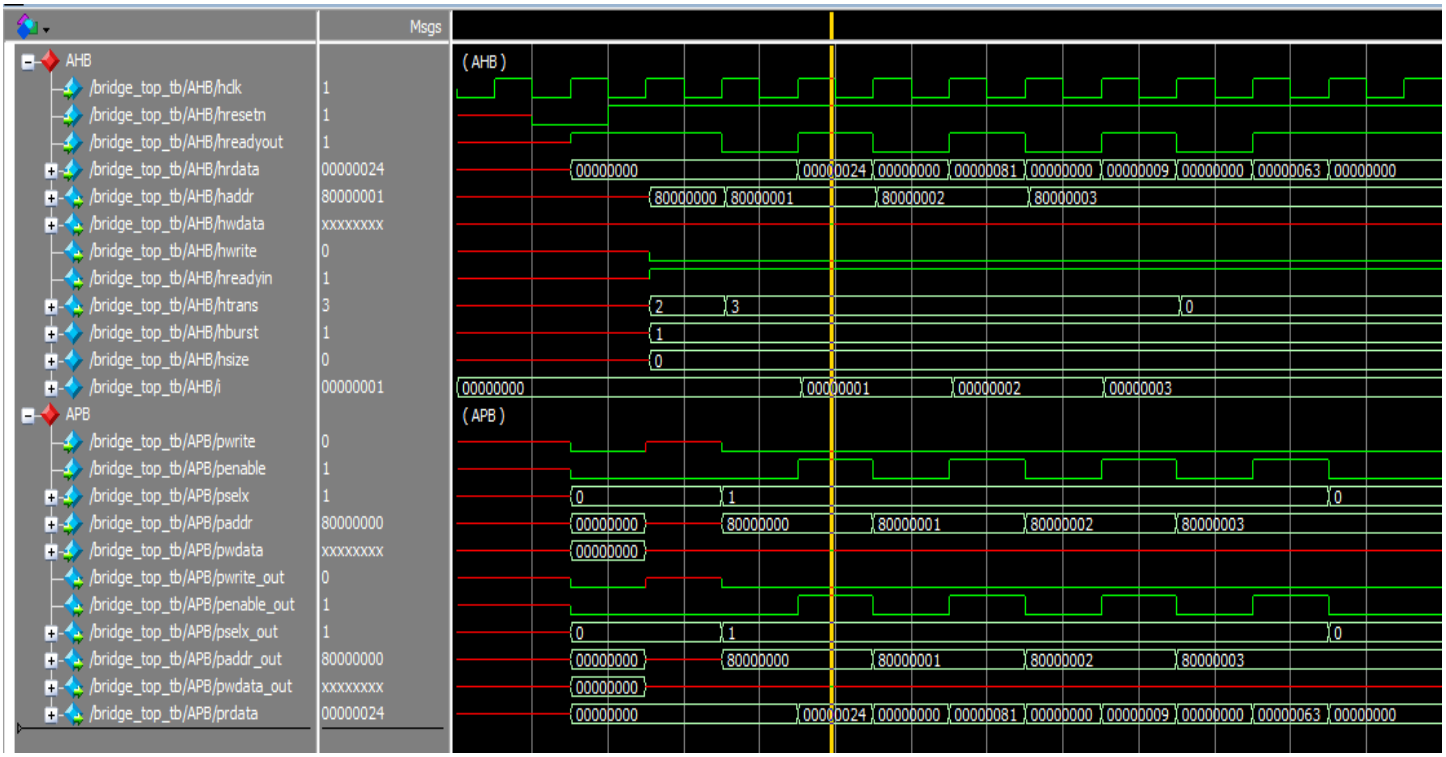
single_read output



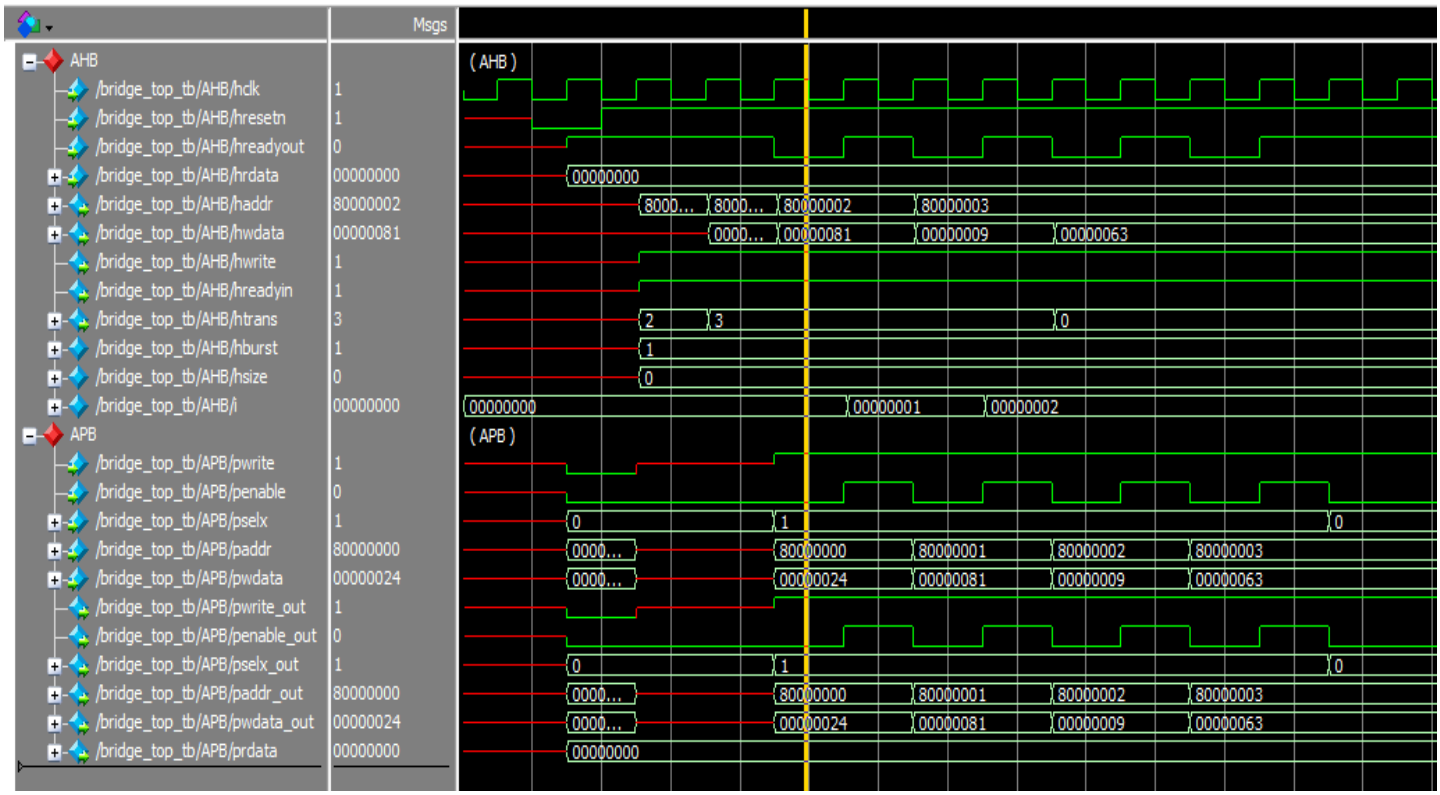
single_write output



burst_4incr_read output



burst_4incr_write output



Bridge Synthesis:-