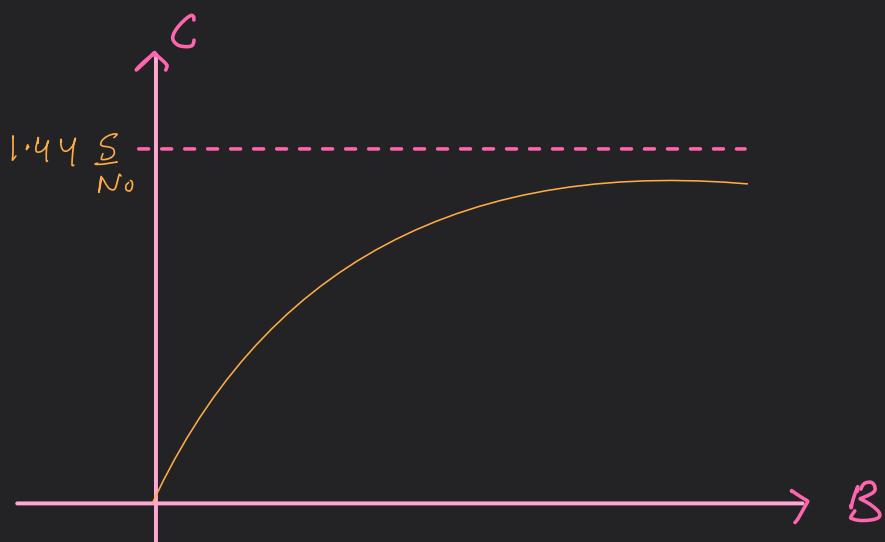


$$= \lim_{t \rightarrow 0} \frac{\frac{d}{dt} (\log_2(1+t))}{\frac{d}{dt}(t)} \cdot \frac{s}{N_0} \quad \frac{d}{dx} \log_a x = \frac{1}{x \ln a}$$

$$= \lim_{t \rightarrow 0} \frac{1}{(1+t) \ln 2} \cdot \frac{s}{N_0}$$

$$= \frac{1}{\ln 2} \cdot \frac{s}{N_0}$$

$$C = 1.44 \left(\frac{s}{N_0} \right)$$



Ques - A radio channel has a bandwidth of 10 kHz & SNR of 15 dB. find the maximum data rate that can be transmitted over this channel.

$$C = B \log_2 \left(1 + \frac{s}{N_0} \right)$$

$$\text{SNR} = 15 \text{ dB} \Rightarrow 10^{1.5} \Rightarrow 31.62 \text{ Hz}$$

$$C = 10 \times 10^3 \times \log_2 \left(1 + 31.62 \right)$$

$$C = 50.27 \text{ kbps}$$

- Ques - find the channel capacity for $\frac{S}{N} = 15$ for the following 3 cases -
- $B = 1 \text{ kHz}$ (twisted pair)
 - $B = 1 \text{ MHz}$ (co-axial cable)
 - $B = 1 \text{ GHz}$ (optical fibre)
 - $B = \infty$

Sol \rightarrow a) $C = B \log_2 \left(1 + \frac{S}{N} \right)$

$$= 1 \log_2 (1 + 15)$$

$$C = 4 \text{ kbps.}$$

b) $C = 1 \log_2 (16)$

$$= 4 \text{ Mbps}$$

c) $C = 1 \log_2 (16)$

$$= 4 \text{ Gbps.}$$

d) $C = 1.44 \left(\frac{S}{N_0} \right)$

TUT -

Ques In communication with AWGN operating at $\text{SNR} > 1$ & $BW = B$ has capacity C_1 if SNR is doubled by keeping B constant to less than C_1 .

$$C = B \log_2 \left(1 + \frac{S}{N} \right)$$

$$C_1 = B \log_2 \left(1 + \frac{S}{N} \right)$$

$$C^* = B \log_2 \left[1 + \frac{2S}{N} \right]$$

$$\frac{C^*}{C_1} = \frac{C \log_2 \left[1 + \frac{2S}{N} \right]}{\log_2 \left[1 + \frac{S}{N} \right]}$$

$$C_2 = C_1 \Rightarrow \log_2 \left[\frac{2S}{N} \right] = 1 + \log_2 \left(\frac{S}{N} \right)$$

$$C_2 = C_1 \left[\left(\log_2 \frac{S}{N} + 1 \right) \right] \log_2 \left(\frac{S}{N} \right)$$

$$C_1 = C_2$$

$$B + C_1 = C_2$$

Ques A communication channel has BW of 3 MHz and SNR of 20dB find channel capacity

Ques BW is 10 kHz and SNR is 30dB find channel capacity

Ques Find the required SNR in dB to achieve 99.97 Mbps with BW of 1 MHz

$$\begin{aligned} C &= B \log_2 \left(1 + \frac{S}{N} \right) \\ 10 \times 10^6 &= 1 \times 10^6 \log_2 \left(1 + \frac{S}{N} \right) \\ 10 &\stackrel{?}{=} \log_2 \left(1 + \frac{S}{N} \right) = \log_2 2^{10} = 1 \left(1 + \frac{S}{N} \right) \\ \Rightarrow 2^{10} - 1 &= \frac{S}{N} \approx 2^{10} \Rightarrow 30 \text{ dB.} \end{aligned}$$

Ques A channel width capacity 5 Mbps has SNR of 15dB find the requirement of BW.

$$C = B \log_2 \left(1 + \frac{S}{N} \right)$$

$$5 \times 10^6 = B \log_2 (1 + 31.62)$$

$$5 \times 10^6 = B \log_2 (32.62)$$

$$5 \times 10^6 = B \times 5$$

$$\boxed{B = 1 \text{ MHz}} \approx \text{ans}$$

l	\mid	0	\mid	P_4	\mid	1	\mid	P_2	\mid	P_1	\mid
-----	--------	-----	--------	-------	--------	-----	--------	-------	--------	-------	--------

Check Bit -

$$P_1 = 1 \oplus 0 = 1$$

$$P_2 = 1 \oplus 1 = 0$$

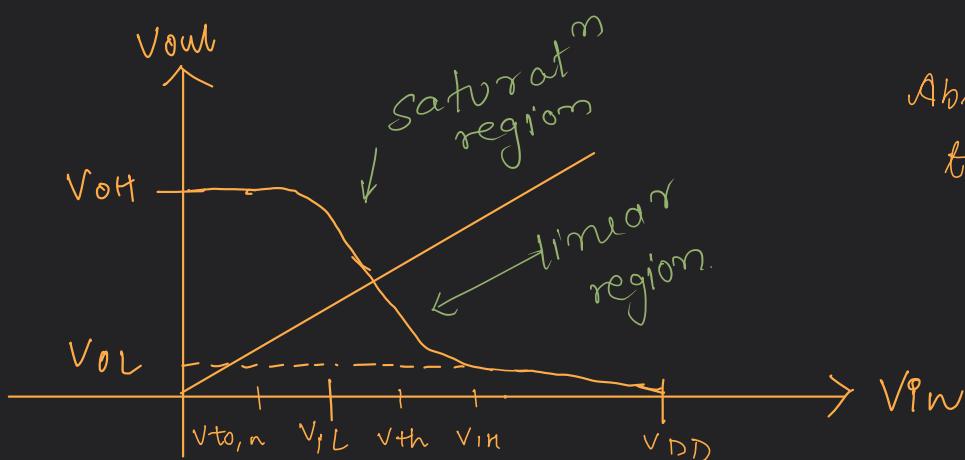
$$P_4 = 0 \oplus 1 = 1$$

code \rightarrow

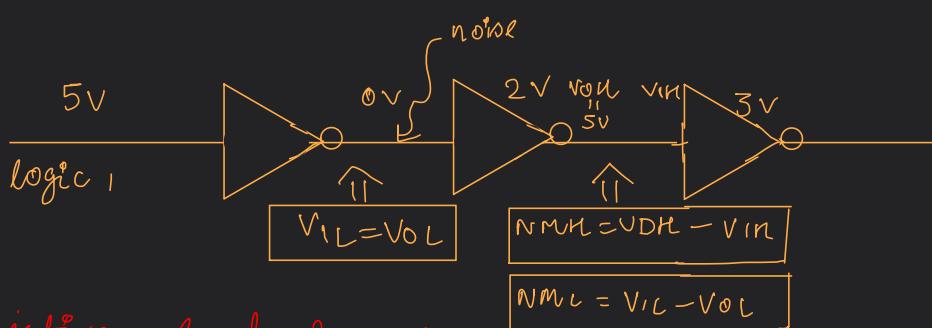
1	\mid	0	\mid	1	\mid	1	\mid	0	\mid	1	\mid
-----	--------	-----	--------	-----	--------	-----	--------	-----	--------	-----	--------

interpreted as logic 0.

$V_{TN} \rightarrow$ It is the switching threshold voltage for which $V_{in} = V_{out}$. Ideally it is $\frac{V_{DD}}{2}$

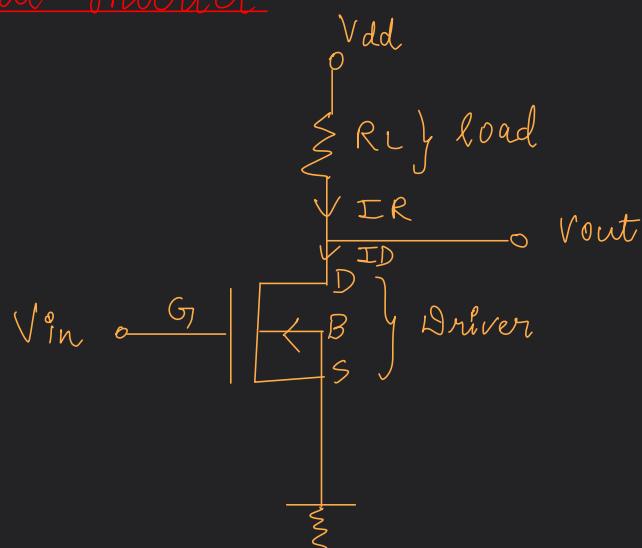


Ability of circuit to tolerate Noise called Noise Margin.



$$\begin{aligned} V_{on} &\rightarrow 5 \\ V_{OL} &\rightarrow 0 \\ V_{in} &\rightarrow 3 \\ V_{IL} &\rightarrow 2 \\ V_{th} &\rightarrow 2.5 \end{aligned}$$

Resistive load Inverter



$$V_{SB} = 0$$

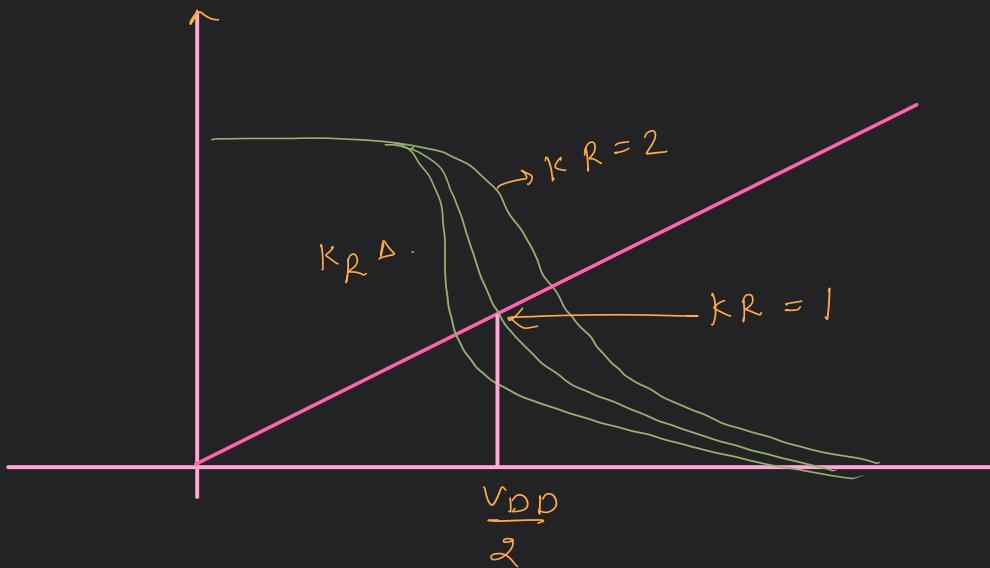
$$\begin{aligned} V_{in} &= V_{gs} \\ V_{out} &= V_{ds} \end{aligned}$$

Voltage Transfer curve (DC Analysis) = In this we came to know while changing I/P how O/P is varying.

- I) $V_{in} < V_{TN}$ cut off mode.
- II) $V_{TN} \leq V_{in} < V_{out} + V_{TN}$ Saturation mode.
- III) $V_{in} \geq V_{out} + V_{TN}$ Linear mode.

Driver - cut off mode ($I_D = 0$)

$$\Rightarrow V_{out} = V_{DD}$$



$$V_{IL} = \frac{2V_{out} + V_{TO^p} - V_{DD} + KR V_{TO^n}}{1 + KR}$$

$$V_{IH} = \frac{V_{DD} + V_{TO^p} + KR(2V_{out} + V_{TO^n})}{1 + KR}$$

for symmetric -

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{TO^n})^2$$

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_{TO^n})^2$$

$$V_{DD \text{ min}} = V_{TO^n} + |V_{TO^p}|$$

Analysis of CMOS Circuits

If 5 transistors are connected in series

$$\left(\frac{\omega}{L}\right)_{eq} = \frac{1}{\sum (\frac{1}{\omega_{IL}})_n}$$

$\Sigma \rightarrow$

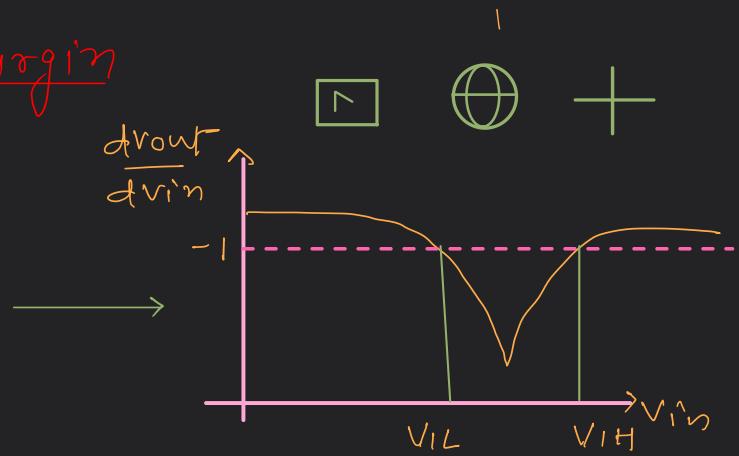
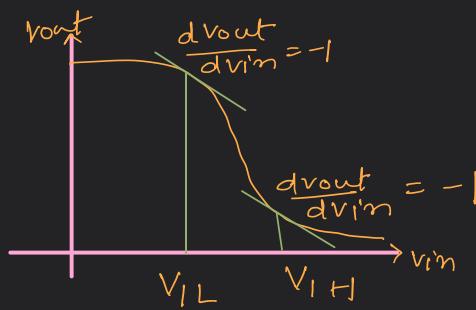
$$\left(\frac{\omega}{L}\right)_{eq} = \frac{1}{(\frac{1}{\omega_{IL}})_1 + (\frac{1}{\omega_{IL}})_2 + \dots + (\frac{1}{\omega_{IL}})_5}$$

Suppose 5 transistors are connected in parallel

$$(\omega_{IL})_{eq} = \varepsilon (\omega/L)_n$$

Ques - Implement XOR using CMOS.

Calculating Noise Margin



$$NM_L = V_{IL} - V_{OL} \quad V_{OL} = 0$$

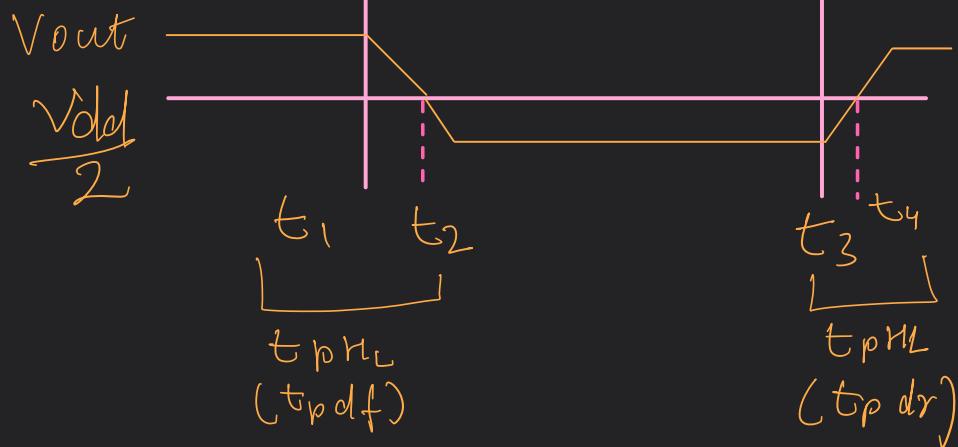
$$NM_H = V_{OH} - V_{IH} \quad V_{OH} = 1.8V$$

Propagation delay of CMOS Inverter

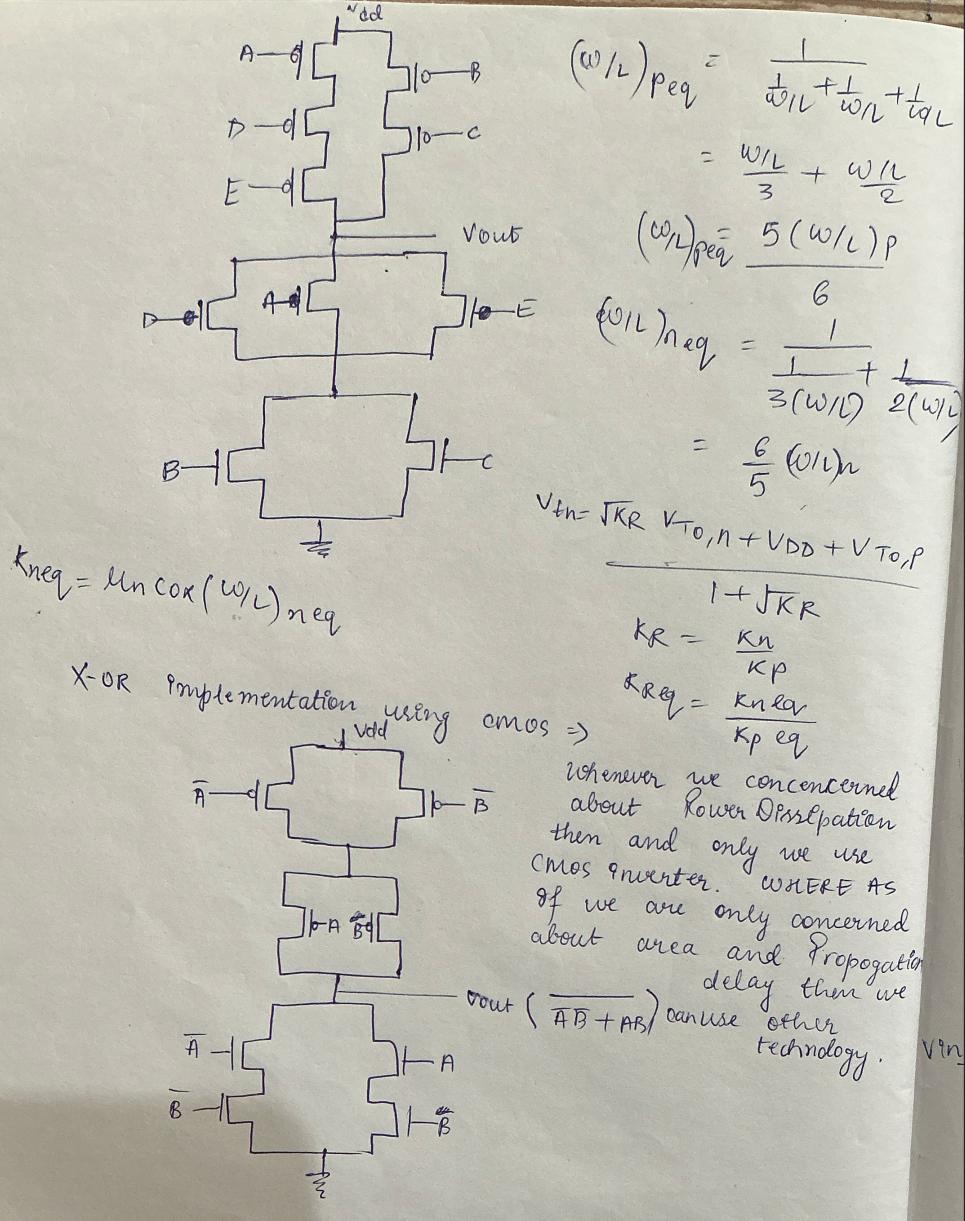


$$t_{pd} = \frac{t_{pH_L} + t_{pLH}}{2}$$

* Main factor is the internal capacitance that's why we are having propagation delay.



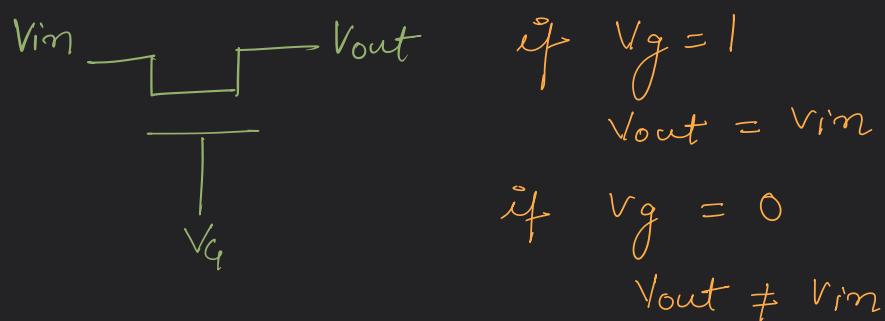
↳ there are five internal MOSFET but we consider only 4 :- C_{GD} , C_{GS} , $\cancel{C_{GB}}$, C_{DB} , C_{SB}



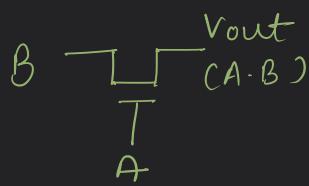
Transmission gate technology

(Pass transistor logic) - PTL

- No. of transistors are less as compared to CMOS
- Resistance will be less as PMOS and NMOS are in parallel
- PTL is only used for switching purposes.



→ to create a AND gate -

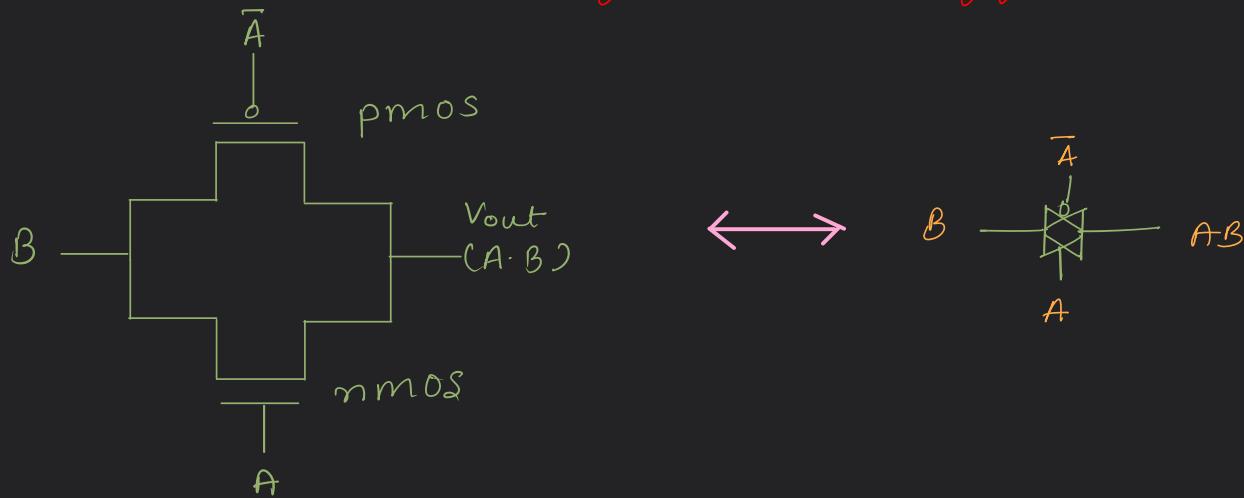


A	B	V _{out}
0	0	0
0	1	0
1	0	0
1	1	1

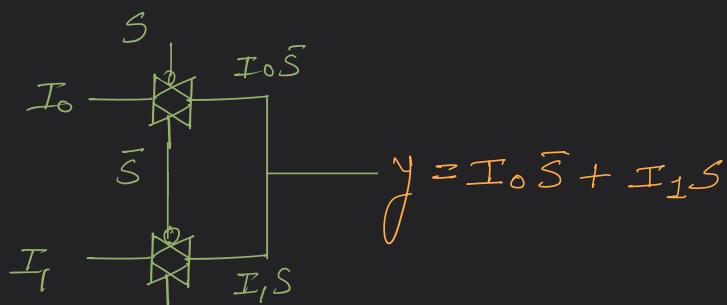
→ if we use nmos only then,
it is good for logic '0'.
but bad for logic '1'.

→ if we use pmos only then,
it is good for logic '1'.
but bad for logic '0'.

Cmos transmission gate technology



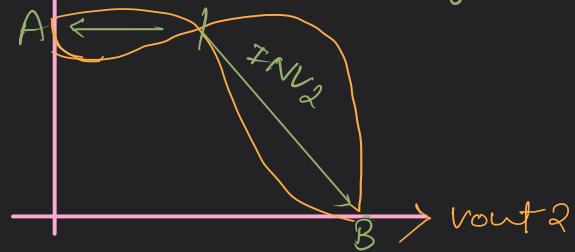
Create 2x1 mux using Cmos transmission gate



→ Implement :

-d by cross coupled inverter structure, we can analyze this graph -

v_{out1} INV₁ C \rightarrow highly unstable.

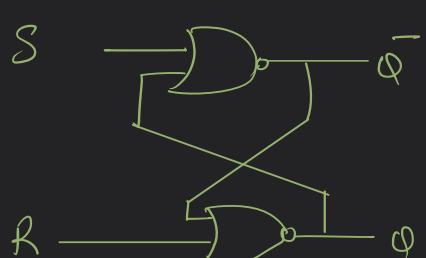


By observing the graph we can say that the ckt. will have 3 operating points A, B & C where A & B are stable points because they are lying in the stable region while the operating point C will be highly unstable point because it is lying in the transition region.

So in this manner it can be proved that the cross coupled inverter structure is the circuit which will always have the stable outputs i-e either state A or B.

If by chance you are getting operating point as C but since it is a unstable point therefore your output will shift either to state A or state B by itself.

CMOS implementation of SR latch -



S	R	Q_{n+1}	\bar{Q}_{n+1}	
0	0	0	1	\rightarrow Hold
0	1	1	0	\rightarrow Reset
1	0	1	0	\rightarrow Set
1	1	not allowed		

