

Experinment No. 12 21118 Title: Sequence defector circuit. objective: To design & implement pequence detector for signence for unng Jk Alip-Alop. Apparatus: Digital board, GP-4 patch-chords, IC741576, JC741508, JC741504, JC741832 & sequiled logic gates if any Theory: The sequence detector is synchronous FSM to defect sequence applied to the input. 2) To checks the input sequence by by bit of moves to the next state if desired bib is obtained. 3) The opp of the crown is zero as long as complete sequence is not deterted. sequence is odiferted at the input side.

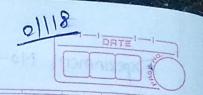
The sequence defector can be implemented using I'm It

() Pf.

4) Moore model can be used for implementation.

· Plu diagram:

uocki -		-1k==
PREJETT -	741576	- 10
CLEAR! -	DUAL	- Ta
		- GND
7cc-	ms Jek ff.	- ek
Clock2 -	JE IT:	
		20
PRESET2 -		200 200
CLEAR 2 -		-2丁



reoledue:

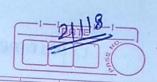
Make the connections as per the logic circuit of sequence detector circuit wing IC 741576 & veerty it truth table.

Design of sequence detector

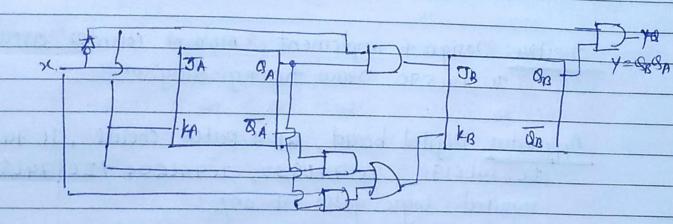
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										-

2 00 01 11 10 0 11 11 1

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Logic diagram



logic gates/ MSI device required for implementation:

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sequence deterta	IC's required	quartity	I olg.
101	NoT	2	J(7404
	AND.	4	1748
# 41 1/21 40 10	Un of	waterly A Var	
Things are seen to	DOAL MS JK FF	#2	IC7476-1 no.

conclusion oncept of sequence detector u studied & implemented