5 DEC

DELD Assignment 05 21118

Title: Design & implement parity generator & checker using Ex-OR.

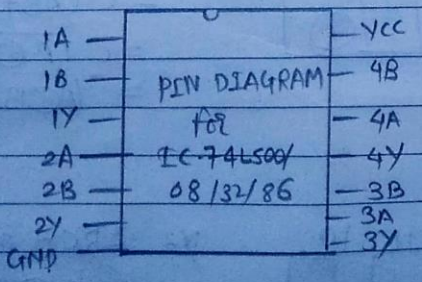
Objective: Design & implement 3 bit (even & odd) parity generator & checker circuit using XOR gates.

Apparatus: Digital Board, GP-4 Patch-Cords, IC-74LS86 & required logic gates.

Theory:

1) Parity generator is a combinational circuit.
2) It generates parity bit in the transmitter.
3) Parity checker checks the parity in the receiver.
4) A combined circuits or devices of parity generators & parity checkers are commonly used in digital systems.
5) In even parity, the added parity bit will make the total number of 1s even amount.
   In odd parity, the added parity bit will make the total number of 1s odd
6) Basic Principle:
   Sum of odd numbers of 1s is always 1 & sum of even numbers of 1s is always zero.
   Such error detecting & correction can be implemented by using Ex-OR gates. (since Ex-OR produces zero o/p when there are even no. of inputs)

Pin Diagram.



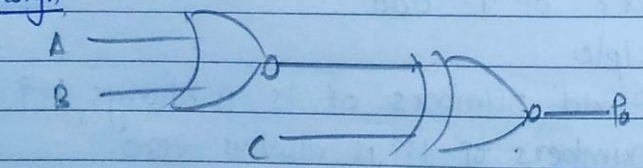
Procedure:

make the connections as per the logic circuit of 3-bit parity generator & 4-bit parity checker & vice-versa & verify the truth table.

Truth Table

Dec Equ.	Input			Output	
	B_2	B_1	B_0	P_o	P_e
0	0	0	0	1	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	0	1

Design



k-map simplifications:

for P_o:

A \ BC	00	01	11	10
0	1		1	
1		1		1

$Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$

$= \bar{C}.(\bar{A}\bar{B} + AB) + C(\bar{A}B + A\bar{B})$

$= \bar{C}\,\overline{(A \oplus B)} + C.(A \oplus B)$

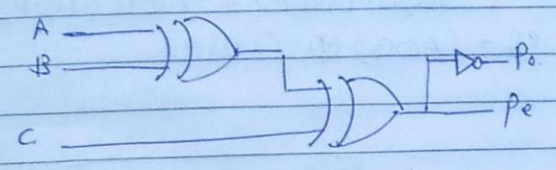
$= \overline{(A \oplus B)} \oplus C$

for P_e:

A \ BC	00	01	11	10
0		1		1
1	1		1	

$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= A \oplus B \oplus C$



for parity checker:

Dec. Eq.	Input:				Output:	
	B_3	B_2	B_1	P	C_{Pe}	C_{Po}
0	0	0	0	0	0	1
1	0	0	0	1	1	0
2	0	0	1	0	1	0
3	0	0	1	1	0	1
4	0	1	0	0	1	0
5	0	1	0	1	0	1
6	0	1	1	0	0	1
7	0	1	1	1	1	0
8	1	0	0	0	1	0
9	1	0	0	1	0	1
10	1	0	1	0	0	1
11	1	0	1	1	1	0
12	1	1	0	0	0	1
13	1	1	0	1	0	0
14	1	1	1	0	1	0
15	1	1	1	1	0	1

k-map simplification:

for C_{Pe} →

AB \ CP	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

$Y = \bar{A}\bar{B}(\bar{C}P + C\bar{P}) + \bar{A}B(\bar{C}\bar{P} + CP) + AB(\bar{C}P + C\bar{P}) + A\bar{B}(\bar{C}\bar{P} + CP)$

$= (\bar{A}\bar{B} + AB)(C \oplus P) + (\bar{A}B + A\bar{B})\overline{(C \oplus P)}$

$= \overline{A \oplus B} \cdot ((\oplus P) + A \oplus B (\overline{(\oplus P)}$

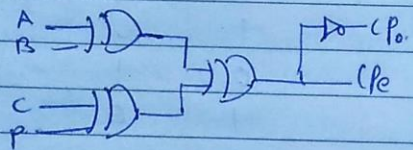
$C_{Pe} = (A \oplus B) \oplus ((\oplus P)$

for C_{Po}:

AB \ C_{Po}	01	11	10
00	1		1
01		1	1
11	1		1
10		1	1

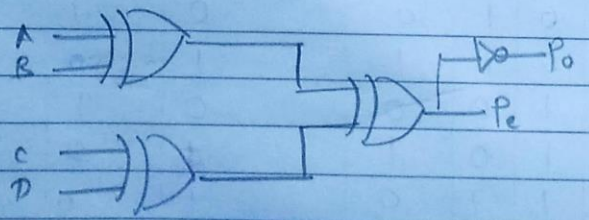
$C_{Po} = \overline{(A \oplus B)} \oplus (\overline{(\oplus P)})$

Also $C_{Po} = \overline{C_{Pe}}$

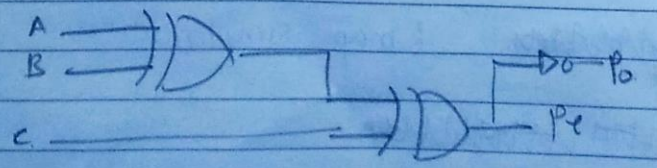


circuit diagram:

4-bit even/odd parity generator



3-bit parity generator



Logic gates / MSI device required for implementation:

Sr. No.	Title	Name of IC	No. of gates req	IC req.
01	3 bit even parity generator	Quad. 2 i/p XOR 7486	2	1
	3-bit odd parity generator	Quad. 2 i/p XOR 7486	3	1
02	4-bit even parity generator	Quad. 2-i/p XOR 7486	3	1

Conclusion:

Designed & implemented 3-bit parity generator & 4-bit parity checker using min. number of logic gates & vice versa.