Experiment No: 05

21118

Title: Digital magnitude comparator circuit.

Objective:

⇒ Design & implement 1-bit digital magnitude comparator ckt using logic gates

⇒ Design & implement 2-bit digital magnitude comparator ckt using logic gates.

Apparatus:

Digital board, GP-4 Patch chords, IC74LS86, IC74LS32, IC74LS08 / IC74LS04 / IC74LS85 & required logic gates

Theory

⇒ Magnitude comparator is a logic circuit, which compares two signals A & B and generates three logical outputs wheather A>B, A=B, A<B.

⇒ IC7485 is a high speed 4-bit magnitude comparator which compares two 4-bit words.

The A=B input must be held high for proper compare operation.

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes.

Three fully-decoded decision about two, 4-bit words (A,B) are made & are externally available at three outputs

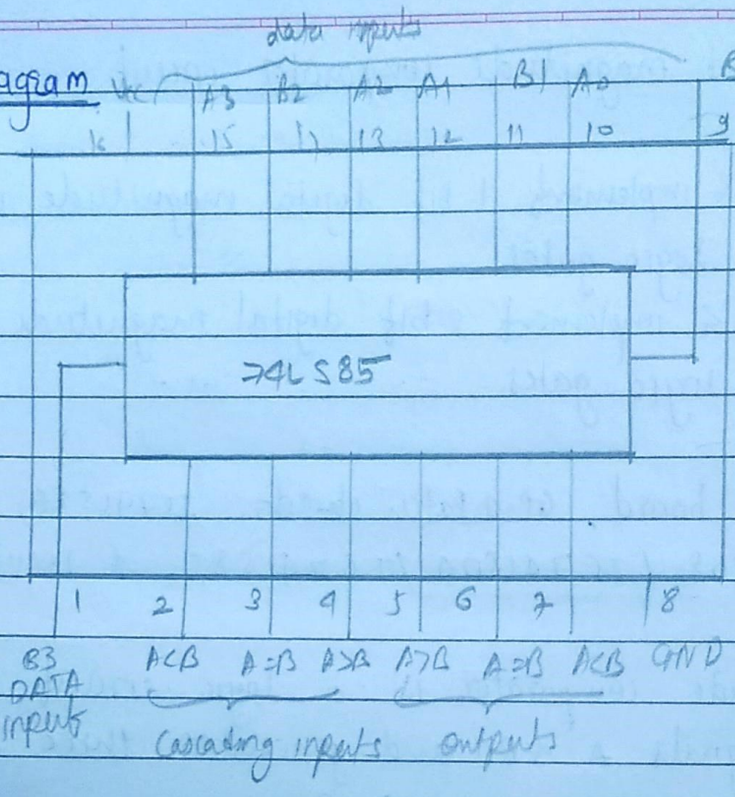
These devices are fully expandable to any number of bits without external gates.

Words of greater words of greater length may be compared by connecting comparators in cascade.

⇒ The A>B, A<B, A=B outputs of a stage handling less significant bits are connected to the corresponding inputs of the next stage handling more-significant bits.

⇒ The stage handling the least significant bits must have a high-level voltage applied to the A=B input. The cascading path is implemented with only a two-gate level delay to reduce overall comparison times for long word

Pin Diagram



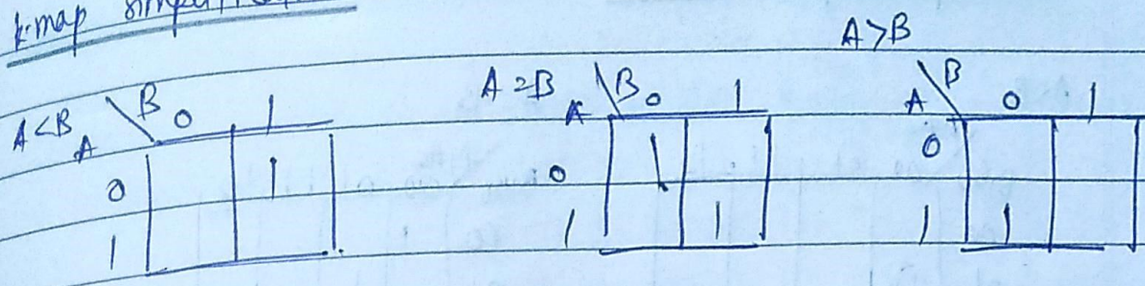
Procedure:

1) make the connections as per the logic circuits of 1-bit digital comparator circuit & verify its truth table
2) Make the connections as per the logic circuit of 1-bit digital comparator circuit & verify its truth table
3) Make the connections as per the pin-diagram of IC 74LS85 & verify it's function table.
4) Make the connections as per the logic circuit of 5-bit digital comparator circuit & verify its function table.
5) Make the connections as per the logic circuits of 8-bit digital comparator circuit & verify its function table.

Design of 1-bit Digital comparator

Input		Output		
A	B	$Y_1 = A<B$	$Y_2 = A=B$	$Y_3 = A>B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

k-map simplification:



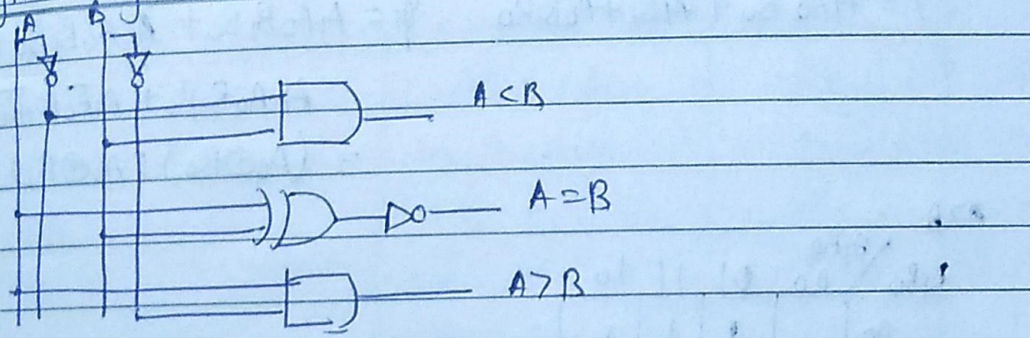
$Y = \bar{A}B$

$Y = \bar{A}\bar{B} + AB$

$= \overline{A \oplus B}$

$Y = A\bar{B}$

logic diagram:

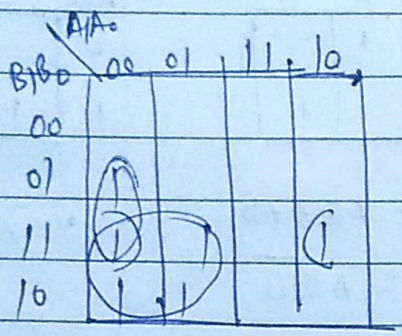


Design of 2-bit digital comparator:

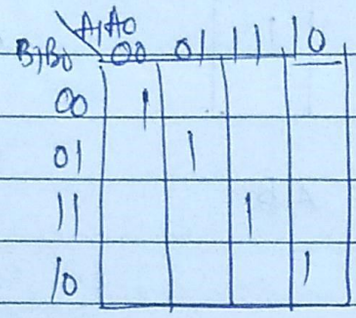
Dec eqn.	Inputs				Outputs		
	A1	A0	B1	B0	$Y_1 = A<B$	$Y_2 = A=B$	$Y_3 = A>B$
0	0	0	0	0	0	1	0
1	0	0	0	1	1	0	0
2	0	0	1	0	1	0	0
3	0	0	1	1	1	0	0
4	0	1	0	0	0	0	1
5	0	1	0	1	0	1	0
6	0	1	1	0	1	0	0
7	0	1	1	1	1	0	0
8	1	0	0	0	0	0	1
9	1	0	0	1	0	0	1
10	1	0	1	0	0	1	0
11	1	0	1	1	1	0	0
12	1	1	0	0	0	0	1
13	1	1	0	1	0	0	1
14	1	1	1	0	0	0	1
15	1	1	1	1	0	1	0

K-map simplification:

A<B



A=B

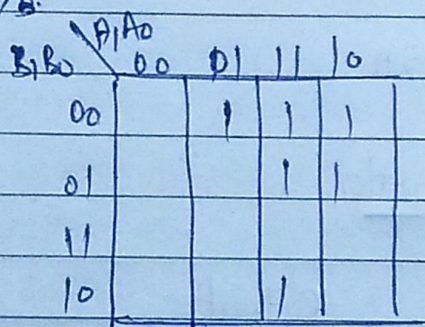


$y = \bar{A}_1\bar{A}_0B_0 + \bar{A}_1B_1 + \bar{A}_0B_1B_0$

$y_1 = \bar{A}_1A_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0B_1B_0 + A_1A_0B_1B_0 + A_1\bar{A}_0B_1\bar{B}_0$

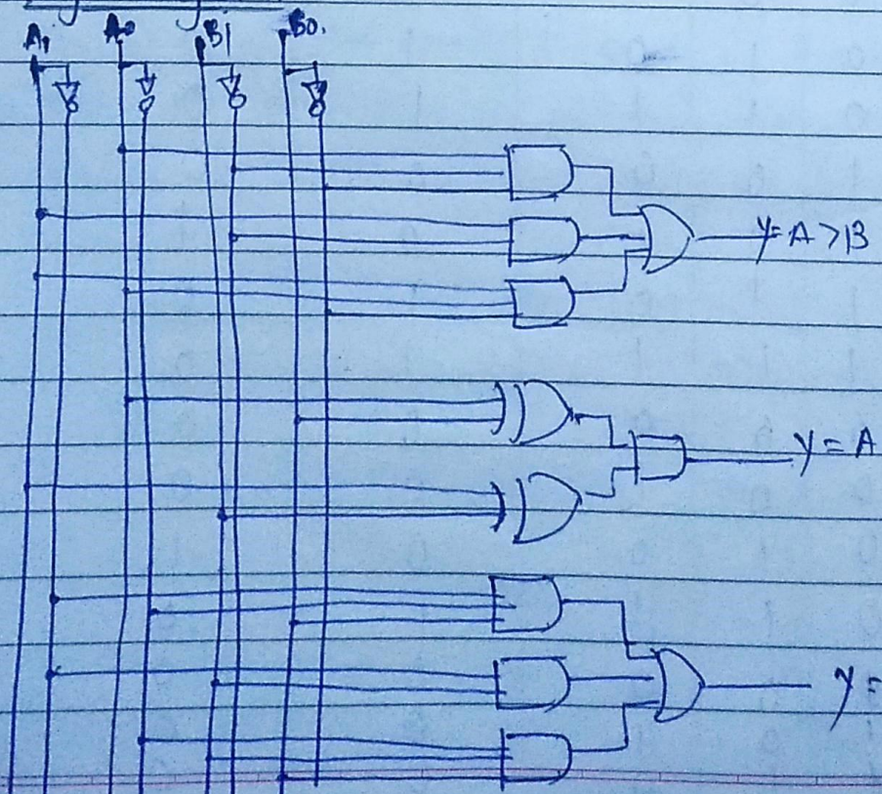
$= (A_0 \oplus B_0)(A_1 \oplus B_1)$

A>A.



$y = A_0\bar{B}_1\bar{B}_0 + A_1\bar{B}_1 + A_1A_0\bar{B}_0$

Logic diagram:



Logic gates/ MSI device required for implementation:

S.No.	Title	Name of IC	No. of gates required	IC required
1.	1-bit comparator using logic gates	AND IC7408	4	1
		NOT IC7404	2	1
		OR IC7432	1	1
2.	2 bit comparator using logic gates (A<B)	AND IC7408	4	1
		NOT IC7404	2	1
		OR IC7432	2	1
	A>B	AND IC7408	4	1
		NOT IC7404	2	1
		OR IC7432	2	1
	A=B	AND IC7408	4	1
		NOT IC7404	3	1
		OR IC7432	3	1

Conclusion

1 bit comparator, 2 bit comparator is studied & implemented using basic logic gates.