

▷

$$A) f(A, B, C, D) = \sum m(1, 2, 3, 4, 9) + d(10, 11, 12)$$

→

$$\text{Given: } f(A, B, C, D) = \sum m(1, 2, 3, 4, 9) + d(10, 11, 12)$$

Solution: The k-map for the given function is 4-variable & it will be represented as

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	X	0	0	0
10	0	1	X	X

X → don't care.

$$Y = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$$

I II III

$$= B\bar{C}\bar{D} + \bar{B}(C+D)$$

$$= \bar{B}(\bar{C}+D) + \bar{B}(C+D) \quad \dots \text{by de-morgan's law.}$$

$$= B \oplus (C+D)$$

Ans.

$$B) f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$$

→

Solution: The k-map for the given function is 4-variable k-map. & it will be represented as

AB \ CD	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	0	0	0	1
10	1	1	1	0

$$Y = A\bar{B} + A\bar{D} + \bar{B}\bar{C} + \bar{B}D + ABC\bar{D}$$

$$Y = \bar{A}(\bar{B}+D) + \bar{B}(\bar{C}+D) + ABC\bar{D}$$

Ans.

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A)

→ Given: BCD Adder using IC 7483.

& to find: operations to verify

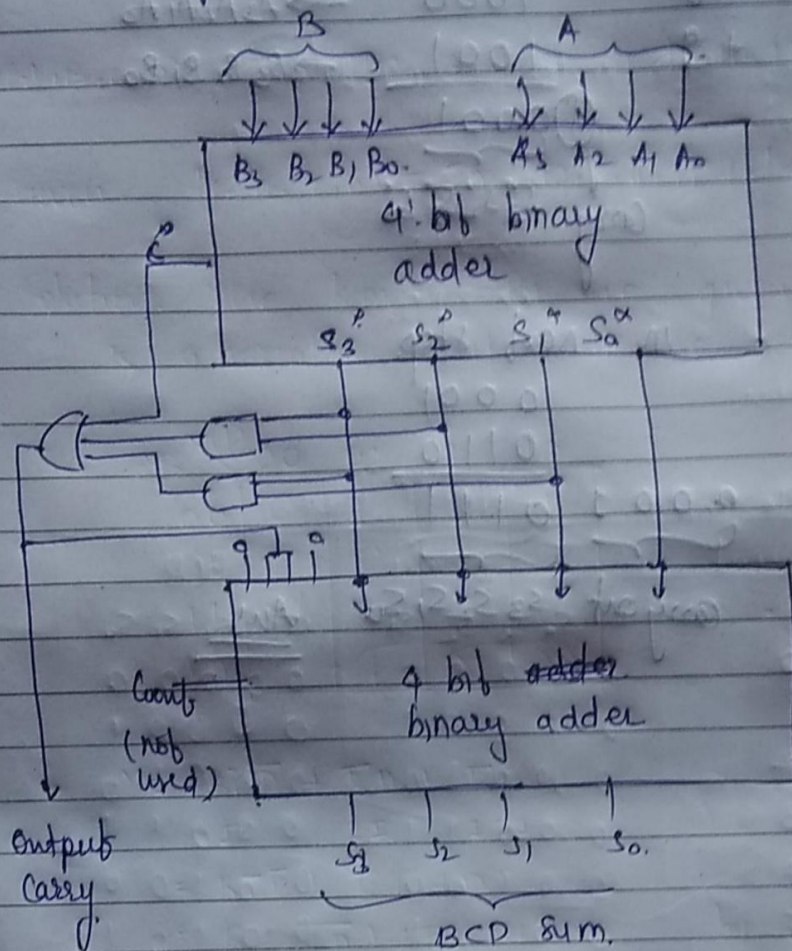
a) $2+3$ b) $7+8$ c) $8+9$

Solution:

Truth table: ^{intermediate values}

Decimal:	Binary	BCD
	C, S_4, S_3, S_2, S_1	C, S_4, S_3, S_2, S_1
0	0 0 0 0 0	0 0 0 0 0
1	0 0 0 0 1	0 0 0 0 1
2	0 0 0 1 0	0 0 0 1 0
3	0 0 0 1 1	0 0 0 1 1
4	0 0 1 0 0	0 0 1 0 0
5	0 0 1 0 1	0 0 1 0 1
6	0 0 1 1 0	0 0 1 1 0
7	0 0 1 1 1	0 0 1 1 1
8	0 1 0 0 0	0 1 0 0 0
9	0 1 0 0 1	0 1 0 0 1
10	0 1 0 1 0	1 0 0 0 0
11	0 1 0 1 1	1 0 0 0 1
12	0 1 1 0 0	1 0 0 1 0
13	0 1 1 0 1	1 0 0 1 1
14	0 1 1 1 0	1 0 1 0 0
15	0 1 1 1 1	1 0 1 0 1
16	1 0 0 0 0	1 1 0 0 0
17	1 0 0 0 1	1 1 0 0 1
18	1 0 0 1 0	1 1 0 1 0

circuit diagram:



1) For BCD addition two 4-bit binary adders are used.

2) The output of first adder is given to the 1st inputs of 2nd adder & 2nd inputs of 2nd adder is based on the truth table which is $C + S_3 S_2 + S_3 S_1$

operations

a) $2 + 3 \Rightarrow$

2

+ 3

binary form

0010 \rightarrow A₃ A₂ A₁ A₀

0011 \rightarrow B₃ B₂ B₁ B₀

0101 \rightarrow S₃ S₂ S₁ S₀

(No carry)

b) $7 + 8 \Rightarrow$

7

+ 8

binary form

0111 \rightarrow A₃ A₂ A₁ A₀

1000 \rightarrow B₃ B₂ B₁ B₀

(No carry)

$$\Rightarrow 8+9$$

$$\begin{array}{r} 8 \quad 1000 \rightarrow A_3 A_2 A_1 A_0 \\ + 9 \quad 1001 \rightarrow B_3 B_2 B_1 B_0 \end{array}$$

$$\begin{array}{r} \textcircled{1} 0001 \\ \downarrow \\ \text{Carry } s_3 s_2 s_1 s_0 \end{array}$$

in next step

$$\begin{array}{r} 0001 \\ 0110 \\ \hline 0001 \quad 0111 \\ \hline \text{Carry out } s_3 s_2 s_1 s_0 \quad \underline{\text{Ans}} \end{array}$$

Q2

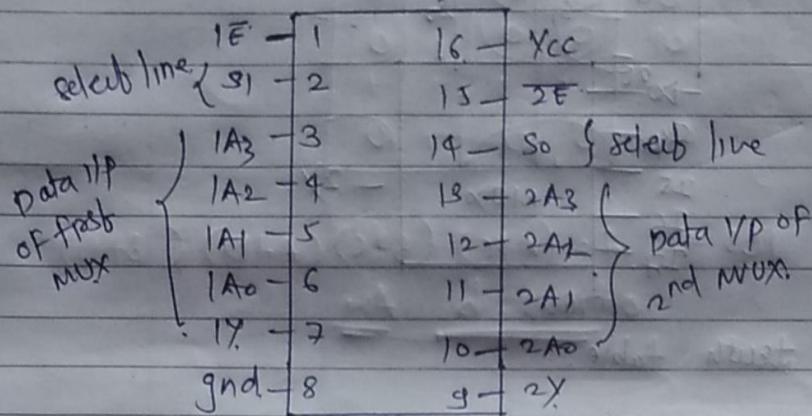
B)

→ To design: full Adder using IC 74153.

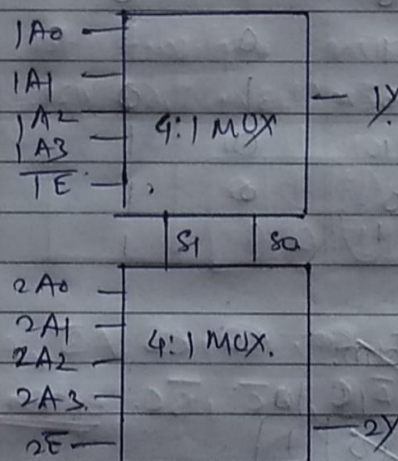
Solution:

IC 74153:

- It is a dual 4:1 Demultiplexer IC.
- pin configuration of IC is as below:



- this IC can also be represented as
(to show in circuit diagrams)



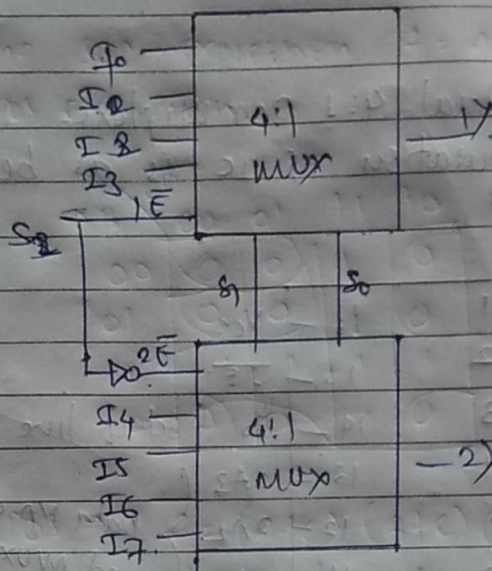
full adder using IC 74153:

→ full adder:

$$\text{Sum: } f(A, B, C) = \sum m(1, 2, 4, 7)$$

$$\text{Carry: } f(A, B, C) = \sum m(3, 5, 6, 7)$$

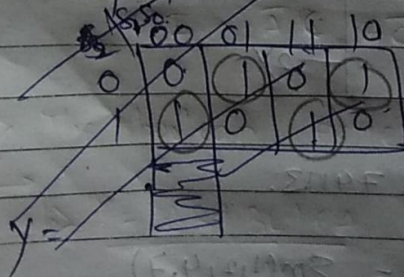
we have to convert this IC into 8:1 MUX, for this we use enable input (pin 15)



truth table:

A	I_0	S_1	S_0	Sum	Carry
0	0	0	0	0	0
0	0	0	1	1	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	0	0	1
1	1	1	1	1	1

K-map for Sum:



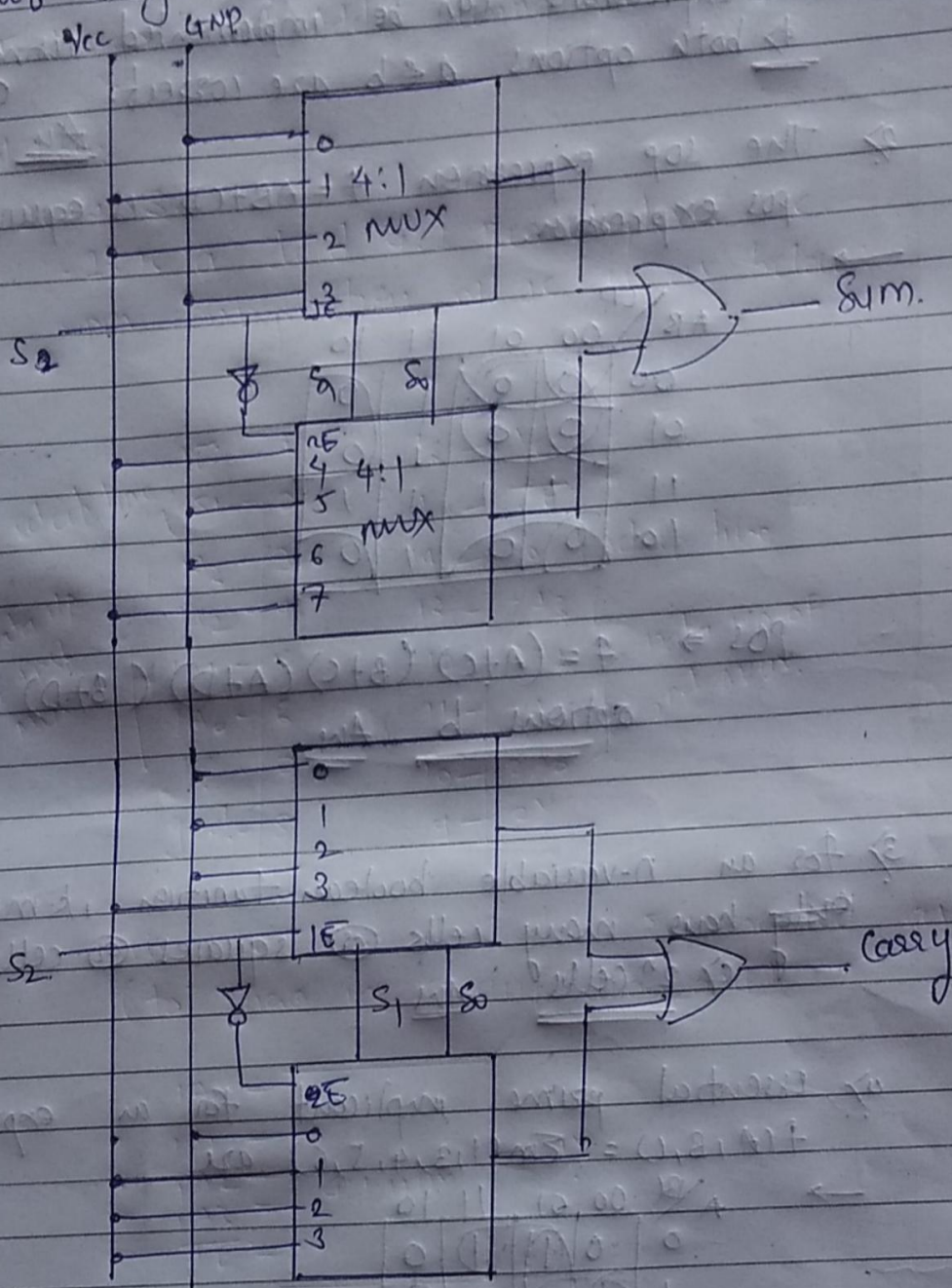
Q4 B)

16:1 MUX

SHREE

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circuit diagram from truth table.



Q. 4

Q. 1) POS expressions can be implemented using
 both options a & b are correct. Ans

Q. 2) The SOP expression $f = AB + CD$ is equivalent to
 POS expression.

→

AB \ CD	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	1	1	1	1
10	0	0	1	0

POS $\Rightarrow f = (A+C)(B+C)(A+D)(B+D)$

options b Ans

Q. 3) For an n-variable boolean function, k-map contains
 only how many cells (a) squares (b) cells.
 c) 2^n cells Ans

Q. 4) Essential prime implicant for an expression
 $f(A, B, C) = \sum m(1, 3, 4, 5, 6)$ are.

→

A \ B	00	01	11	10
0	0	0	1	0
1	1	1	0	1

PI: ~~AB~~, ~~BC~~, ~~AC~~, ~~AB~~ AB, AC, BC

EPI: $\overline{A}B, \overline{A}C, \overline{B}C$ option b Ans

Q. 5) The boolean expression for y is

→
 b) $y = AB + BC + CA$

Ans

Q4 >

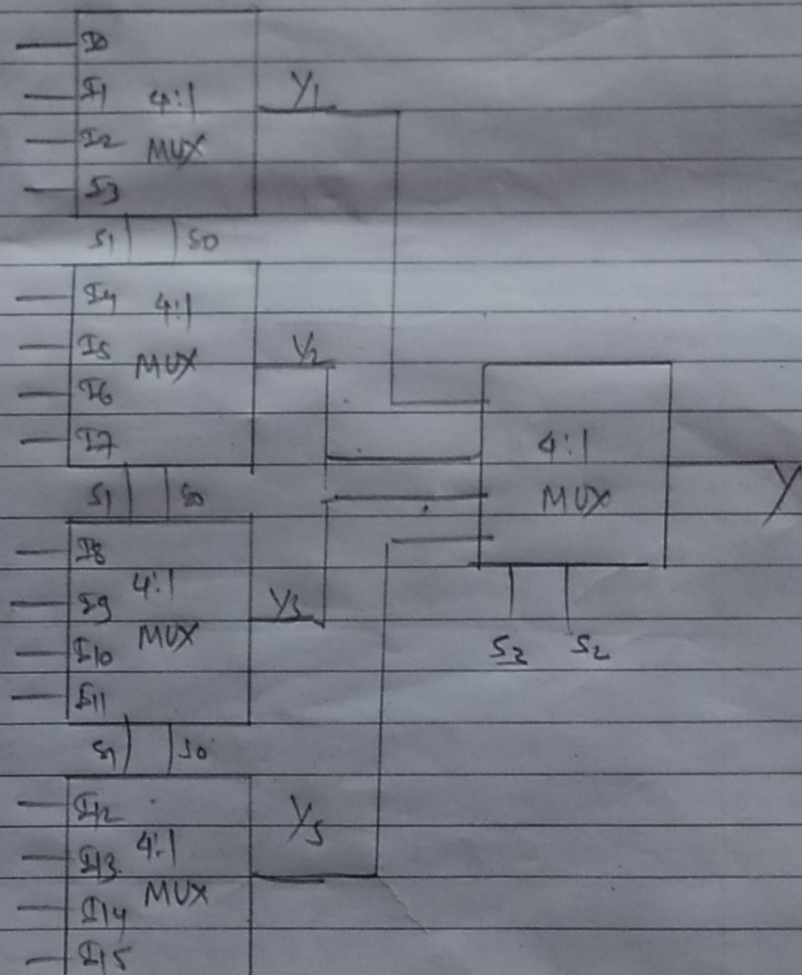
16:1 MUX using 4:1 MUXES

→

16:1 MUX → 16 input & 1 output
also 4 select lines (S_0, S_1, S_2, S_3)

4:1 MUX → 4 input & 1 output.

∴ we require at least 4 4:1 MUXES.



1> The Y_1, Y_2, Y_3, Y_4 outputs of first level muxes are connected as input to 2nd level mux.

2> In 1st level input is selected by select lines

$S_1, S_0 \leftarrow$ in 2nd level by select lines S_2, S_1
 3) The output of the 2nd level mux will be
 the output of 4-to-1 mux.

$$\text{Input 1} \oplus \text{Input 2} \leftarrow \text{XOR 1st}$$

$$\text{2nd XOR 1st} \oplus \text{2nd XOR 2nd} \leftarrow \text{XOR 2nd}$$

Level 1st to 2nd level mux output is
 Level 2nd to 3rd level mux output is
 Level 3rd to 4th level mux output is