Experiment No. 09 21118

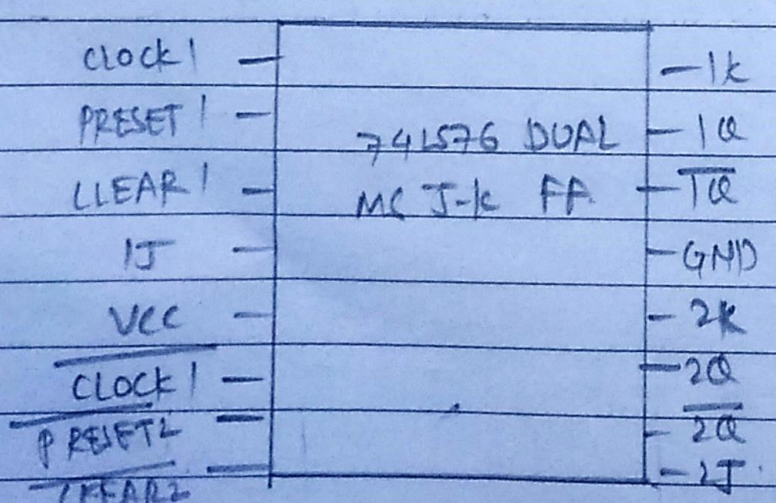
Title: UP/DOWN Counter.

Objective: Design & implement 3-bit Synchronous UP/DOWN counter using mode control switch (Use IC 74LS76) & verify it's truth table.
Draw timing-diagram
When M=0: circuit performs UP-counting operation
When M=1: Circuit performs DOWN-counting operation

Apparatus:
Digital Board, GP-4 patch chords, IC 74LS76, IC 74LS32, IC 74LS04 / IC 74LS08 & required logic gates.

Theory:
1) Counter is a sequential logic device which is used to count the number of pulses given to the ckt.
2) Counter is classified into two categories synchronous & synchronous.
3) In Asynchronous counter output of first flip-flop goes to the clock of next & so on. & input of of all flip flop is connected to Vcc for IC 74LS76.
4) All set & reset pins are connected to Vcc.

Pin diagram:



Procedure

Make the connections as per the logic circuit of 3-bit synchronous UP/DOWN Counter circuit using IC-74LS76 & verify it's Truth table.

Observation table

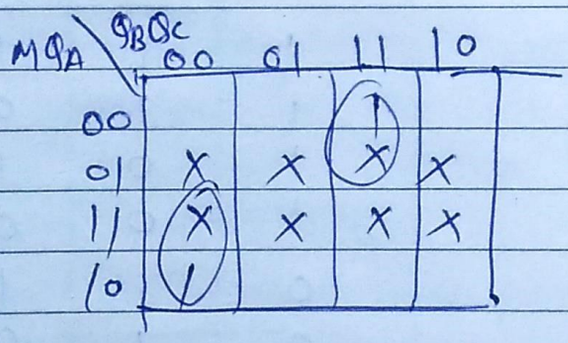
clock pulse.	Mode Control (M)	Output		
		Q_A	Q_B	Q_C
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	1
3	1	1	0	0
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	1	0	0	0

Design of 3-bit synchronous UP/DOWN counter using Mode control input (switch)

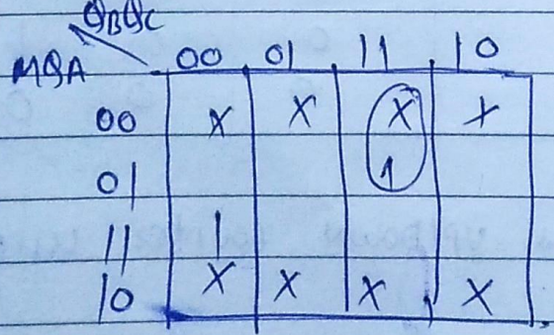
M	PRESENT STATE			NEXT STATE			INPUT					
	Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	1	0	0	X	1	X	X	1

0	0	1	0	0	1	1	0	X	X	0	1	X
0	0	1	1	1	0	0	1	X	X	1	X	1
0	1	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	1	1	0	X	1	1	X	X	X
0	0	1	0	1	1	1	X	X	X	0	1	X
0	0	1	1	0	0	0	X	X	X	1	X	1
1	1	0	1	1	1	0	X	X	X	0	X	1
1	1	0	0	1	0	1	X	X	X	1	X	X
1	1	0	1	1	0	0	X	0	0	X	X	1
1	1	0	0	0	1	1	X	1	1	X	1	X
1	0	0	1	0	1	0	X	X	X	0	X	1
1	0	0	0	0	0	1	0	X	X	1	1	X
1	0	0	1	0	0	0	0	0	0	X	X	1
1	0	0	0	1	1	1	0	1	1	X	1	X

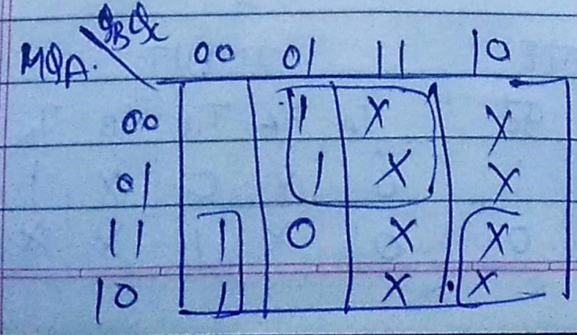
k.map simplification:



$$J_A = \bar{M} Q_B Q_C + M \bar{Q}_B \bar{Q}_C$$



$$K_A = \bar{M} Q_B Q_C + M \bar{Q}_B \bar{Q}_C$$



$$J_B = \bar{M} Q_C + M \bar{Q}_C$$

$M Q_A$ \ $Q_B Q_C$	00	01	11	10
00	x	x	1	
01	x	x	1	
11	x	x		1
10	x	x		1

$K_B = \overline{M} Q_C + M \overline{Q}_C$

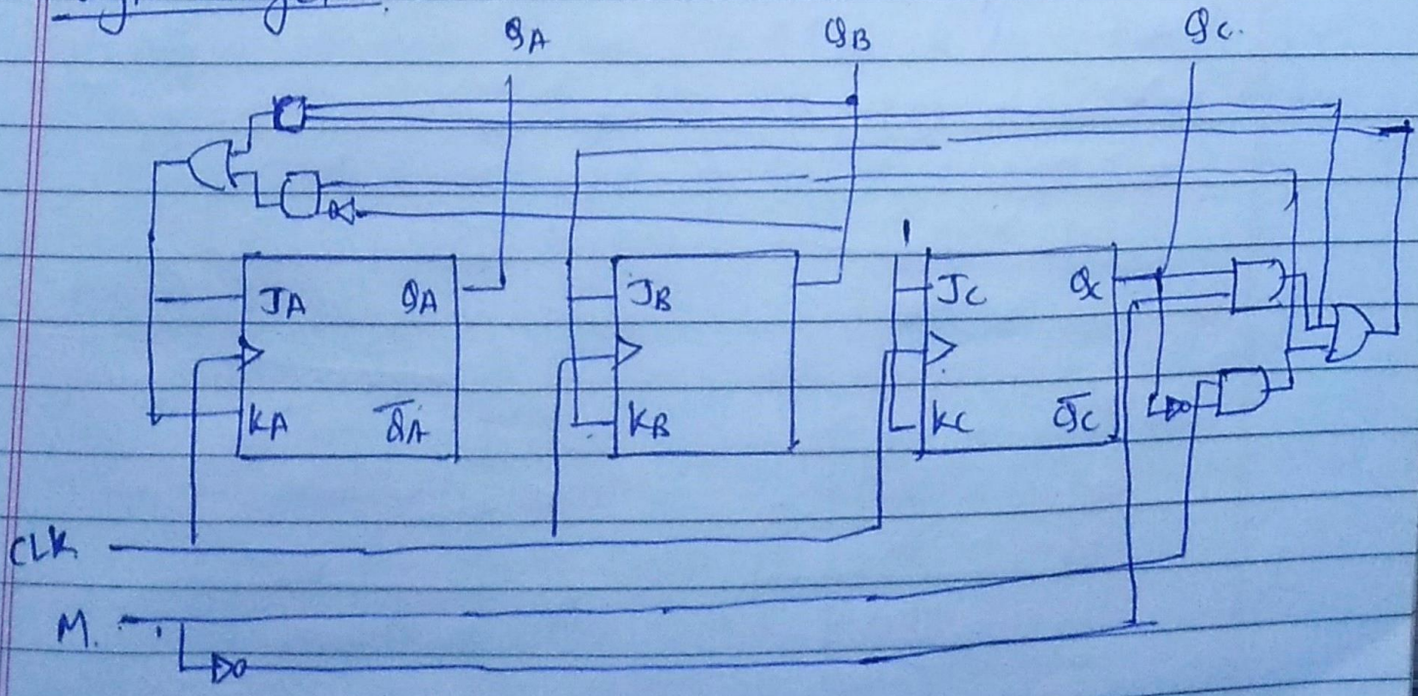
$M Q_A$ \ $Q_B Q_C$	00	01	11	10
00	1	x	x	1
01	1	x	x	1
11	1	x	x	1
10	1	x	x	1

$J_C = 1$

$M Q_A$ \ $Q_B Q_C$	00	01	11	10
00	x	1	x	x
01	x	1	1	x
11	x	1	1	x
10	x	1	1	x

$K_C = 1$

logic diagram:



logic gates/ MSI Device required:

Sl No.	Title	Name of Ic	No. of gates req.	IC req.

01	3-bit Synchronous UP/DOWN counter	Quad JK FF7476	–	2
		Hex inverter 7404	3	1
		Quad-2-i/p AND 7408	4	1
		Quad-2-i/p OR 7432	2	1

Conclusion

Designed & implemented 3-bit Synchronous UP/DOWN counter using mode control switch (Use IC-74LS76)