Experiment No. 12 21/18

Title: Sequence detector circuit.

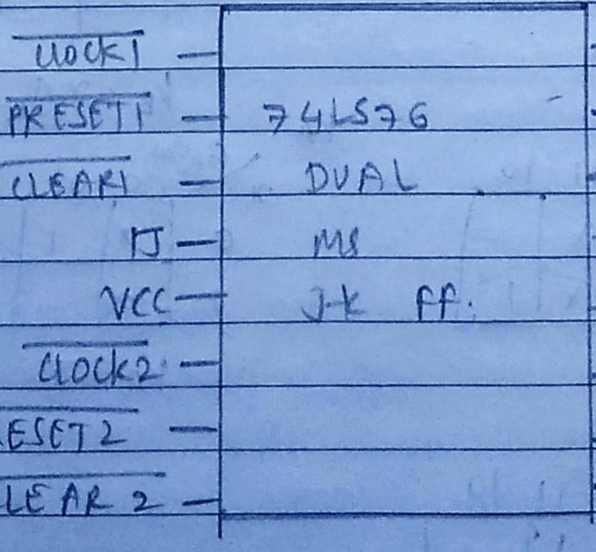
Objective: To design & implement sequence detector for sequence 101 using JK flip-flop.

Apparatus: Digital board, GP-4 patch-chords, IC 74LS76, IC74LS08, IC-74LS04, IC74LS32 & required logic gates if any.

Theory:

1) The sequence detector is synchronous FSM to detect sequence applied to the input.
2) It checks the input sequence bit by bit & moves to the next state if desired bit is obtained.
3) The o/p of the circuit is zero as long as complete sequence is not detected.
4) The o/p becomes one as soon as the complete sequence is detected at the input side.
5) The sequence detector can be implemented using JK ff (or) D ff.
6) Moore model can be used for implementation.

Pin diagram:



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Procedure:

Make the connections as per the logic circuit of sequence detector circuit using IC 74LS76 & verify it's truth table.

Design of sequence detector

X	Q_B	Q_A	Q_B^+	Q_A^+	J_B	K_B	J_A	K_A	Y
0	0	0	0	0	0	x	0	x	0
0	0	1	1	0	1	x	x	1	0
0	1	0	0	0	x	1	0	x	0
0	1	1	1	0	x	0	x	1	1
1	0	0	0	1	0	x	1	x	0
1	0	1	0	1	0	x	x	0	0
1	1	0	1	1	x	0	1	x	0
1	1	1	0	1	x	1	x	0	1

k-map simplification

J_B

x \ Q_BQ_A	00	01	11	10
0	0	1	x	x
1	0	0	x	x

$J_B = \bar{x} Q_A$

K_B

x \ Q_AQ_B	00	01	11	10
0	x	x	0	1
1	x	x	1	0

$K_B = x Q_A + \bar{x} \bar{Q_A}$

J_A

x \ Q_BQ_A	00	01	11	10
0		x	x	
1	1	1	x	1

$J_A = x$

K_A

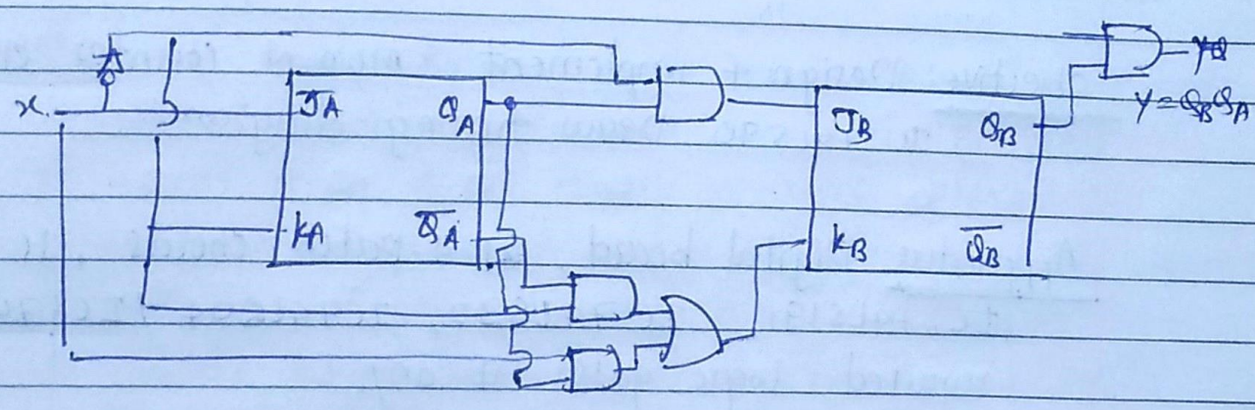
x \ Q_BQ_A	00	01	11	10
0	x	1	1	x
1	x			x

$K_A = \bar{x}$

x \ Q_BQ_A	00	01	11	10
0			1	
1			1	

$Y = Q_B Q_A$

Logic diagram



Logic gates/ MSI device required for implementation:

Sequence detector →	IC's required	quantity	IC req.
101	NOT	1	IC7404
	AND	4	IC7408
	OR	1	
	DUAL MS JK FF	2	IC7476 1 no.

Conclusion

Concept of sequence detector is studied & implemented