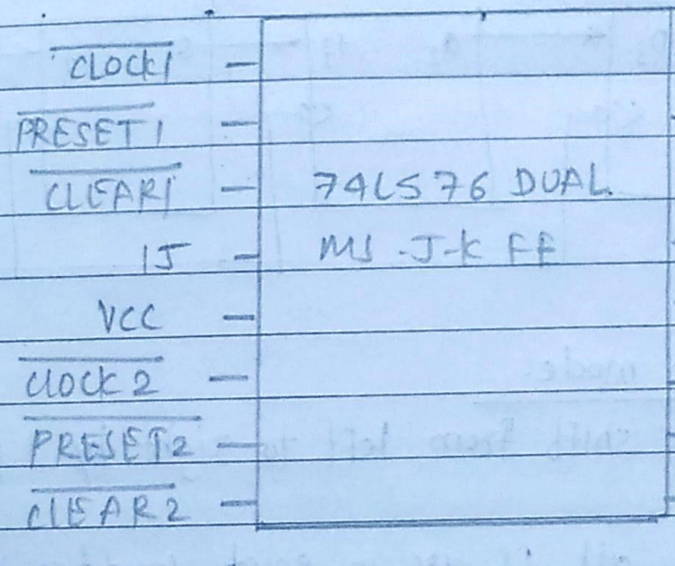
Title: Shift Registers

Objective: To study shift registers SISO, SIPO, PISO, PIPO

Apparatus: Digital board, GP-G patch chords, IC 74LS76, IC74LS08, IC74LS04, IC74LS32 & required logic gates if any.

Pin Diagram:



Theory:

1) SISO

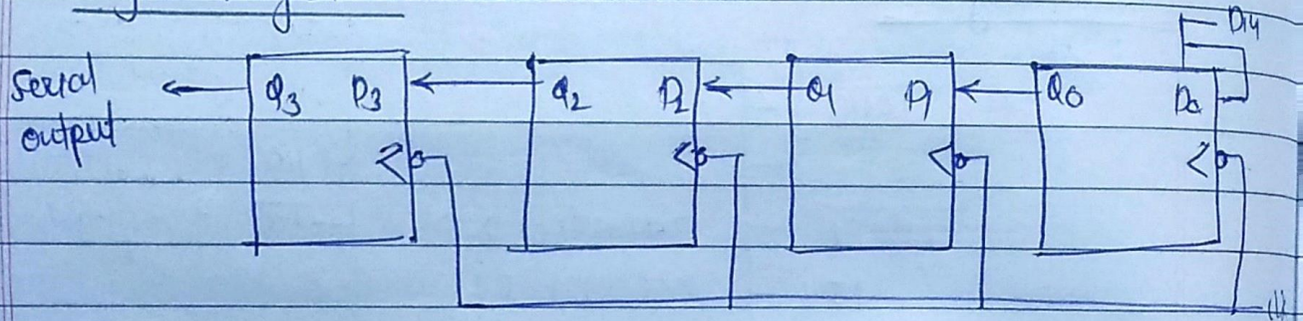
left shift mode :

1) data is shifted left by 1 position per 1 clock cycle.
2) Consider 4 ff initially all in reset condition.
3) If Din=1 is connected to D_0 of ff-0, the output of ff-0 is connected to D_1 of ff-1 & so on.
4) Hence on the first falling edge the output will be 0001
5) The Q values of the rest ff's will then change respectively corresponding to successive clock pulses

Q_3 Q_2 Q_1 Q_0

Q_3	Q_2	Q_1	Q_0	D_{IN}
0	0	0	0	
0	0	0	1	1
0	0	1	1	1
0	1	1	1	1
1	1	1	1	1

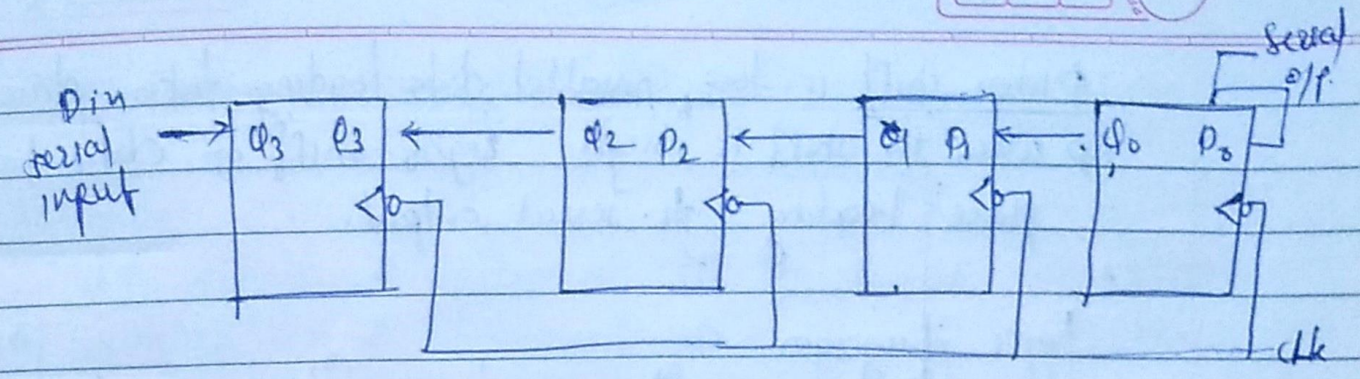
logic diagram



Right shift mode:

1) Data bits shift from left to right by 1 position per clock cycle.
2) Initially all ff are in reset condition.
3) $D_{IN} = 1$ is applied to D_3 of ff-3; o/p of ff-3 is connected to ff-2 & so on.
4) When the first clock pulse is applied, Q_3 becomes 1. The o/p's of respective ff's change after successive clock pulses.

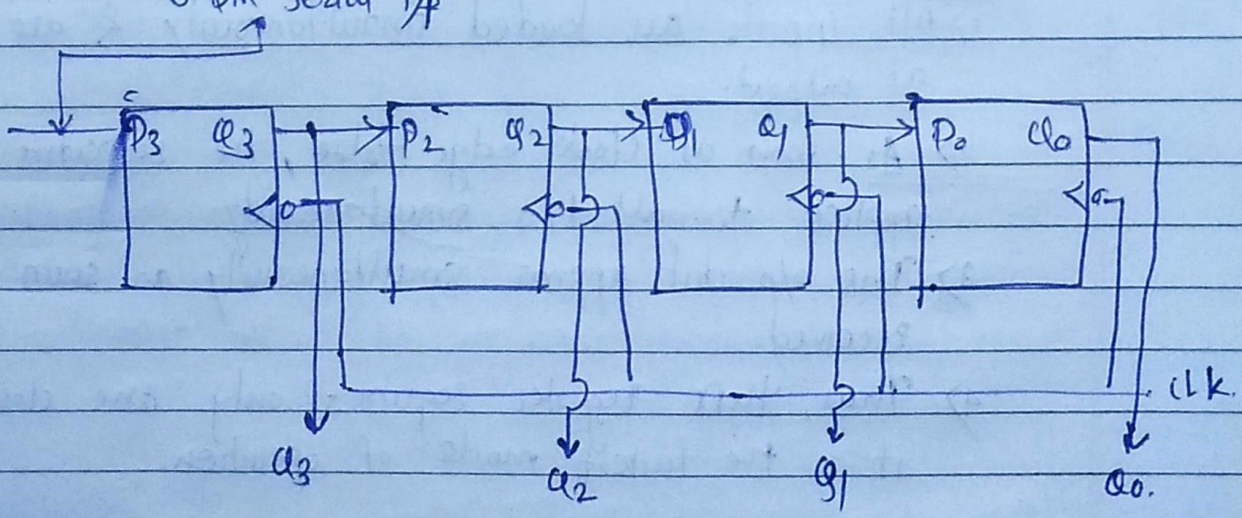
Q_3	Q_2	Q_1	Q_0	D_{IN}
0	0	0	0	
1	0	0	0	1
1	1	0	0	1
1	1	1	0	1
1	1	1	1	1



2) SIPO

1) In this operation, data is entered serially & taken out in parallel
2) The outputs are disabled as long as the data is loading bit by bit.
3) When the data is loaded completely all the o/p's are enabled simultaneously.
4) for a four bit input, output is displayed after 4 clock pulses. So the time required is SISO.

logic diagram.

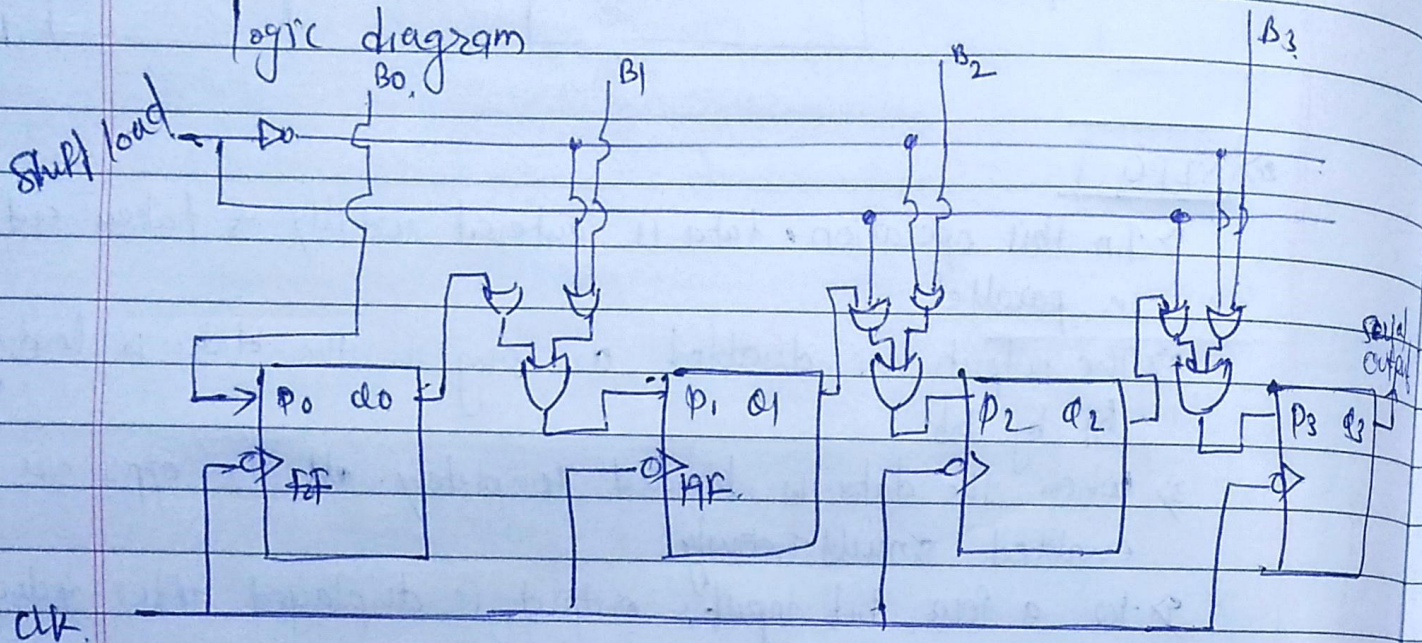


3) PISO

1) In this mode, the bits are entered in parallel in shift register.
2) output of previous ff is connected to the input of the next ff via a combinational circuit.
3) There are two modes in which the combinational circuit can work namely shift & load.

2) When shift is low, parallel data loading takes places.
3) When the shift is high right shift of data takes place leading to serial output.

logic diagram



4) PIPO

1) All inputs are loaded simultaneously & are available at output.
2) As soon as clock edge 'false', the respective I/p bit is applied to all ff's simultaneously.
3) The o/p bit appear simultaneously as soon as i/p is received.
4) Thus, this register requires only one clock pulse & it is the fastest mode of operation.

Conclusion

Concept of shift registers : SISO, SIPO, PISO, PIPO has been studied.