

25 sep

DELP
Assignment - (Unit II & I)

21118

Page No.	
Date	

- Q) Write the logic expression for given truth table & draw the logic diagrams.

inputs | outputs.

A B | S C

0 0 | 0 0

0 1 | 1 0

1 0 | 1 0

1 1 | 0 1

inputs | outputs

A B | P Q

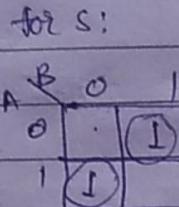
0 0 | 0 0

0 1 | 0 1

1 0 | 1 0

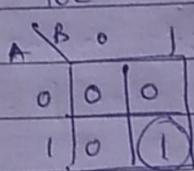
1 1 | 0 0

for S:



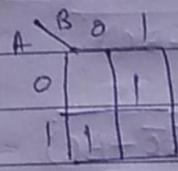
$$\therefore S = A\bar{B} + \bar{A}B \\ = A \oplus B$$

for C:



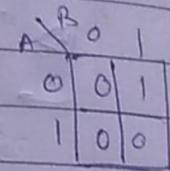
C = AB

for P:



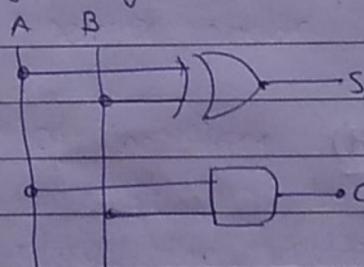
$$P = A\bar{B} + \bar{A}B \\ = A \oplus B$$

for Q:

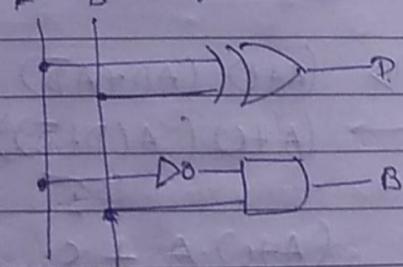


B = \bar{A}B

logic diagram:



logic diagram:



- Q) Simplify the boolean function:

i) $f(x_1, y_1, z) = \sum m(2, 3, 4, 5)$

→ 3-variable k-map.

x	y	z	00	01	11	10
0	0	0	1	1	1	1
1	1	1	1	1	0	0

$$Y = \underbrace{x\bar{y}}_{F} + \underbrace{\bar{x}y}_{E} \quad F \equiv \text{M}(2, 3) \quad E \equiv \text{M}(4, 5)$$

ii) $f(x_1, y_1, z) = \sum m(3, 4, 6, 7)$

→ 3-variable k-map

x	y	z	00	01	11	10
0	0	0	1	1	1	1
1	1	1	1	1	0	0

$$Y = \underbrace{x\bar{z}}_{F} + \underbrace{\bar{x}z}_{E} + \underbrace{yz}_{G} \quad F \equiv \text{M}(3, 4) \quad E \equiv \text{M}(6, 7) \quad G \equiv \text{M}(7)$$

Page No.	1	0
Date	0	0

Q) Simplify using boolean algebra rules:

$$\rightarrow \overline{AB} (\overline{A} + B) (\overline{B} + B)$$

$$\rightarrow B + \overline{B} = 1$$

∴ given eqn reduces to

$$\overline{AB} (\overline{A} + B) = (\overline{A} + \overline{B})(\overline{A} + B)$$

$$A \oplus \overline{A} + \overline{AB} \cdot B = \overline{A} + \overline{AB} + \overline{BA} + B\overline{B}$$

$$B\overline{B} = 0 \Rightarrow \overline{A} + \overline{AB} + \overline{A}\overline{B}$$

$$\overline{A} + \overline{A}(B + \overline{B})$$

$$\overline{A} \quad \underline{\text{Ans}}$$

Q) $A \cdot (\overline{B}C + BC)$

→

$$\overline{A} + \overline{(\overline{B}C + BC)}$$

$$\overline{A} + (\overline{A} \oplus C)$$

$$\overline{A} + (B \oplus C)$$

$$\overline{A} + \overline{B}C + B\overline{C}$$

$$\underline{\text{Ans}}$$

$$A \oplus \overline{A} = \overline{AB} + A\overline{B}$$

$$= \overline{AB} + A\overline{B}$$

$$= (\overline{A} + B)(A + \overline{B})$$

Q) $(A+C)(AD + A\overline{D}) + AC + C$

$$\rightarrow (A+C)(A(D + \overline{D})) + \underbrace{AC}_{1} + \underbrace{C}_{1}$$

$$(A+C) \cdot A + C$$

$$A \cdot + A \cdot C + C$$

$$A(C+1) + C$$

$$A+C$$

$$\underline{\text{Ans}}$$

Q) $\overline{A}(A+B) + (B+A\overline{A})(A+\overline{B})$

$$\rightarrow \overline{A}(A+B) + (A+B)(A+\overline{B})$$

$$\overbrace{A \cdot A}^0 + \overbrace{A \cdot B}^1 + \underbrace{A \cdot A + A \cdot \overline{B}}_A + B \cdot A + B \cdot \overline{B}$$

$$\overline{AB} + A + \overline{AB} + AB$$

$$\overline{AB} + \overline{A}\overline{B} + A(\overline{B}+1)$$

$$\overline{AB} + \overline{A}\overline{B} + A$$

$$\overline{AB} + \overline{A}(\overline{B}+1)$$

$$\overline{AB} + A$$

$A+B$... by boolean algebra rule.

Ans

v) $\overline{AB} + A(B+C) + B(B+C)$

$$\rightarrow AB + AB + AC + B + BC$$

$$AB + AC + B$$

$$B + AC$$

Ans

vi) $(A \cdot (\overline{C} + \overline{B}\overline{D}) + \overline{B}\overline{C}), \overline{E}$

$$(A \cdot (\overline{C} \cdot \overline{B}\overline{D}) + \overline{B} + C), \overline{E}$$

$$(A \cdot (\overline{C} \cdot (\overline{B} + \overline{D})) + \overline{B} + C), \overline{E}$$

$$(ABC + A\overline{C}\overline{D} + \overline{B} + C), \overline{E}$$

$$+ (A\overline{C}(\overline{B} + \overline{D}) + \overline{B} + C), \overline{E}$$

Ans

vii) $A + \overline{AB} + \overline{ABC} + \overline{ABCD} + \overline{ABCDE}$

$$\rightarrow A + \overline{A}\overline{B} + \overline{ABC} + \overbrace{\overline{ABC}(D+E)}$$

$$A + \overline{A}(B+C) + \overbrace{\overline{ABC}(D+E)}$$

$$A + \overbrace{\overline{A}(B+C)} + \overbrace{\overline{ABC}(D+E)}$$

$$A + \overline{A} + \overline{B} + C + \overbrace{\overline{ABC}(D+E)}$$

Ans

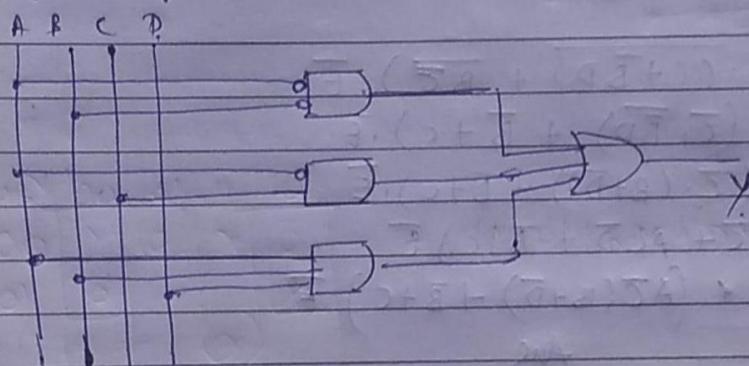
- 4) Reduce the expression $f = \sum m(0, 1, 2, 3, 6, 7, 13, 15)$ to its minimum SOP form. Draw logic diagram & mention the number of basic gates required to implement the clbf

4-variable k-map

AB\CD	00	01	11	10
00	1	1	1	D
01			1	1
11		1	D	
10				

$$Y = \overline{AB} + \overline{AC} + ABD$$

logic diagram



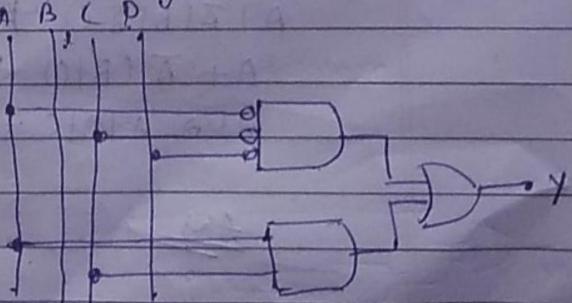
- 5) solve following using k-map. Draw logic diagram

$$\rightarrow f = \sum m(0, 4, 10, 11, 14, 15)$$

AB\CD	00	01	11	10
00	1	1		
01	1			
11				
10				

logic diagram

$$Y = \overline{ACD} + AC$$



$$ii) f = \sum m(10, 11, 14, 15)$$

→ AB CP 00 01 11 10

AB	CP	00	01	11	10
00					
01					
11					
10					

logic diagram



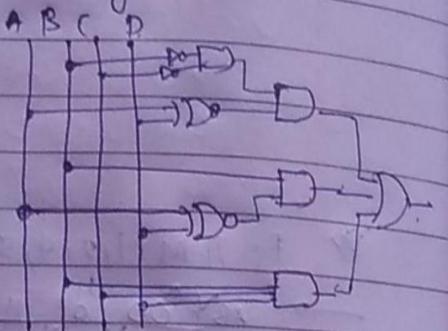
$$y = AC$$

$$iii) f = \sum m(0, 5, 7, 9, 12, 14, 15)$$

→ AB CP 00 01 11 10

AB	CP	00	01	11	10
00		1			
01			1	1	
11		1	1	1	1
10			1	1	1

logic diagram

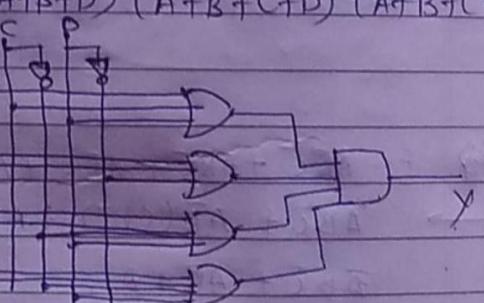


$$\begin{aligned} y &= \overline{ABC}D + A\overline{B}C\overline{D} + ABD' + BCD + ABCD + ACD' + ABD \\ &= \overline{BC}(AD + AD') + B(AD + AD') + BC(D \\ &= \overline{AB} + BD + AC'D + ACD \\ &= \overline{BC}(\overline{A}\overline{C}D) + B(A\overline{C}D) + BCD \end{aligned}$$

$$iv) f = \prod M(4, 6, 10, 12, 13, 15)$$

→ AB CP 00 01 11 10

AB	CP	00	01	11	10
00					
01		0	0	0	0
11		0	0	0	0
10		0	0	0	0

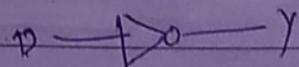


$$v) f = \sum m(4, 8, 12, 10) + d(0, 6, 2, 14)$$

→ AB CP 00 01 11 10

AB	CP	00	01	11	10
00		X			
01		1	1	1	1
11		1	1	1	1
10		1	1	1	1

logic diagram



$$y = \overline{D}$$

vii) $f = \sum m(1, 2, 4, 9, 15) + d(0, 6, 12, 14)$

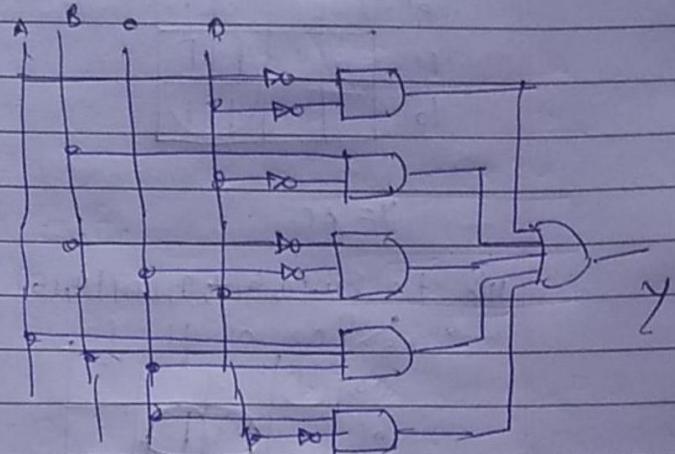
$\rightarrow AB \setminus C \oplus D$ or $11 \setminus 0$

	A	B	C	D	Y
00	X	1	1	1	0
01	1	1	1	0	X
11	X	1	1	X	1
10	0	1	1	1	0

Y = $\overline{AD} + B\overline{D} + \overline{B}\overline{C}D + AB(C + \overline{D})$

logic diagram & eqn.

$$Y = \overline{AD} + B\overline{D} + \overline{B}\overline{C}D + AB(C + \overline{D})$$



viii) $f = \prod m(1, 2, 4, 9, 15) \cdot d(0, 3, 6)$

$\rightarrow AB \setminus C \oplus D$ or $00 \setminus 10$

	A	B	C	D	Y
00	X	0	1	0	0
01	0	1	1	X	0
11	0	1	0	0	1
10	1	0	1	0	0

$$f = (A + D)(B + C + D)(A + B + C + D)$$

viii) $f = \overline{ABC} + \overline{ABC} + \overline{AB}C + ABC + ABC$

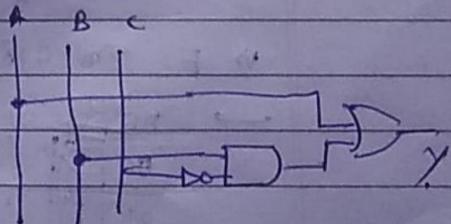
$\rightarrow \overline{ABC} + \overline{AB}(C + \overline{C}) + AB(C + \overline{C})$

$\overline{ABC} + \overline{AB} + AB$

$\overline{ABC} + A$

$A + B\overline{C}$... by boolean algebra law.

logic diagram



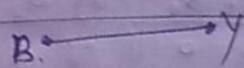
$$\rightarrow f = ABC + \bar{A}B + AB\bar{C}$$

$$\rightarrow f = AB(C+1) + \bar{A}B$$

$$= AB + \bar{A}B$$

$$= B$$

logic diagram



Q. 3 bit binary to gray-code

truth table:

B_3	B_2	B_1	G_3	G_2	G_1
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

$$G_3 \Rightarrow$$

k-map

B_3	B_2	B_1	00	01	11	10
0	0	0	0	0	1	1
1	0	1	0	1	0	0

$$G_2 \Rightarrow$$

k-map

B_3	B_2	B_1	00	01	11	10
0	0	0	0	0	1	1
1	1	0	1	0	0	0

$$G_2 = \bar{B}_2 B_2 + B_2 \bar{B}_2 \\ = B_2 \oplus B_2$$

$$G_1 \Rightarrow$$

k-map

B_3	B_2	B_1	00	01	11	10
0	0	0	0	0	0	0
1	0	1	0	1	0	0

$$G_1 = \bar{B}_2 B_1 + B_2 \bar{B}_1 \\ = B_1 \oplus B_2$$

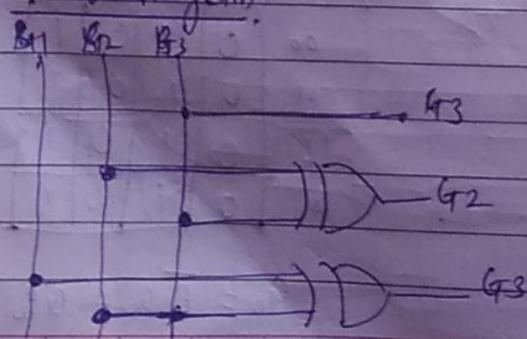
logic eqns.

$$G_3 = B_3$$

$$G_2 = B_2 \oplus B_3$$

$$G_1 = B_1 \oplus B_2$$

circuit diagram



4-bit binary to gray code:

truth table:

B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

deriving eqns using k-map
 $G_3 \Rightarrow$

B_3B_2	B_1B_0
00	00
01	01
11	11
10	10

$$G_3 = B_3$$

$G_2 \Rightarrow$

B_3B_2	B_1B_0
00	00
01	11
11	00
10	10

$$G_2 = \overline{B_2}B_2 + B_3\overline{B_2}$$

$$= B_2 \oplus B_3$$

B_3B_2	B_1B_0
00	00
01	11
11	00
10	10

$$G_1 = B_2\overline{B_1} + \overline{B_2}B_1 \\ = B_1 \oplus B_2$$

B_3B_2	B_1B_0
00	00
01	10
11	01
10	01

$$G_0 = \overline{B_1}B_0 + B_1\overline{B_0} = B_1 \oplus B_0$$

? logic eqns.

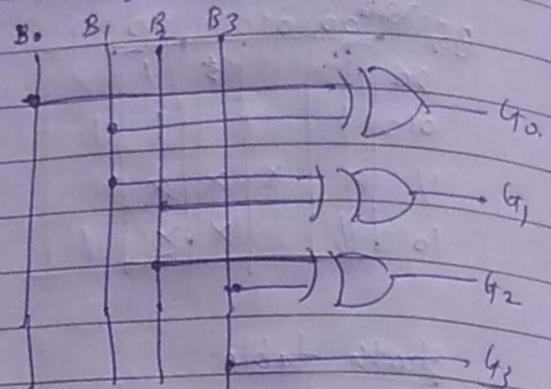
$$G_0 = \overline{B_3} B_0 + B_0 \oplus B_1$$

$$G_1 = B_1 \oplus B_2$$

$$G_2 = B_2 \oplus B_3$$

$$G_3 = B_3$$

logic diagram



→ BCD to excess-3:

$$\text{Karnaugh Map: } E_3(B_3, B_2, B_1, B_0) = \sum m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$$

		B ₃ B ₂	00	01	11	10
		B ₁ B ₀	00	01	11	10
B ₃ B ₂	B ₁ B ₀	00	1	1	1	1
		01	1	X	X	X
B ₃ B ₂	B ₁ B ₀	11	X	X	X	X
		10	1	X	X	X

$$E_3 = B_3 + B_2 B_0 + B_2 B_1$$

$$E_2(B_3, B_2, B_1, B_0) = \sum m(1, 2, 3, 4, 9) + d(10, 11, 12, 13, 14, 15)$$

		B ₃ B ₂	00	01	11	10
		B ₁ B ₀	00	01	11	10
B ₃ B ₂	B ₁ B ₀	00	1	1	1	1
		01	1	X	X	X
B ₃ B ₂	B ₁ B ₀	11	X	X	X	X
		10	1	X	X	X

$$E_2 = B_2 \overline{B_1} \overline{B_0} + \overline{B_2} B_0 + B_2 B_1$$

$$= \overline{B_2} (B_1 + B_0) + B_2 (\overline{B_1} \cdot \overline{B_0})$$

$$= \overline{B_2} (B_1 + B_0) + B_2 (\overline{B_1} + B_0) \dots \text{by}$$

$$= \overline{B_2} \overline{(B_1 + B_0)} \quad \text{De Morgan's}$$

$$= \overline{B_2} \overline{B_1} \overline{B_0} = B_2 \oplus (B_0 + B_1)$$

$$E_1(B_3, B_2, B_1, B_0) = \sum m(0, 3, 4, 7, 8) + d(10, 11, 12, 13, 14, 15)$$

		B ₃ B ₂	00	01	11	10
		B ₁ B ₀	00	01	11	10
B ₃ B ₂	B ₁ B ₀	00	1	1	1	1
		01	1	X	X	X
B ₃ B ₂	B ₁ B ₀	11	X	X	X	X
		10	1	X	X	X

$$E_1 = \overline{B_1} \overline{B_0} + B_1 \overline{B_0}$$

$$= \overline{B_1} \oplus \overline{B_0}$$

$$E_0(B_3, B_2, B_1, B_0) = \Sigma m(0, 2, 4, 6, 8) + d(10, 11, 12, 13, 14, 15)$$

$B_3 B_2$	00	01	11	10
00	1		1	
01	1		1	
11	x	x	x	x
10	1	x	x	

$$E_0 = \overline{B}_3 \overline{B}_2 \oplus B_2$$

$$E_0 = \overline{B}_3$$

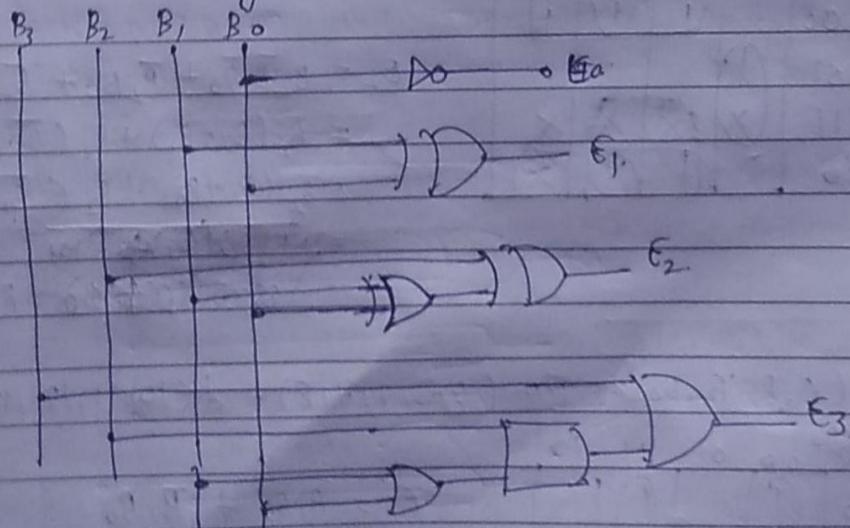
truth table

logic eqns

B_3	B_2	B_1	B_0	E_2	E_1	E_0	$E_0 = \overline{B}_3$
0	0	0	0	0	0	1	1
0	0	1	0	0	1	0	$E_1 = B_2 \oplus B_0$
0	0	1	1	0	1	0	$E_2 = \overline{B}_3 \oplus (B_0 + B_1)$
0	1	0	0	0	1	1	$E_3 = B_3 + B_2(B_1 + B_0)$
0	1	0	1	0	0	0	
0	1	1	0	1	0	1	
0	1	1	1	1	0	0	
0	0	0	0	1	0	1	
1	0	0	1	1	1	0	

+ 0 + 0

circuit diagram.



Excess-3 to BCD:

truth table

$E_3\ E_2\ E_1\ E_0$	$B_3\ B_2\ B_1\ B_0$
0 0 1 1	0 0 0 0
0 1 0 0	0 0 0 1
0 1 0 1	0 0 1 0
0 1 1 0	0 0 1 1
0 1 1 1	0 1 0 0
1 0 0 0	0 1 0 1
1 0 0 1	0 1 1 0
1 0 1 0	0 1 1 1
1 0 1 1	1 0 0 0
1 1 0 0	1 0 0 1

dealing logic expr using k-map:

$B_3 \Rightarrow$

$E_3\ E_2 \backslash E_1\ E_0$	00	01	11	10
00	✗	✗	✗	✗
01
11	1	✗	✗	✗
10	.	.	1	.

$$B_3 = E_3 E_2 + E_1 E_0$$

$B_2 \Rightarrow$

$E_3\ E_2 \backslash E_1\ E_0$	00	01	11	10
00	(x) x	.	(x)	.
01	.	1	.	.
11	x	x	x	.
10	1	1	1	1

$$B_2 = \overline{E_1} \overline{E_2} + E_2 E_1 E_0 + \overline{E_1} \overline{E_0}$$

$B_1 \Rightarrow$
 $E_3\ E_2 \backslash E_1\ E_0$

$B_1 \Rightarrow$

$E_3 E_2 \backslash E_1 E_0$	00	01	11	10
00	X	X	X	X
01	X		1	
11	X	X	X	
10		1		

$$B_1 = \overline{E_1} E_0 + E_1 \overline{E_0}$$

$$= E_1 \oplus E_0.$$

$B_2 \Rightarrow$

$E_3 E_2 \backslash E_1 E_0$	00	01	11	10
00	X	X	X	X
01	1		1	
11	1	X	X	X
10	1			1

$$B_2 = \overline{E_0}$$

\therefore logic equations:

$$B_0 = F_0$$

$$B_1 = E_1 \oplus E_2$$

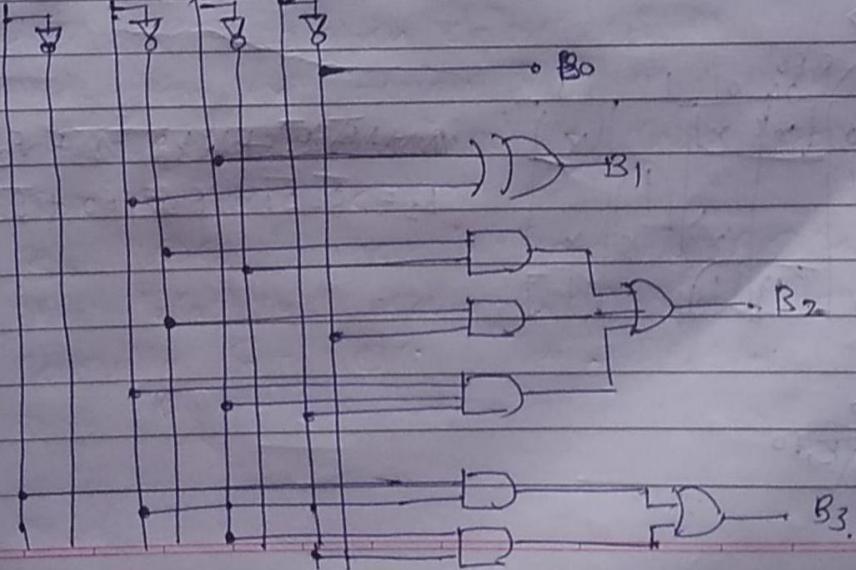
$$B_2 = \overline{E_2} \overline{E_1} + \overline{E_2} E_0 + E_2 E_1 E_0$$

$$B_3 = E_3 E_2 + E_1 E_0.$$

$B_F \Rightarrow$

logic diagram

$E_3 \quad E_2 \quad E_1 \quad S_0.$



⇒ 3-bit even parity generator

truth table:

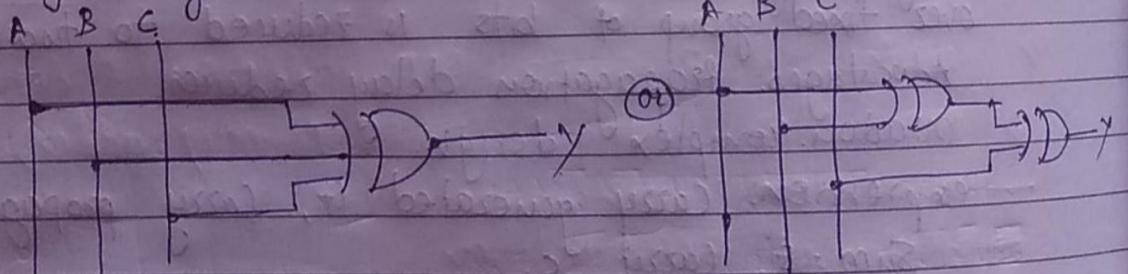
3-bit message			even parity bit generator
A	B	C	y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Deriving logic eqns using k-map.

A	BC	00	01	11	10
0	.	1	1	1	1
1	1	1	1	1	1

$$\begin{aligned}
 y &= \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC \\
 &= \overline{A}(\overline{B}C + B\overline{C}) + A(\overline{B}\overline{C} + BC) \\
 &= \overline{A}(B \oplus C) + A(\overline{B} \oplus C) \\
 &= A \oplus B \oplus C
 \end{aligned}$$

Logic diagram:



3-bit odd parity generator:

truth table

3-bit message			odd parity generator
A	B	C	y
0	0	0	1

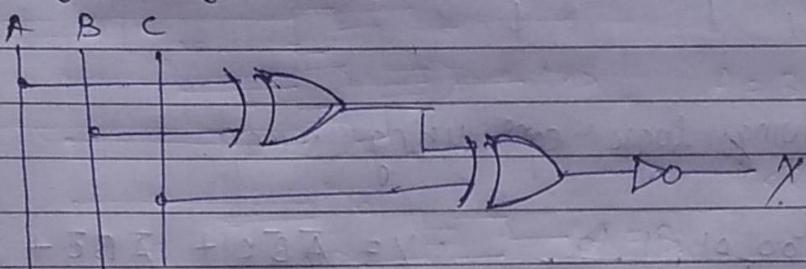
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Deriving egn using k-map

A	BC	00 01 11 10
0	1	1 1 1 1
1	1	1 1 1 1

$$\begin{aligned}
 Y &= ABC + \overline{ABC} + A\overline{B}C + A\overline{B}\overline{C} \\
 &= \overline{A}(B\overline{C} + BC) + A(\overline{B}C + \overline{B}\overline{C}) \\
 &= \overline{A}(B \oplus C) + A(B \oplus C) \\
 &= A \oplus B \oplus C
 \end{aligned}$$

Logic diagram:



→ Explain Look Ahead carry generator in detail.

→ This is the block that reduces propagation delay. The ripple carry design is suitable transformed such that Carry logic over fixed group of bits is reduced to two-level logic.

Advantages: Propagation delay reduces.

Disadvantages: complex design.

expression: carry generated = G_i , carry propagated = P_i .

Sum = S_i , carry = C_i .

$$S_i = P_i \oplus C_{i-1} \quad \text{where } G_i = C_{i-1}, P_i = A_{i-1} \oplus B_{i-1}$$

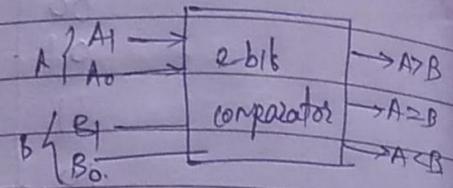
$$C_i = P_i C_{i-1} + G_{i-1} \quad \text{where } G_{i-1} = A_{i-1} \cdot B_{i-1}$$

$$\text{Generally } S_i = P_i \oplus C_{i-1}, C_i = P_i G_{i-1} + G_i$$

10

\rightarrow Two bit comparators:

input		output				
A ₁	A ₀	B ₁	B ₀	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0



Solving eqns using k-map:

$A \geq B$	$A > B$	$A = B$	$A < B$	$A \leq B$
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	1	1	0	0

$$A = B \rightarrow A \overset{S.P.}{\sim} B. 0. 01. 1110.$$

00	1	.	1	
01	.	1	.	
11	.	.	1	.
10	.	.	1	1

$$Y = A_1 \overline{B_1} + A_0 \overline{B_1} \overline{B_0} + A_1 A_0 \overline{B_0}$$

$$\begin{aligned}
 Y &= \overline{A_1} \overline{A_0} \overline{B_1} B_0 + \overline{A_1} A_0 \overline{B_1} B_0 \\
 &\quad + A_1 A_0 B_1 B_0 + A_1 \overline{A_0} \overline{B_1} B_0 \\
 &= \overline{A_1} \overline{B_1} (A_0 \overline{B_0} + A_0 B_0) + \\
 &\quad A_1 B_1 (A_0 B_0 + \overline{A_0} \overline{B_0})
 \end{aligned}$$

$$= \overline{A_1} \overline{B_0} (\overline{A_0} \oplus \overline{B_0}) + A_1 B_1 (\overline{A_0} \oplus \overline{B_0})$$

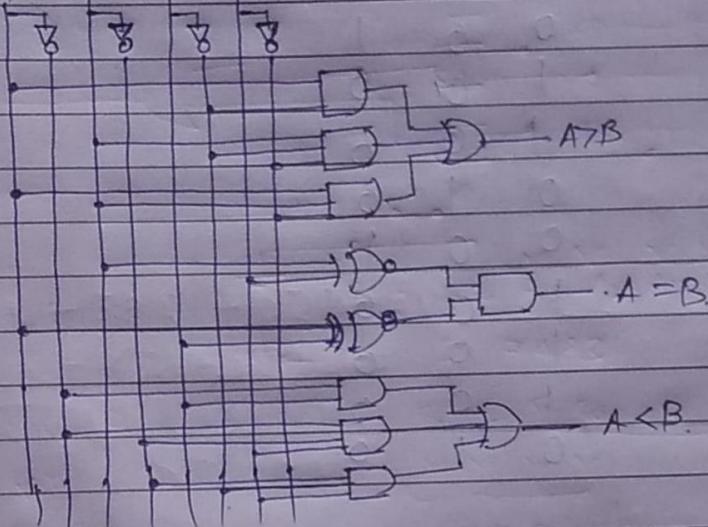
$$= \overline{A_1} \overline{B_0} (\overline{A_0} \oplus \overline{B_0}) (\overline{A_1} \oplus \overline{B_1})$$

$A < B \Rightarrow$	$A_1 A_0 \quad B_1 B_0$	00	01	11	10
		1	0	1	1
		0	1	1	0
		1	1	0	0
		1	0	0	1

$$y = \overline{A_1} B_1 + \overline{A_1} \overline{A_0} B_0 + \overline{A_0} B_1 B_0.$$

logic diagram:

$A_1 \quad A_0 \quad B_1 \quad B_0$



logic eqns.

$$A > B \Rightarrow A_1 \overline{B}_1 + A_0 \overline{B}_1 \overline{B}_0 + A_1 A_0 \overline{B}_0$$

$$A = B \Rightarrow (\overline{A_0} \oplus \overline{B_0}) (\overline{A_1} \oplus \overline{B_1})$$

$$A < B \Rightarrow \overline{A_1} B_1 + \overline{A_1} \overline{A_0} B_0 + \overline{A_0} B_1 B_0.$$

1) write the rule for BCD addition & design 4-bit BCD adder using IC 7483 (binary adder)

Rules of BCD addition.

1) Add only individual 4-bit groups.

2) while adding 4-bit groups add ~~like~~ just like binary addition.

3) If ans is in the range [10, 15] add 6 i.e. 0110 to the ans.

4) If carry is generated, add it to next group.

e.g. consider addition of 8765 & 3343

$$\begin{array}{r}
 \text{8765} \xrightarrow{\text{BCD form}} \begin{array}{r} 1001 \\ 0111 \\ 0110 \\ 0101 \end{array} \\
 \text{3343} \xrightarrow{\text{BCD form}} \begin{array}{r} 0011 \\ 1001 \\ 0100 \\ 0011 \end{array} \\
 \hline
 \begin{array}{r} 1000 \\ 0000 \\ 1010 \\ 1000 \end{array} \\
 \begin{array}{r} 0110 \\ 0110 \\ 0110 \\ 0000 \end{array}
 \end{array}$$

: Ans will be 12708

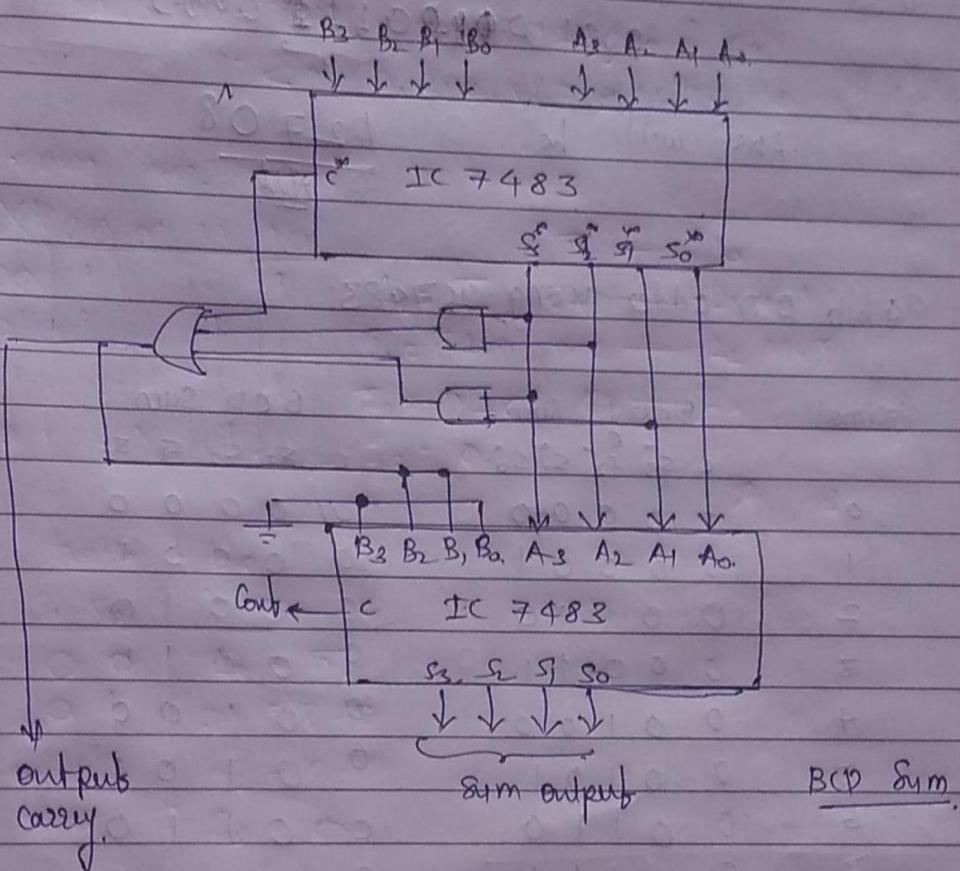
4-bit BCD adder using IC 7483:

Decimal	Binary Sum	BCD Sum
	$c s_3 s_2 s_1 s_0$	$c s_3 s_2 s_1 s_0$
0	0 0 0 0 0	0 0 0 0 0
1	0 0 0 0 1	0 0 0 0 1
2	0 0 0 1 0	0 0 0 1 0
3	0 0 0 1 1	0 0 0 1 1
4	0 0 1 0 0	0 0 1 0 0
5	0 0 1 0 1	0 0 1 0 1
6	0 0 1 1 0	0 0 1 1 0
7	0 0 1 1 1	0 0 1 1 1
8	0 1 0 0 0	0 1 0 0 0
9	0 1 0 0 1	0 1 0 0 1
10	0 1 0 1 0	1 0 0 0 0
11	0 1 0 1 1	1 0 0 0 1
12	0 1 1 0 0	1 0 0 1 0
13	0 1 1 0 1	1 0 0 1 1
14	0 1 1 1 0	1 0 1 0 0
15	0 1 1 1 1	1 0 1 0 1
16	1 0 0 0 0	1 0 1 1 0
17	1 0 0 0 1	1 0 1 1 1
18	1 0 0 1 0	1 1 0 0 0

from truth table:

$$\begin{aligned}
 Y &= C^* + S_3^* \cdot (S_2^* + S_1^*) + S_2^* S_1^* \\
 &= C^* + S_3^* \cdot S_2^* + S_3^* S_1^* + S_2^* S_1^* \\
 &= C^* + S_3^* S_2^* + S_2^* S_1^*
 \end{aligned}$$

ckt diagram



12) Realize the following functions using appropriate MUX.

$$F(A, B, C, D) = \sum m(0, 1, 2, 8, 10, 12, 15)$$



K-map

		00	01	11	10
		00	01	11	10
		CD	AB	AB	AB
		00	01	11	10
00	00	1	1	1	1
01	01	1	1	1	1
11	11	1	1	1	1
10	10	1	1	1	1

$$F_1 = \bar{C} + \bar{D}$$

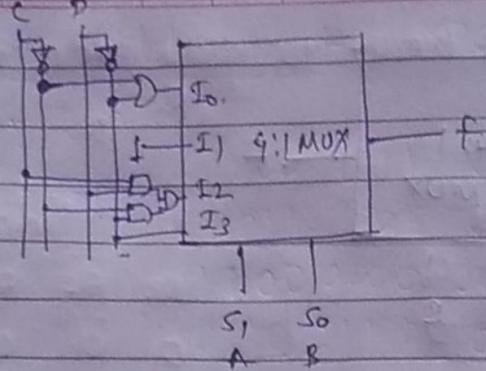
$$F_2 = 1$$

$$F_3 = \bar{C}\bar{D} + CD$$

$$F_4 = \bar{D}$$

truth table:

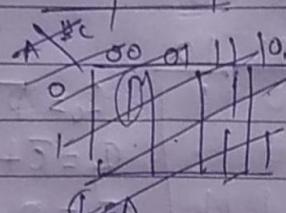
S	S0	Y
00	00	$F_0 = C + D$
01	01	$F_1 = 1$
11	11	$F_2 = \bar{C}\bar{D} + CD$
10	10	$F_3 = \bar{D}$



$$\text{I} \gg f(A_1B_1C) = \Sigma m(0, 3, 6, 7)$$

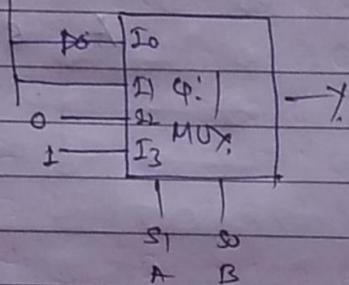
A	B	γ
0	0	\bar{C}
0	1	C
1	0	0
1	1	1

k-map rep:



C	A'B	AB
0	1	1
1	1	1

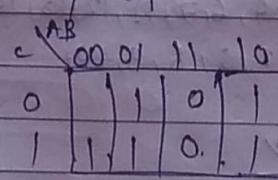
$$I_0 = \bar{C} \quad I_1 = C \quad I_2 = I_3 = 0$$



$$\text{II} \gg f(A_1B_1C) = \Sigma m(4, 2, 3, 4, 5)$$

A	B	γ
0	0	C
0	1	1
1	1	1
1	0	0

k-map rep:



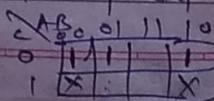
C	I ₀
0	1
1	0

$$I_0 = C \quad I_1 = 1 \quad I_2 = 0 \quad I_3 = 1$$

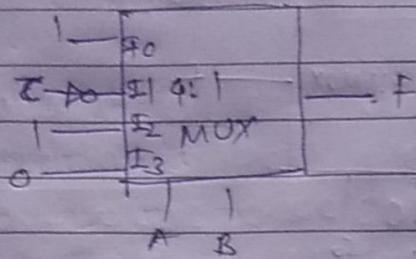
$$\text{III} \gg f(A_1B_1C) = \Sigma m(0, 2, 4) + d(1, 5)$$

A	B	γ
0	0	0
0	1	0
1	0	0
1	1	1

k-map rep:



$$I_0 = 1 \quad I_1 = \bar{C} \quad I_2 = 1 \quad I_3 = 0 \quad I_4 = 0$$



$$\nabla f(A, B, C, D) = \bar{D}M(1, 3, 6, 8, 10, 12) + d(9)$$

$$= \sum m(0, 2, 4, 5, 7, 11, 13, 14, 15) + d(9)$$

K-map seq.

$\bar{A}\bar{B}$	\bar{P}	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	I_{13}	I_{14}	I_{15}
00	1																
01	1	1	1	1	1												
11		1	1	1	1												
10	X	1	1														

$I_0 = \bar{P}$
 $I_1 = \bar{C} + D$
 $I_2 = \bar{C} + D$
 $I_3 = \bar{D}$
 $I_4 = \bar{C} + D$
 $I_5 = \bar{C} + D$
 $I_6 = \bar{D}$
 $I_7 = \bar{D}$

truth table

$\bar{A}\bar{B}$	\bar{Y}
00	$I_0 = \bar{P}$
01	$I_1 = \bar{C} + D$
11	$I_2 = \bar{C} + D$
10	$I_3 = \bar{D}$

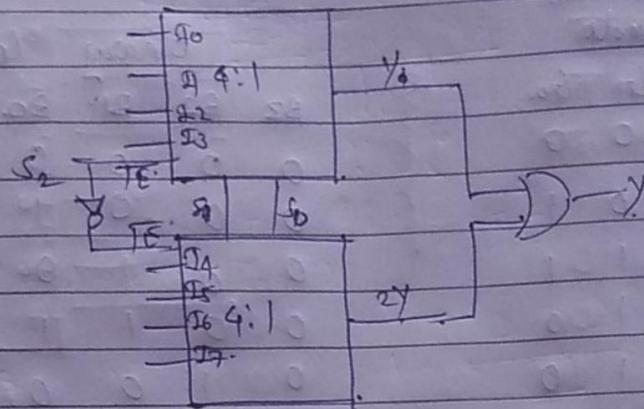
$$\nabla f = \bar{D}M(3, 4, 6, 7, 11, 12, 13, 14, 15)$$

$$= \sum m(1, 2, 4, 5, 8, 9, 10)$$

A	B	C	\bar{Y}	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	\bar{I}_8	\bar{I}_9	\bar{I}_{10}	\bar{I}_{11}	\bar{I}_{12}	\bar{I}_{13}	\bar{I}_{14}	\bar{I}_{15}
0	0	0	1															
0	0	1	1															
0	1	0	1															
0	1	1	0															
1	0	0	0															
1	0	1	0															
1	1	0	0															

$\bar{D} \rightarrow \bar{I}_4$
 $\bar{C} \rightarrow \bar{I}_3$
 $\bar{B} \rightarrow \bar{I}_2$
 $\bar{A} \rightarrow \bar{I}_1$

13) Design 8:1 MUX using two 4:1 MUX.



14) Design 4:1 MUX using three 2:1 MUX.

4:1 MUX:

S_1	S_0	Y
0	0	I ₀
0	1	I ₁
1	0	I ₂
1	1	I ₃

2:1 MUX

S_0	Y
0	I ₀
1	I ₁

consider

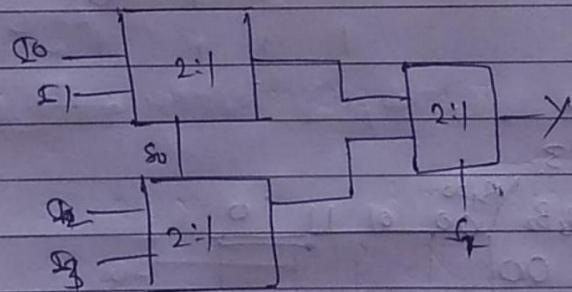
$$S=0, S_0=0.$$

first two MUX produce

I₀, I₂ as output.

S₁ being 0, if select

I₀ as output



for $S=0$ & $S_0=1$

first two muxes produce I₂ as output.

S_1, S_0 being 0, if produces I₁ as output.

(3) Design 3-bit binary to gray code converter using MUX.

→ Truth Table:

Grade Code	Binary Code
G ₃ G ₂ G ₁ G ₀	B ₃ B ₂ B ₁ B ₀
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 1	0 0 1 0
0 0 1 0	0 0 1 1
0 1 1 0	0 1 0 0
0 1 1 1	0 1 0 1
0 1 0 1	0 1 1 0
0 1 0 0	0 1 1 1
1 1 0 0	1 0 0 0
1 1 0 1	1 0 0 1
1 1 1 1	1 0 1 0
1 1 1 0	1 0 1 1
1 0 1 0	1 1 0 0
1 0 1 1	1 1 0 1
1 0 0 1	1 1 1 0
1 0 0 0	1 1 1 1

B ₃ → G ₃	G ₃ → B ₃
B ₂ → G ₂	G ₂ → B ₂
B ₁ → G ₁	G ₁ → B ₁
00	1 1 1 1
01	1 1 1 1
11	1 1 1 1
10	1 1 1 1

$$G_2 = \overline{B_3}B_2 + \overline{B_2}B_3 \\ = B_2 \oplus B_3$$

G ₁ ⇒	B ₃ B ₂ B ₁ B ₀	G ₁ ⇒	B ₃ B ₂ B ₁ B ₀
00	0 0 1 1	00	0 0 1 1
01	1 1 1 1	01	0 0 1 1
11	1 1 1 1	11	1 1 0 0
10	0 0 1 1	10	1 1 0 0

$$G_1 = B_2 \overline{B_1} + B_1 \overline{B_2} \\ = B_1 \oplus B_2$$

	$B_3 B_2$	$B_3 B_1$	$B_3 B_0$	$B_2 B_1$	$B_2 B_0$	$B_1 B_0$	B_3	G_0
00	0	(1)	0	(1)	0	0	0	0
01	0	0	1	a	1	1	1	1
11	0	1	0	1	0	1	1	1
10	0	1	0	0	1	0	0	0

$$\begin{aligned} G_0 &= \overline{B}_3 B_0 + B_1 \overline{B}_0 \\ &= B_0 \oplus B_1 \end{aligned}$$

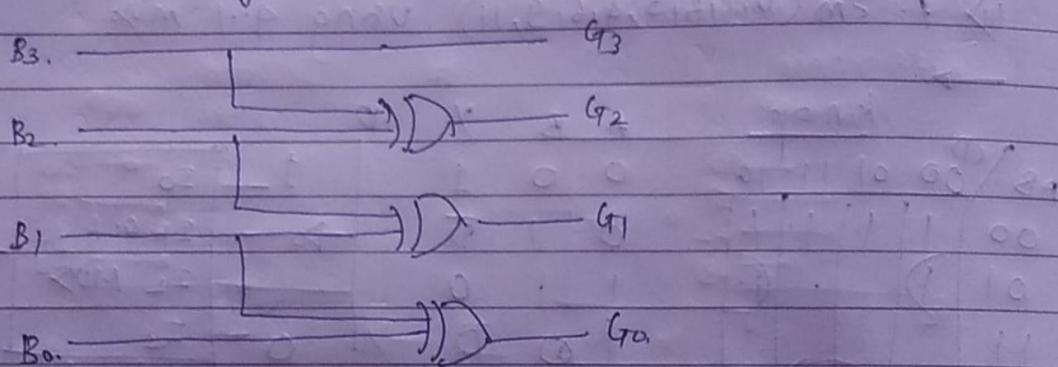
e.g NS:- $G_3 = B_3$

$$G_2 = B_3 \oplus B_2$$

$$G_1 = B_2 \oplus B_1$$

$$G_0 = B_1 \oplus B_0$$

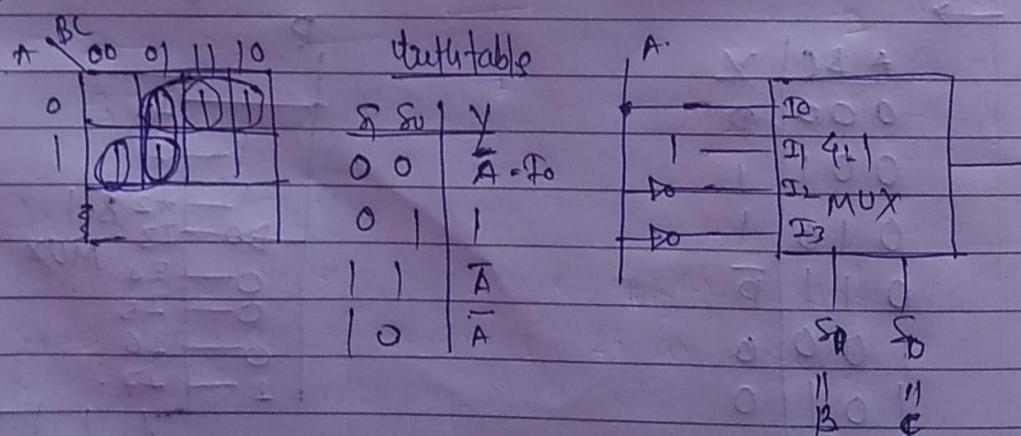
circuit diagram:



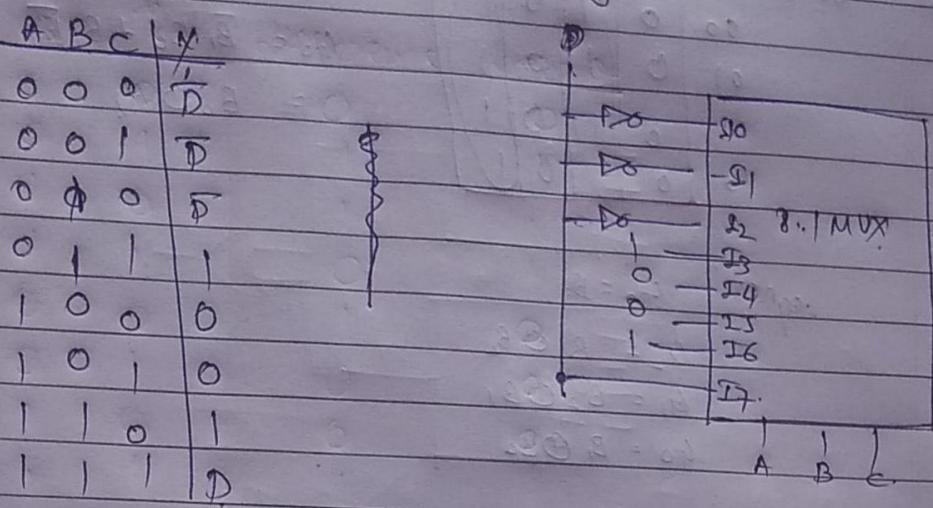
Q6) Implement the following variable reduction

$f = \Sigma m(1, 2, 3, 4, 5)$ Using 4:1 MUX

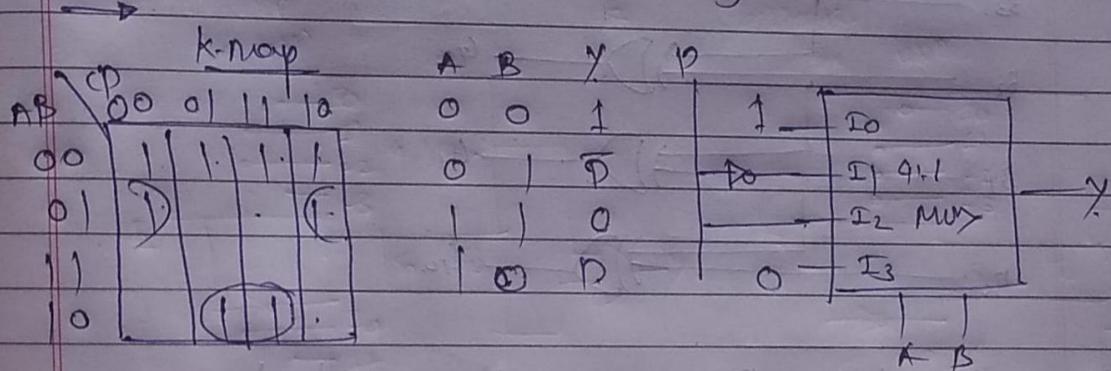
→



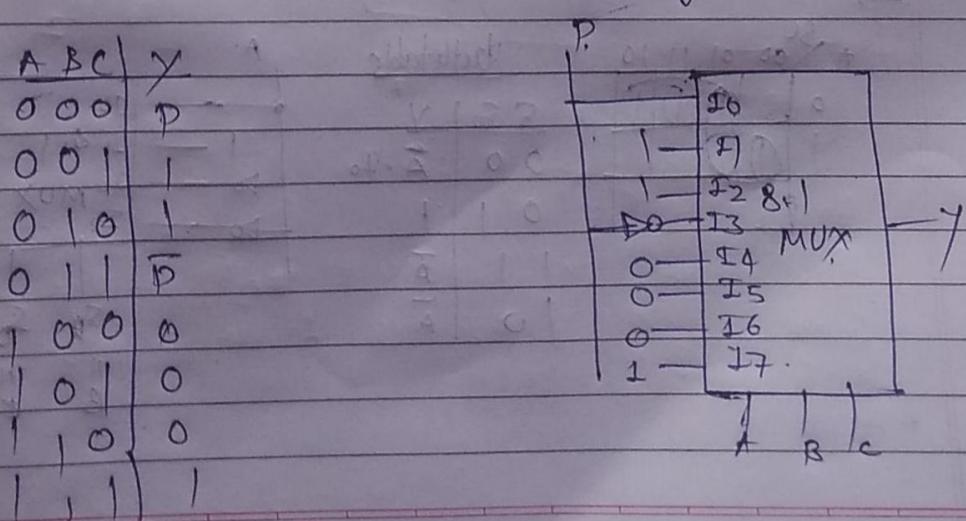
ii) $f = \sum m(0, 2, 4, 6, 7, 12, 13, 15)$ using 8:1 MUX.



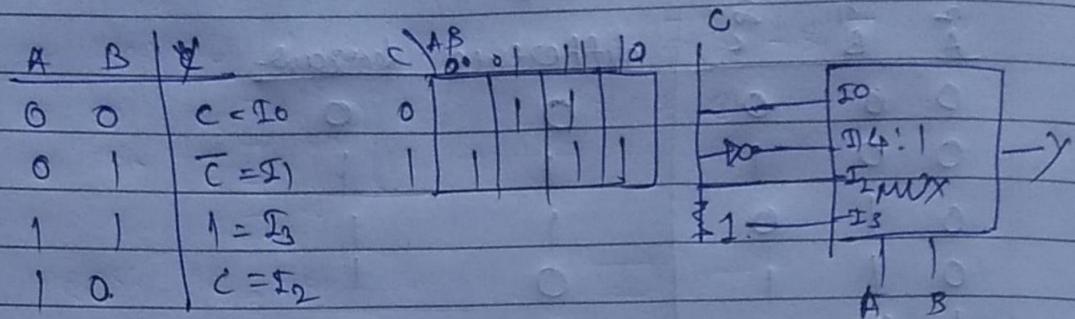
iii) $f = \sum m(0, 1, 2, 3, 4, 6, 9, 11)$ using 4:1 MUX.



iv) $f = \sum m(1, 2, 3, 4, 5, 6, 7, 14, 15)$ using 8:1 MUX.



$\Rightarrow f = \sum m(1, 3, 4, 6, 7)$ Using 4:1 MUX.



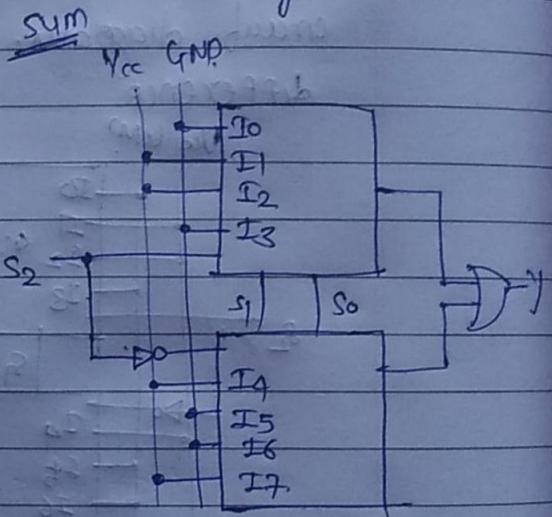
Design full adder & full subtractor using MUX.



Full Adder:

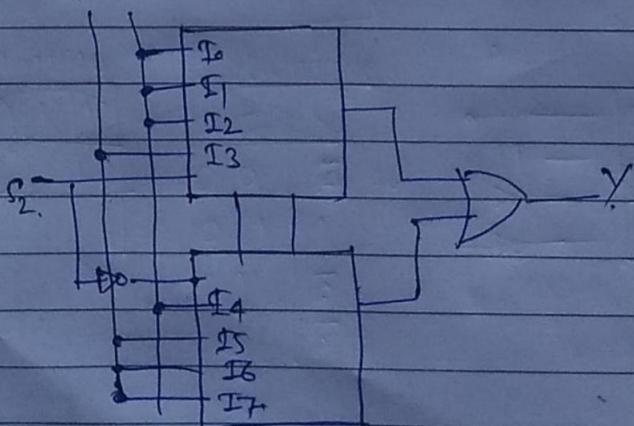
A	B	S_0	C	sum	carry
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	1	1	1

circuits diagram



Carry

Vcc GND



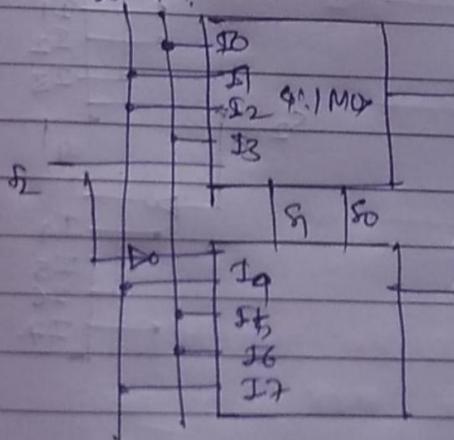
full subtractor using 8:1 mux

A	B	S_0	difference borrow	
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

circuit diagram

difference

Vcc GND



borrow

Vcc GND

