

## Title: Binary adder & subtractor circuits

### Objectives

- 1) design & implement full adder circuit using basic gates & universal logic gates.
- 2) Design & implement full subtractor circuit using basic gates & universal logic gates.

### Apparatus

Digital board, GP-4-batch chord, IC74LS86, IC74LS32, IC74LS08/ IC74LS04 & IC74LS00 & required logic gates.

### Theory

- 1) Binary adder & subtractor are a combinational logic circuits which is used to perform binary addition & subtraction.
- 2) Full adder has three inputs & two outputs. The first two inputs are A & B & third input is an input carry designed as  $C_{in}$ . When full adder logic is designed we will be able to string eight of them together to create a byte-wide adder & cascade the carry bit from one adder to the next.
- 3) The full subtractor is a combinational circuit with three inputs A, B, C & two outputs D &  $\bar{C}$ . A is the 'minuend', B is 'subtrahend', C is the 'borrow' produced by the previous stage, D is the difference output &  $\bar{C}$  is the borrow output.

### Pin Diagram

1A	—		—	VCC
1B	—	Pin diagram	—	4B
1Y	—	for	—	4A
2A	—	IC74LS00/	—	4Y
2B	—	08/32/86	—	3B
2Y	—		—	3A
GND	—		—	3Y



## procedure

- 1) Make the connections as per the logic circuit of full adder circuit & verify its truth table.
- 2) Make the connections as per the logic of full subtractor ckt & verify its truth table

## Design of full Adder:

Dec. Eq <sup>n</sup>	Input			Output	
	A	B	C <sub>in</sub>	Sum	Carry
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

## k-map simplification:

A	BC <sub>in</sub>			
	00	01	11	10
0		1		1
1	1		1	

$$S = \Sigma(1, 2, 4, 7)$$

$$S = AB\bar{C}_{in} + A\bar{B}C_{in} + ABC_{in} + \bar{A}\bar{B}\bar{C}_{in}$$

$$= C_{in}(AB + \bar{A}\bar{B}) + \bar{C}_{in}(A\bar{B} + \bar{A}B)$$

$$= C_{in}(A \oplus B) + \bar{C}_{in}(A \oplus B)$$

$$S = (A \oplus B) \oplus C_{in}$$

A	BC <sub>in</sub>			
	00	01	11	10
0			1	1
1		1	1	1

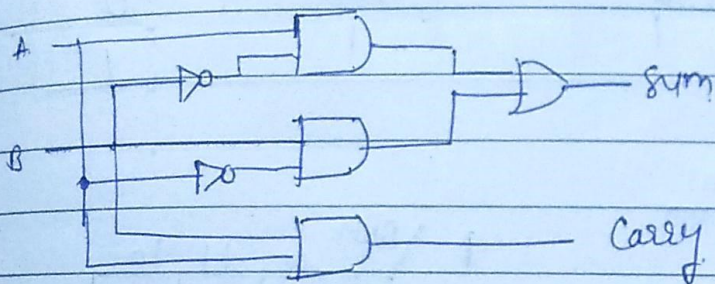
$$Carry = (A, B, C_{in}) = \Sigma(3, 5, 6, 7)$$

$$Carry = BC_{in} + AC_{in} + AB$$

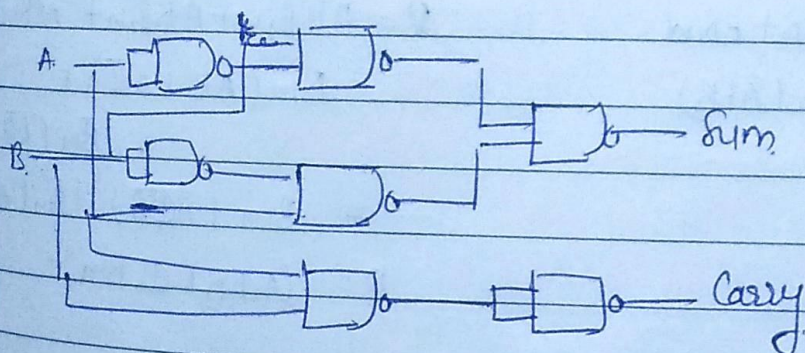
$$= C_{in}(A + B) + AB$$



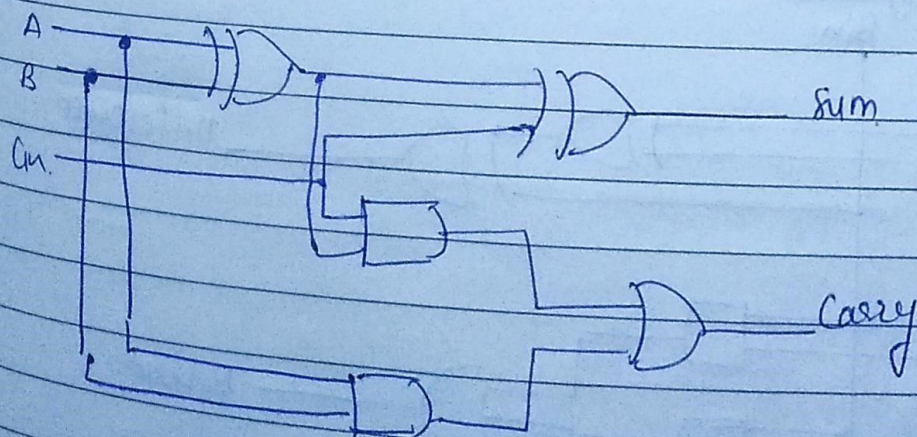
## HA using basic gates



## HA using NAND gate:



## Full adder:





## Design of full subtractor

Dec eqn	input			Output	
	A	B	B <sub>in</sub>	difference	Borrow
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

### k-map simplification:

A \ B B<sub>in</sub>

	00	01	11	10
0		1	1	1
1			1	

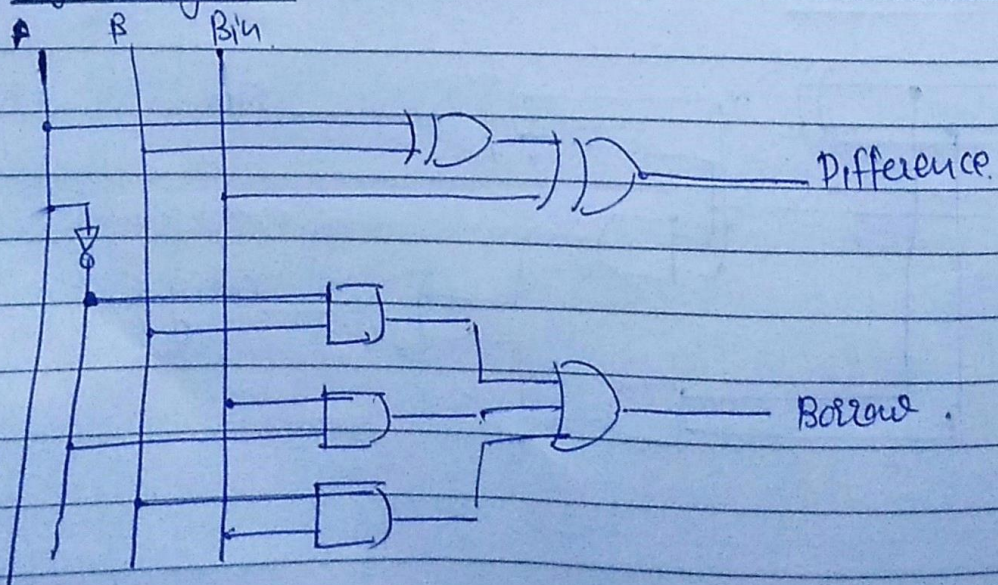
$$\begin{aligned} B_{out} &= \bar{A}B_{in} + \bar{A}B + AB_{in} \\ &= \bar{A}B + B_{in}(A+B) \end{aligned}$$

A \ B B<sub>in</sub>

	00	01	11	10
0		1	1	1
1	1		1	

$$\begin{aligned} D &= A\bar{B}\bar{B}_{in} + \bar{A}B\bar{B}_{in} + AB_{in} + \bar{A}B\bar{B}_{in} \\ &= B_{in}(AB + \bar{A}\bar{B}) + \bar{B}_{in}(A\bar{B} + \bar{A}B) \\ &= B_{in}(A \oplus B) + \bar{B}_{in}(A \oplus B) \\ D &= (A \oplus B) \oplus B_{in} \end{aligned}$$

### logic diagram





logic gates / MSI device required for implementation

S.No	Title	Name of IC	No. of gates req.	IC req.
01	full adder circuit using basic logic gates	HEX Inverter 7404	4	1
		Quad. 2-i/p AND 7408	6	2
		Quad. 2-i/p OR - 7432	3	1
	full adder circuit using universal logic gates	<del>HEX Inverter 7404</del>	1	3
		Quad. 2-i/p AND 7408	9	3
		Quad. 2-i/p NOR 7402	9	
02	full subtractor circuit using basic logic gates	HEX inverter 7404	4	1
		Quad. 2-i/p AND 7408	4	1
		Quad. 2-i/p OR - 7432	3	1

Conclusion:

Successfully designed & implemented full adder using basic gates & universal gates.

Successfully designed & implemented full Subtractor using basic gates & universal gates.