Experiment No. 11 21/18

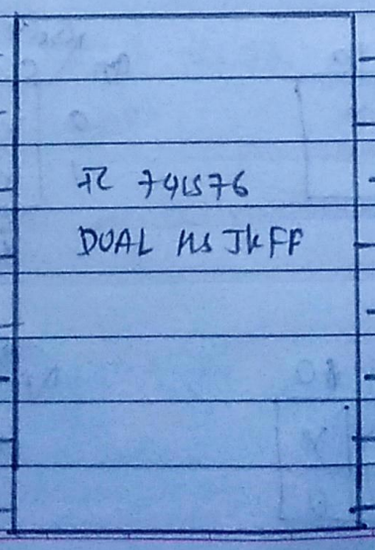
Title: Sequence Generator Circuit

Objective: Design & implement the following sequence generator circuit using IC-74LS76 & verify it's truth table.
Sequence: (1, 3, 5, 6, 7, 1)

Apparatus: Digital Board, GP-4, Patch Chords, IC74LS76, IC74LS32, IC74LS04/IC74LS08 & required logic gates.

Theory
1) Sequence generator is a sequential logic ckt which can be used to generate pre-determined sequence.
2) There are two categories - Sequential & non-sequential sequence generators.
3) Ring counter can be constructed using IC-74LS76. In case of ring counter output of last FF is connected to J_A of first flip-flop & complementry o/p of last ff is connected to K_A i/p of first flip-flop
4) Output of first flipflop (Q_A & $\bar{Q}_A$) is connected to the inputs of second flip-flop (J_B & K_B) & so on. And connect set & reset pin to Vcc.

Pin diagram



Procedure

1) make the connections as per the logic circuit of sequence generator circuit using IC-74LS76 & verify its Truth table.

Design of sequence Generator circuits with lockout condition:

Sl. No.	Present state			Next State			Input					
	Q_A	Q_B	Q_C	Q_A^+	Q_B^+	Q_C^+	J_A	K_A	J_B	K_B	J_C	K_C
1	0	0	1	0	1	1	0	X	1	X	X	0
3	0	1	1	1	0	1	1	X	X	1	X	0
5	1	0	1	1	1	0	X	0	1	X	X	1
6	1	1	0	1	1	1	X	0	X	0	1	X
7	1	1	1	0	0	1	X	1	X	1	X	0
0	0	0	0	X	X	X	X	X	X	X	X	X
2	0	1	0	X	X	X	X	X	X	X	X	X
4	1	0	0	X	X	X	X	X	X	X	X	X

K-map simplifications:

J_A

Q_A \ J_A	00	01	11	10
0	X	0	1	X
1	X	X	X	X

$J_A = Q_B$

J_B

Q_A \ J_B	00	01	11	10
0	X	1	X	X
1	X	1	X	X

$J_B = 1$

J_C

Q_A \ J_C	00	01	11	10
0	1	X	X	X
1	X	1	X	1

$J_C = 1$

K_A

Q_A \ Q_BQ_C	00	01	11	10
0	X	X	X	X
1	X	0	1	0

$K_A = Q_BQ_C$

K_B

Q_A \ Q_BQ_C	00	01	11	10
0	X	X	1	X
1	X	X	1	0

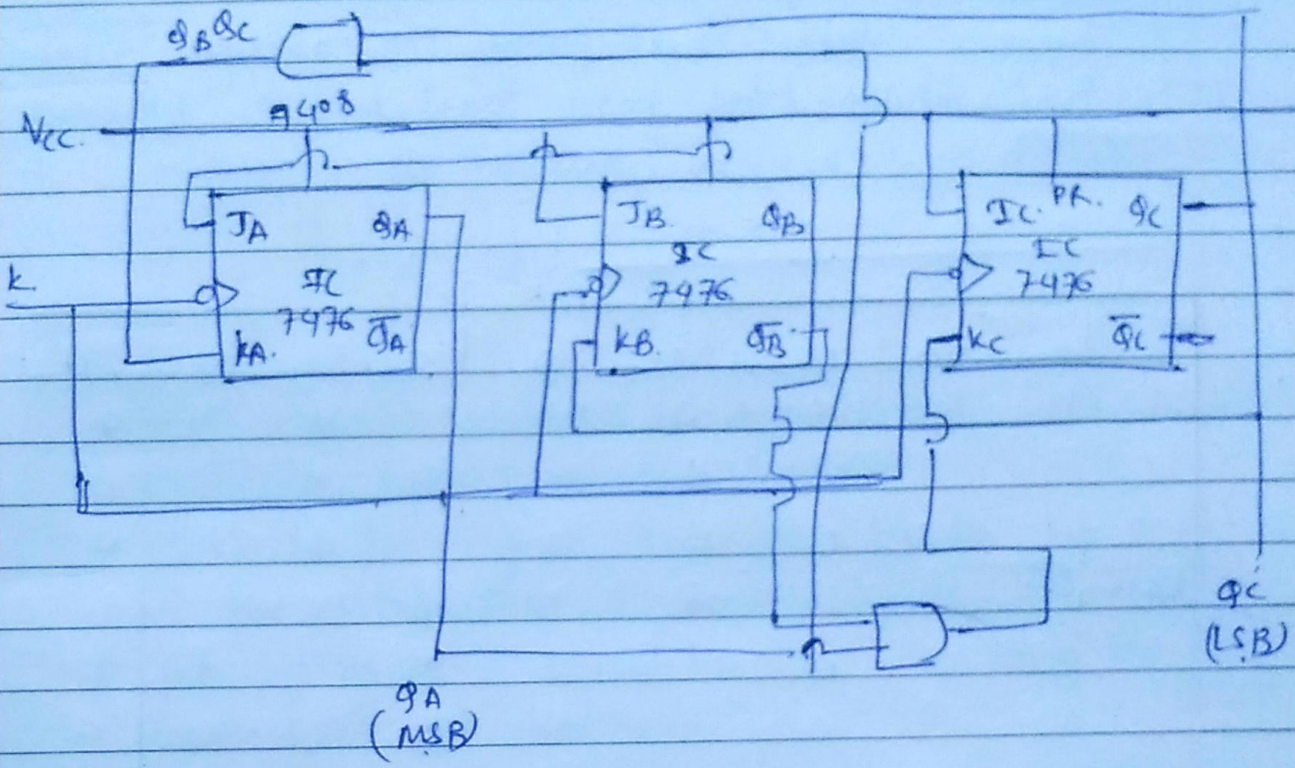
$K_B = Q_C$

K_C

Q_A \ Q_BQ_C	00	01	11	10
0	X	0	0	1
1	X	1	0	X

$K_C = Q_A\overline{Q_B}$

logic diagram



input expression in the ckt: $J_A = Q_A$

$J_B = Q_B Q_C$

$J_B = 1$

$K_B = Q_C$

$J_C = 1$

$K_C = Q_A \overline{Q}_B$

logic gates / MSI device required for implementation.

SR NO	Title	Name of IC	No. of gates req.	IC req.
0	Sequence generator with lockout condⁿ	Dual MS JK FF	3	IC7476-2
		NOT	1	IC7404
		AND	2	IC7408

Conclusion

Concept of sequence generator is studied & implemented.