Experiment No. 10 | 21118 | DATE

Title: Realization of mod-N counter using (decade counter IC 7490)

Objective: Design & implement MOD-N counter circuit using IC 74LS90. Draw timing diagram.

Apparatus: Digital board, GP-4-patch chords, IC-74LS90, IC-74LS191, IC-74LS32, IC74LS04 / IC-74LS08 & required logic gates, if any.

Theory:

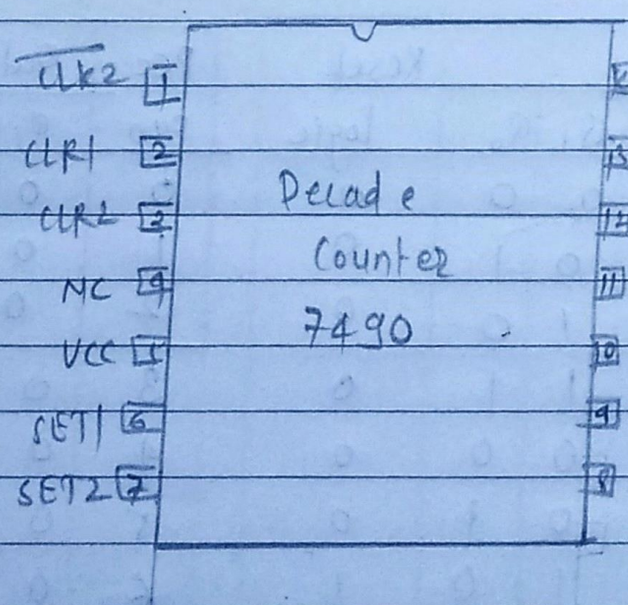
1) Counter is a sequential logic device which counts number of pulses given to the circuit.
2) Counter is classified into two categories Synchronous & Asynchronous.
3) In Asynchronous counter output of first ff ~~is connected to~~ goes to the clock of next & so on, and input of all flip flop is connected to Vcc for IC-74LS76.
4) IC 7490 is called 4-bit MS-JK ff decade (BCD) ~~counter~~ ripple counter. It contains 4 MS ff internally connected to provide MOD-2 i.e. divide by 2 & MOD-5 i.e. divide by 5 counter. MOD-2 & MOD-5 counters can be used independently @ in cascading. Each counter has a separate clock input to initiate state changes of the counter on the high to low clock transition.

Since the o/p from the divide by 2 section is not internally connected to the succeeding stages, the device may be operated in various counting modes. It is also provided with additional gating to provide a divide by 2 counter & binary counter for which the count cycle length is divided by 5.

The device may be operated in various counting modes

There are two reset inputs $R_0(1)$ & $R_0(2)$ both of which need to be connected to the 'logic 1' for clearing all flip-flops.
Two set inputs $R_9(1)$ & $R_9(2)$ when connected to logic are used for setting counter to 1001 (BCD 9).
IC 74191 is a 4-bit binary parallel presettable programmable UP/DOWN synchronous counter. It contains 4 MS JK FF with internal gating & steering logic to provide asynchronous reset & synchronous count up/down operations.
D_0 to D_3 are the parallel data inputs. Information present on the parallel data inputs D_0 to D_3 is loaded into the counter & appears on the output when the load PL input is low this operation is overrides the counting function.

Pin Diagram:



Procedure

Make the connections as per the logic circuit of MOD-M counter circuit using IC-74LS90 & verify its truth table.

Observation table

Decade counter

clock pulse	Output			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Design of MOD-63 counter using IC7490

Dec eqn.	output-1 Q_3	Q_2	Q_1	Q_0	Reset logic
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1

Dec eqn	output-2 Q_3	Q_2	Q_1	Q_0	Reset logic X
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1

Logic gates / MSI device required for implementation:

Sr NO	Title	Name of IC	Number of gate req	IC req
01	MOD-N counter	MOD-10 counter 7490	2	2
		AND 7408	2	1
		OR 7432	1	1

Conclusion

Designed & implemented MOD-63 counter using IC-74LS90