

7 Dec

DELD Assignment 08

2/1/18



Title: Ripple Counter Circuit

Objective: Design & implement 3-bit asynchronous (Ripple) UP/DOWN counter circuit using IC 74LS76.

Apparatus: Digital Board, GP-4 Patch Cords, IC 74LS76, IC 74LS32, IC 74LS04/IC-74LS08 & required logic gates if any.

Theory:

- 1) Counter is sequential logic device which counts no. of pulses given to circuit.
- 2) Counter is classified in two categories. Synchronous & Asynchronous.
- 3) In Asynchronous counter output of first flip-flop goes back to the clock of next & so on., and input of all flip-flop is connected to VCC for IC-74LS76.
- 4) All set & reset pins are connected to VCC.

Pin diagram:

clock ₁		1k
PRESET ₁		10
CLEAR ₁	74LS76 DUAL	10
J	MS J-K FF	0ND
VCC		2k
clock ₂		20
PRESET ₂		20
CLEAR ₂		2J

procedure:

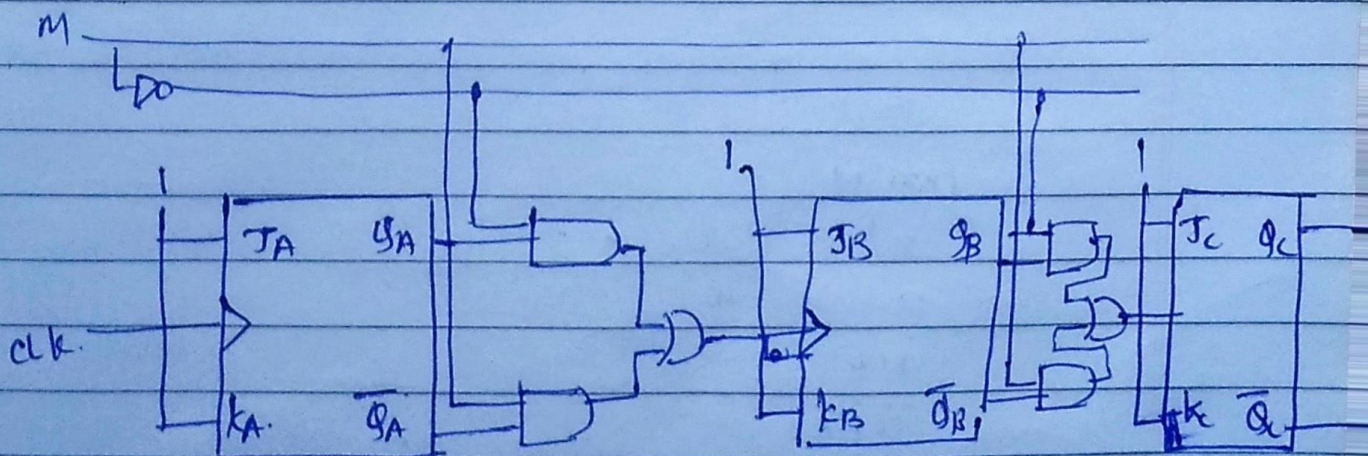
- 1) make the connections as per the logic circuit of 3-bit ripple up counter circuit using IC-74LS76 & Verify its TT.
- 2) Make the connections as per the logic of 3-bit ripple down counter circuit using IC-74LS76 & Verify its TT.

Design of 3-bit Asynchronous up/down-Counter: Logic Diagram:

M	Q	\bar{Q}	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

M	Q	\bar{Q}	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$Y = M\bar{Q} + \bar{M}Q$$



up counter $\Rightarrow Q_A Q_B Q_C$

down counter $\Rightarrow \bar{Q}_A \bar{Q}_B \bar{Q}_C$

Observation Table

clock Pulse.	UP			DOWN		
	Q_A	Q_B	Q_C	\bar{Q}_A	\bar{Q}_B	\bar{Q}_C
0	0	0	0	1	1	1
1	0	0	1	1	1	0
2	0	1	0	1	0	1
3	0	1	1	1	0	0
4	1	0	0	0	1	1
5	1	0	1	0	1	0
6	1	1	0	0	0	1
7	1	1	1	0	0	0

Logic gates / MSF device required for implementation:

Sr. No.	Title	Name of the IC	No. of gates	IC req.
01	3-bit ripple up/down counter.	JK FF 7476	3	2
		AND 7408	4	1
		OR 7432	2	1
		NOT 7404	1	1

Conclusion

Designed & implemented 3-bit Asynchronous (Ripple) UP counter circuit using IC 7476.