DELD Unit Test-2 21118 SHREE

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Q2 B) $f_1(A,B,C) = \Sigma(0,3,4,7)$

$f_2(A,B,C) = \Sigma(1,2,5,7)$

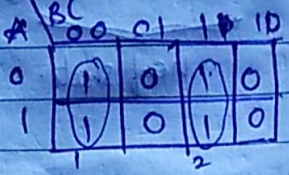
→

~~[illegible] the inputs~~

here A, B, C are the inputs

(i) : the K-map simplification will be

for f_1:

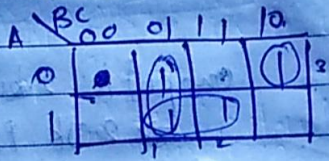


1 ⇒ $\bar{B}\bar{C}$

2 ⇒ BC

$\Big\}$ $y = \bar{B}\bar{C} + BC$

for f_2:



1 ⇒ $\bar{B}C$

2 ⇒ AC

3 ⇒ $A\bar{B}\bar{C}$

$\Big\}$ $y = AC + \bar{B}C + A\bar{B}\bar{C}$

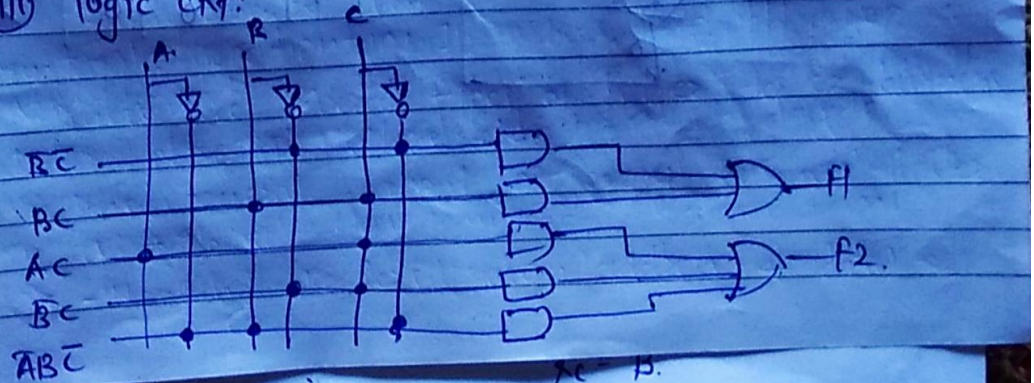
$\therefore f_1 = \bar{B}\bar{C} + BC$

$f_2 = AC + \bar{B}C + A\bar{B}\bar{C}$

(ii) PLA Table:

term	input			output	
	A	B	C	f_1	f_2
$\bar{B}\bar{C}$	-	0	0	1	-
BC	-	1	1	1	-
AC	1	-	1	-	1
$\bar{B}C$	-	0	1	-	1
$A\bar{B}\bar{C}$	0	1	0	-	1

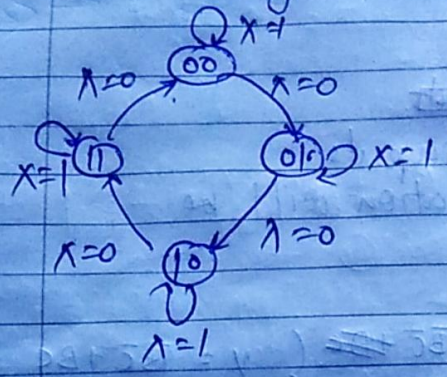
(iii) logic ckt:



Q4.B

A)

→ State diagram:

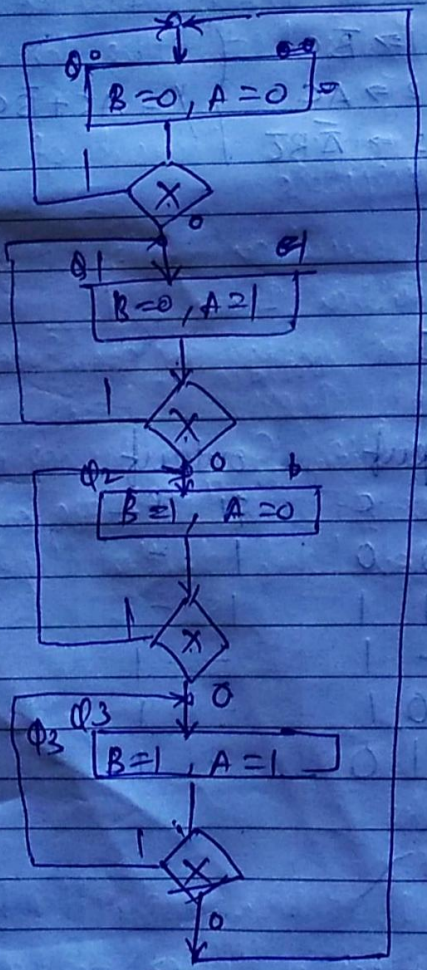


State table.

Present state	Y/P 0		output
Q_0	Q_1	01	Q_1 00
Q_1	Q_2	10	Q_2 01
Q_2	Q_3	11	Q_3 10
Q_3	Q_0	10	Q_0 11

next state

ASM chart:

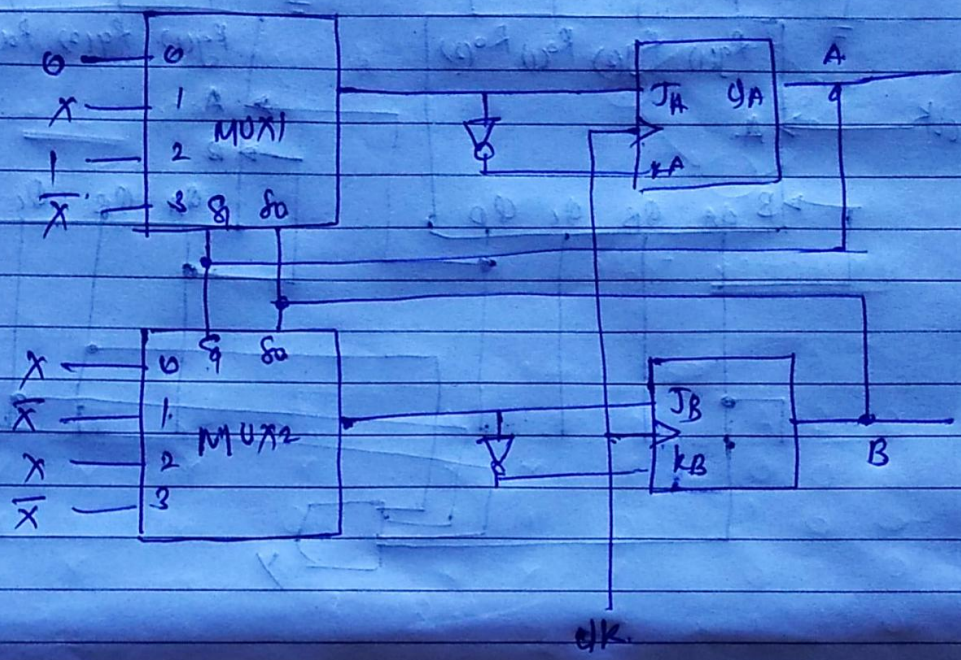


output is 2 bit
⇒ 2 JK FF's required
2 4:1 MUX required.

table:

Present state		Next state		I/p Condⁿ	MUX I/p	
A	B	A^+	B^+		MUX1	MUX2
0	0	0	0	$\bar{X}$	0	X
0	0	0	1	X		
0	1	0	1	$\bar{X}$	X	$\bar{X}$
0	1	1	0	X		
1	0	1	0	$\bar{X}$	1	X
1	0	1	1	X		
1	1	1	1	$\bar{X}$	$\bar{X}$	$\bar{X}$
1	1	0	0	X		

Logic diagram



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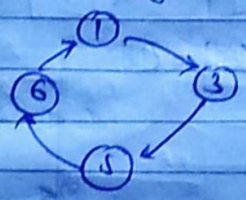
Q1 A)

→ The required sequence is 1→3→5→6→1

State diagram:



* highest state is 6. (110)
∴ we need 3 ff

Excitation table:

Q_n			Q_{n+1}									
C	B	A	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	X	X	X	X	X	X	X	X	X
0	0	1	0	1	1	0	X	1	X	X	0
0	1	0	X	X	X	X	X	X	X	X	X
0	1	1	1	0	1	1	X	X	1	X	0
1	0	0	X	X	X	X	X	X	X	X	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	1	X	1	X	1	1	X
1	1	1	X	X	X	X	X	X	X	X	X

k-map simplification:

J_C ⇒

C \ BA	00	01	11	10
0	X		1	X
1	X	X	X	X

$J_C = B$

J_B ⇒

C \ BA	00	01	11	10
0	X	1	X	X
1	X	1	X	X

$J_B = 1$

J_A ⇒

C \ BA	00	01	11	10
0	X	X	X	X
1	X	X	X	1

$J_A = 1$

K_B ⇒

C \ BA	00	01	11	10
0	X	X	X	X
1	X		X	1

$K_C = B$.

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$k_B \Rightarrow$

C \ BA	00	01	11	10
0	x	x	1	x
1	x	x	x	1

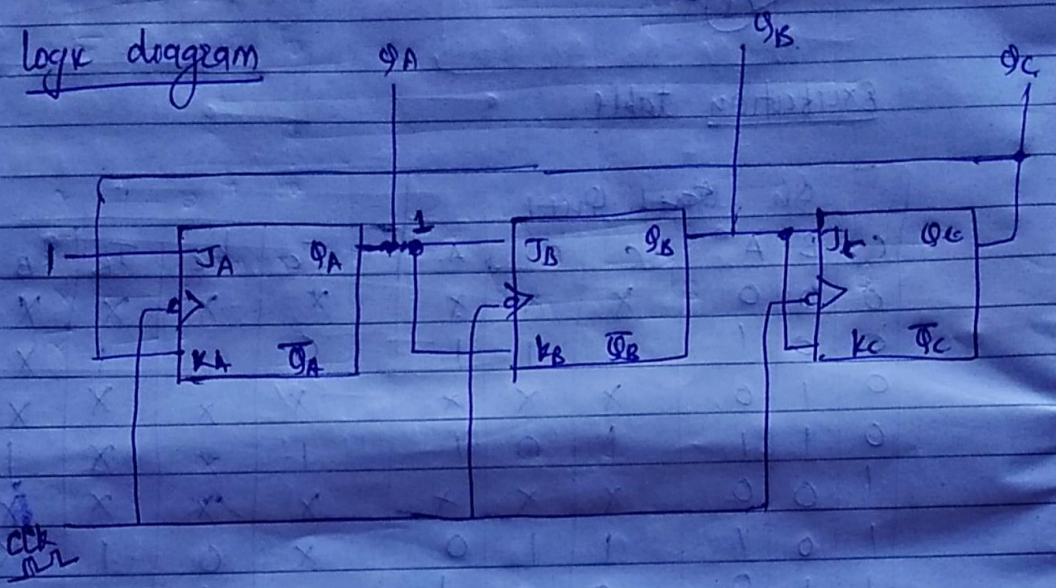
$k_B = 1$

$k_A \Rightarrow$

C \ BA	00	01	11	10
0	x			x
1	x	1	x	1

$k_A = C$

Logic diagram



(A)

→ MOD 08

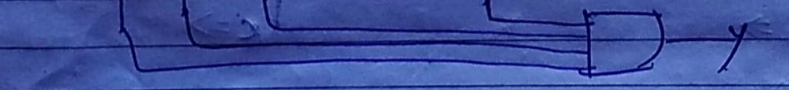
The total no. of ICs required : 2 IC 7490.

Design of reset logic:

78 = 0111 1000

Q_D	Q_C	Q_B	Q_A
0	1	1	1

Q_D	Q_B	Q_C	Q_A
1	0	0	0



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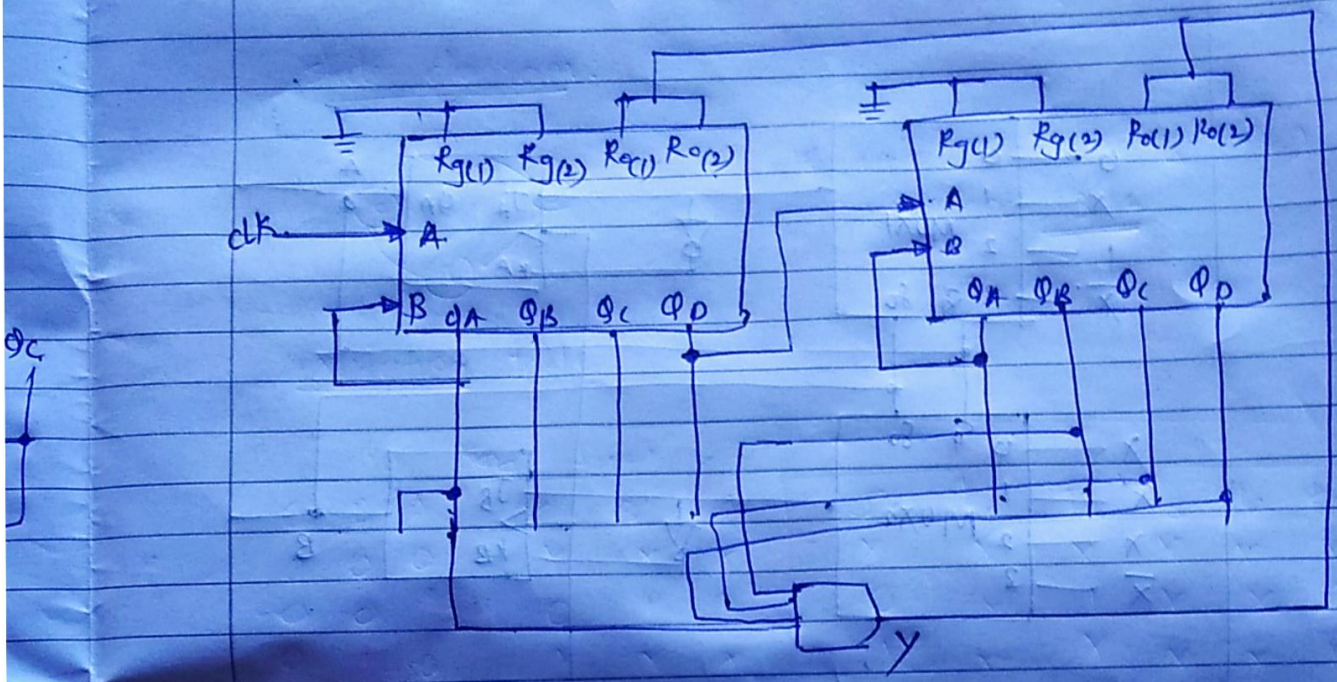
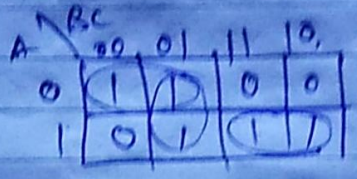
Logic design:



Q4.

→ $F1(A,B,C) = \Sigma(0,1,3,5,7)$

① k-map

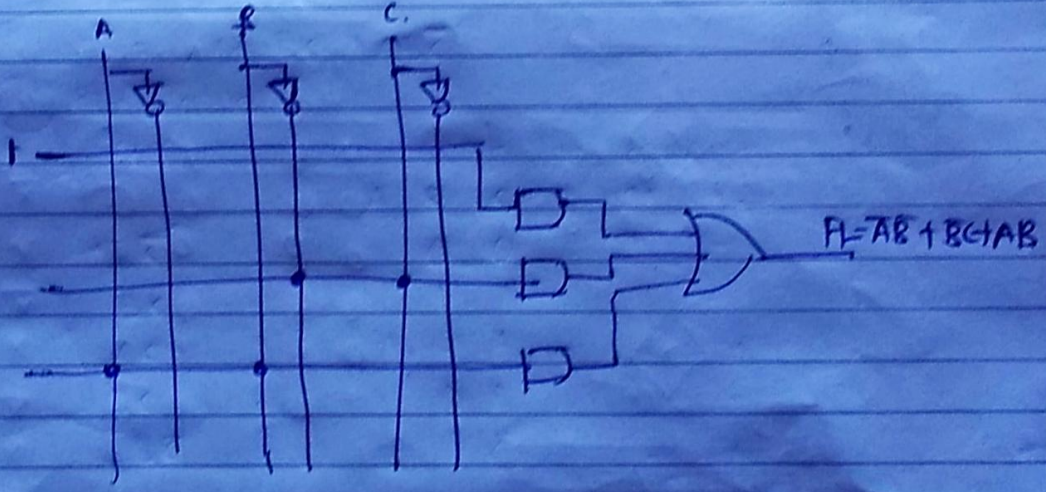


$F1 = \overline{A}\overline{B} + BC + AB$

② PAL table

Product term.	Inputs			outputs
	A	B	C	
$\overline{A}\overline{B}$	0	0	-	f1
$\overline{B}C$	0	0	1	f1
AB	1	1	-	f1

③ logic diagram.



A)

1) → The toggle condition in JK master-slave flip-flop occurs when. J=1 & K=1

2) → How many ff are required to construct decade counter. 4

3) → the group of flip-flops connected together forms counter

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4) → o/p changes corresponding to falling edge of clock signal in case of Negative edge triggered FF

5) → output of the given ckt is $Q_3Q_2Q_1Q_0 = 0101$