Title: Multiplexer / Demultiplexerobjective:

- 1) Verification of function table of IC 74LS153
- 2) Design & implement 8:1 MUX using IC 74LS153 & verify its truth table
- 3) Realization of the following boolean expression using IC 74LS153 & verify its truth table

$$f(A_1B_1C_1D_1) = \sum m(1, 2, 3, 4, 5, 6, 14, 15)$$

- 4) Verification of function table of IC 74LS138
- 5) Realization of the following boolean expression using IC 74LS138 & verify its truth table

$$f(A_1B_1C_1) = \sum m(2, 3, 4, 5, 8, 9, 14, 15)$$

Apparatus: Digital board, GP-4-patch chords, IC-74LS32, IC74LS08 / IC74LS04 / IC74LS153 / IC74LS138 & required logic gates

Theory:

- 1) Multiplexer is a combinational logic device which has many inputs & one output which can be selected according to select input.
- 2) IC74LS158 is dual 4:1 MUX. It is a 16-pin dual in-line packaged IC, which has two enable pins (STROBE Active low). We can design 8:1 MUX using cascading of two 4:1 MUX. This is achieved with the help of enable/strobe inputs & MUX tree is designed.

To implement 8:1 MUX we need 3 select lines & one output.

- 3) DEMUX / deoder is a combinational logic device, which has one input & many output, one output can be selected according to select input.

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IC 74LS138 is a 3 to 8 line decoder/DEMUX.

It is 16-pin dual packaged IC, which has 3-enable pins (2-STROBE Active Low & one Active High).

IC 74LS138 produces complementary output i.e. Active low.

We can design any combinational circuits using IC 74LS138. Decoder performs inverse operation to that of MUX.

Pin diagram

TE	V	Vcc	A	V	Vcc
S1	7	$\bar{2E}$	B	7	$\bar{Y_3}$
IA3	4	80	C	9	$\bar{Y_6}$
IA2	6	2A3	G1	6S	$\bar{Y_5}$
IA1	1	2A2	G2	1	$\bar{Y_4}$
IA0	5	2A1	G3	3	$\bar{Y_3}$
IY	3	2A0	\bar{Y}_6	8	\bar{Y}_2
IND		2Y	GND		\bar{Y}_1

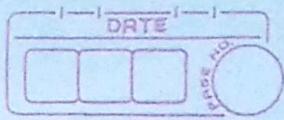
Procedure

- 1) Make connections as per the pin-diagram of IC 74LS138 & verify its truth table.
- 2) Make connections as per logic circuit of 8:1 MUX & Verify its truth table.
- 3) Make connections as per logic circuit of the given function & verify its truth table.
- 4) Make connections as per the pin diagram of IC 74LS138 & verify its truth table.
- 5) Make the connections as per the logic circuit of given function & verify its truth table.

Design of Multiplexer:

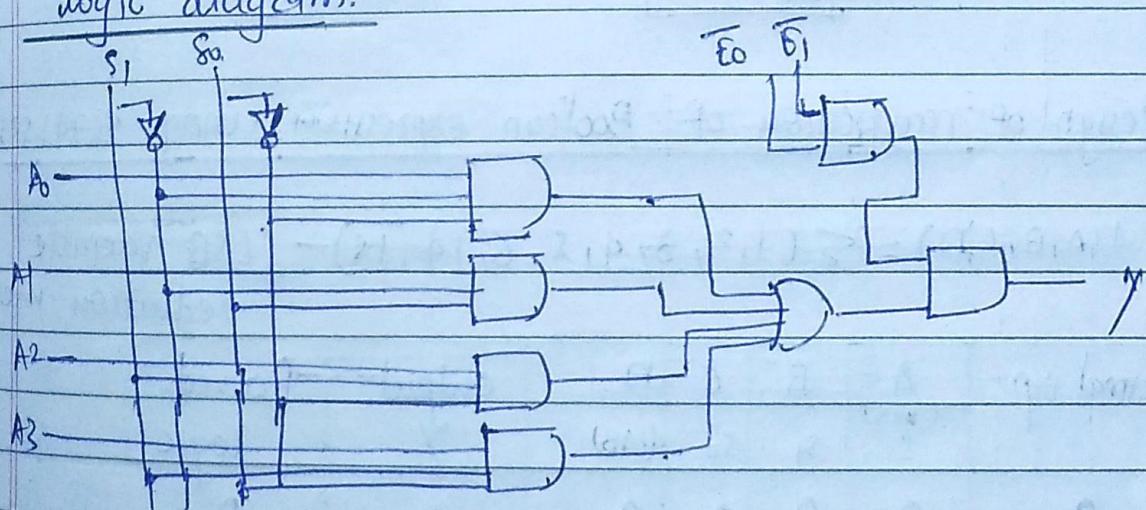
function table: IC74LS153

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Chip Enable I/P	Select Input	Output	
1E	2E	S1(MSB) S0(LSB)	MUX-1 (1Y) MUX2(2Y)
0	0	0 0	1A0 ~2A0
0	0	0 1	1A1 ~2A1
0	0	1 0	1A2 ~2A2
0	0	1 1	1A3 ~2A3

logic diagram:

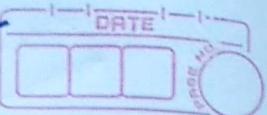


Design of 8:1 MUX using IC 74LS153

design table:

S2(MSB)	S1	S0(LSB)	Output(Y)
0	0	0	1A0
0	0	1	1A1
0	1	0	1A2
0	1	1	1A3
1	0	0	2A0
1	0	1	2A1
1	1	0	2A2
1	1	1	2A3

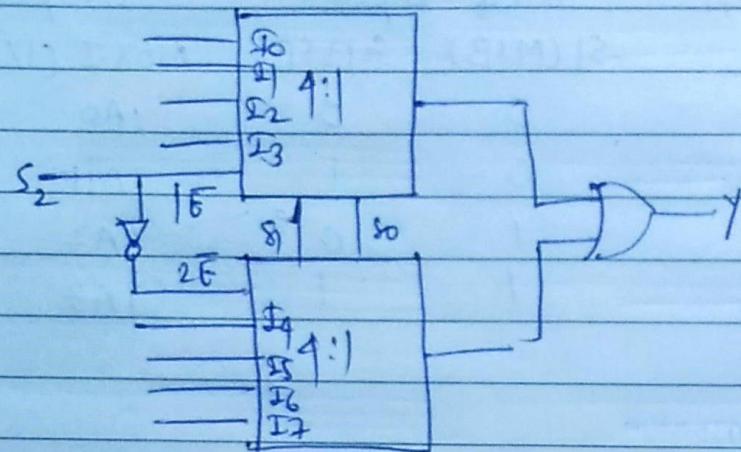
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logic diagram

$8:1 \Rightarrow 3$ select lines

$4:1 \Rightarrow 2$ select lines



Abbrev	Meaning
I0	1A0 0
I1	1A1
I2	1A2
I3	1A3
I4	2A0
I5	2A1
I6	2A2
I7	2A3

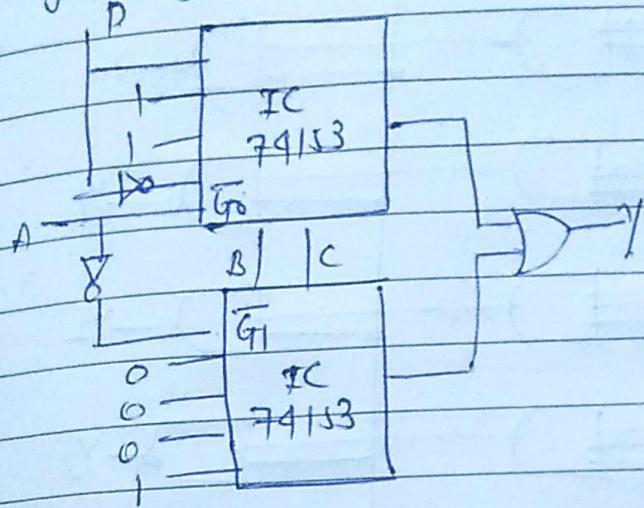
Design of realization of Boolean expression using IC74LS153

$$f(A, B, C, D) = \sum(1, 2, 3, 4, 5, 6, 14, 15) \quad (\text{LSB variable reduction method})$$

Decimal Eq	A (MSB) S ₂	B S ₁	C S ₀	D (LSB)	Output Y	Pearced logic
0	0	0	0	0	0	D
1	0	0	0	1	1	
2	0	0	1	0	1	
3	0	0	1	1	1	
4	0	1	0	0	1	
5	0	1	0	1	1	
6	0	1	1	0	1	D
7	0	1	1	1	0	
8	1	0	0	0	0	0
9	1	0	0	1	0	
10	1	0	1	0	0	0
11	1	0	1	1	0	
12	1	1	0	0	0	0
13	1	1	0	1	0	
14	1	1	1	0	1	
15	1	1	1	1	1	

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logic diagram.



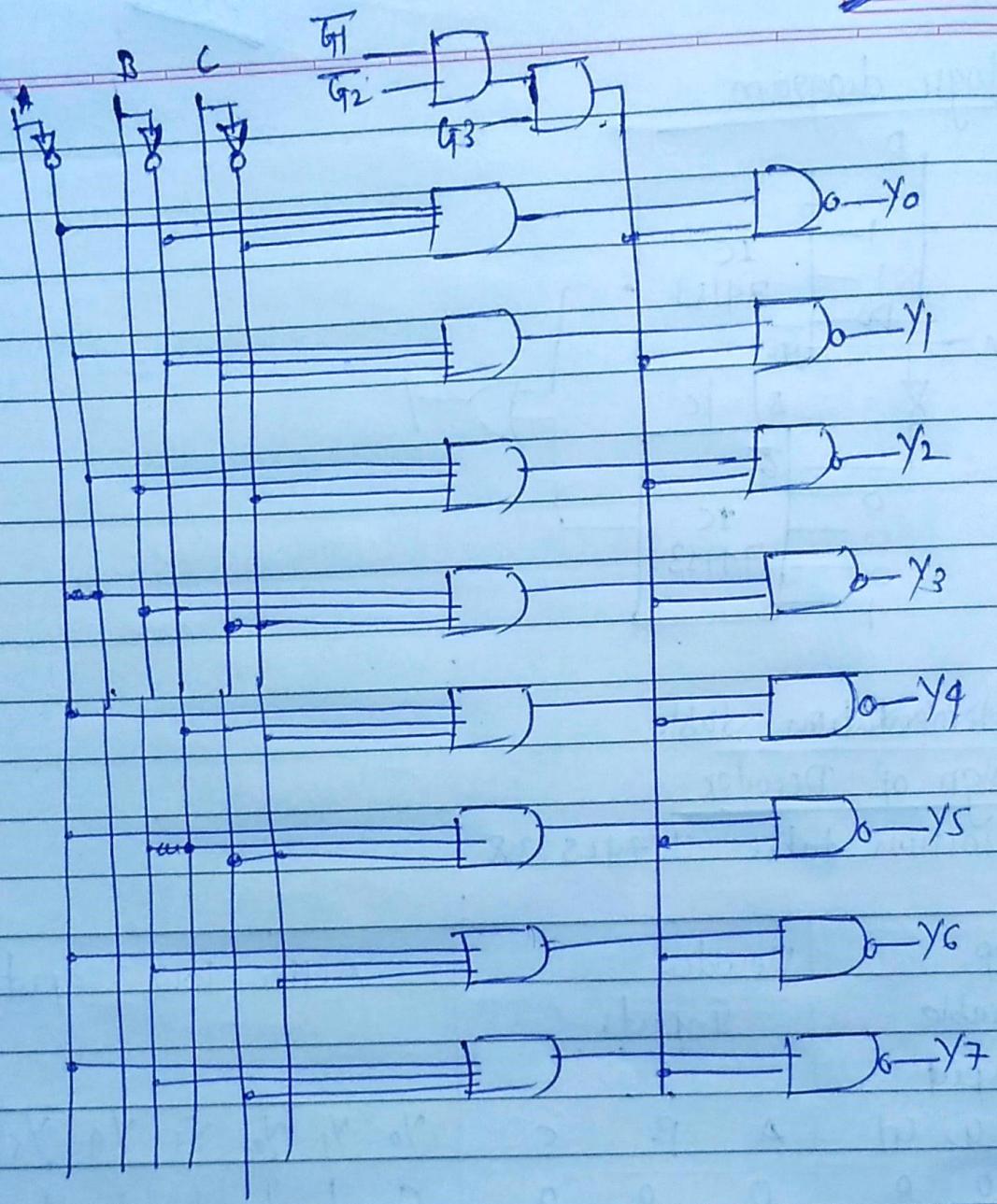
Implementation table

Design of Decoder

function table: IC74LS138

Chip Enable	Decoder Inputs	Active Low Outputs
Input:	A R C	$Y_0 \ Y_1 \ Y_2 \ Y_3 \ Y_4 \ Y_5 \ Y_6 \ Y_7$
1 0 0	0 0 0	0 1 1 1 1 1 1 1
1 0 0	0 0 1	1 0 1 1 1 1 1 1
1 0 0	0 1 0	1 1 0 1 1 1 1 1
1 0 0	0 1 1	1 1 1 1 0 1 1 1
1 0 0	1 0 0	1 1 1 1 1 0 1 1
1 0 0	1 0 1	1 1 1 1 1 1 0 1
1 0 0	1 1 0	1 1 1 1 1 1 1 0
0 0 0	1 1 1	1 1 1 1 1 1 1 0

logic diagram



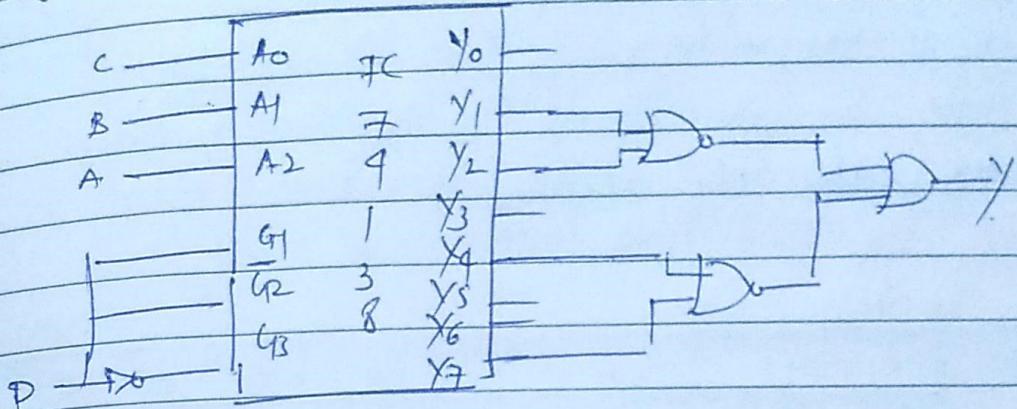
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Design of realization of boolean expression using IC74LS138

$$f(A, B, C, D) = \sum(2, 3, 4, 5, 8, 9, 14, 15)$$

Decimal eqn	A	B	C	Output f(A, B, C)
0	0	0	0	0
1	0	0	1	\overline{D}
2	0	1	0	\overline{D}
3	0	1	1	0
4	1	0	0	\overline{D}
5	1	0	1	0
6	1	1	0	0
7	1	1	1	\overline{D}

Logic diagram



Logic gates/ MSI device required for implementation:

No.	Title	Name of IC	No. of gates req.	TC req
01	Design of 8:1 MUX	Hex Inverter 7404	1	1
		Quad-2-input OR 7432	1	1
		4:1 MUX 74153	2	1
02	Realization of boolean expression using LUB reduction method	Hex Inverter 7404	2	1
		Quad-2-input OR 7432	1	1
		4:1 MUX 74153	2	1
03	Realization of boolean expression using MSB reduction method	Hex Inverter 7404	2	1
		Quad-2-input OR 7432	1	1
		4:1 MUX 74153	2	1
04	Realization of boolean expression using decoder IC	Quad-2-input NAND 7400	3	1
		Quad-2-input OR 7432	1	1
		3:8 decoder 74138	1	1

Conclusion

Sufficiently verified function table of IC-74LS153, designed & implemented 8:1 MUX using IC74LS153 & verified its TT. Realized the boolean expression using IC74153 (MSB reduction & LUB reduction), verified for table of IC74138, realized boolean expression using IC74138.