

## **VLSI SUMMER SCHOOL**

### **PARTICIPANTS**

**SAKETH 15EE10038**

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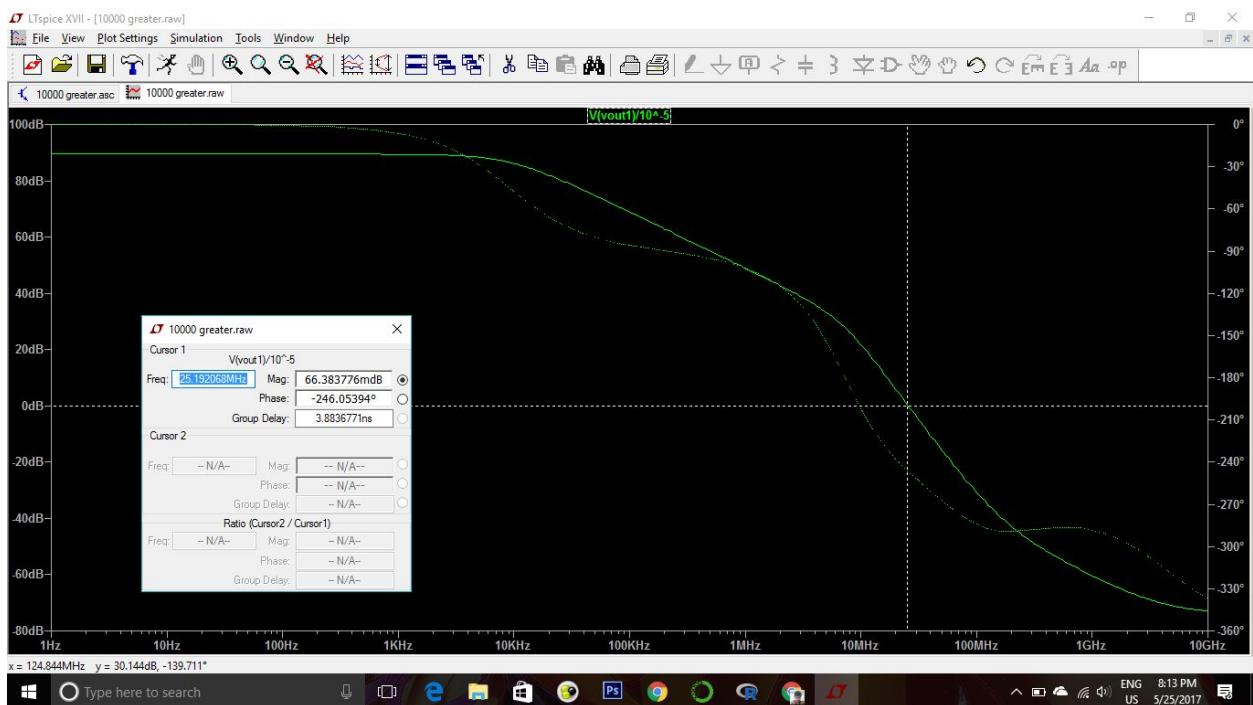
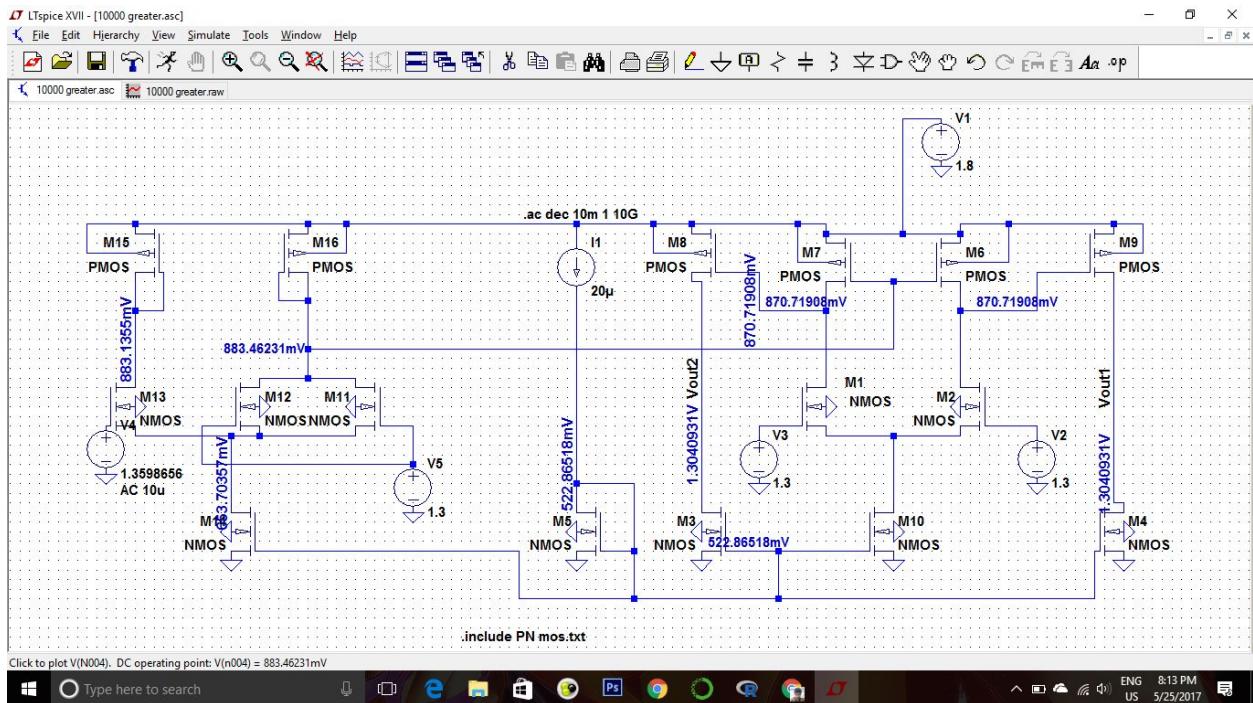
**SAUMYA JAIN 15EE10040**

[saumya.dakshana2015@gmail.com](mailto:saumya.dakshana2015@gmail.com)

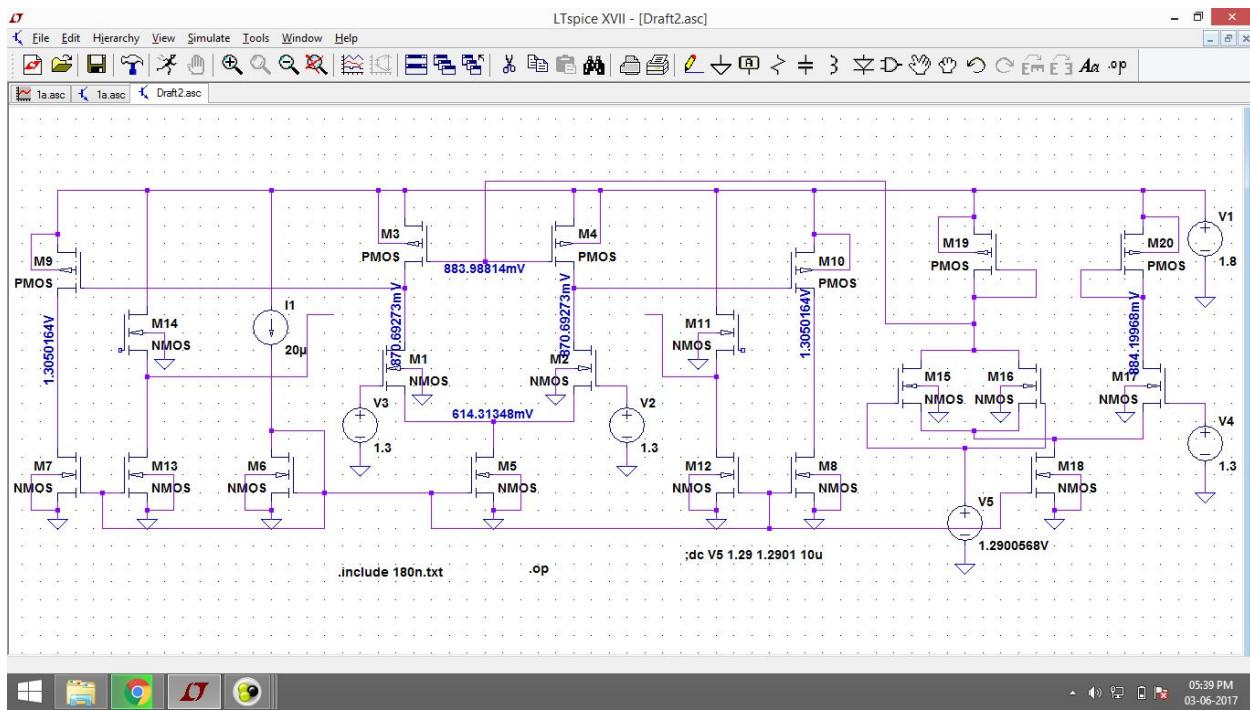
**Vasisht Duddu (Intern)**

[vduddu@tutamail.com](mailto:vduddu@tutamail.com)

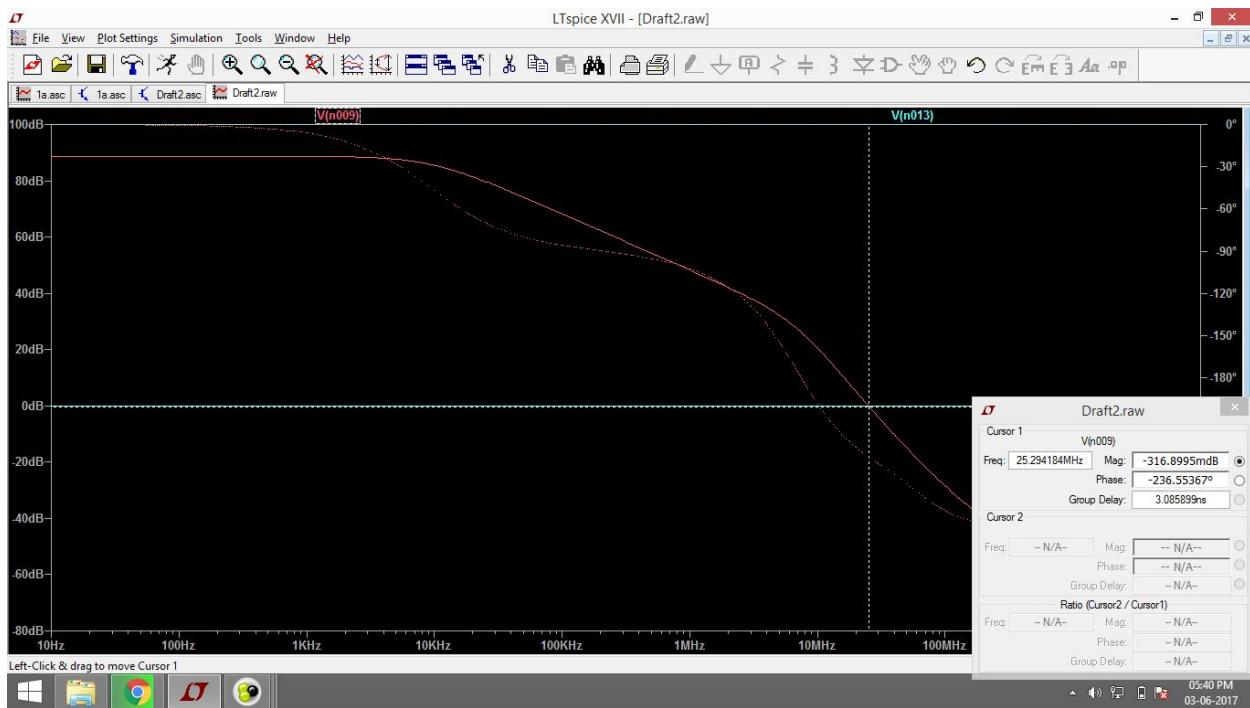
## Two stage op-amp with one CMFB



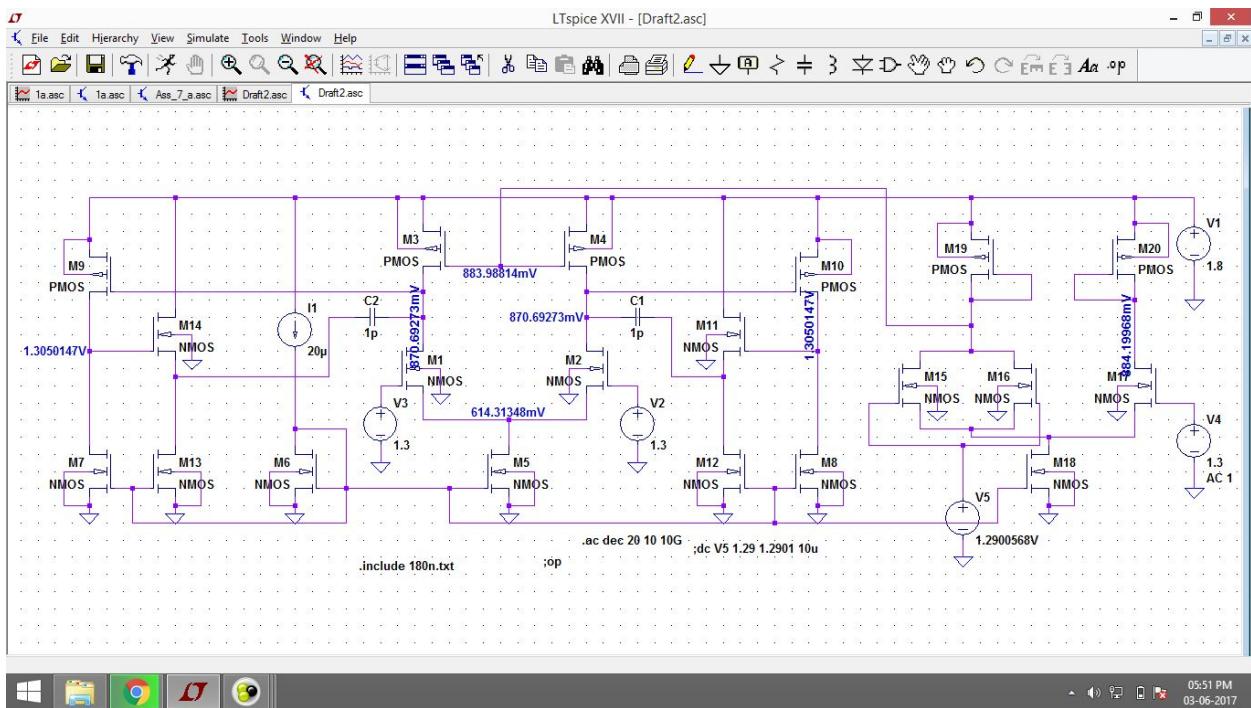
## Two stage op-amp with one CMFB(before compensation):



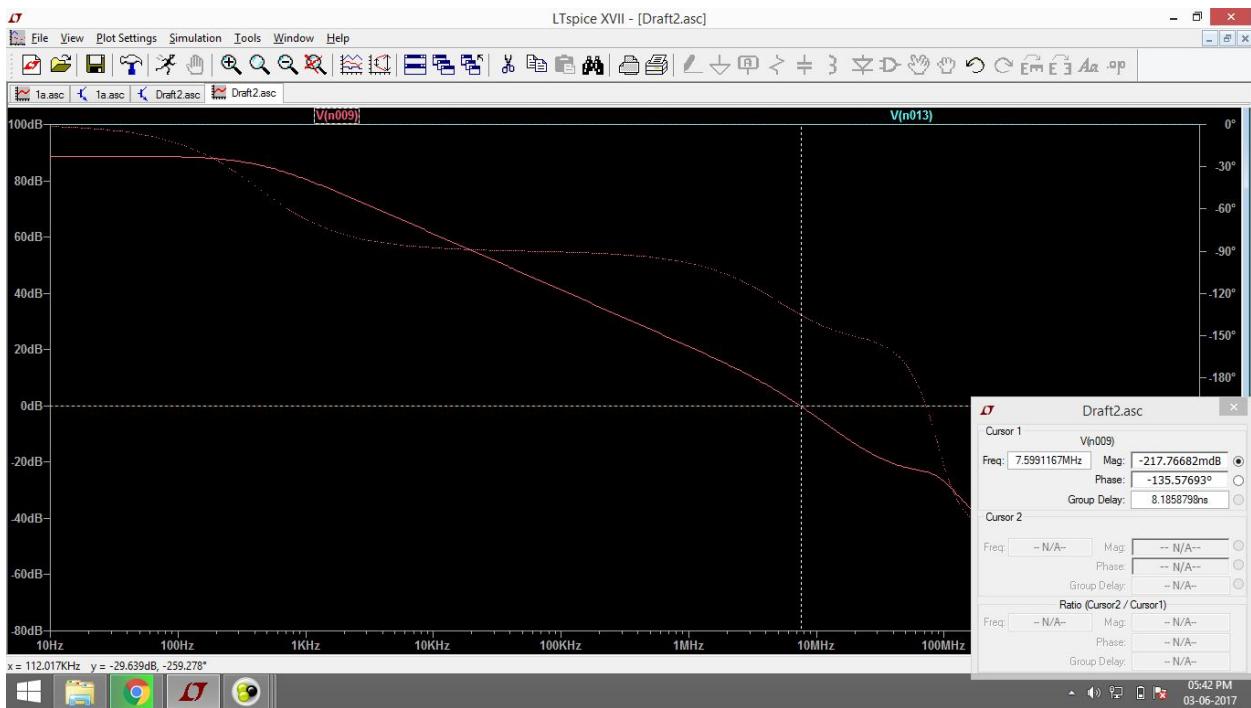
## Frequency response:



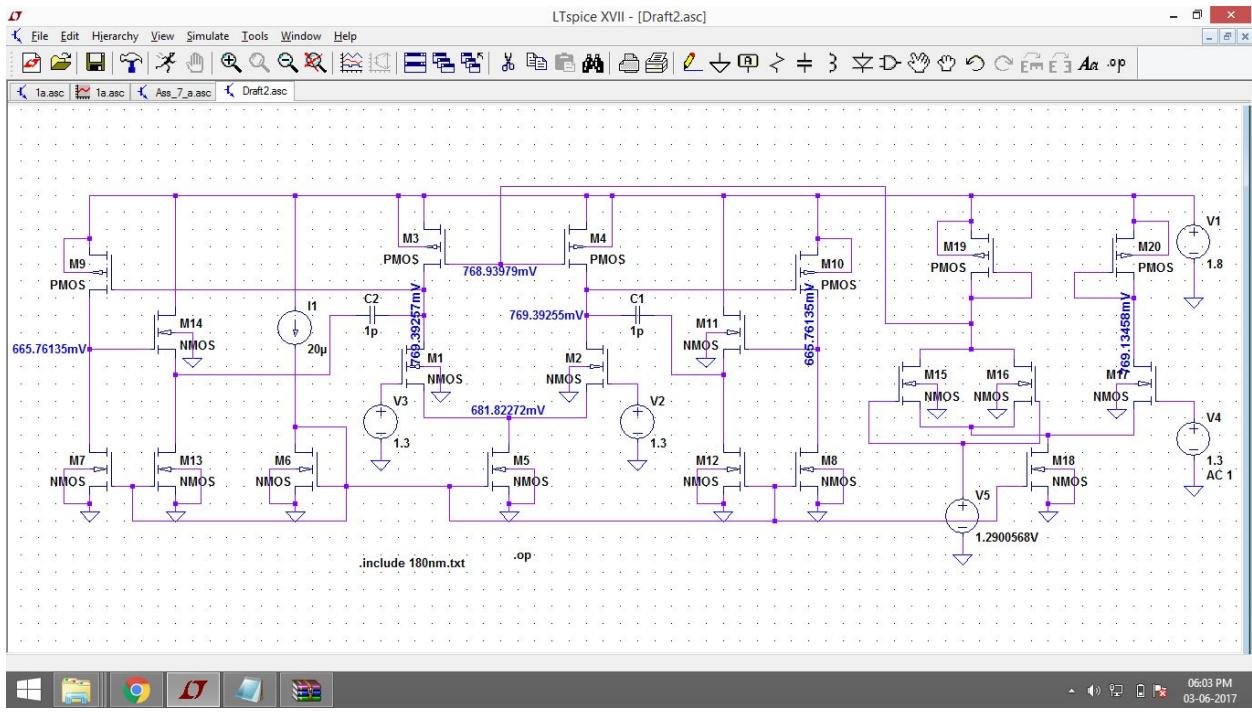
## After compensation:



## Frequency response:



When  $V_{tn}$  was reduced by 25%, and  $|V_{tp}|$  was increased by 25%:



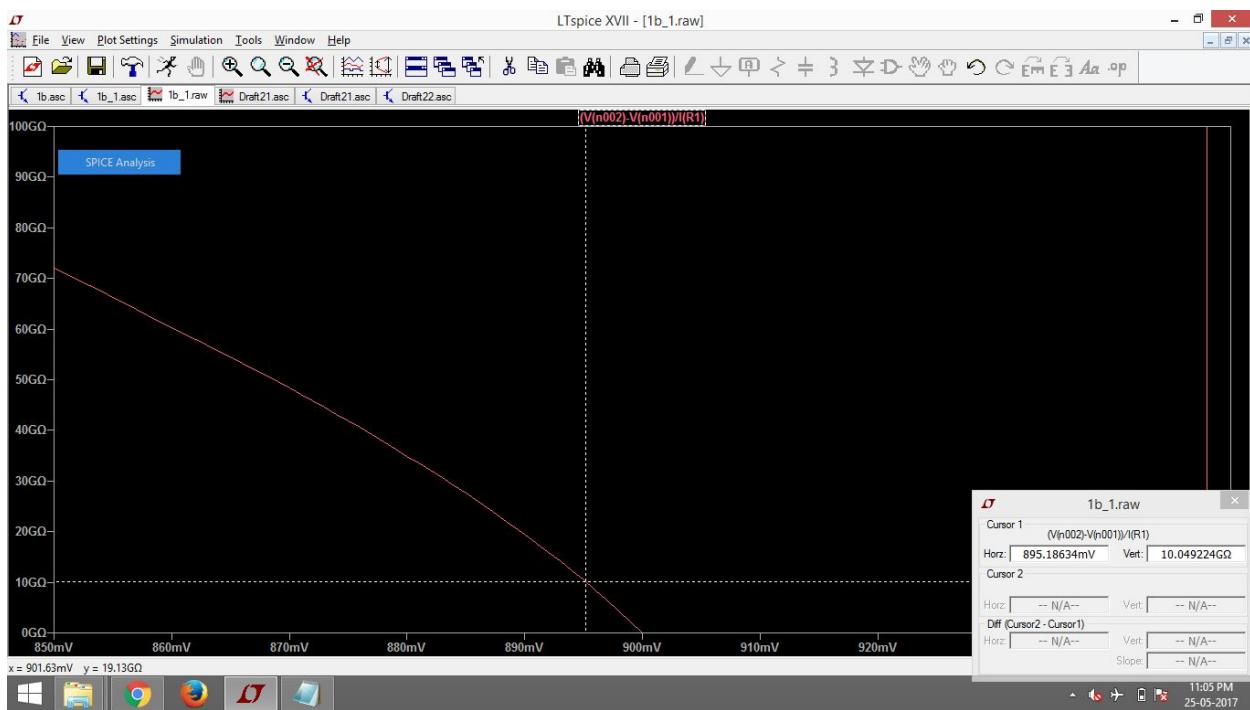
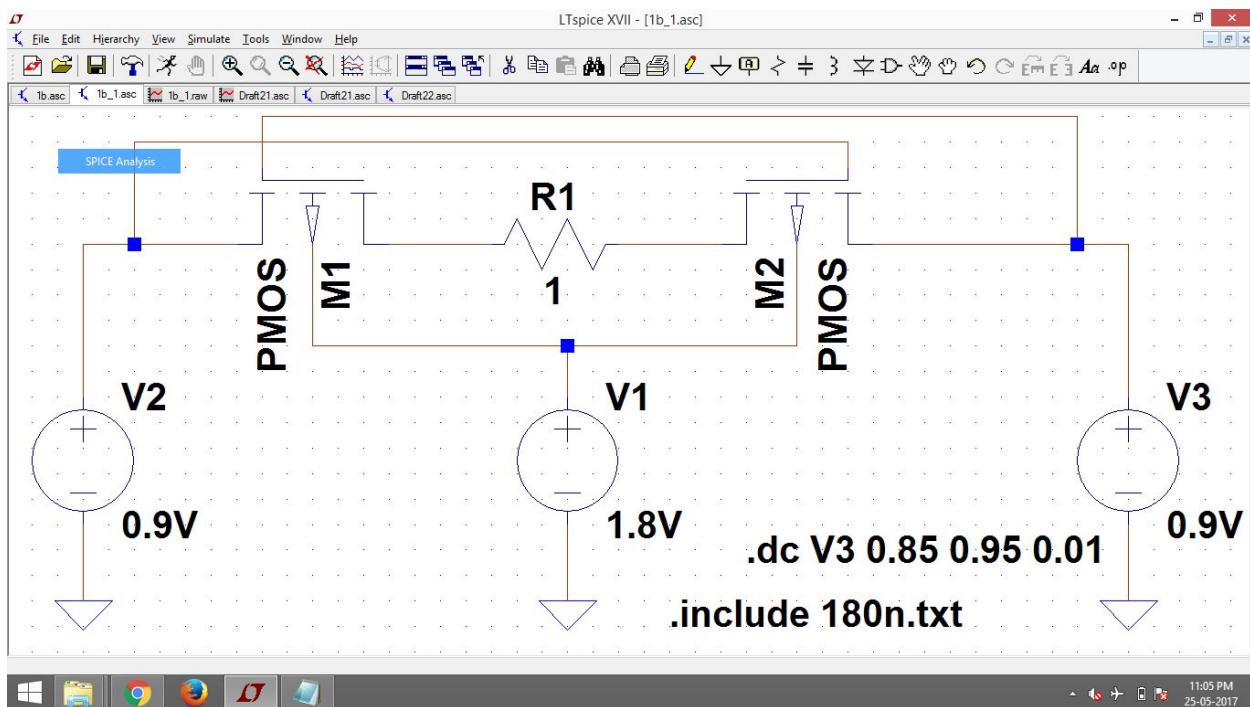
Total change in DC bias point of first stage:

Initially: 870.69273mV

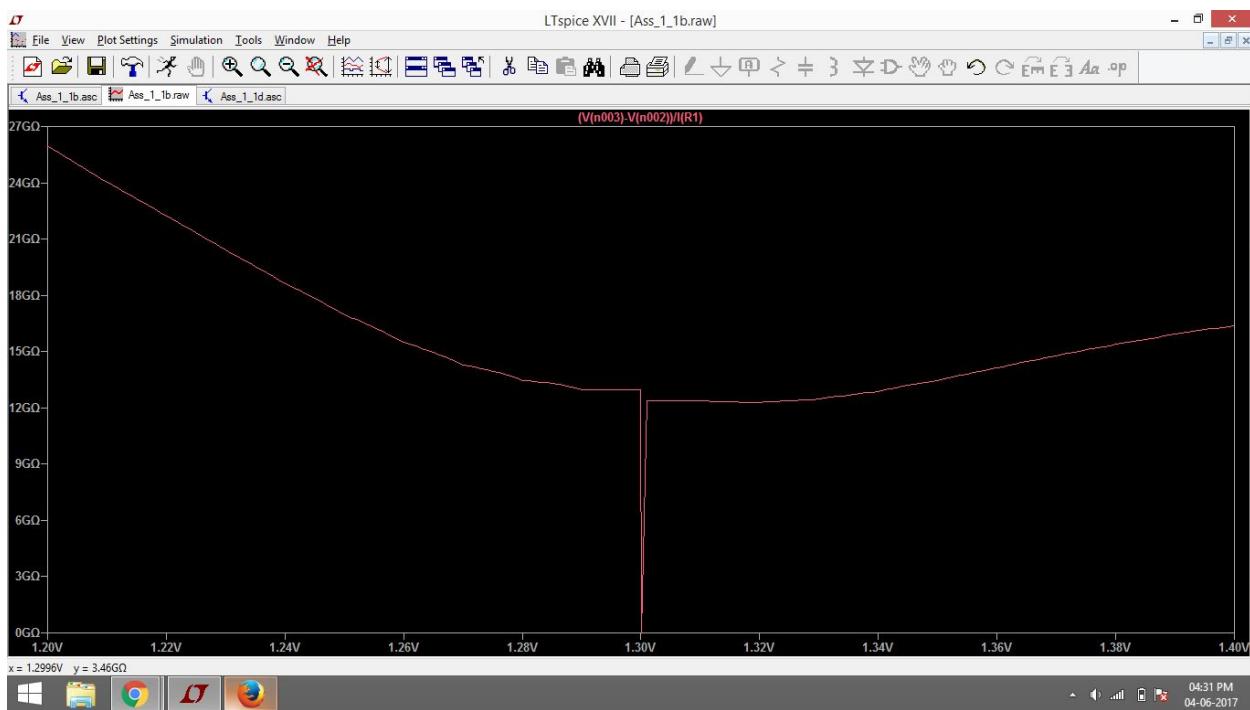
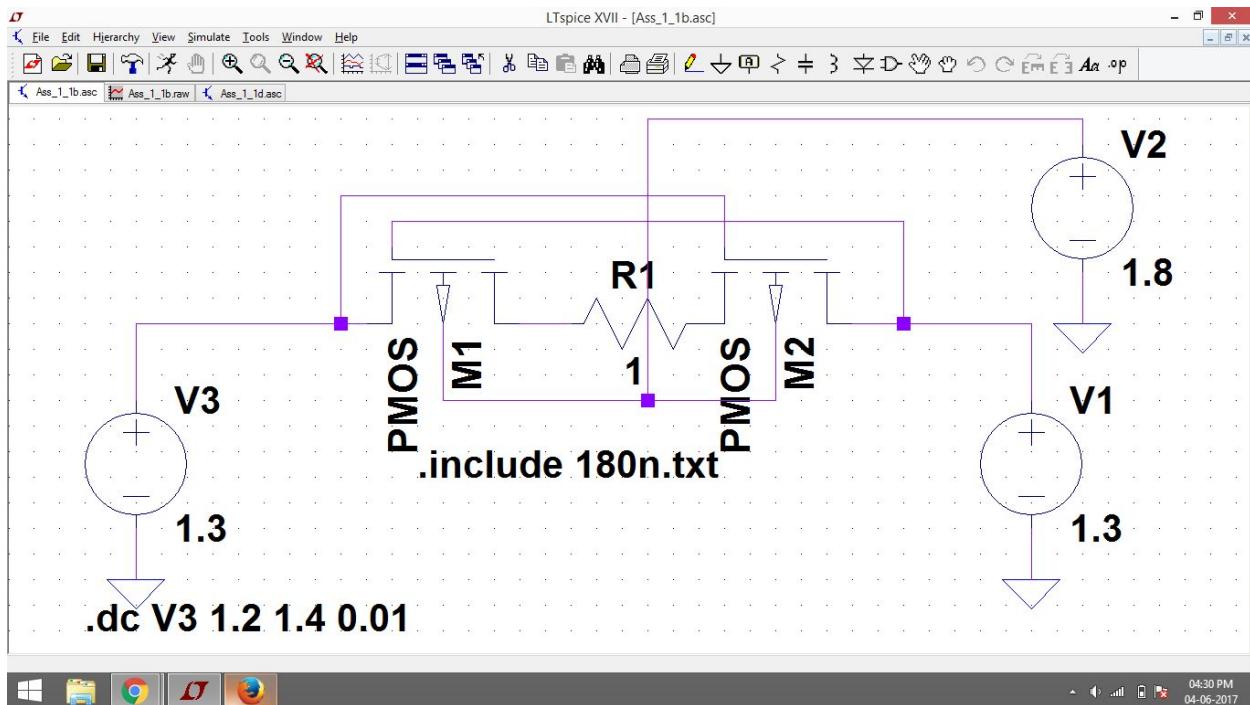
After changing: 769.39255mV

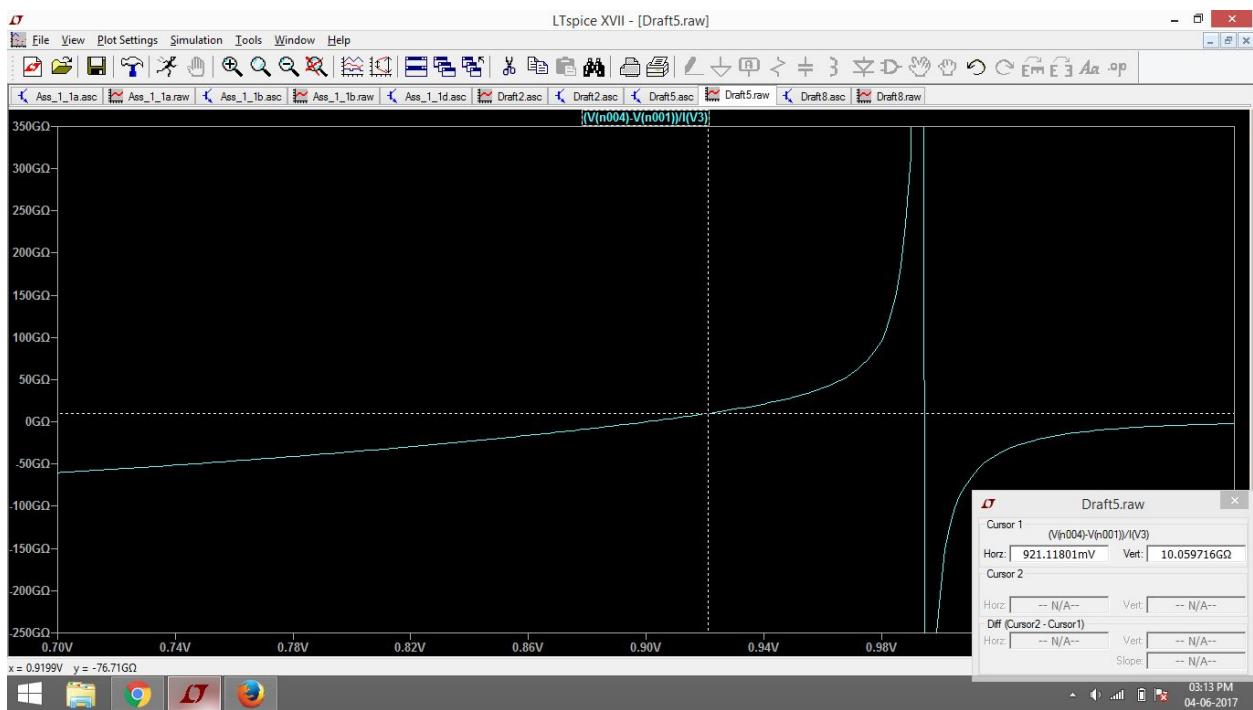
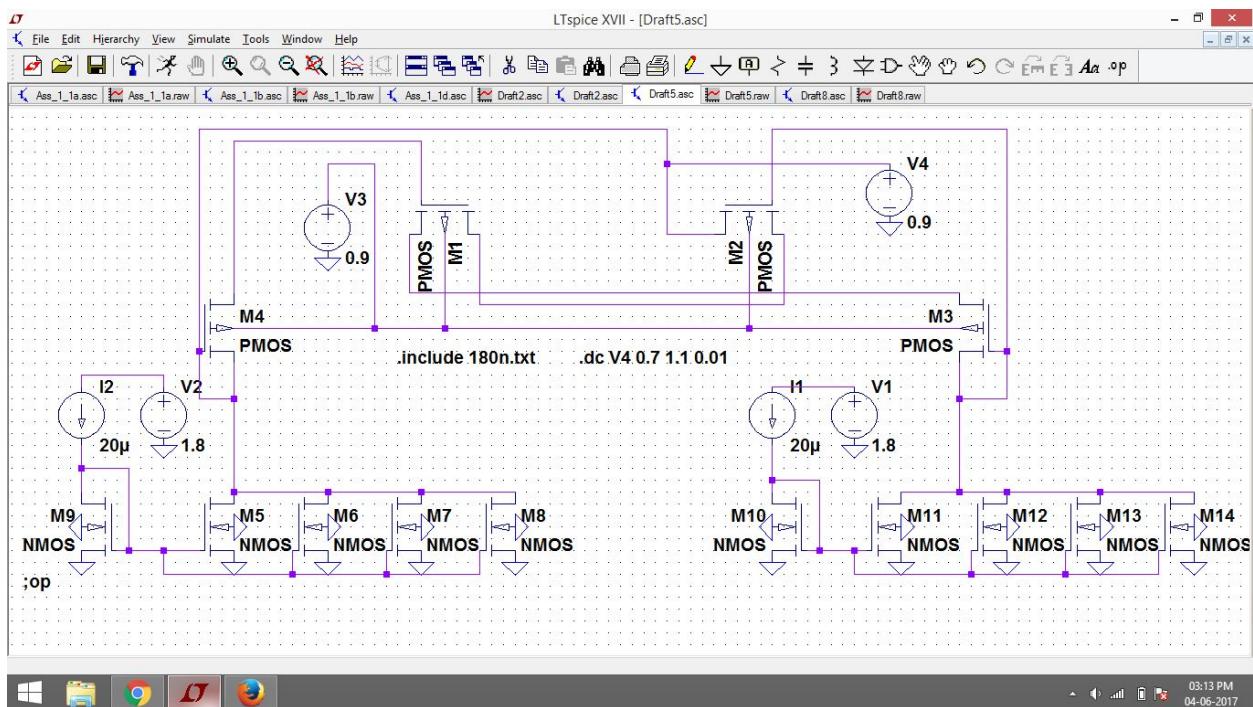
Difference: 101.30018mV

## 10G-ohm resistance:

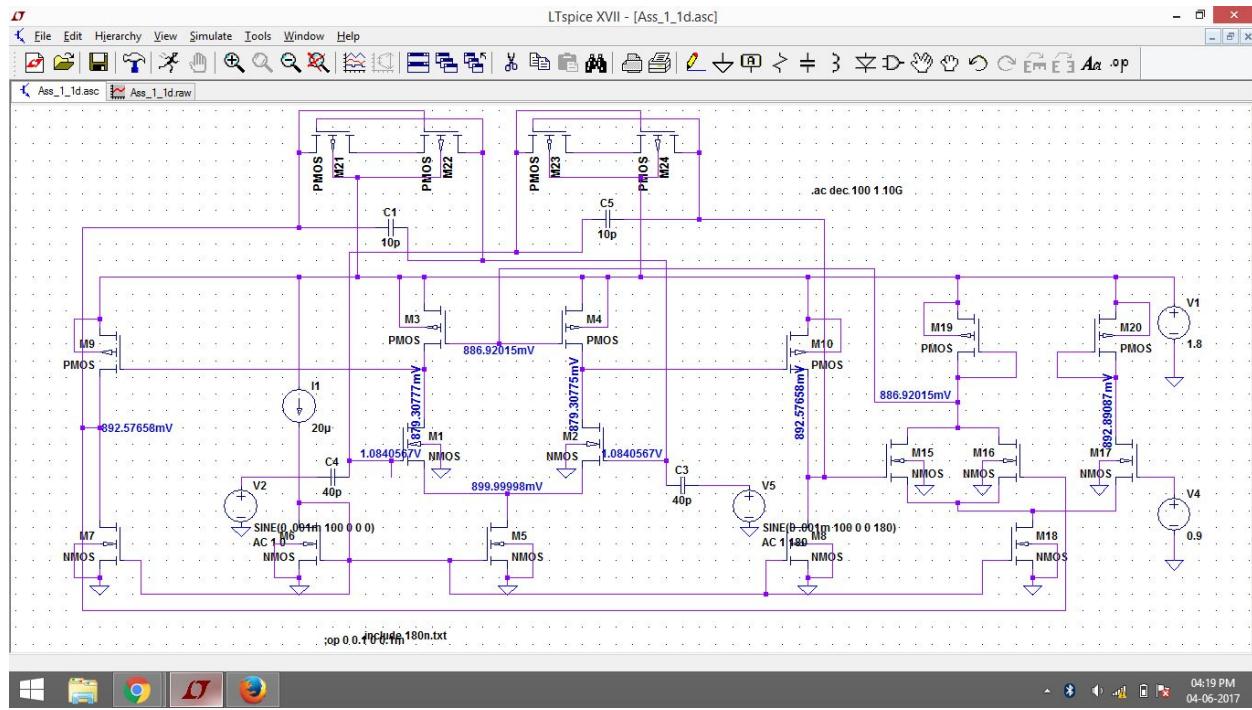


## 10 G-ohm resistance(corrected):

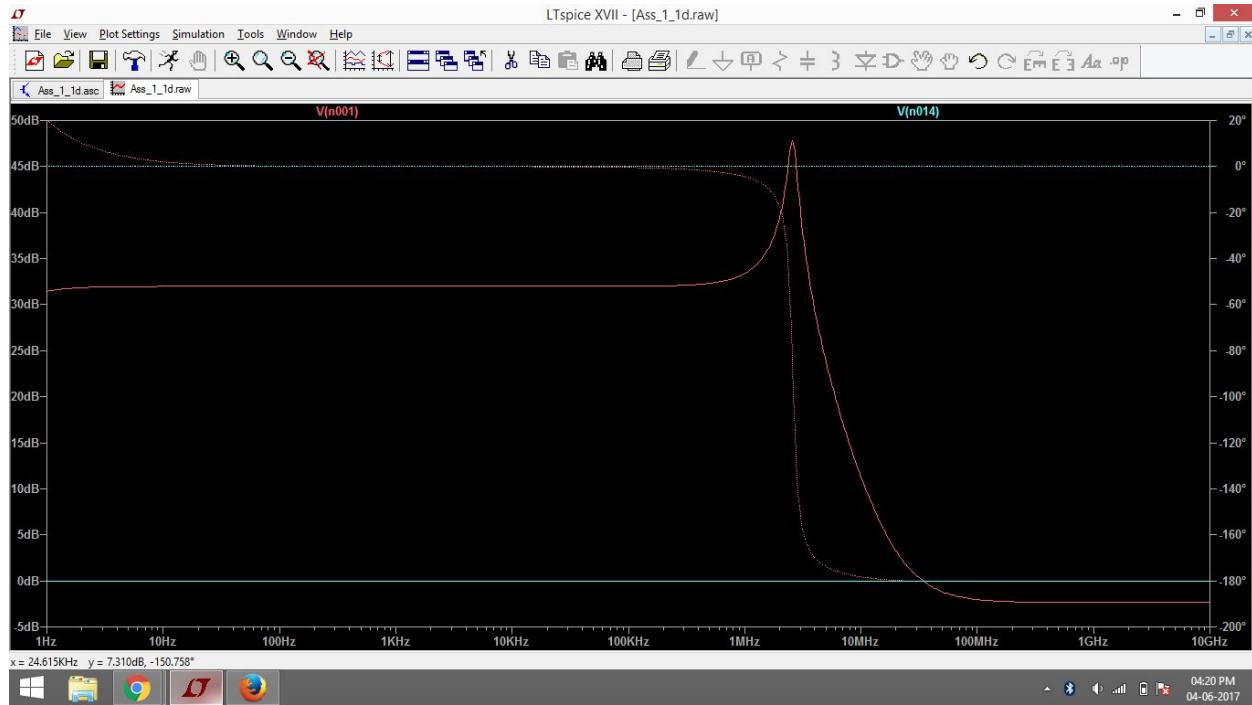




## Capacitive feedback for differential gain ~ 40

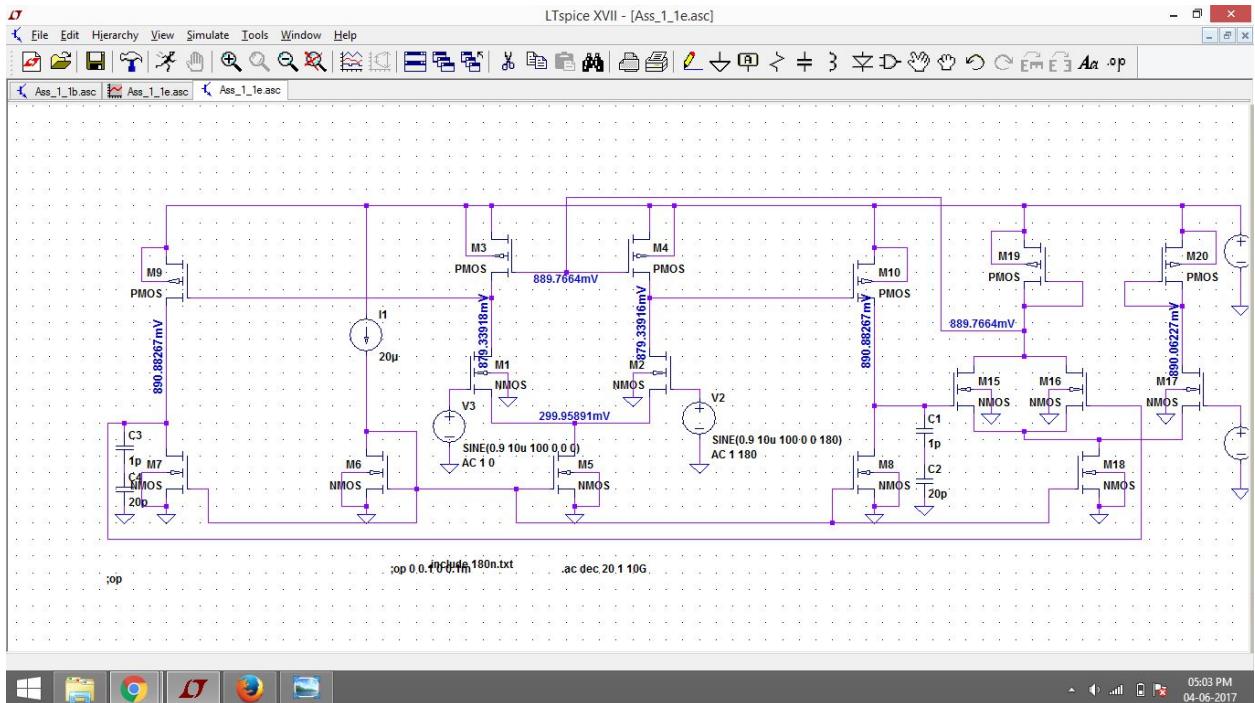


## Frequency response:

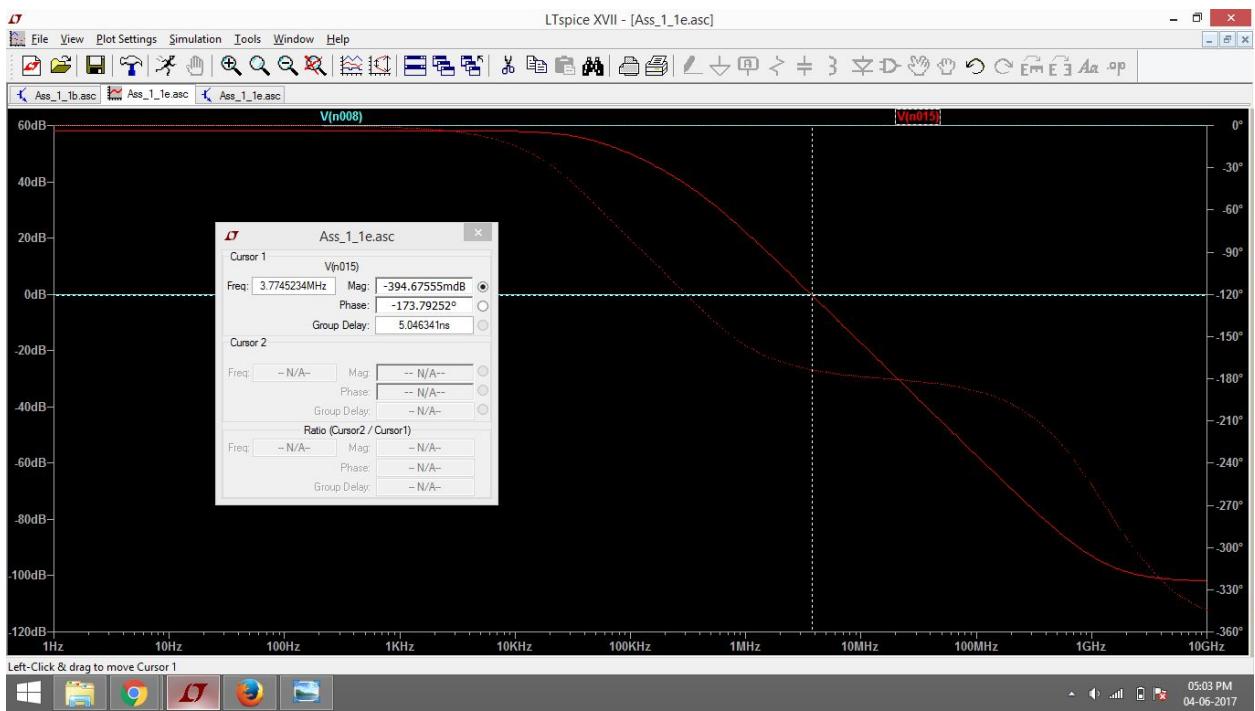


## Compensation of differential loop:

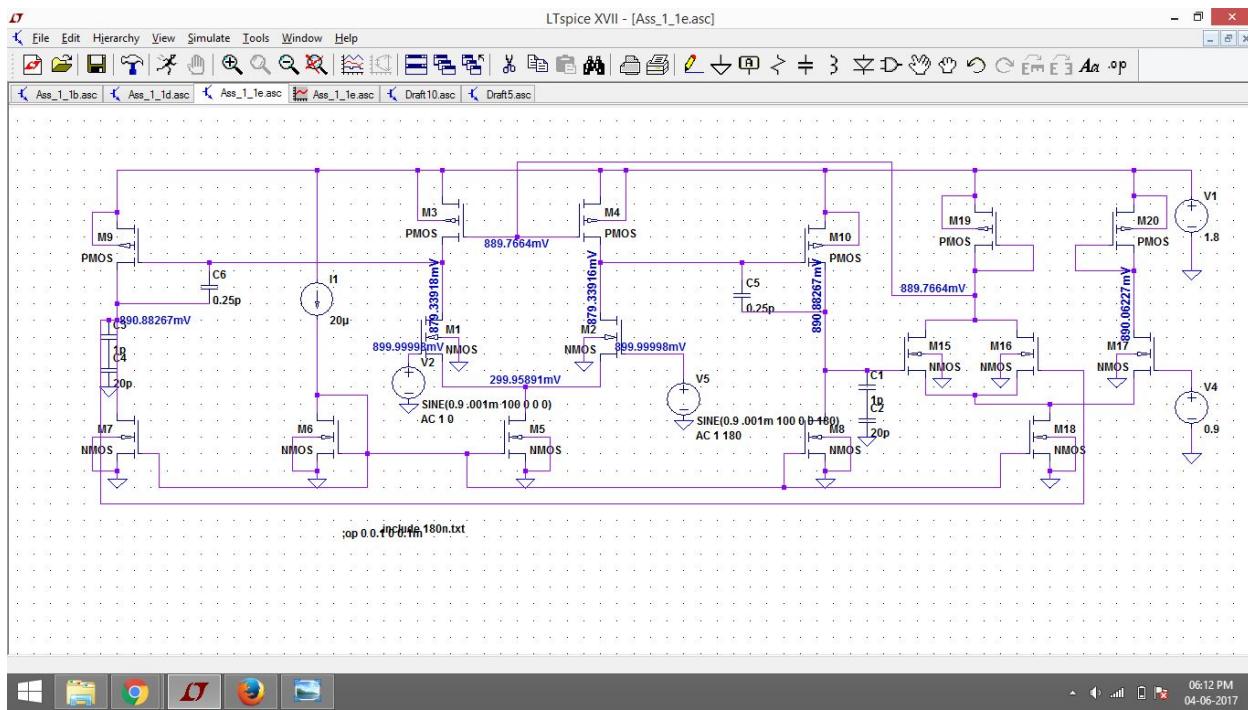
### Before compensation:



## Frequency Response:

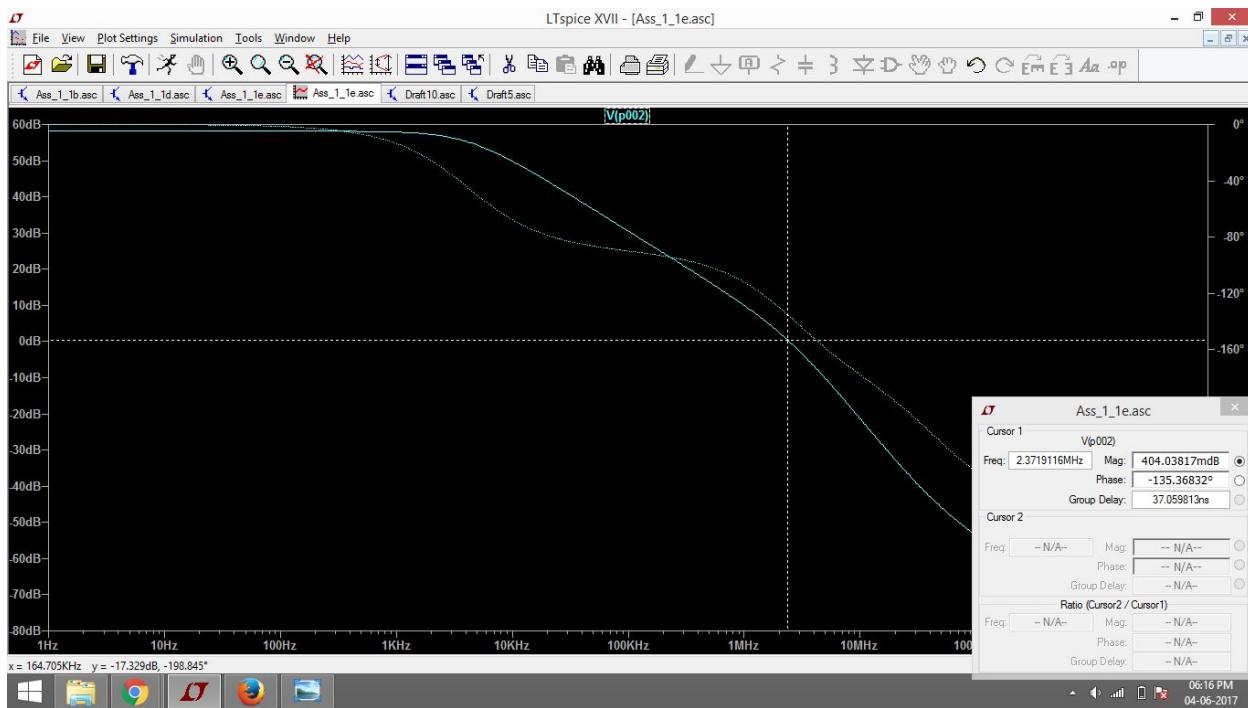


## After Compensation:

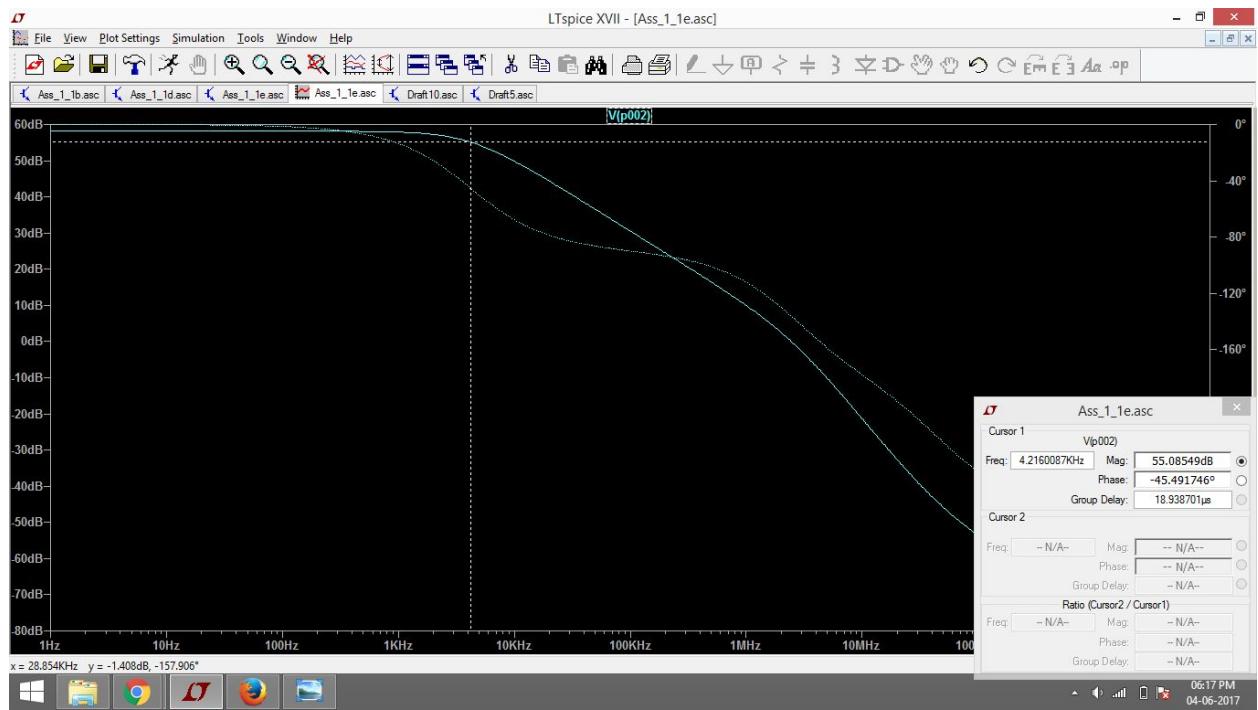


## Frequency Response:

Phase margin = 45

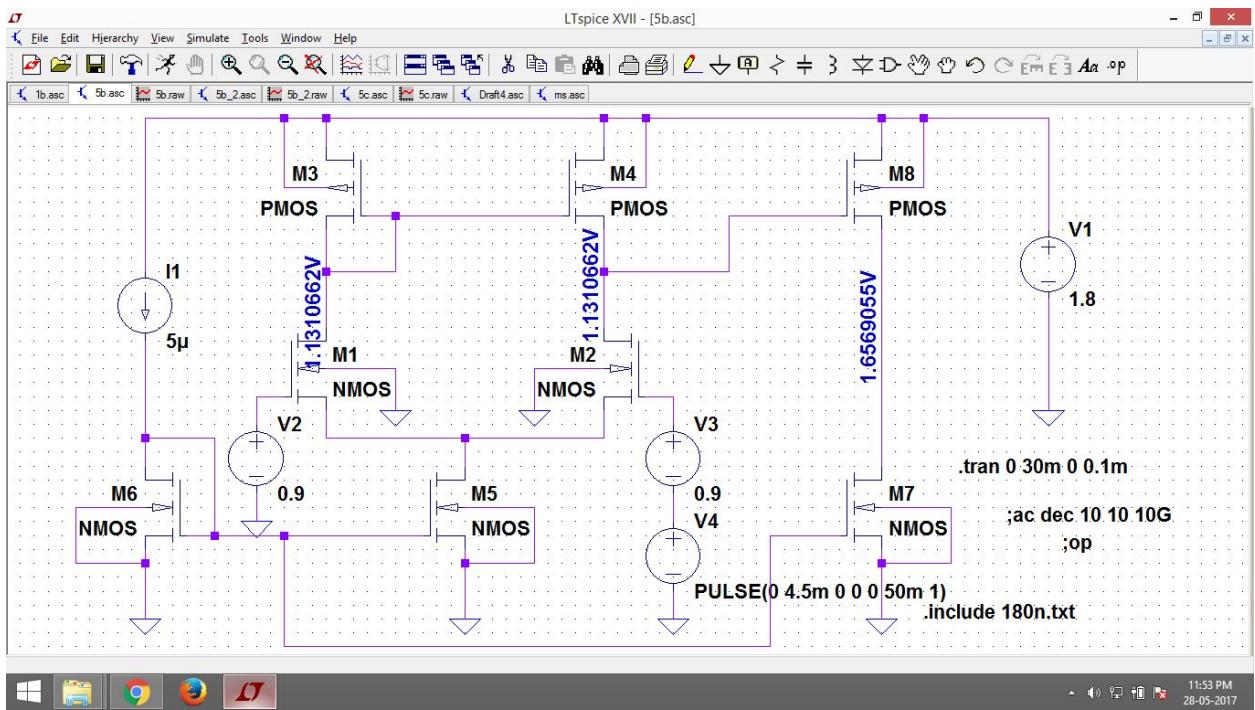


**Bandwidth: 4.2kHz**

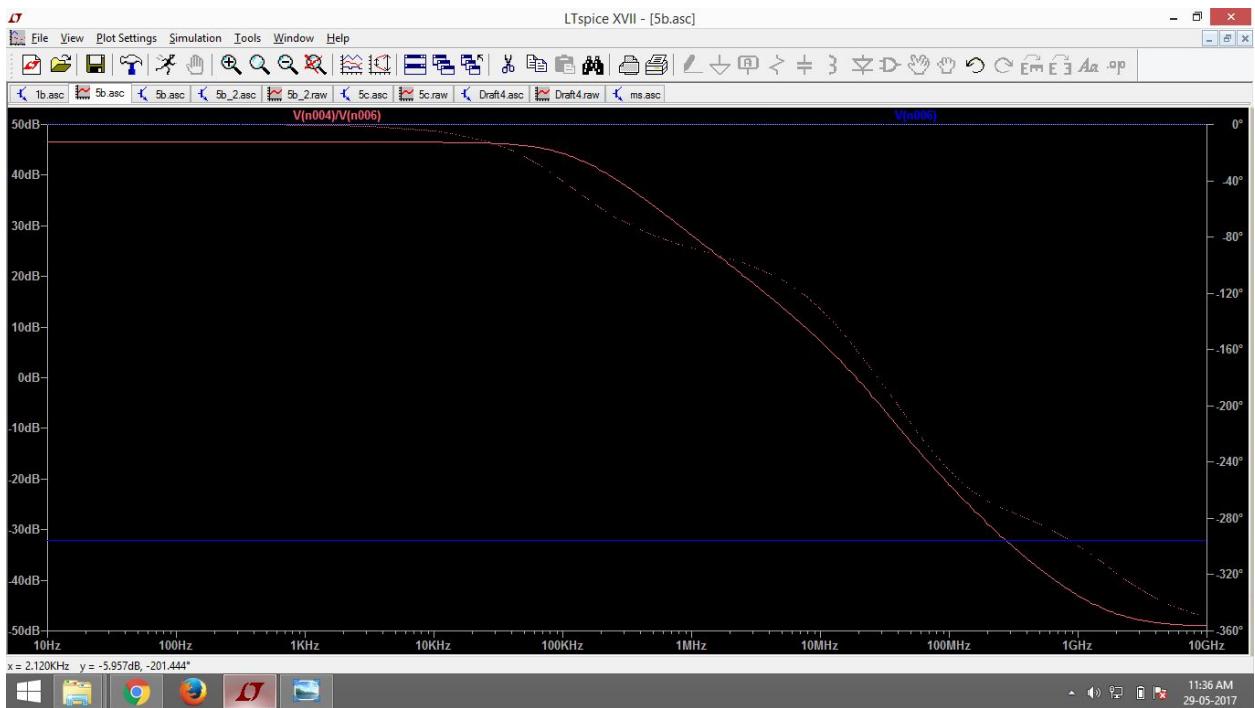


**Two stage op-amp with high resistance feedback**

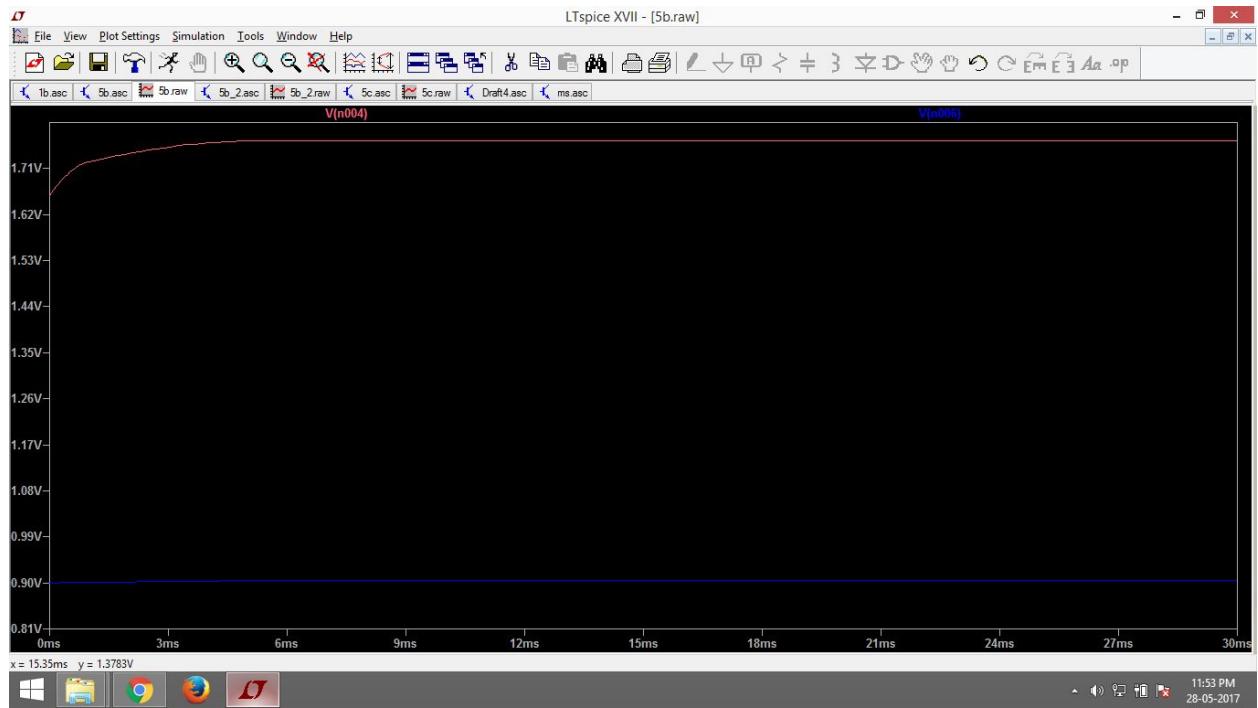
## N-Mos Comparator:



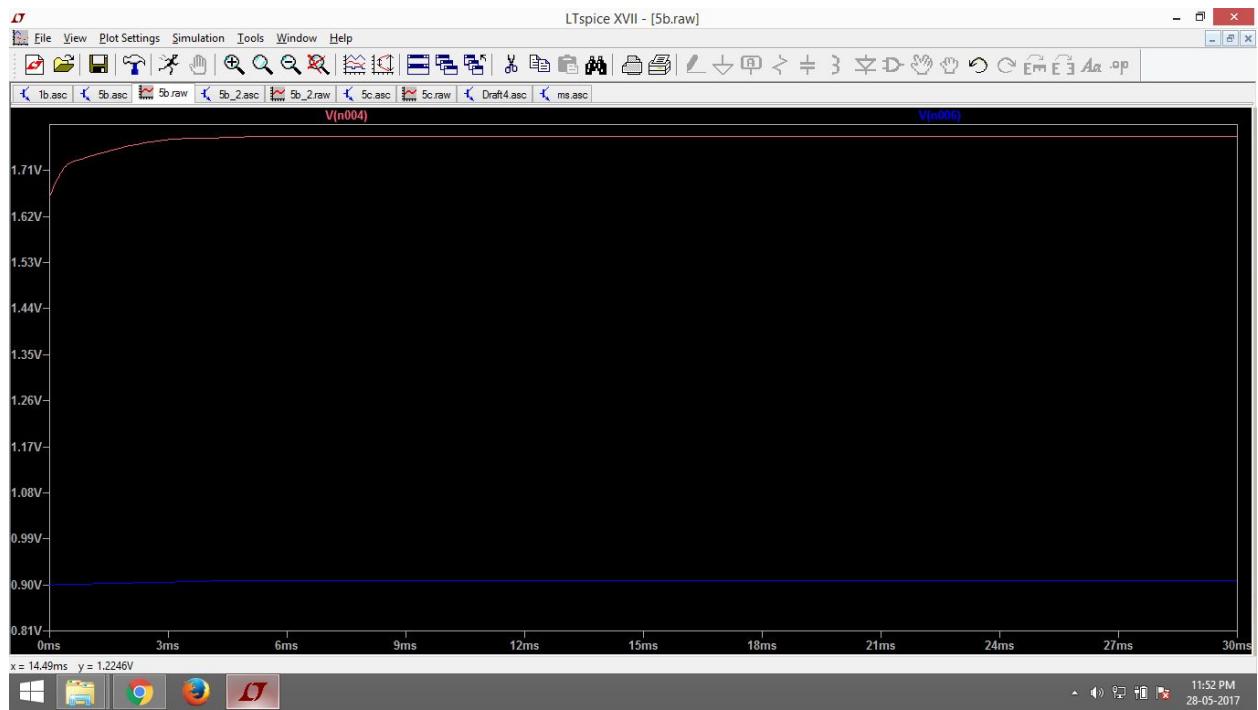
## Frequency Response:



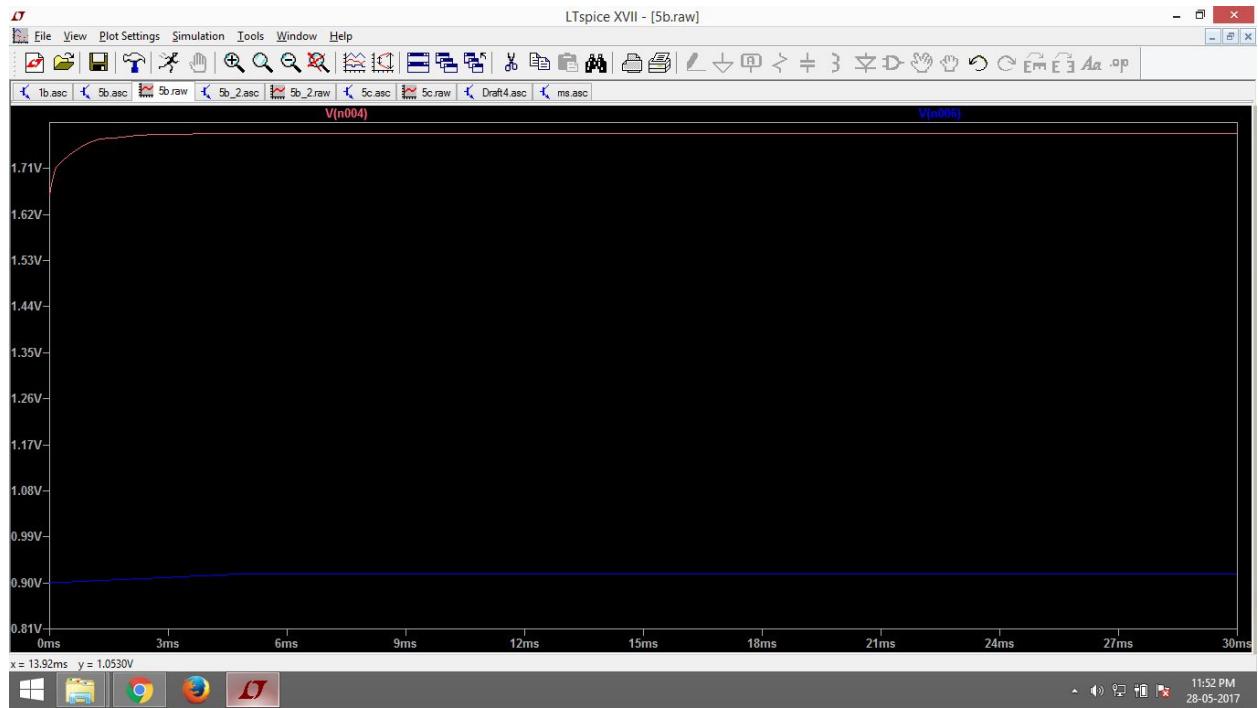
$V_{dd}/2 + V_{dd}/400:$



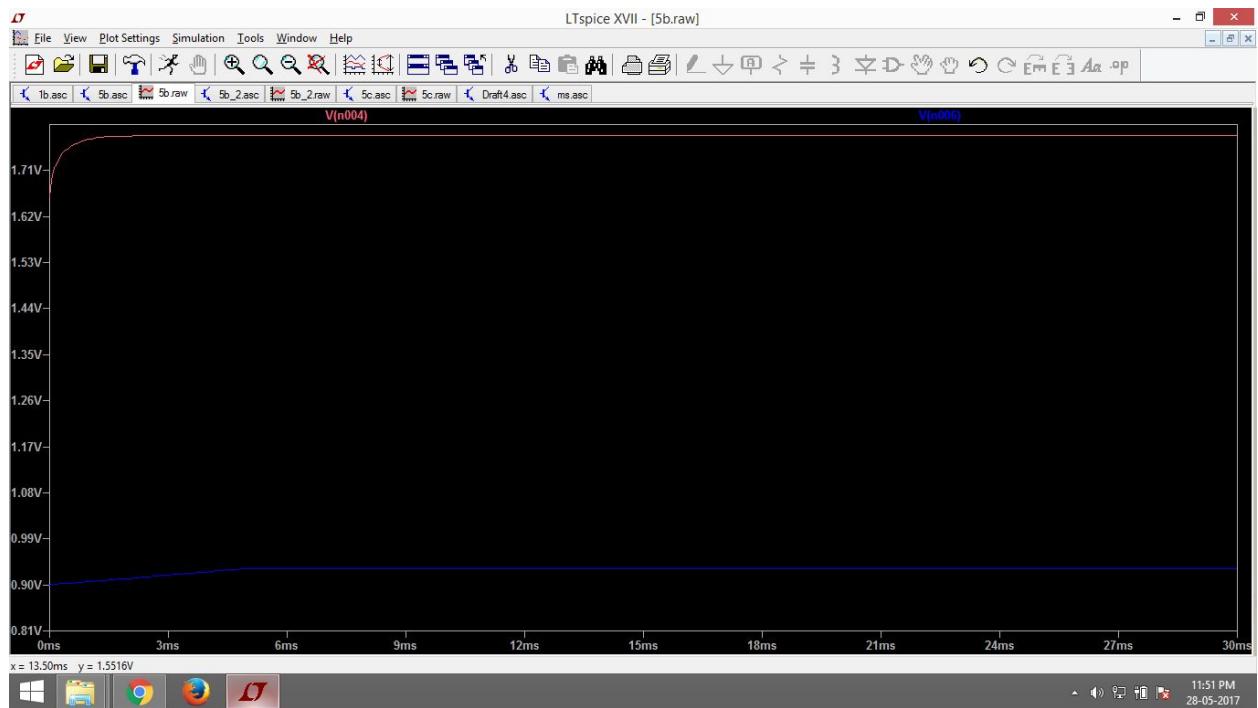
$V_{dd}/2 + V_{dd}/200:$



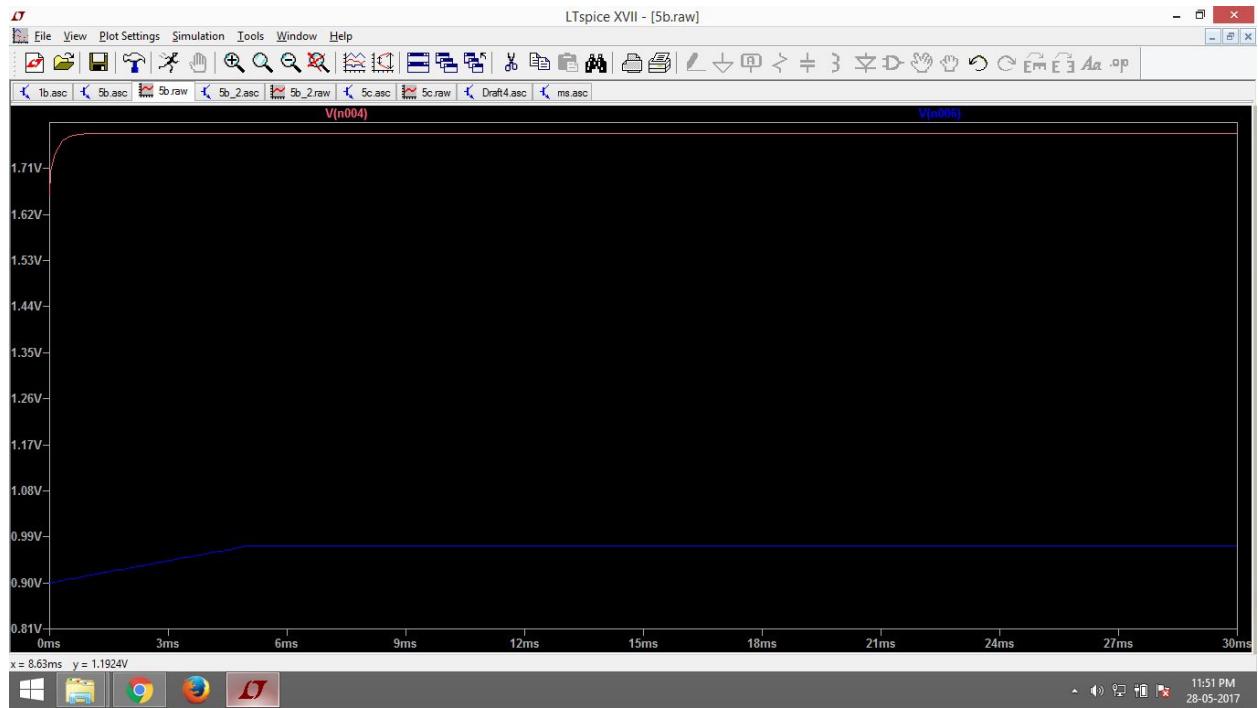
$V_{dd}/2 + V_{dd}/100:$



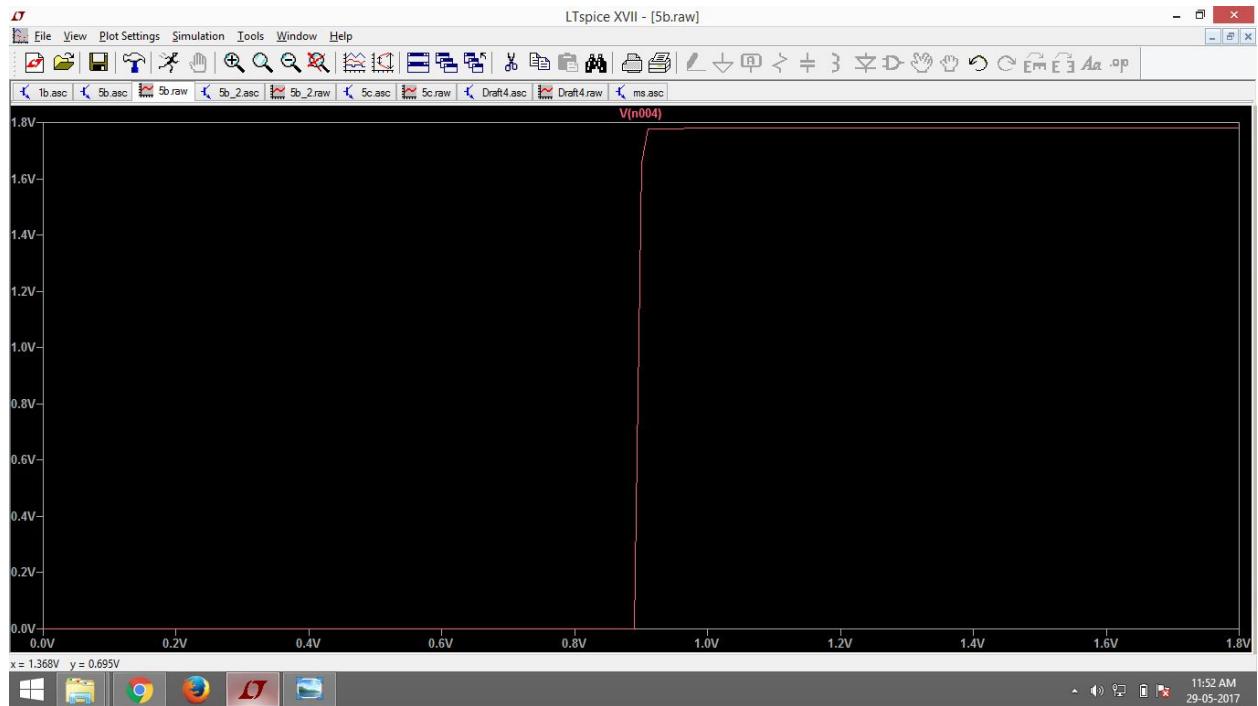
$V_{dd}/2 + V_{dd}/50:$



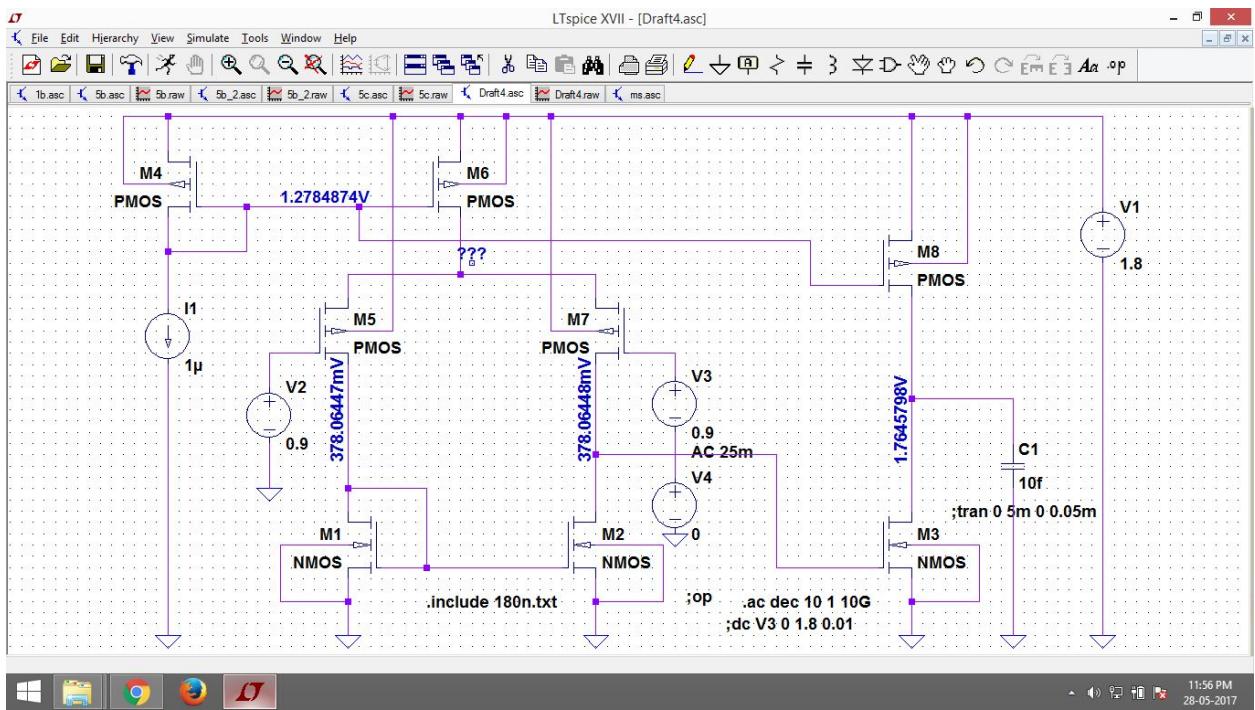
$V_{dd}/2 + V_{dd}/25:$



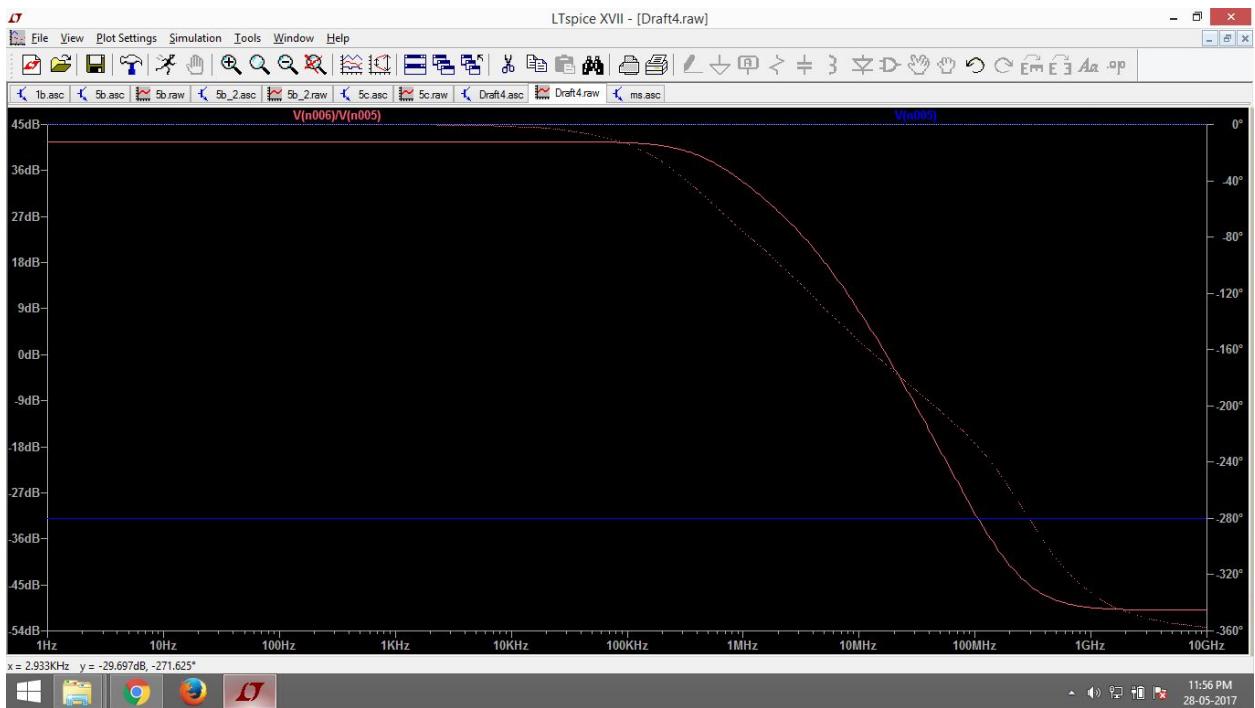
Dc sweep at input branch:



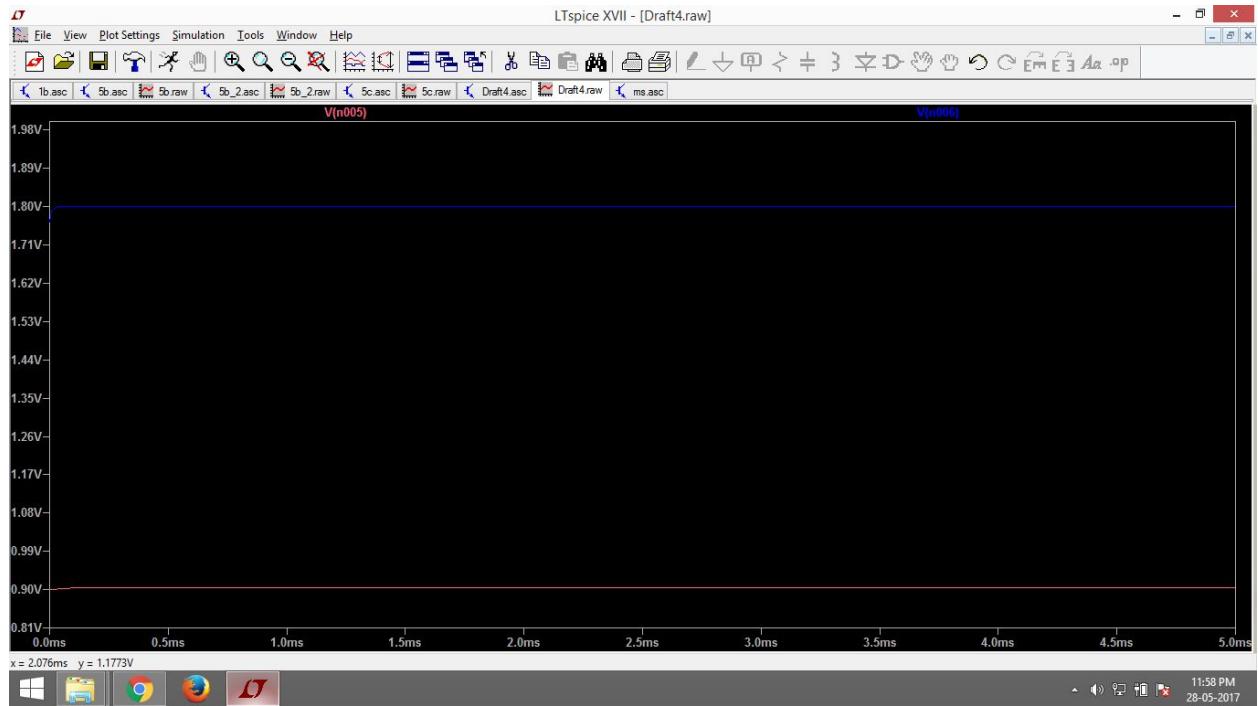
## P-mos Comparator:



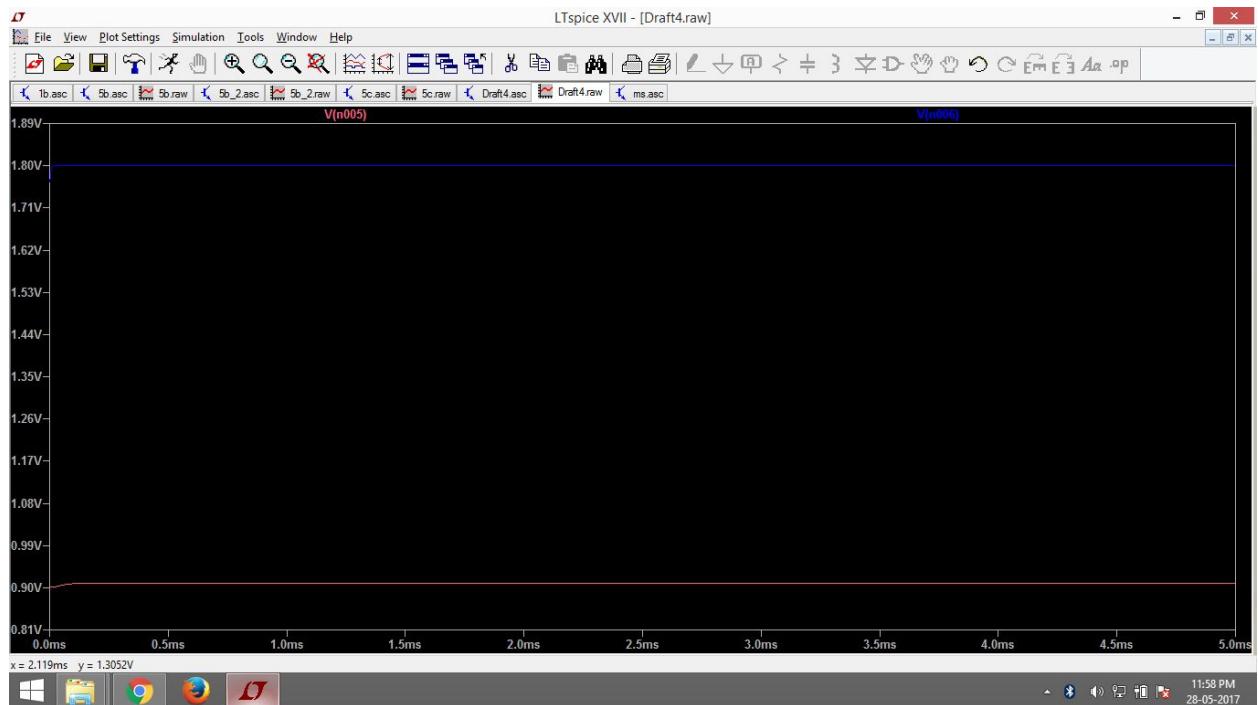
## Frequency Response:



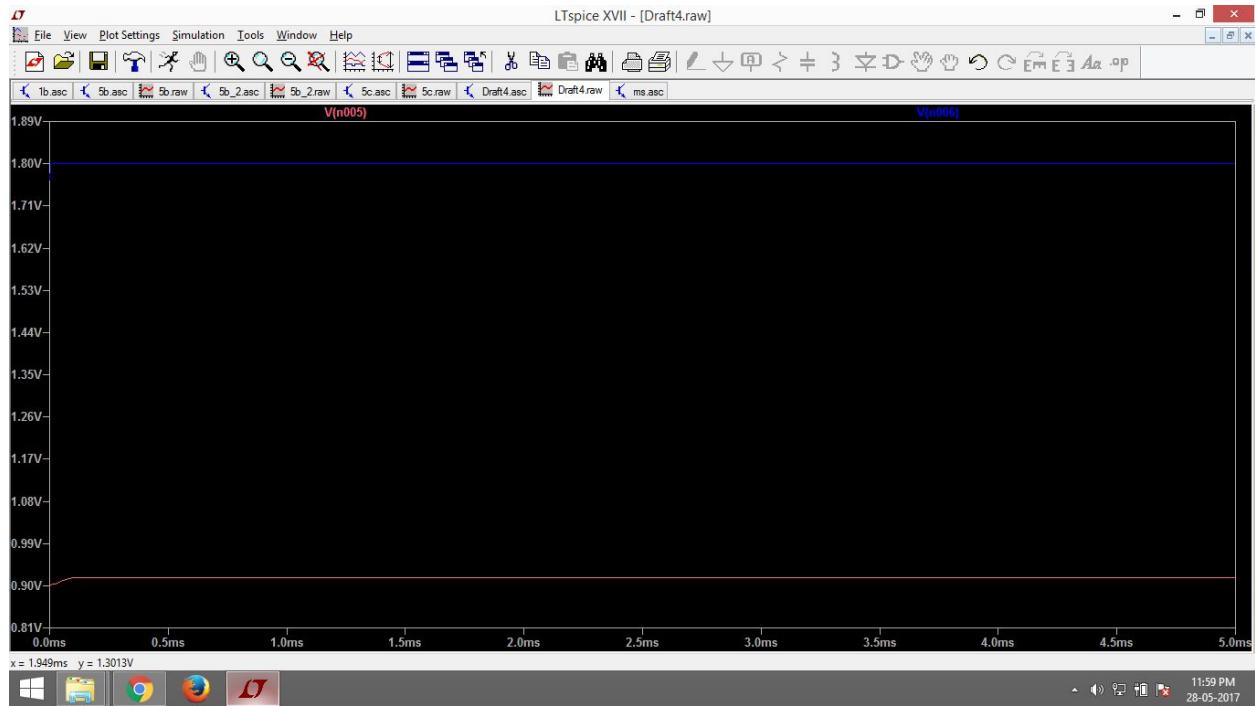
$V_{dd}/2 + V_{dd}/400:$



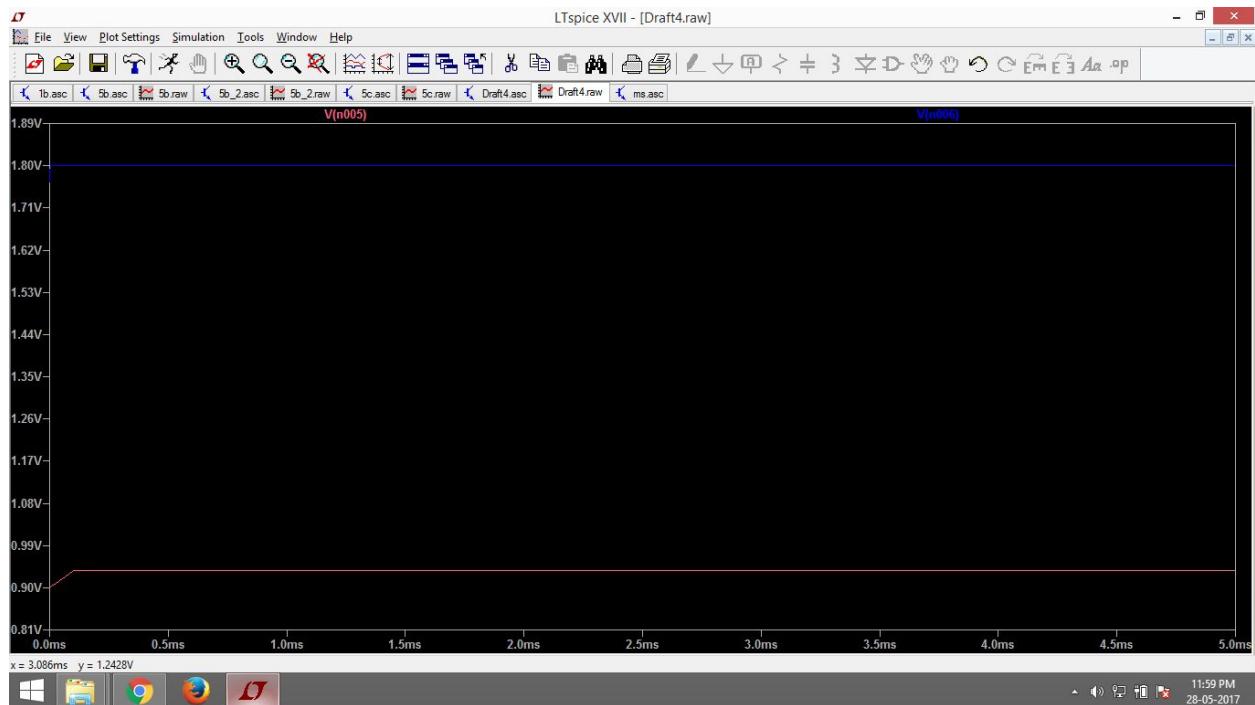
$V_{dd}/2 + V_{dd}/200:$



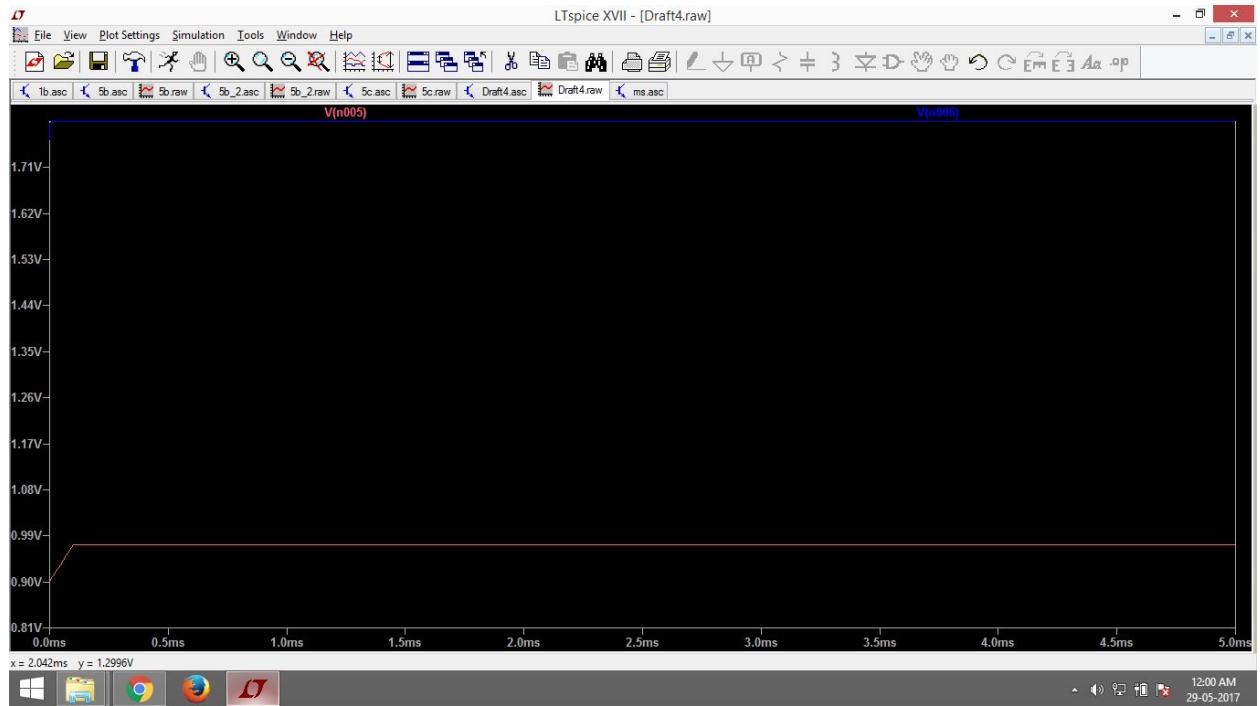
$V_{dd}/2 + V_{dd}/100:$



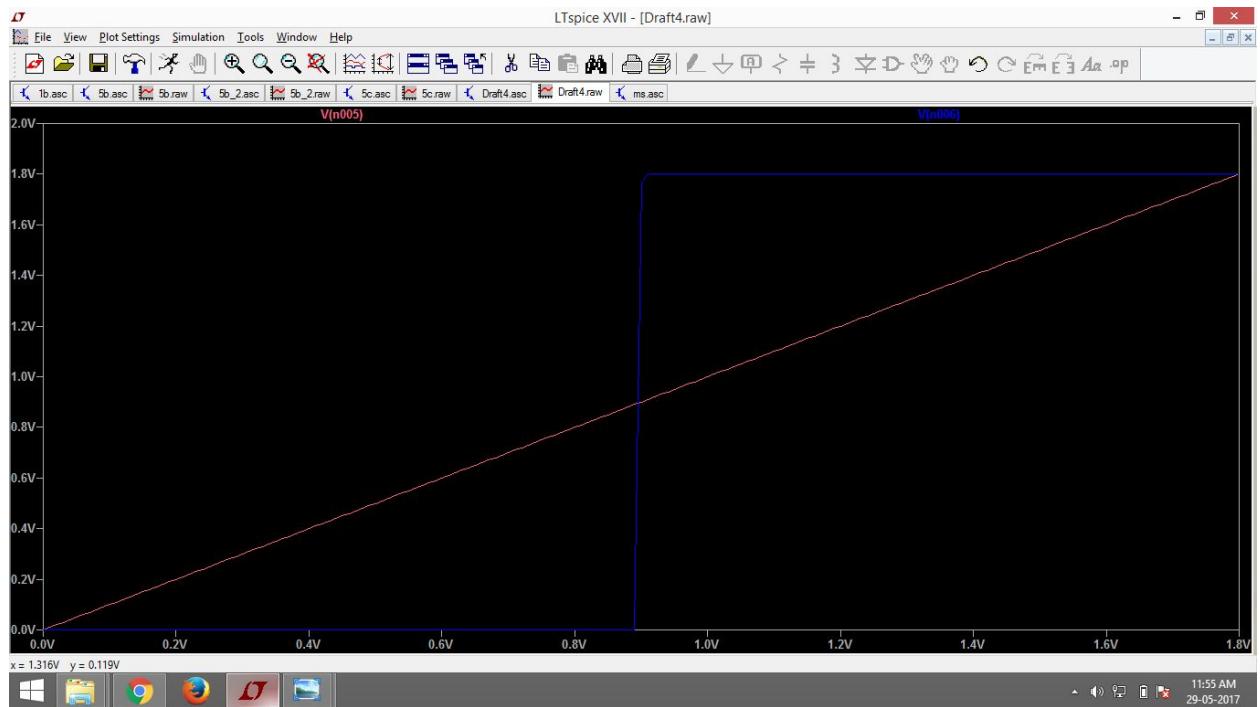
$V_{dd}/2 + V_{dd}/50:$



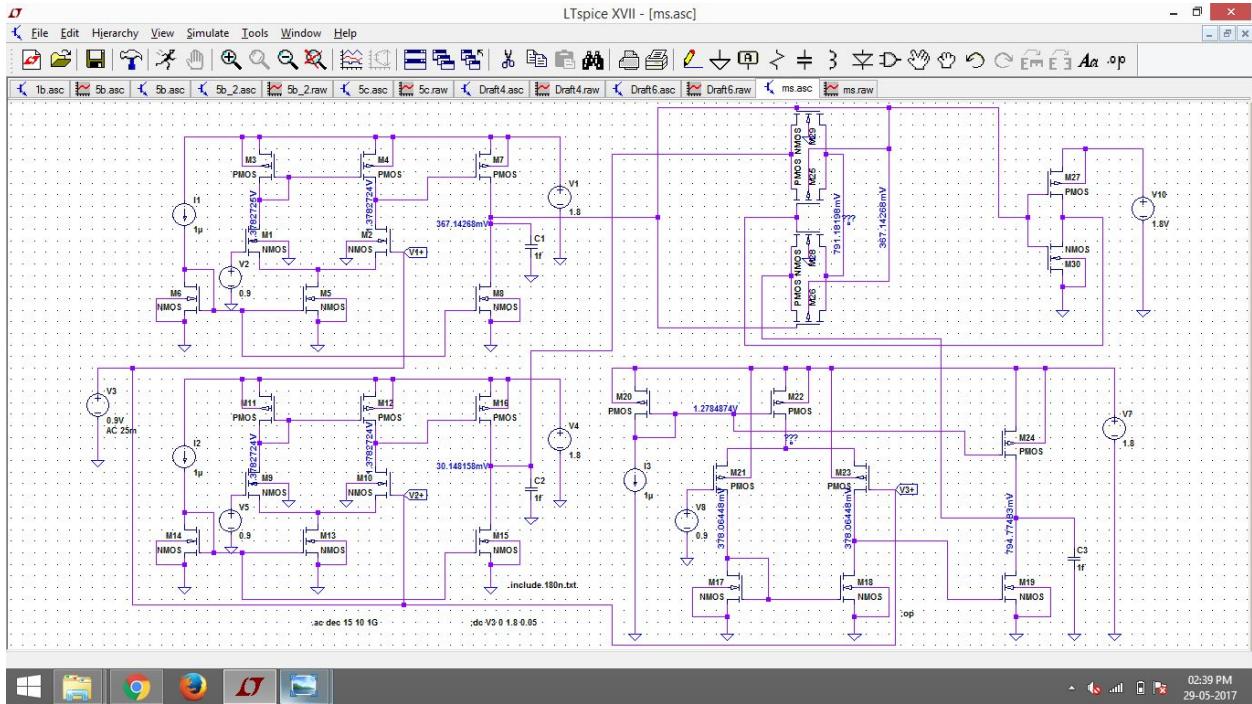
$V_{dd}/2 + V_{dd}/25:$



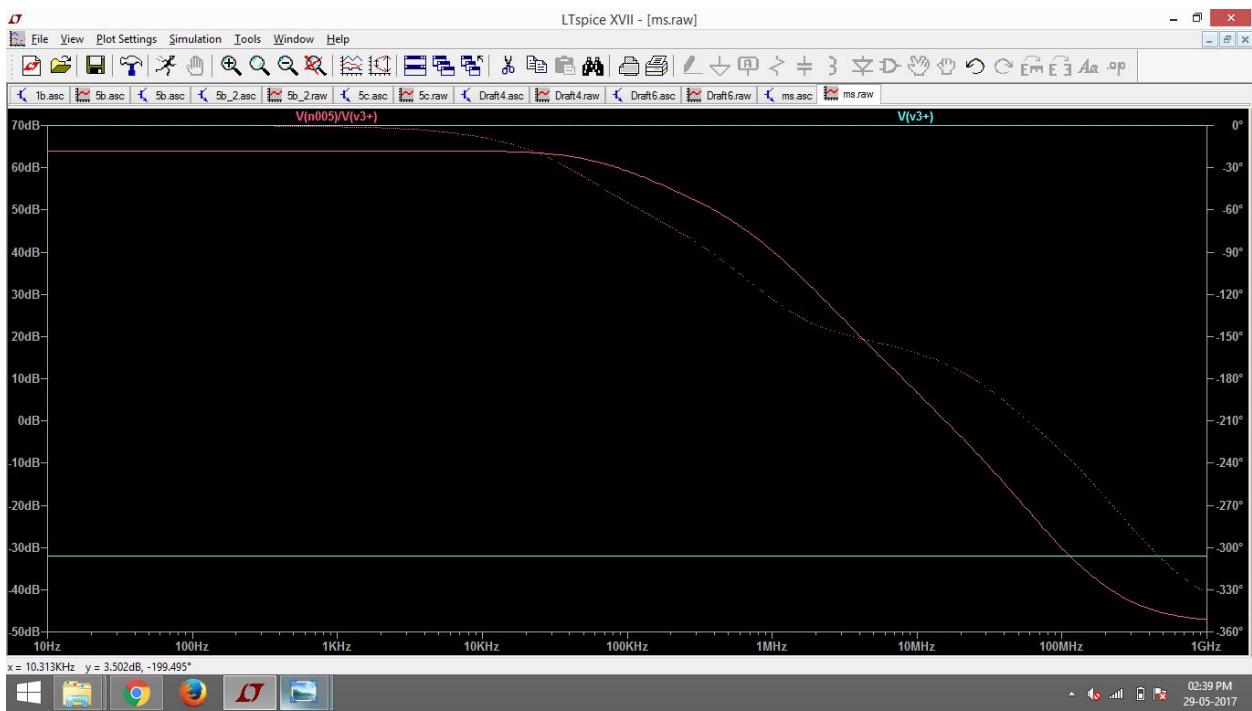
Dc Sweep at input:



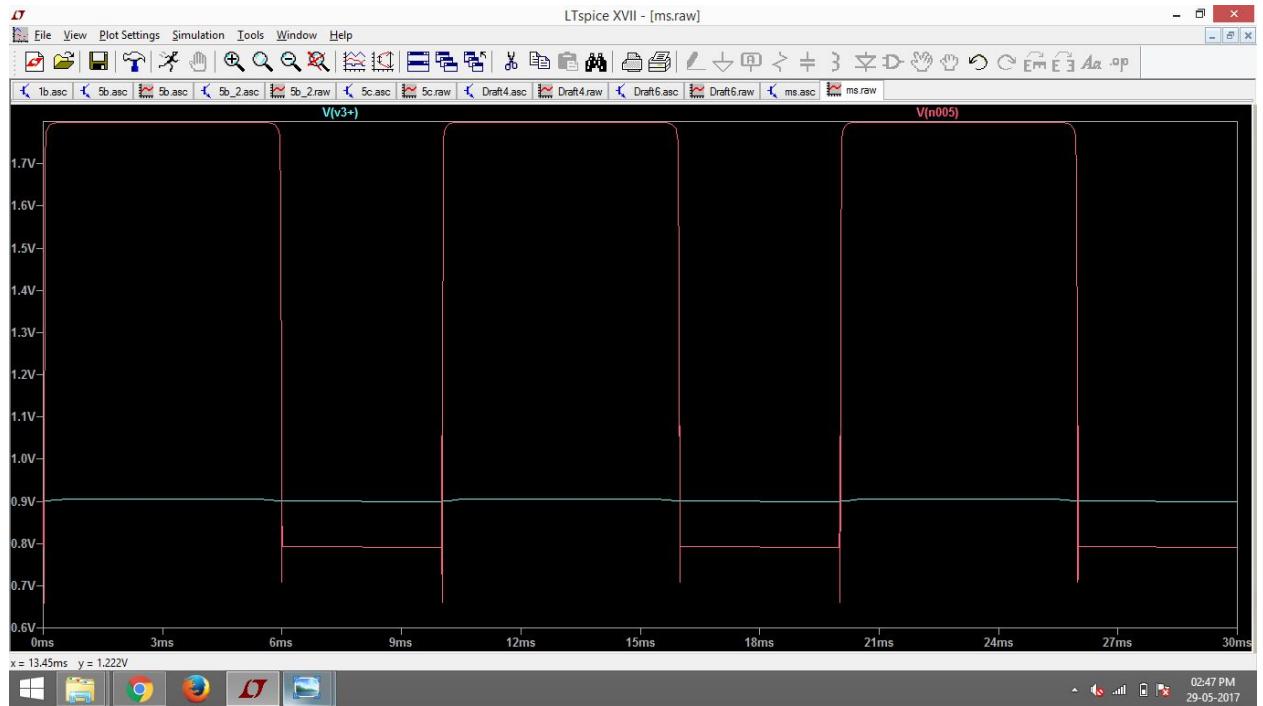
## Comparator:



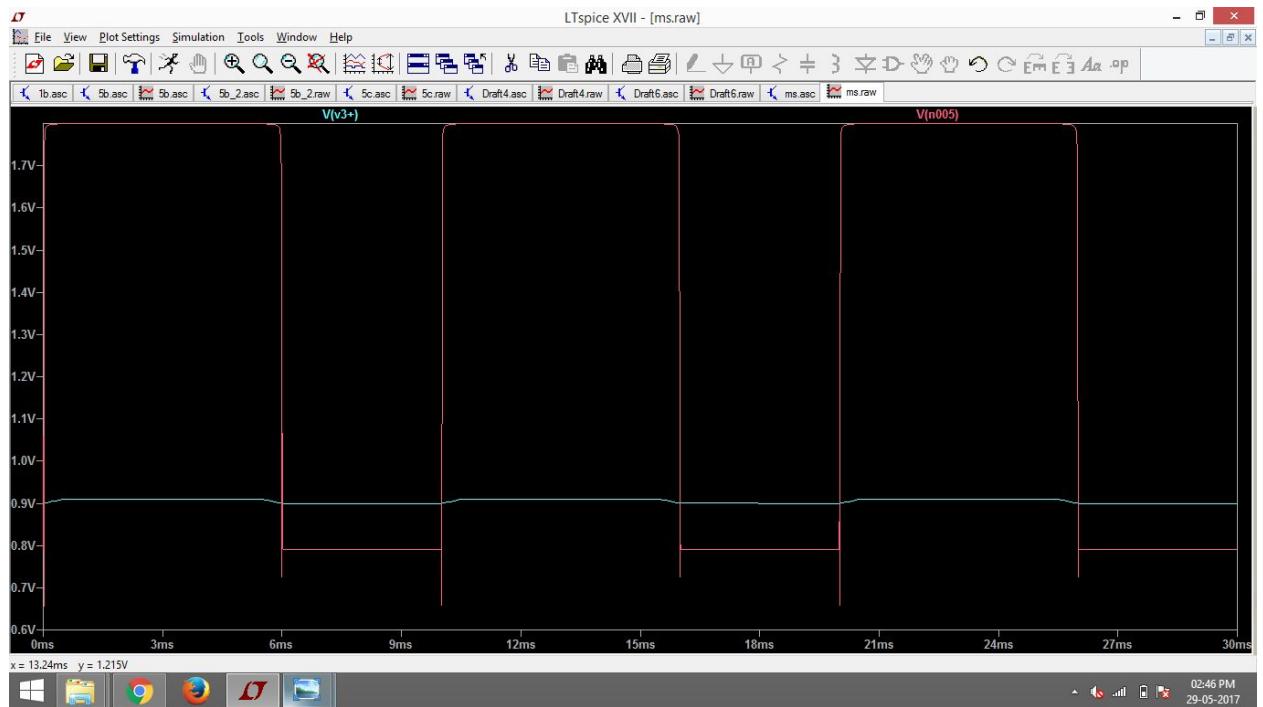
## Frequency response:



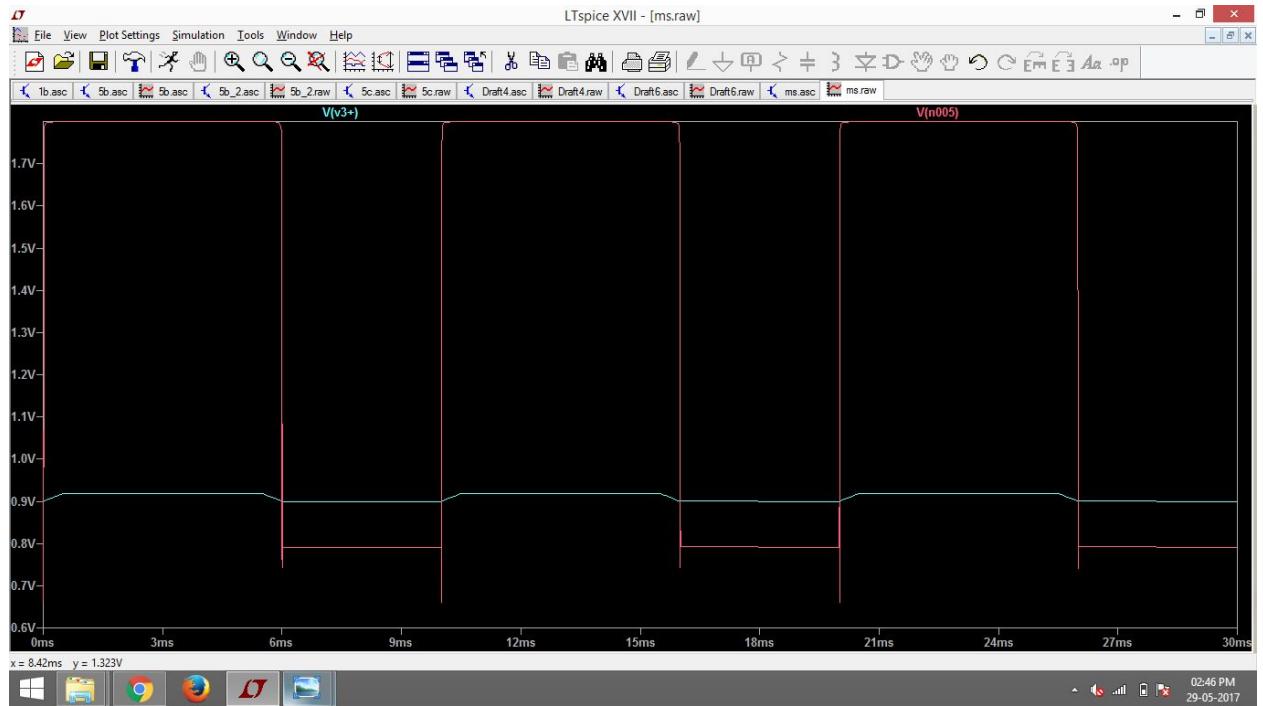
$V_{dd}/2 + V_{dd}/400:$



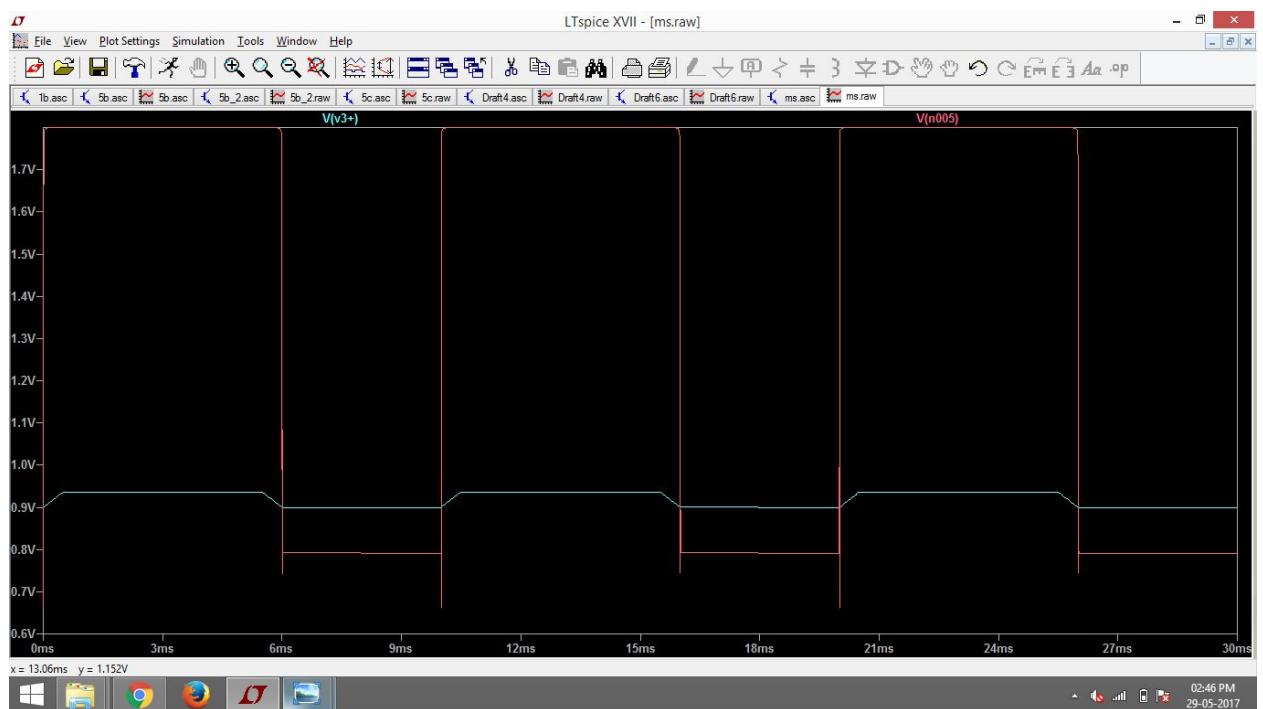
$V_{dd}/2 + V_{dd}/200:$



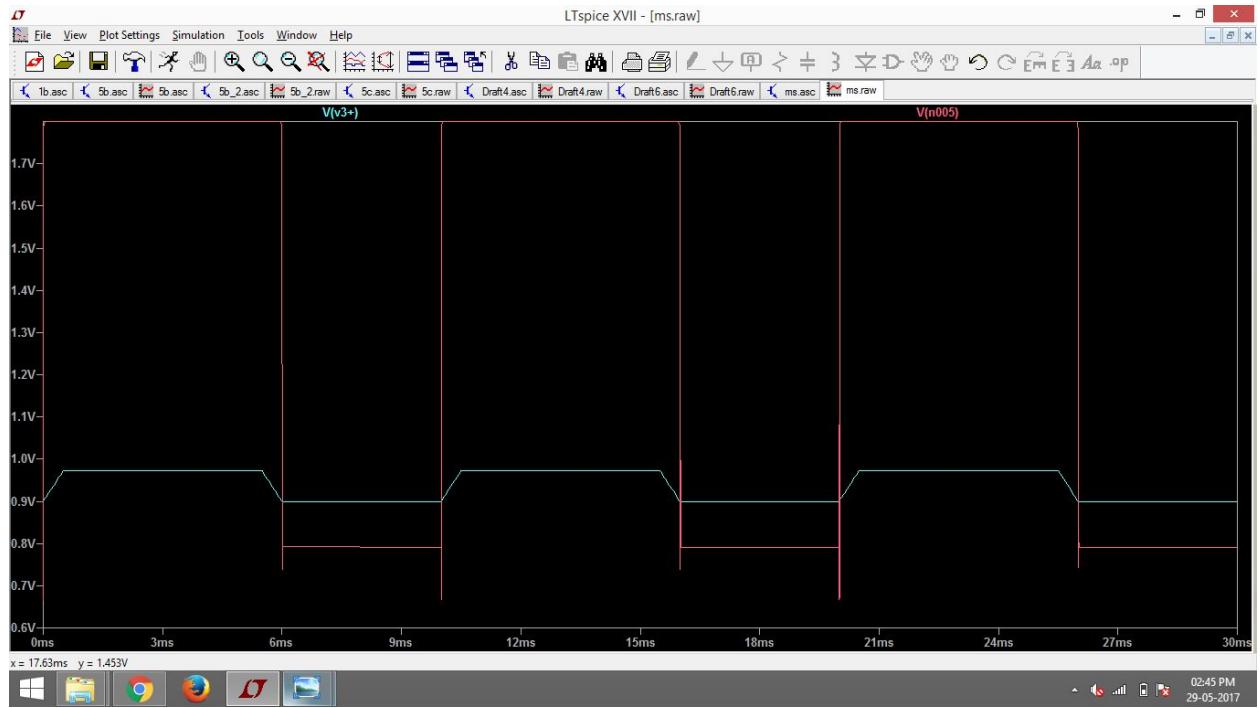
$V_{dd}/2 + V_{dd}/100:$



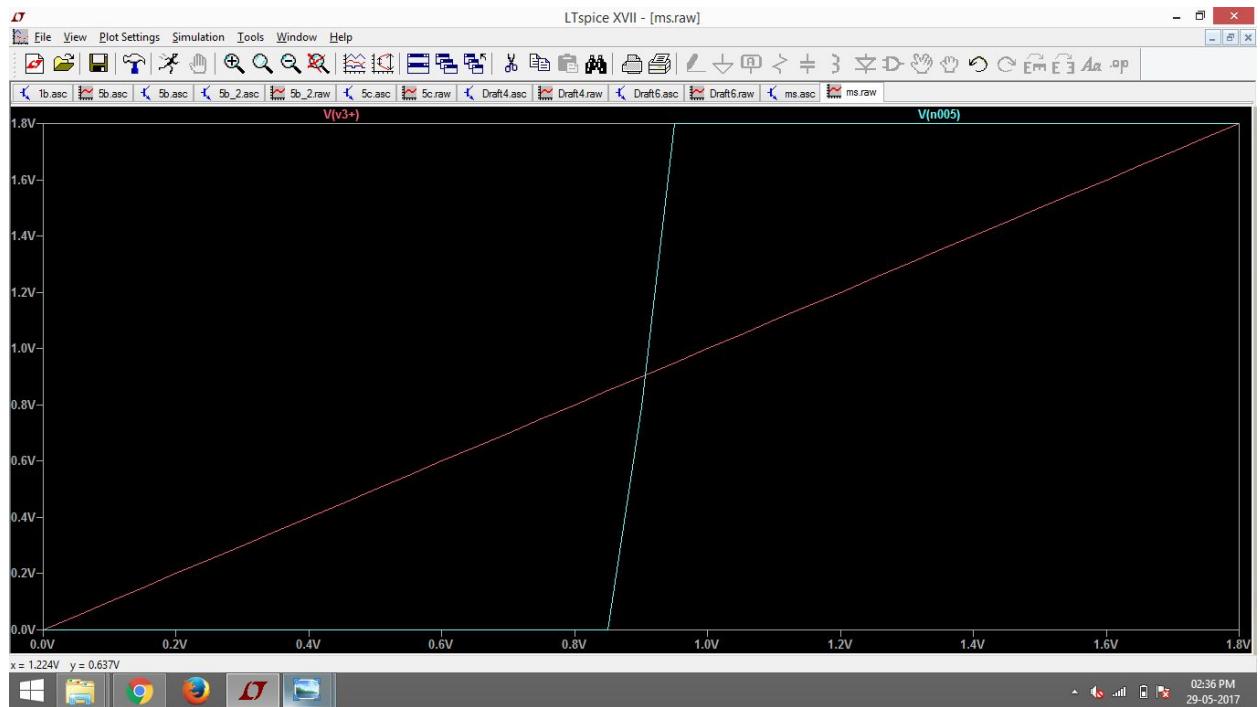
$V_{dd}/2 + V_{dd}/50:$



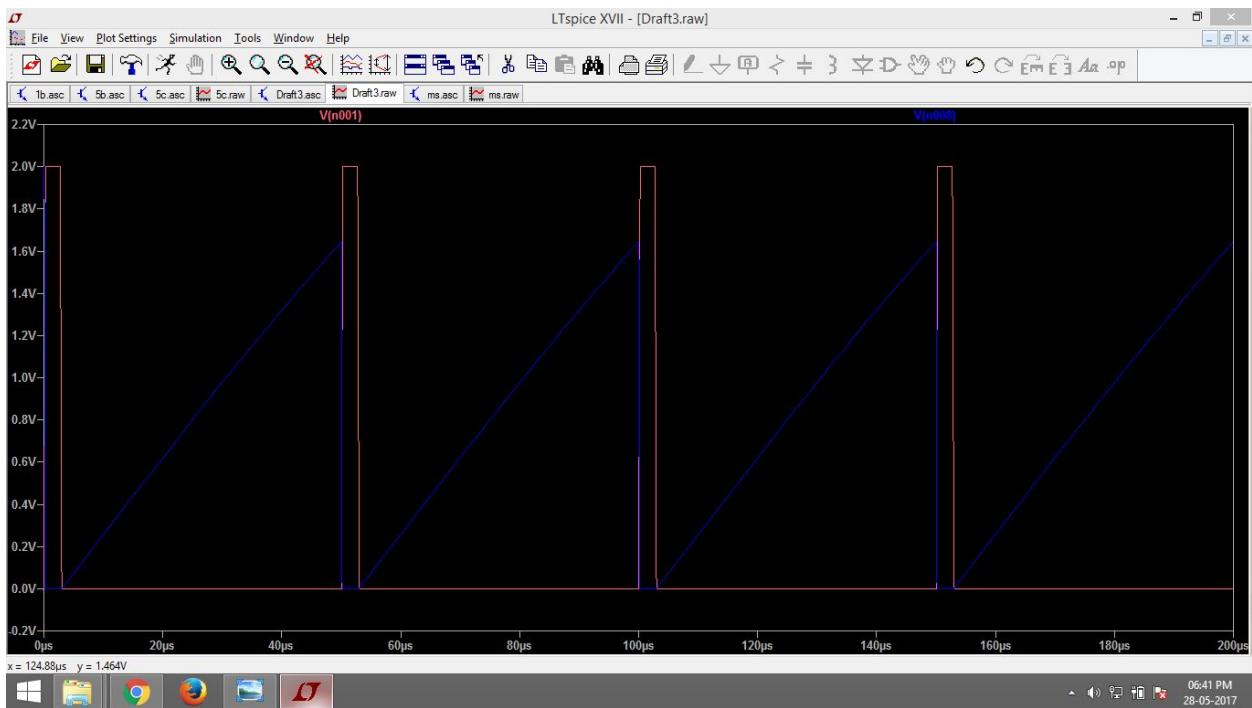
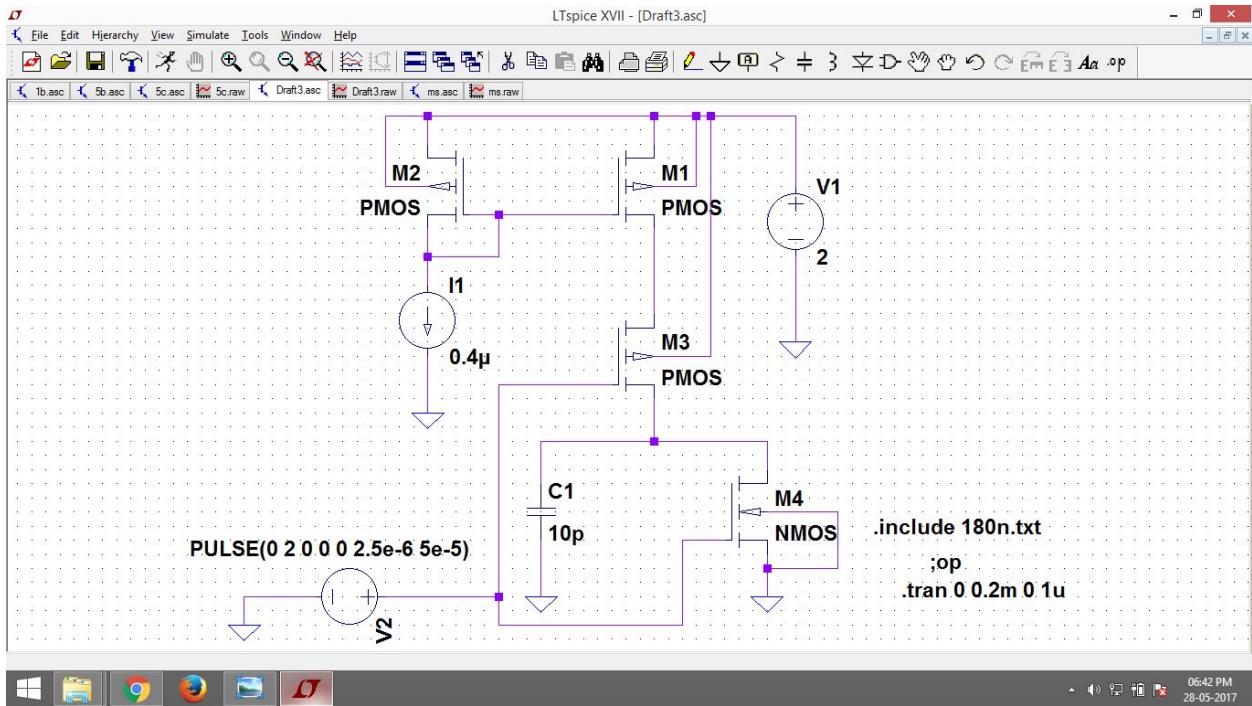
$V_{dd}/2 + V_{dd}/25:$



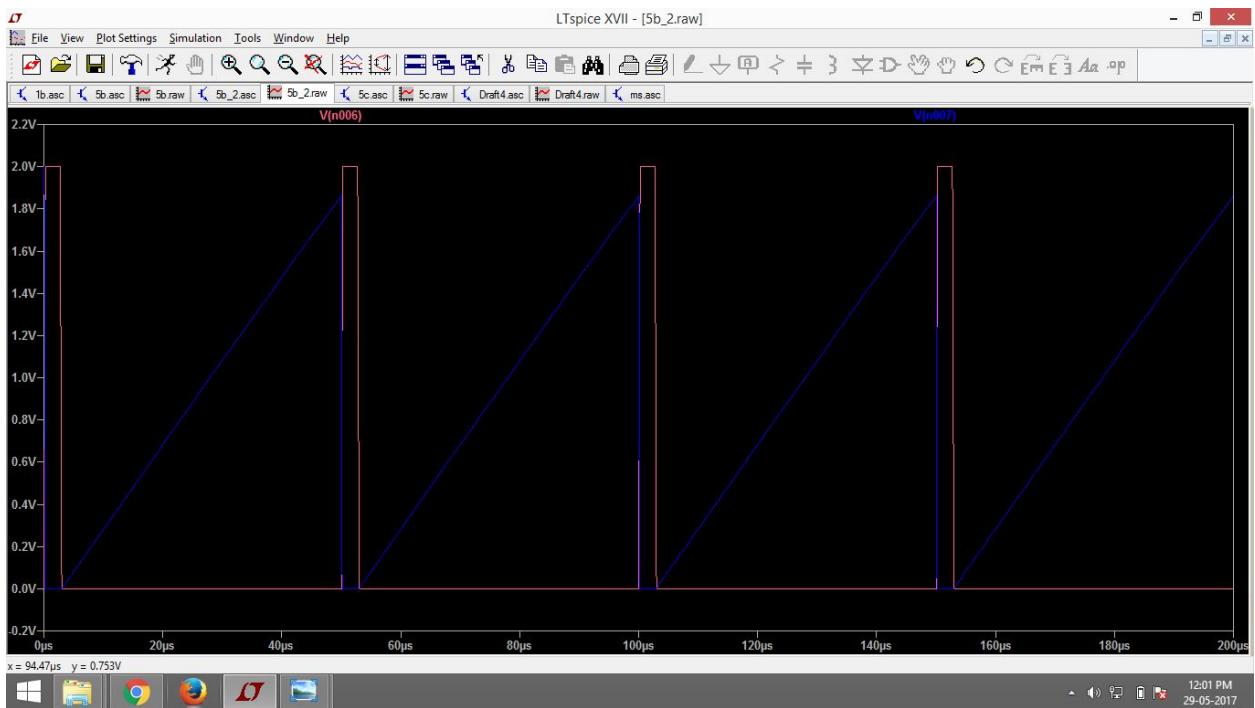
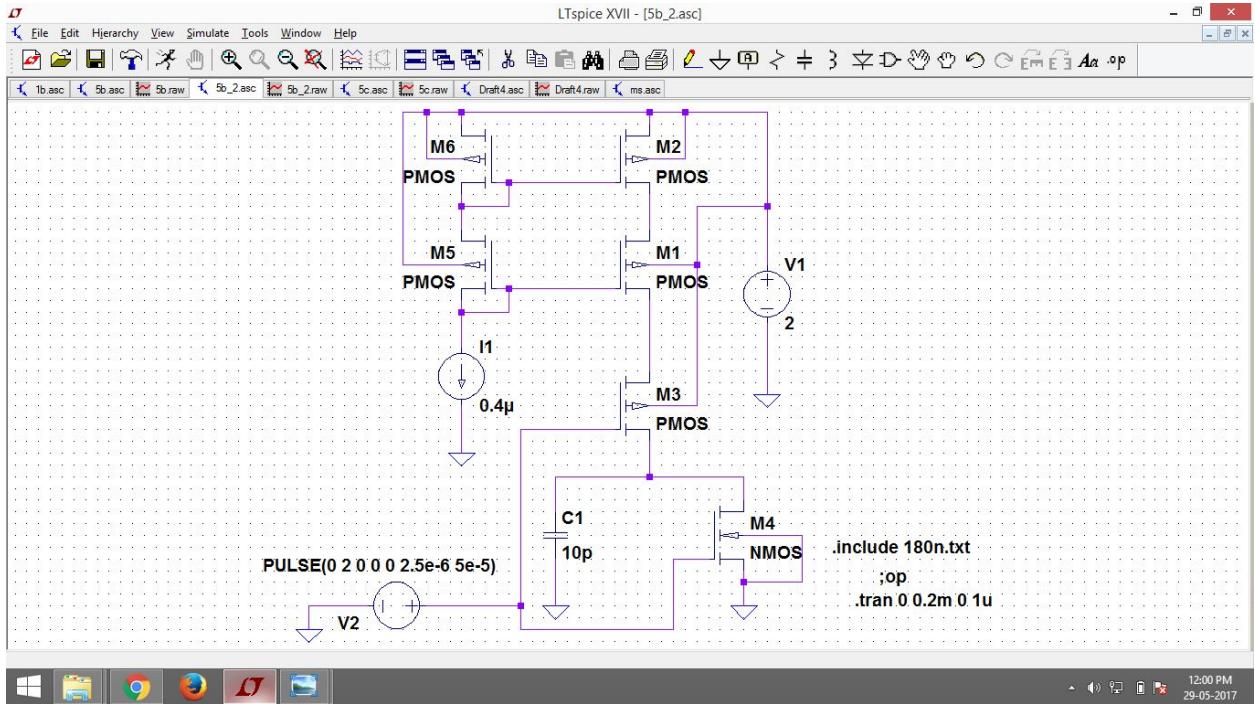
Dc Sweep at input:



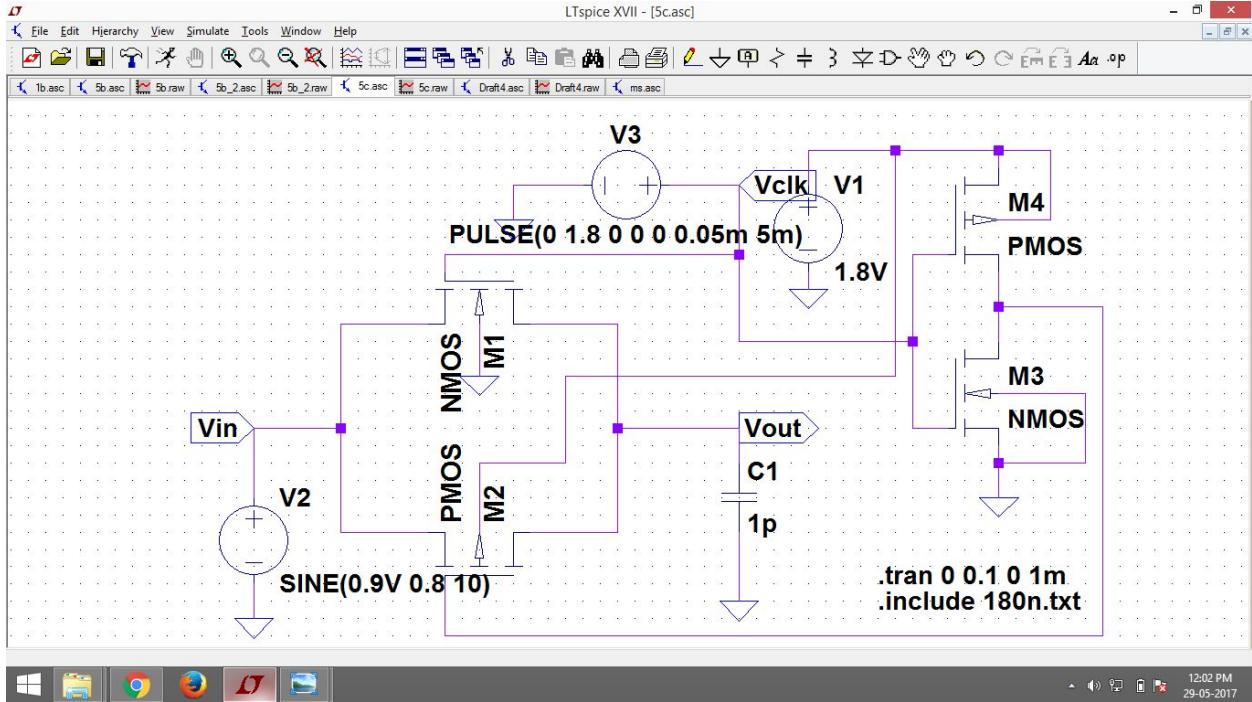
## Ramp Circuit(Biased with simple current mirror):



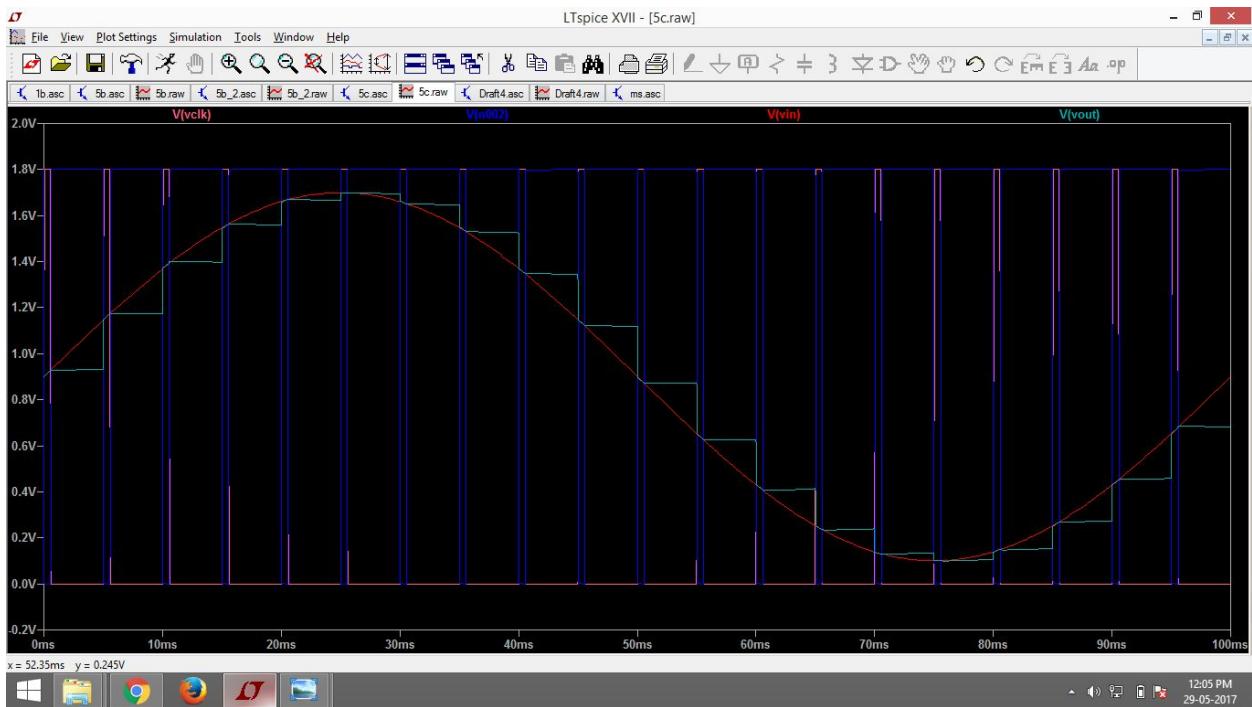
## Ramp Circuit(Biased with cascode mirror):



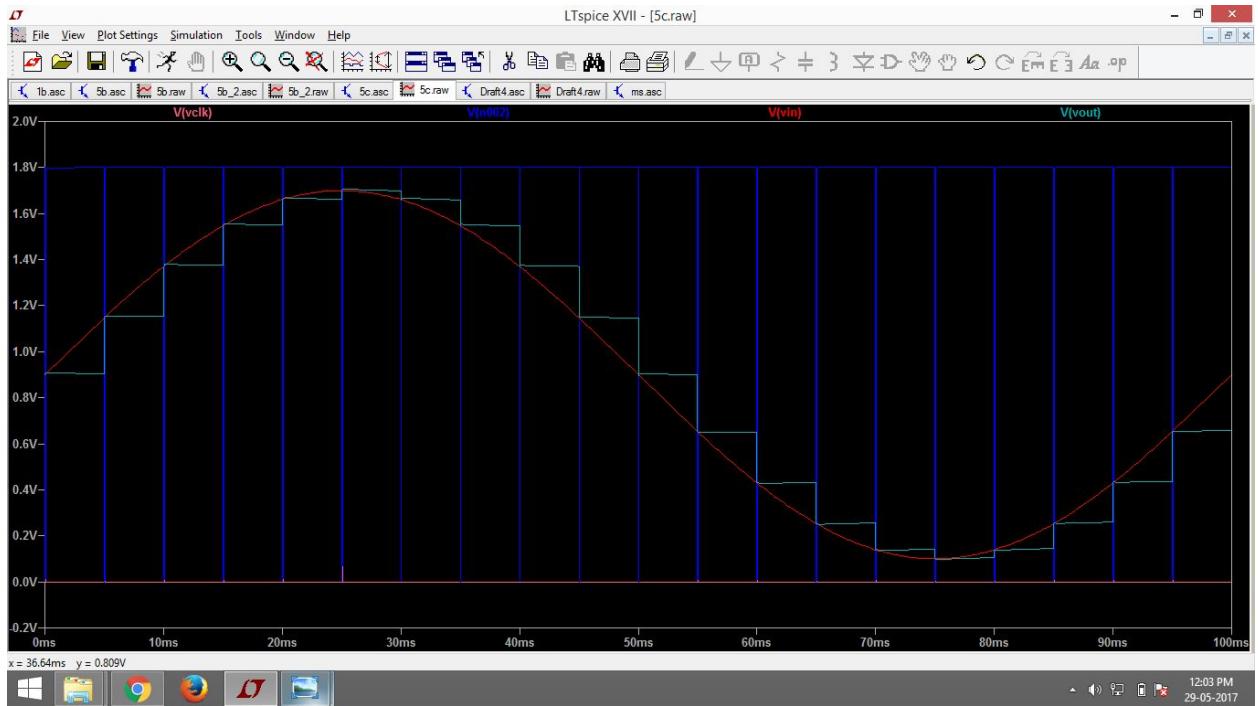
## Transmission Gate based sampling Circuit:



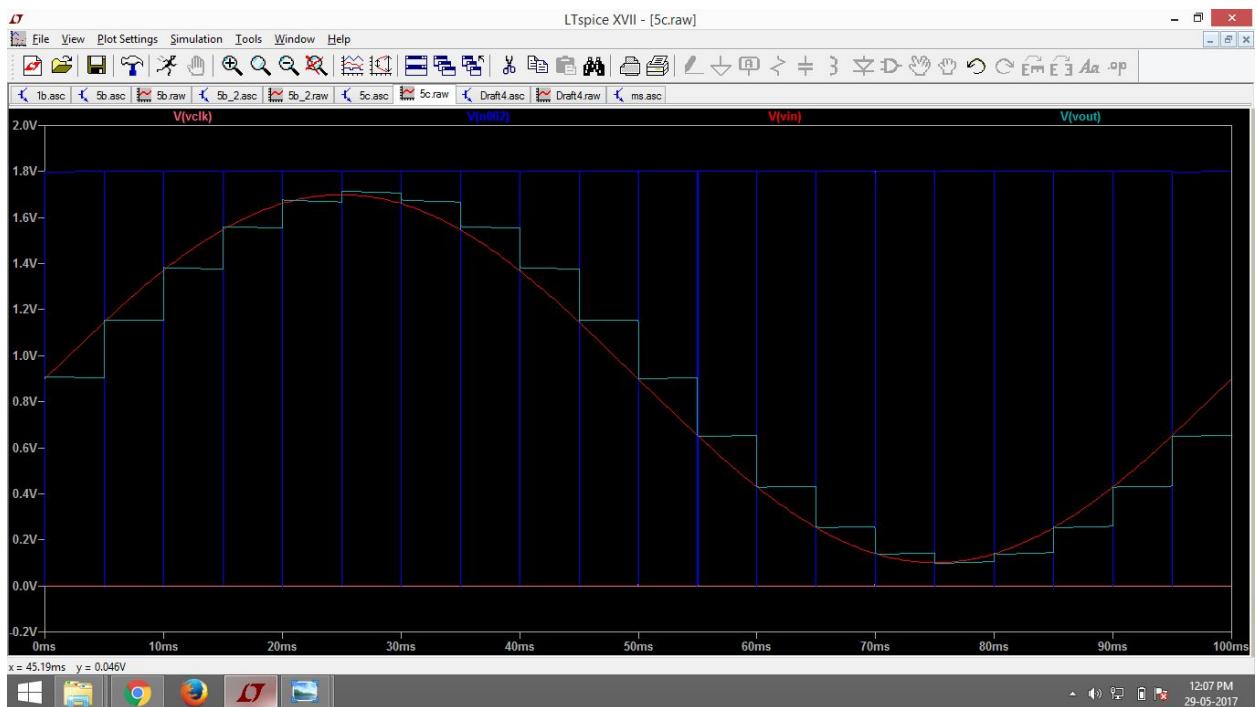
When duty cycle = 0.1:



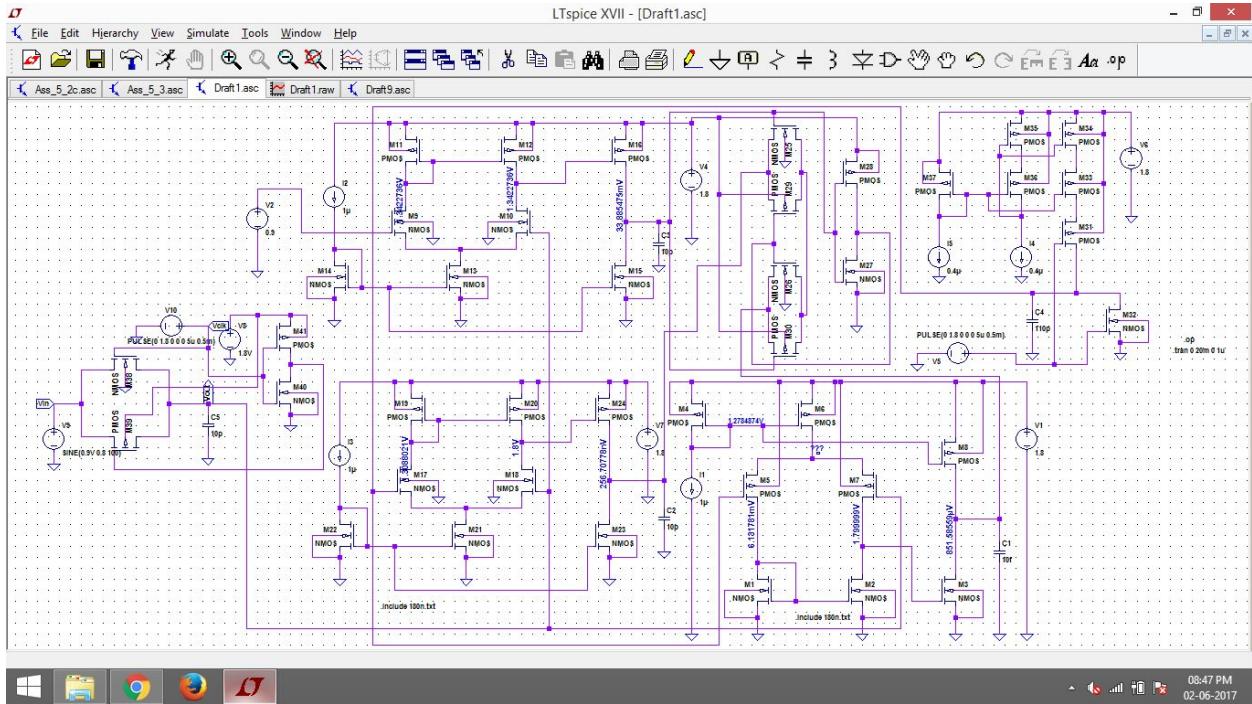
**When duty cycle = 0.01:**



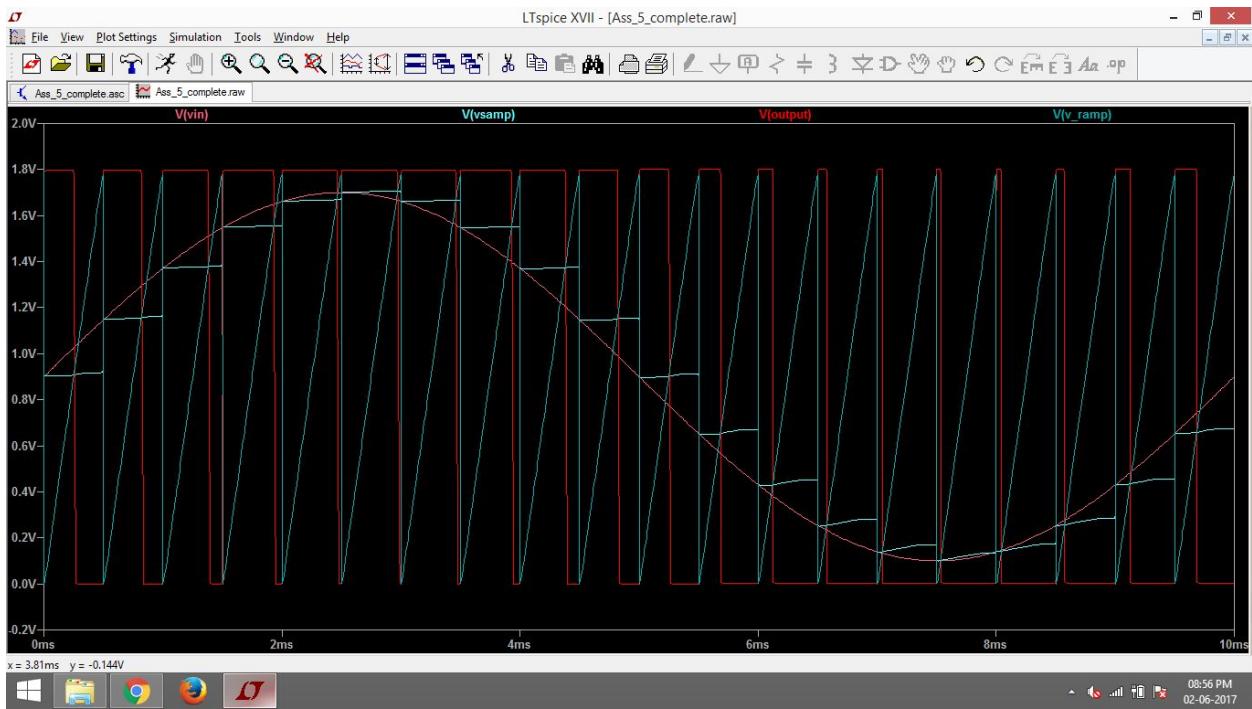
**When duty cycle = 0.001:**

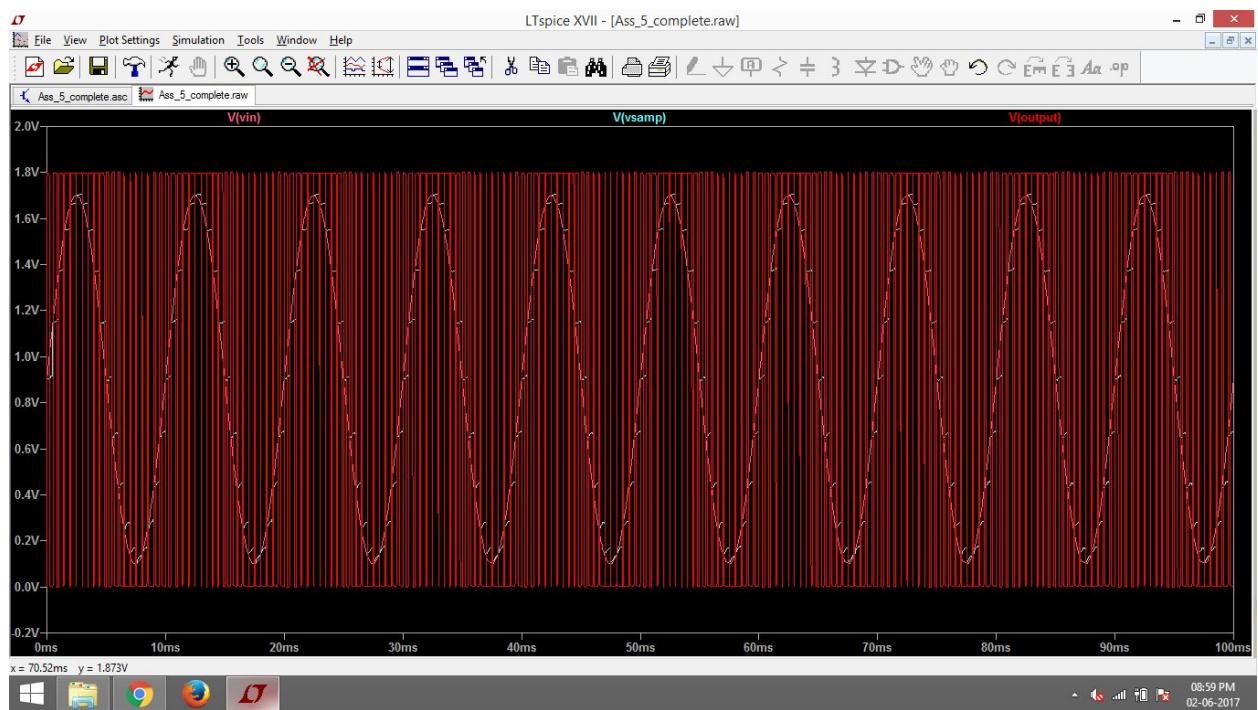
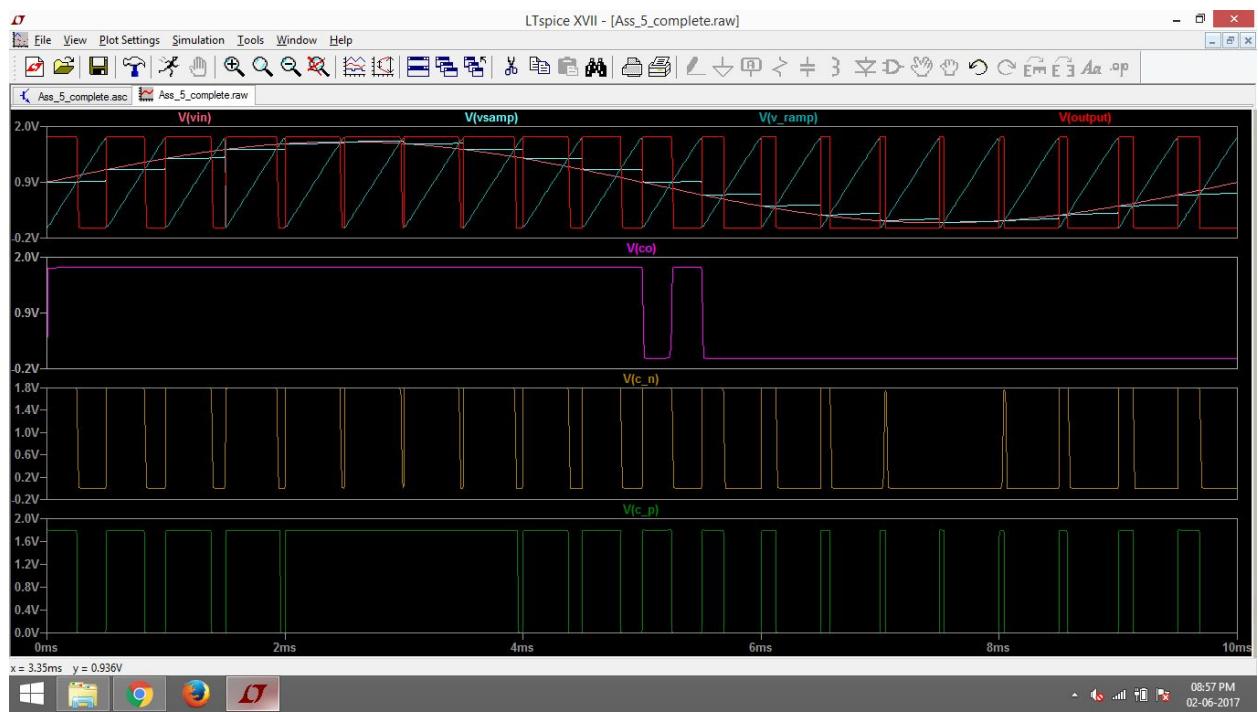


## Comparator with ramp input and sampled input:

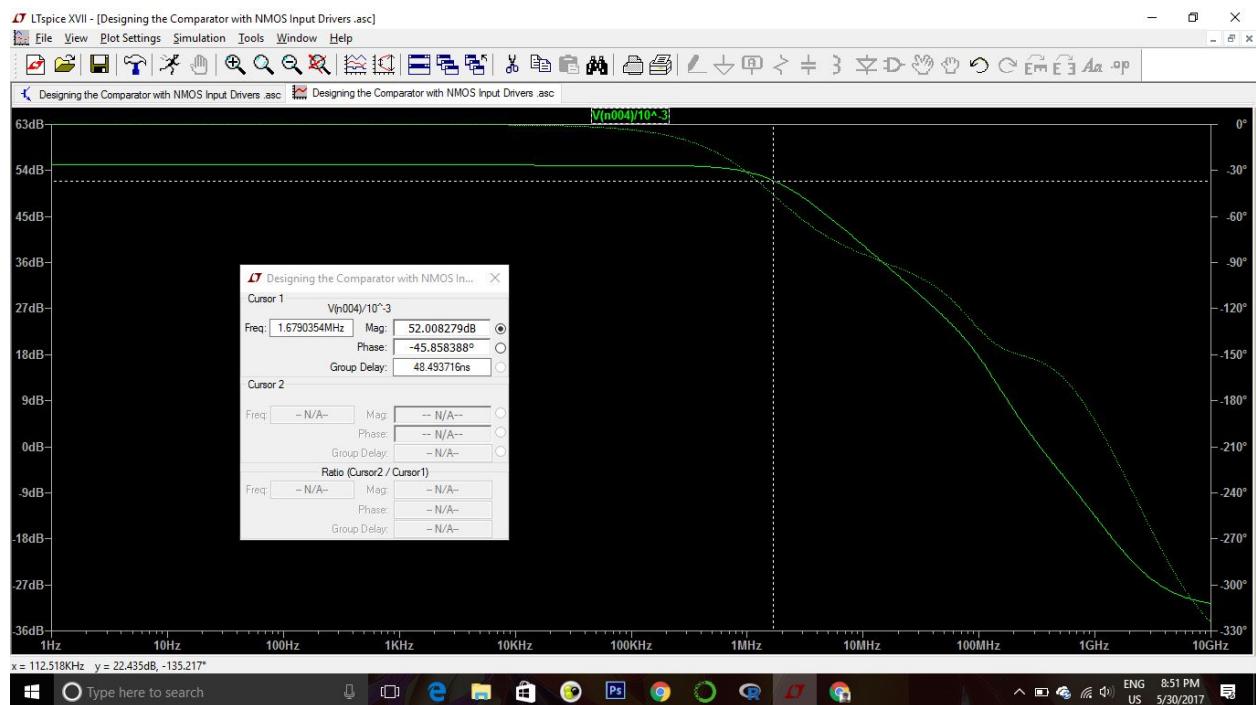
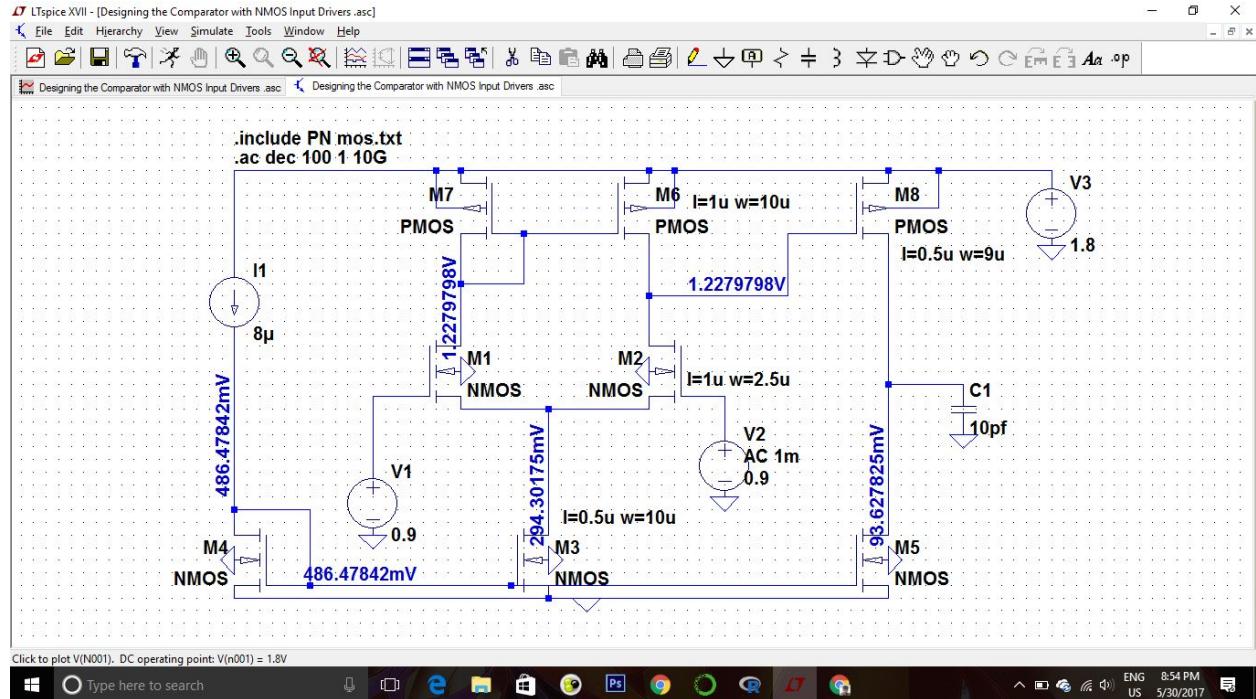


## Transient response:





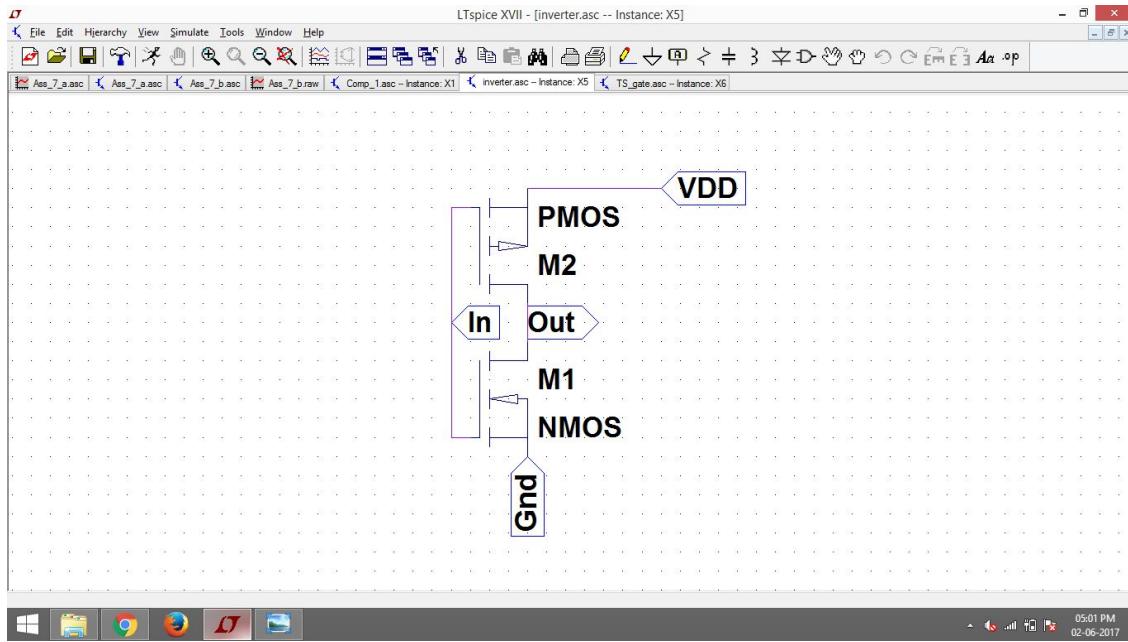
# OPEN LOOP GAIN 400 BANDWIDTH 1Mhz.



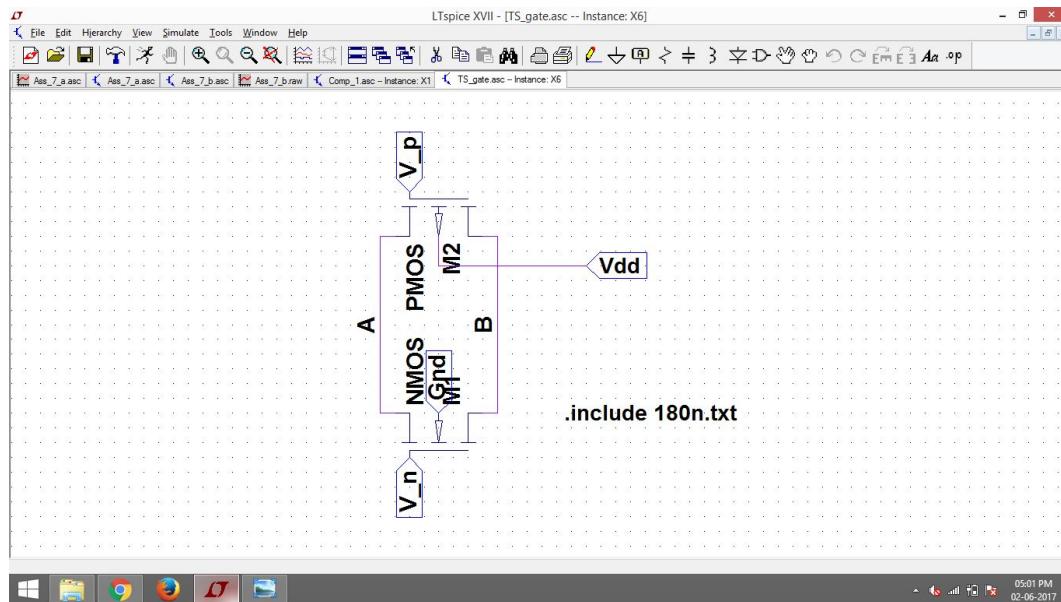
# Assignment 7:

Symbols used:

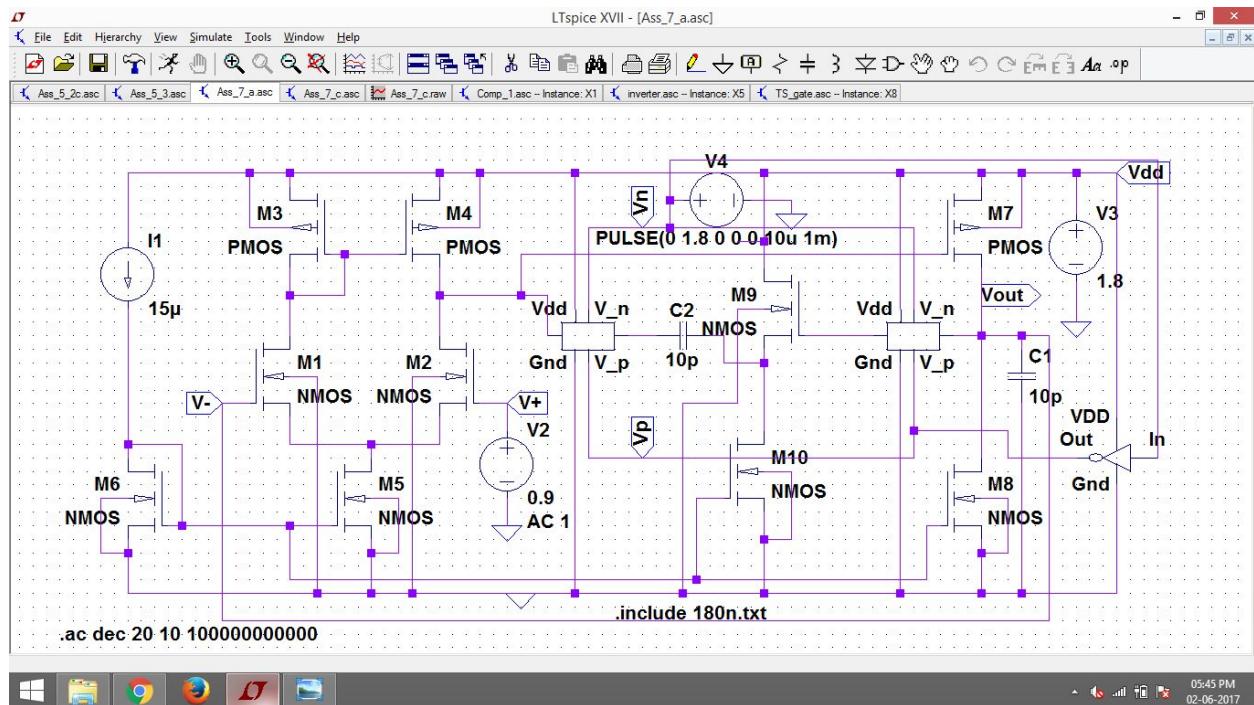
a. Inverter:



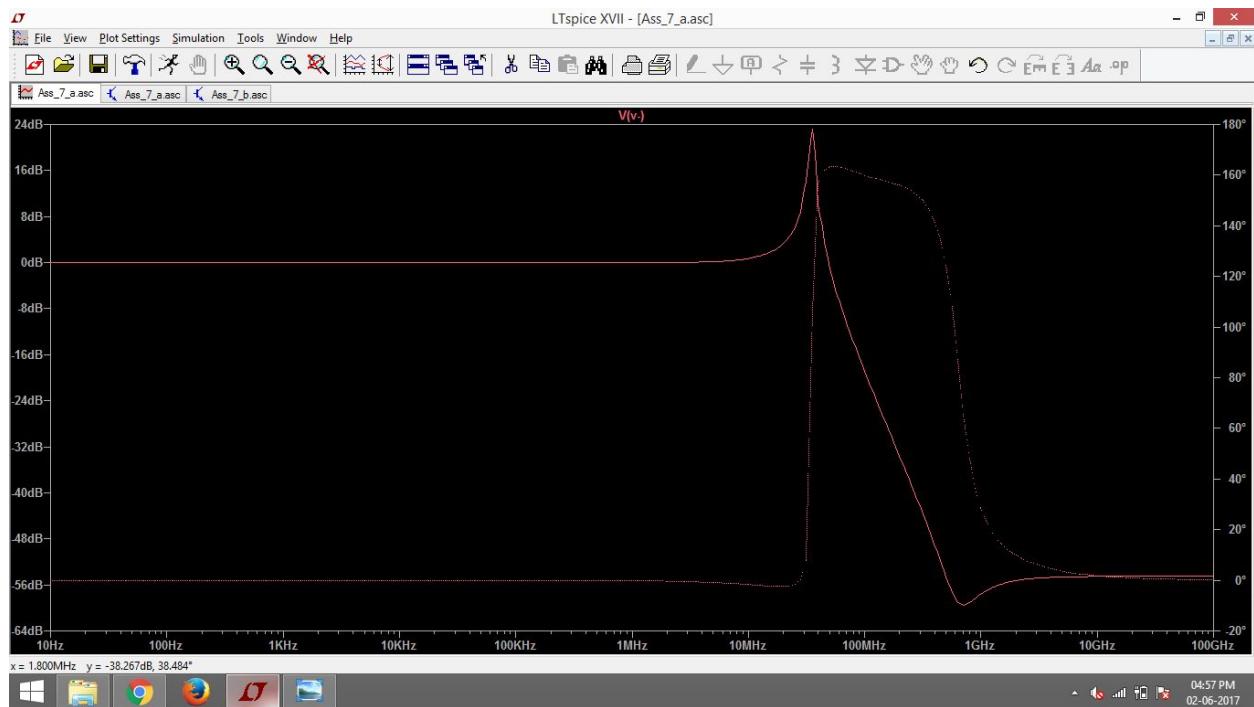
B. Transmission Gate:



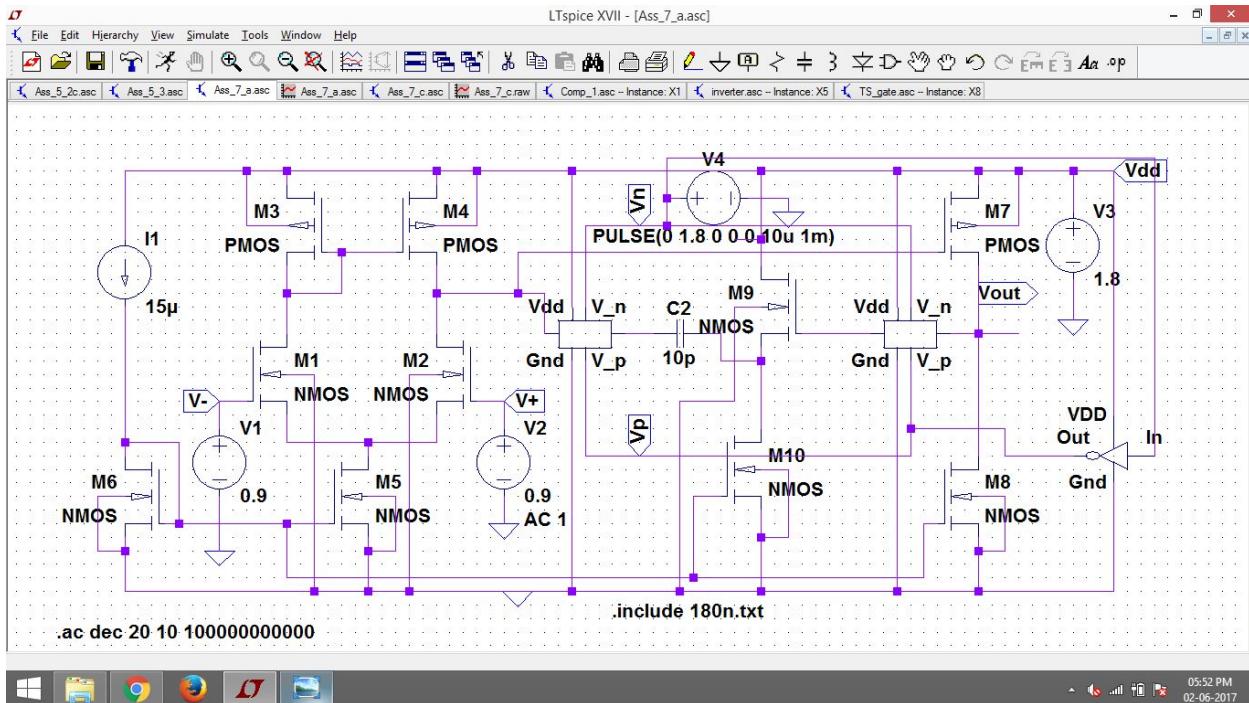
# 1. Amplifier compensated for phi-1 phase(unity gain feedback):



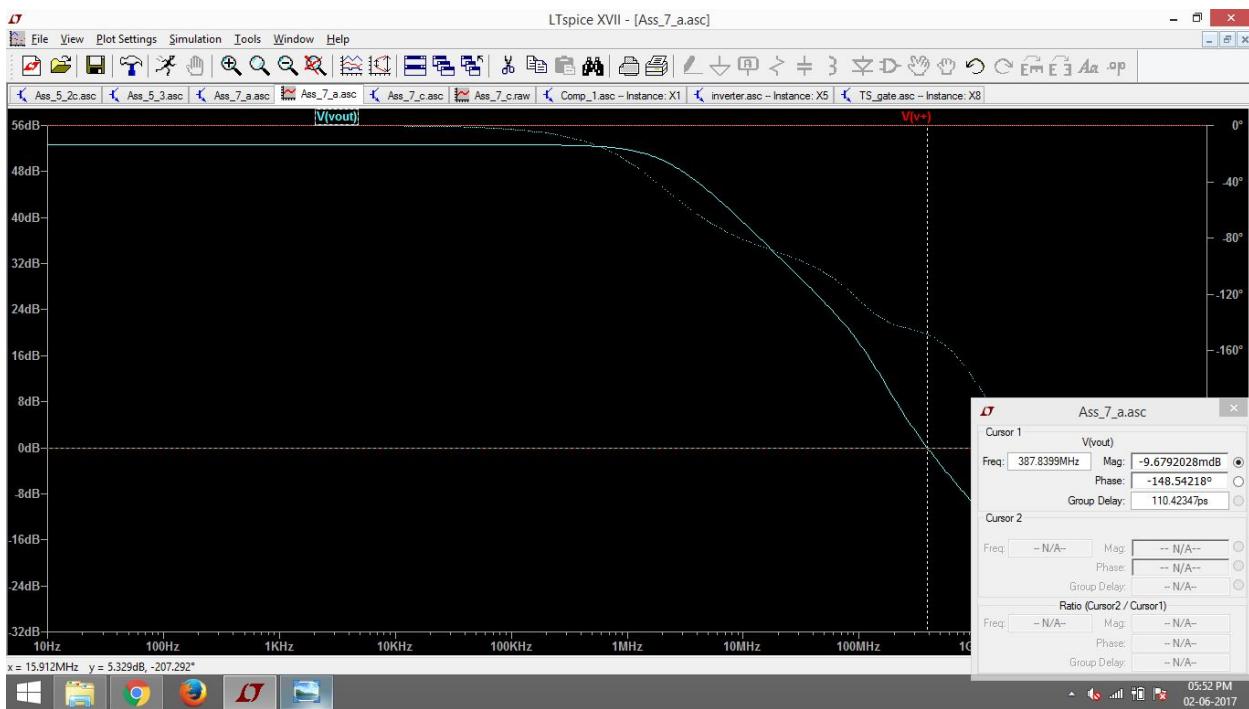
## Frequency response:



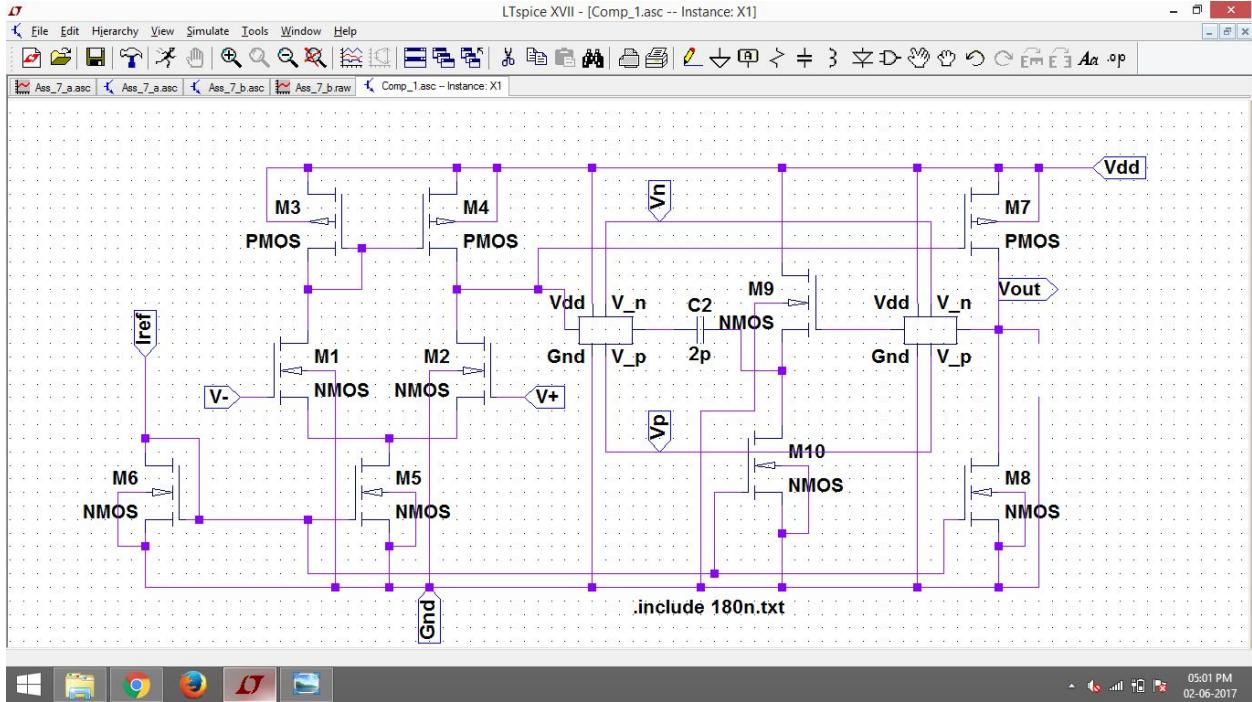
## Open loop analysis:



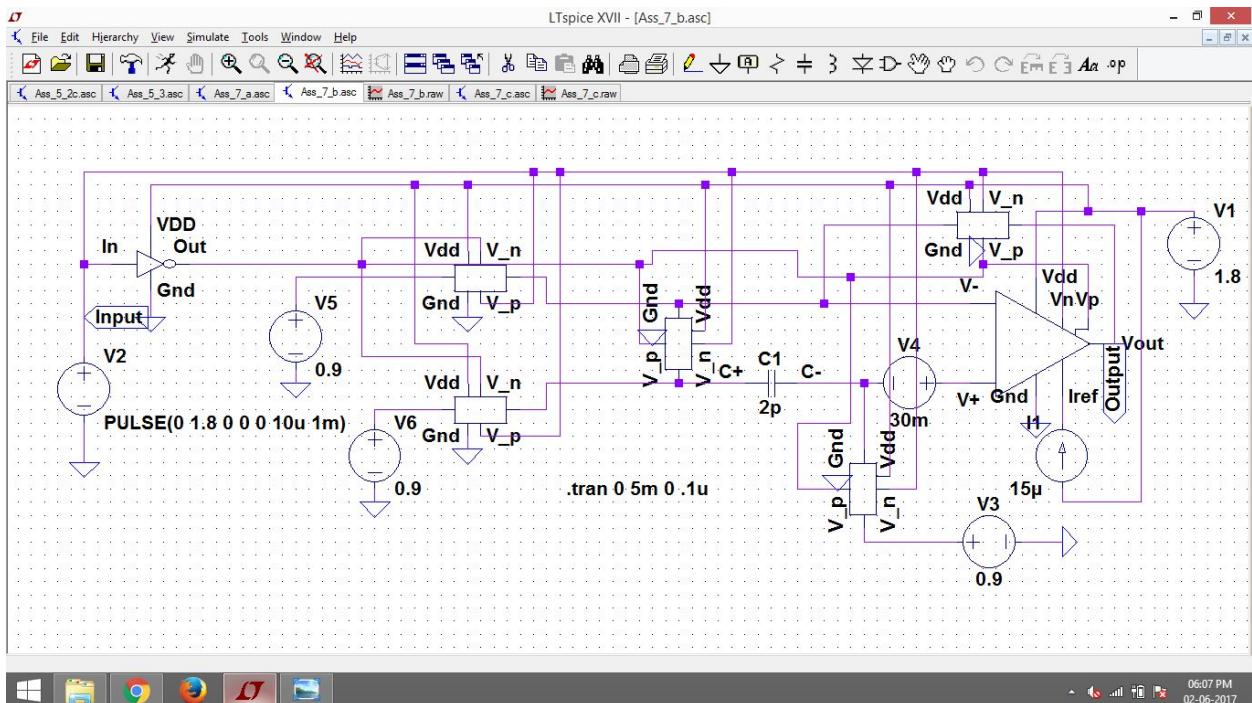
## Frequency response:



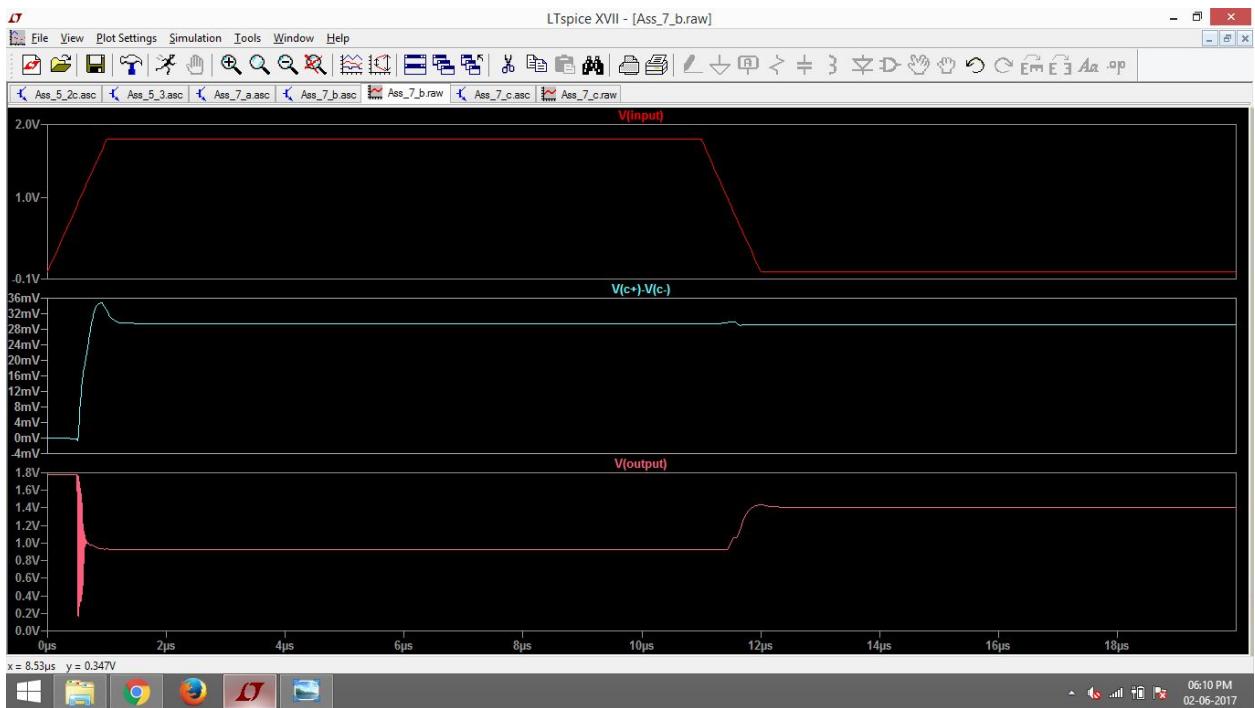
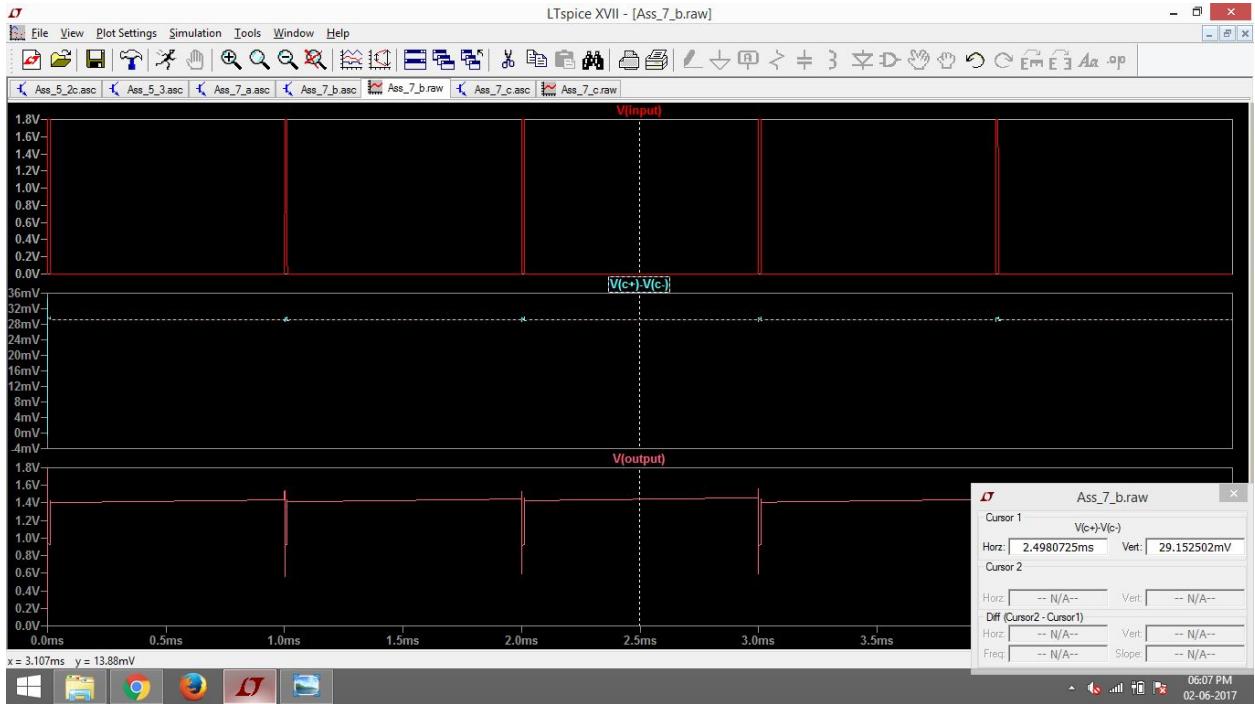
### C. Comparator(used as symbol):



### 2. When $V_{off} = 30mV$ , $V_{in\_1} = V_{in\_2} = 0.9V$

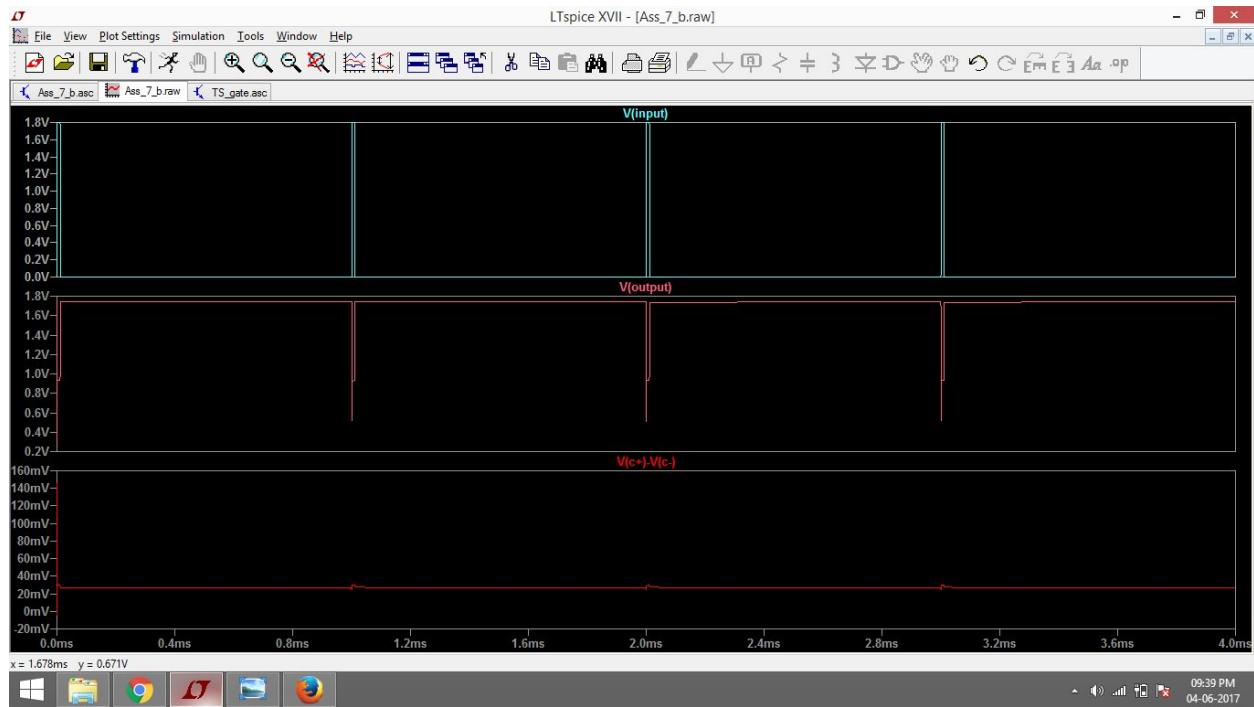
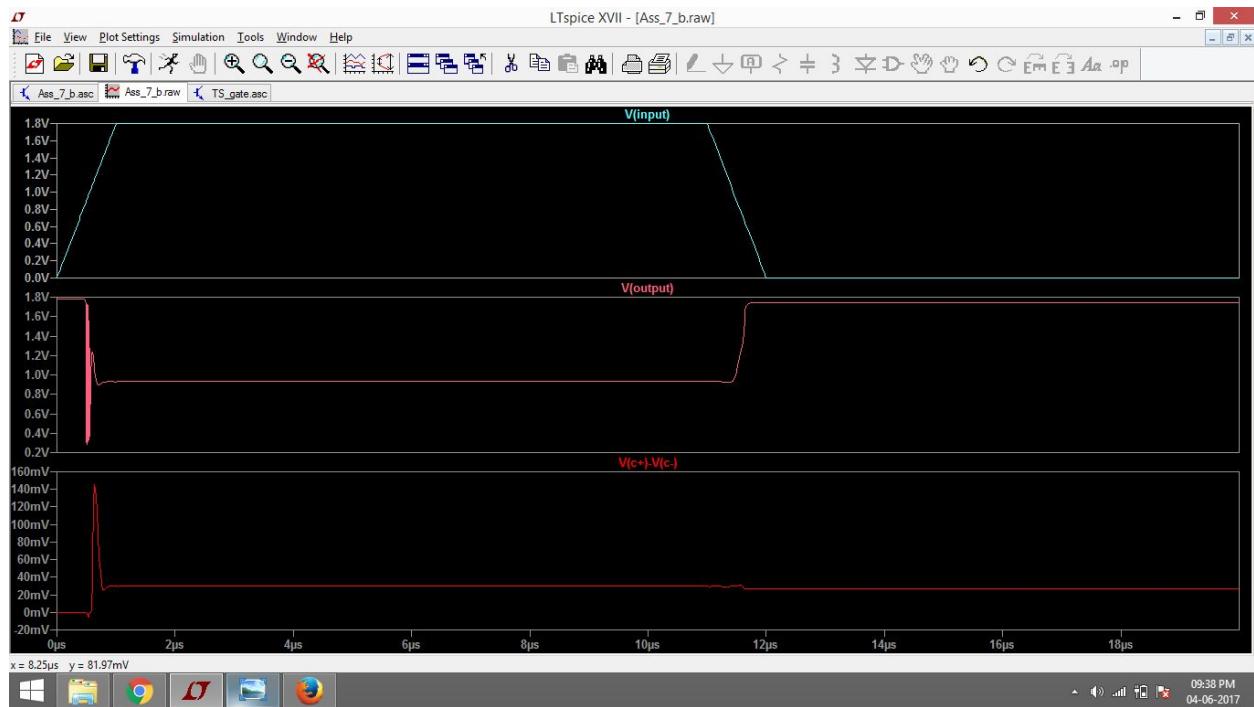


## Transient Response:



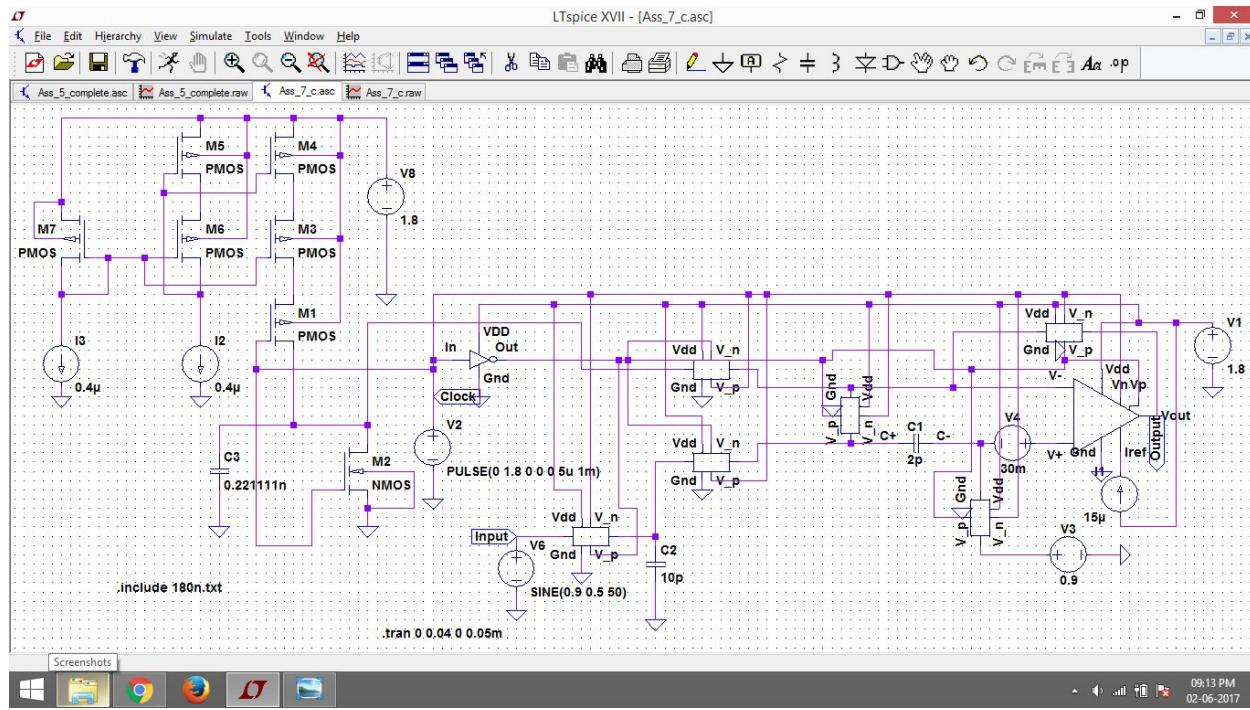
**Doubt: On changing the dimensions of transmission gate, the magnitude of Vout was changing. Why?**

**After changing the dimensions of transmission gate's transistors:  
Transient Response:**



Still Vout is reaching only up to 1.74V.

### 3. Comparator with sampled and ramp inputs.



### Transient response:

