

## Full Cadence Flow (Virtuoso) for a CMOS Inverter Design

Technology: IHP BiCMOS 0.25 micron Single poly, 4 Metal.

---

Create your home directory under root with the name "student".

For example " `/home/student` "

So, now your user id is "student" and also attaché a group ID, for example "cadence" with this user id. While creating your user id, you have to set your password properly.

Keep the login shell `:/bin/csh`

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Path Setup :

Create a directory

"cad" under root : `/cad`

Now create a subdirectory "cadence" under "cad" : `/cad/cadence`

Install the cadence software in this "cadence" directory.

`/cad/cadence`

---

Create a subdirectory "ihp\_lib" under "cad" i.e `/cad/ihp_lib`

Install the Tech Library under the ihp\_lib directory.

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Creating working directory:

Once you install the tech file under ihp\_lib directory, open this, you will find a directory IHP, along with other directories like sg25h1\_m4, sgb25vd\_m4 etc. Now open the IHP directory, you will find a directory "rev41201". Open this rev41202 directory, you will find a directory "work". Open this work directory, you will find a tar file "`skel.tar.gz`". Now select this tar file, right click -> extract here. Once you will do it, you will find a folder "skel" in the same place. Just rename this folder with your own name, for example "student". Now, open a terminal, type "csh". Then type "`chown -R student:cadence /cad/ihp_lib/IHP/rev41201/work/student`". This will change the owner from root to your own user ID.

So, your home directory is: `/home/student`

and your working directory is: /cad/ihp\_lib/IHP/rev41201/work/student

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creat a .cshrc file (or copy the following) under your home directory as mentioned below:

---

```
# @(#)cshrc 1.11 89/11/29 SMI
umask 022
set path=(/bin /usr/bin /usr/ucb /etc .)
if ( $?prompt ) then
set history=32
endif
#
#
set SHELL = /bin/tcsh
umask 022
set filec
##### DEFAULT PATH SET-UP #####
#-----
#set prompt="`whoami`@%M %c %t>"
#set path=($path ~ashis/bin)
set path=($path /opt/sfw/bin)
set path=($path /opt/sfw/esp/bin)
set path=($path /opt/sfw/teTeX/bin/sparc-sun-solaris2.9)
set path=($path /cad/Adobe/Acrobat7.0/bin)
set path=($path /opt/MOZfirefox/reloc/sfw/lib/firefox)
#set path=($path /cad/cadence/IC5.0/tools.lnx86/bin)
#set path=($path /cad/cadence/IC5.0/tools.lnx86/dfII/bin)
#set path=($path /cadt/cadence/assura3.1.6/bin)
#set path=($path /cad/cadence/assura3.1.6/tools/bin)
#set path=($path /cad/cadence/assura3.1.6/tools/dfII/bin)
#set path=($path /cad/cadence/assura3.1.6/tools/assura/bin)
#set path=($path /cad/cadence/seultra/tools/bin)
#set path=($path /cad/cadence/seultra/tools/dfII/bin)
#set path=($path /cad/cadence/seultra/tools/dsm/bin)
setenv OA_HOME /cad/cadence/OA
set path = ($path $OA_HOME/bin)
```

```
source /cad/cadence/smTool/tools.lnx86/stream_mgt/install/setup.csh
#ALIAS#
```

```

alias ls 'gls --color'
alias a 'acroread'
alias vi 'gvim'
alias gv 'ggv'

#LICENSE FILE#
setenv LM_LICENSE_FILE 5280@DOE55:5280@DOE34:5280@DOE35
setenv CDS_LIC_FILE 5280@DOE55:5280@DOE34:5280@DOE35

#CADENCE PATH#
#####
#setenv CDS instdir
setenv CDS /cad/cadence/IC5141
setenv CDS_INSTALL_DIR $CDS/tools/dfII
#setenv LD_LIBRARY_PATH
"/usr/openwin/lib:/usr/dt:/usr/dt/lib:$CDS/tools/lib:$CDS/tools/verilog/#lib:/usr/X11
/lib:/usr/lib:/usr/X11R5/lib:$CDS/tools/leapfrog/lib"
#setenv SHLIB_PATH
/usr/lib:/lib:/usr/lib/X11:$CDS/tools/lib:$CDS/tools/verilog/lib:$CDS/tools/#leapfrog
/lib
#setenv CDS_LIC_FILE $CDS/share/license/license.dat
setenv PATH
"$CDS/tools/bin:$CDS/tools/dfII/bin:$CDS/tools/leapfrog/bin:$CDS/tools/dracula/b
in:$CDS/tools/dsm/bin:$CDS/tools/specctra/bin:$CDS/tools/pcb/bin:${PATH}"
setenv DD_DONT_DO_OS_LOCKS SET
#####
setenv CDS_INST_DIR /cad/cadence/IC5141
setenv CLS_CDSD_COMPATIBILITY_LOCKING NO
#setenv CDS_LIC_FILE /software/licenses/license_80c473bf
setenv CDS_LIC_TIMEOUT 30
setenv CDS_NUM_USER_COLORS 85
setenv PSF_LARGE_FILE_ON TRUE
setenv NOAUTOSTARTFRAME 1
setenv CDS_Netlisting_Mode Analog

#CADENCE PATH#
#####
set path=($path /cad/cadence/IUS6.2/tools/bin)
set path=($path /cad/cadence/IUS6.2/tools/bin/64bit)
#####

```

```

##### MMSIM6.1 #####
set path=($path /cad/cadence/MMSIM60/tools/bin)
set path=($path /cad/cadence/MMSIM60/tools/bin/64bit)

#####
##### NEOCELL3.4 #####
set path=($path /cad/cadence/NEOCELL3.4/tools/bin)
set path=($path /cad/cadence/NEOCELL3.4/tools/bin/64bit)

#####
##### CONFRML6.2 #####
set path=($path /cad/cadence/CONFRML6.2/tools/bin)
set path=($path /cad/cadence/CONFRML6.2/tools/bin/64bit)

#####
##### AMLS6.2 #####
set path=($path /cad/cadence/ANLS6.2/tools/bin)
set path=($path /cad/cadence/ANLS6.2/tools/bin/64bit)

#####
##### PACIFIC 6.1 #####
set path=($path /cad/cadence/PACIFIC6.1/tools/bin)
set path=($path /cad/cadence/PACIFIC6.1/tools/bin/64bit)
#####
##### SOC6.2 #####
set path=($path /cad/cadence/SOC6.2/tools/bin)
set path=($path /cad/cadence/SOC6.2/tools/bin/64bit)

#####
##### SPB15.7 #####
set path=($path /cad/cadence/SPB15.7/tools/bin)
set path=($path /cad/cadence/SPB15.7/tools/bin/64bit)

#####
##### SEV-2007 #####
set path=($path /cad/cadence/SEV-2007/tools/bin)
set path=($path /cad/cadence/SEV-2007/tools/bin/64bit)

```

```

#####
set path=($path /cad/cadence/VSDE4.1/tools/bin)
set path=($path /cad/cadence/VSDE4.1/tools/bin/64bit)

#####
set path=($path /cad/cadence/iscape/iscape/bin)
#####
setenv CDSHOME /cad/cadence/IC5141
set path=($path /cad/cadence/IC5141/tools/dfII/bin)
set path=($path /cad/cadence/IC5141/tools/bin)
set path=($path /cad/cadence/IC5141/tools/dracula/bin)
#####
set path=($path /cad/cadence/ASSURA3.1.6/tools/bin)
#set path=($path /cad/cadence/ASSURA3.1.6/tools/bin/64bit)
set path=($path /cad/cadence/ASSURA3.1.6/tools/assura/bin)
#####
set path=($path /cad/cadence/ET6.2/tools/bin)
set path=($path /cad/cadence/ET6.2/tools/bin/64bit)

#####
set path=($path /cad/cadence/VIP21/tools/bin)
set path=($path /cad/cadence/VIP21/tools/bin/64bit)

#####
set path=($path /cad/cadence/smTool/tools/bin)
set path=($path /cad/cadence/smTool/tools/bin/64bit)

#####
setenv NEOHOME /cad/cadence/NEOCKT
set path=($path $NEOHOME/bin)

alias ihph1m4 'setenv PROJECT /cad/lib_ihp/IHP/rev41201; setenv
PROJECTDATA $PROJECT/work/$LOGNAME; cd $PROJECTDATA/cds; source
cshrc.cadence; icfb&'

-----

```

### Schematic:

Once you will create your home directory and working directory, logout from the root, and login with your own login.

Then, open a terminal, just type "ihph1m4" as shown in Fig 1.



Fig 1

This will open the cadence environment as shown in Fig 2.

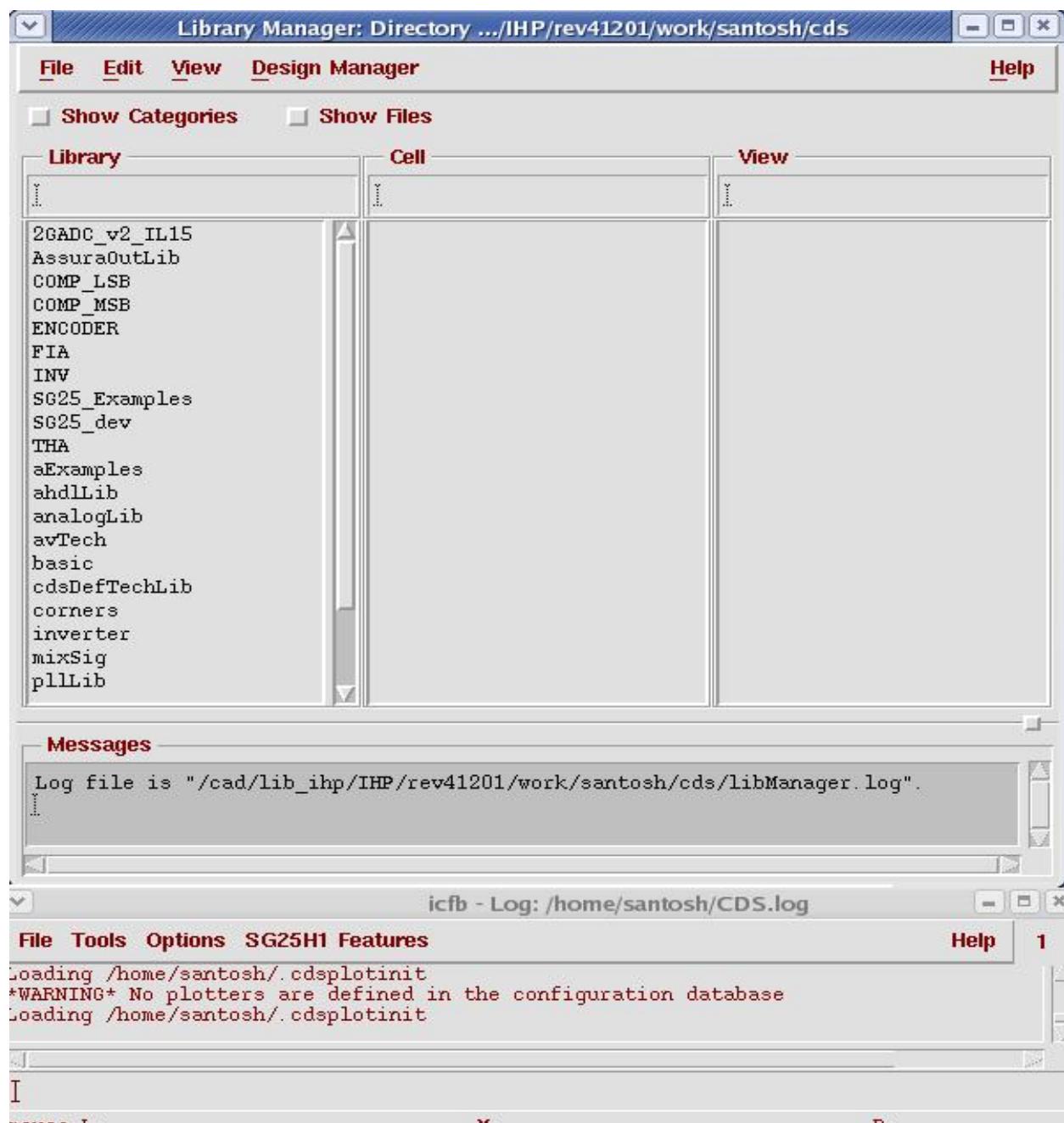


Fig 2

Now go to edit->Library Path. The following window will open.

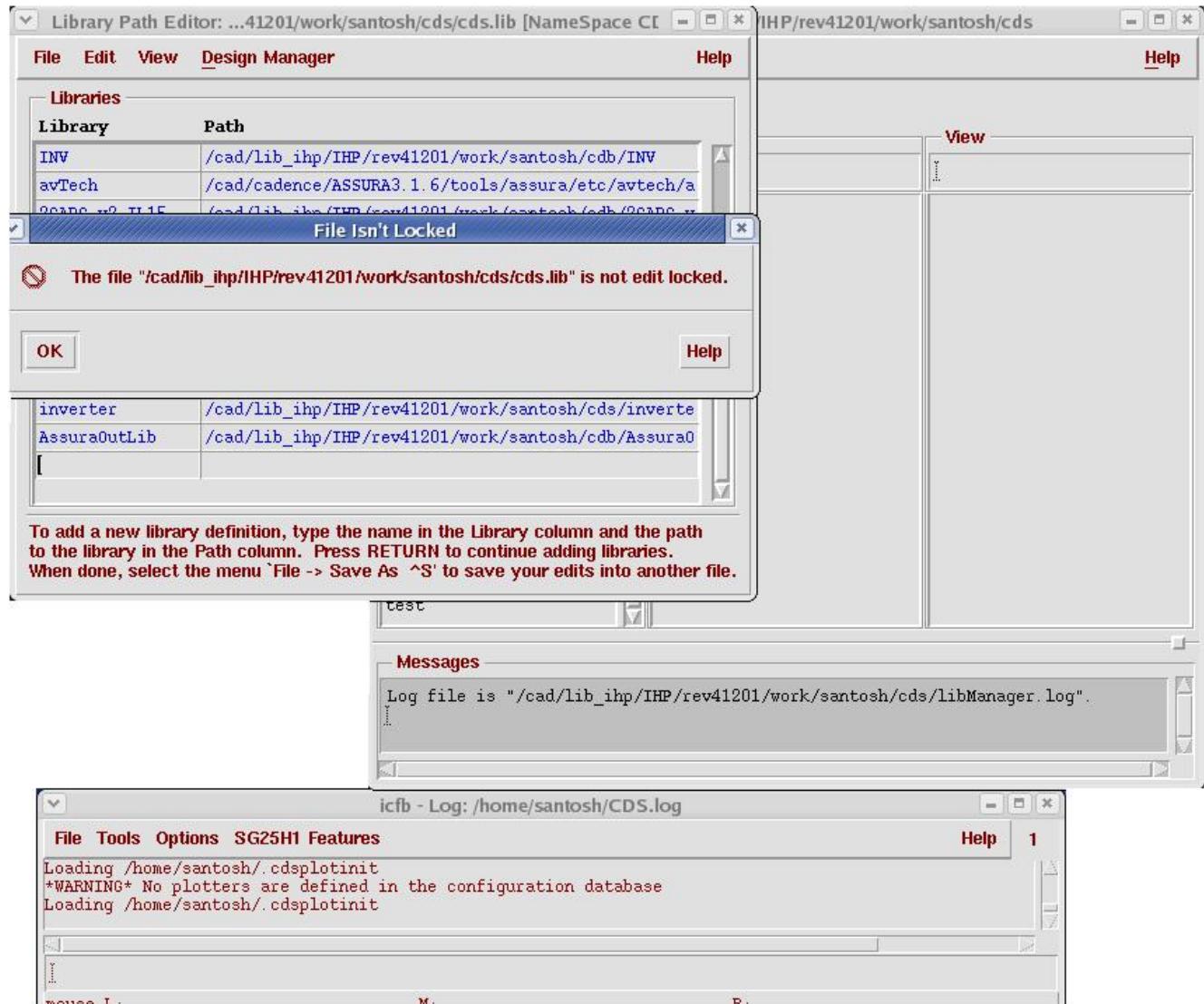


Fig 3

Press the ok button. Then set the path of different libraries as given below:

```
cdsDefTechLib /cad/cadence/IC5141/tools/dfII/etc/cdsDefTechLib
analogLib /cad/cadence/IC5141/tools/dfII/etc/cdslib/artist/analogLib
basic /cad/cadence/IC5141/tools/dfII/etc/cdslib/basic
ahdILib /cad/cadence/IC5141/tools/dfII/samples/artist/ahdILib
aExamples /cad/cadence/IC5141/tools/dfII/samples/artist/aExamples
rfLib /cad/cadence/IC5141/tools/dfII/samples/artist/rfLib
rfExamples /cad/cadence/IC5141/tools/dfII/samples/artist/rfExamples
```

```

pllLib /cad/cadence/IC5141/tools/dfII/samples/artist/pllLib
mixSig /cad/cadence/IC5141/tools/dfII/samples/artist/mixSig
corners /cad/cadence/IC5141/tools/dfII/samples/artist/corners
spectreHDL /cad/cadence/IC5141/tools/dfII/samples/artist/spectreHDL
SG25_dev /cad/lib_ihp/IHP/rev41201/lib/SG25_dev
SG25_Examples /cad/lib_ihp/IHP/rev41201/lib/SG25_Examples

```

Once you will set the path for all the libraries, go to file->save as, then press "ok", "yes", "ok".

Now close this Library path editor window.

Go to Library manager, file->New->Library. A new library window will open as shown in Fig 4.

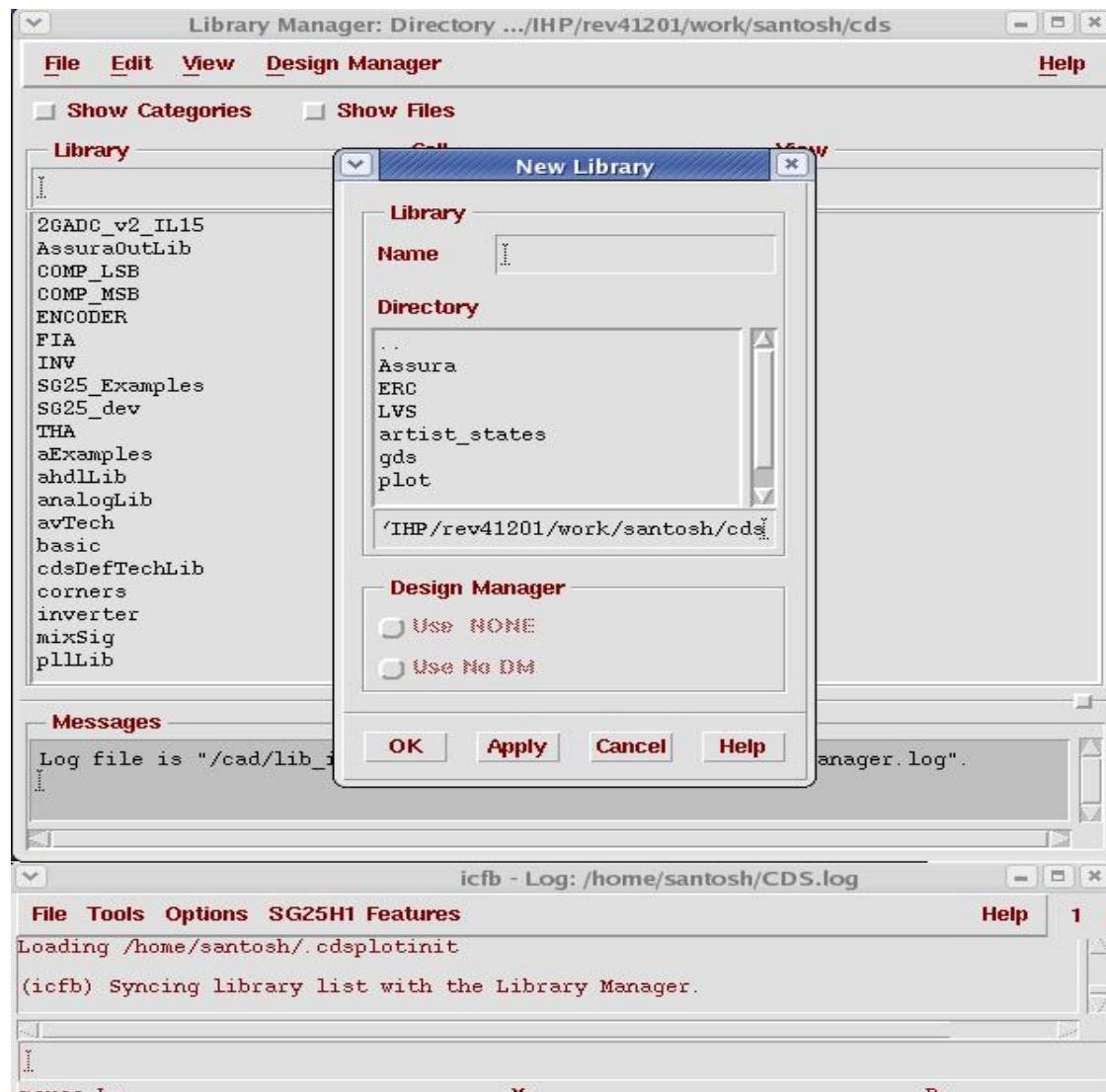


Fig 4

Give the name as INV\_S and press ok. Once you will press ok, you will find a window as shown in Fig 5:

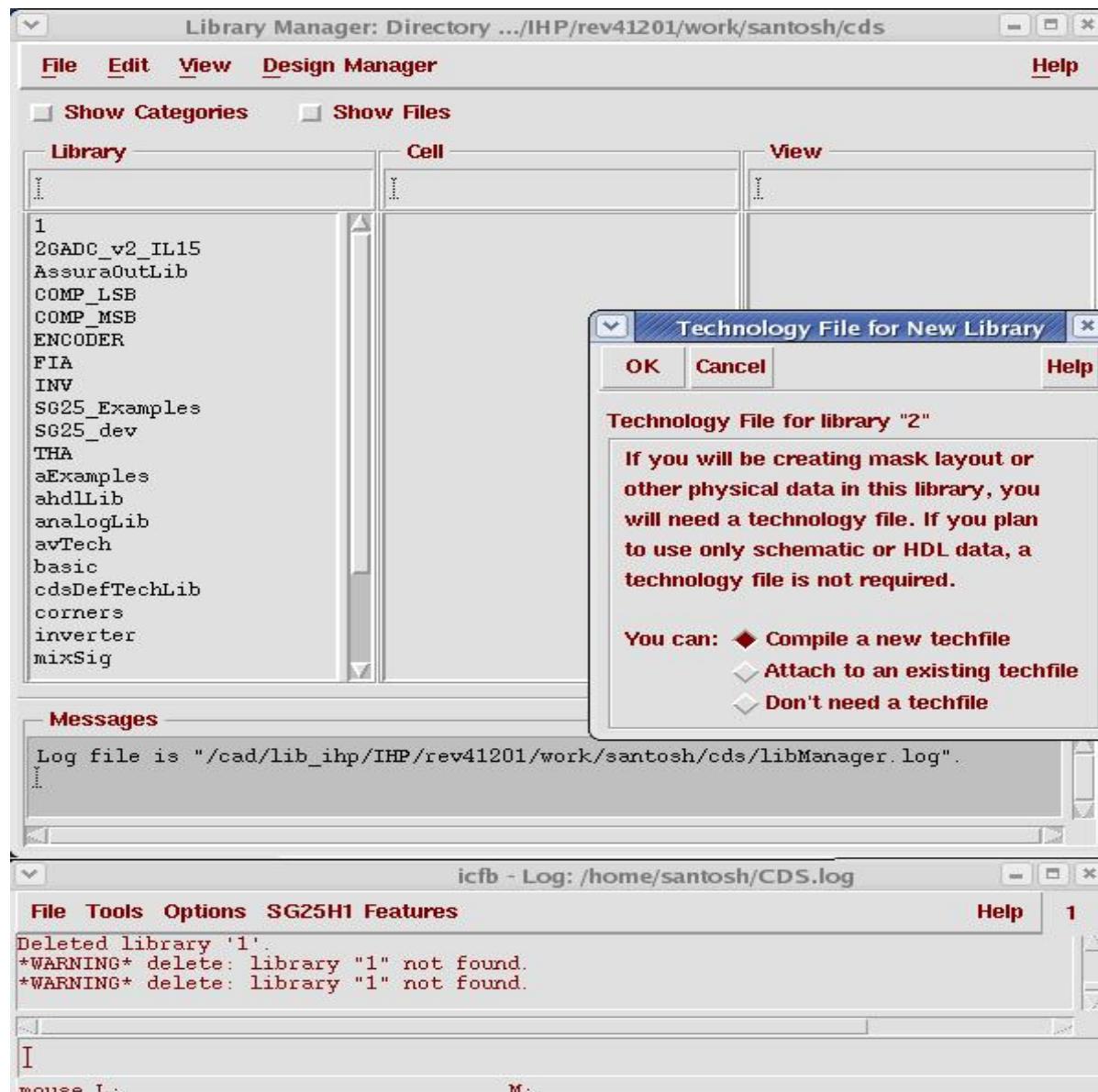


Fig 5

Select the option: Attaché to the existing tech file, then press ok. Now you will see a window as shown in Fig 6:

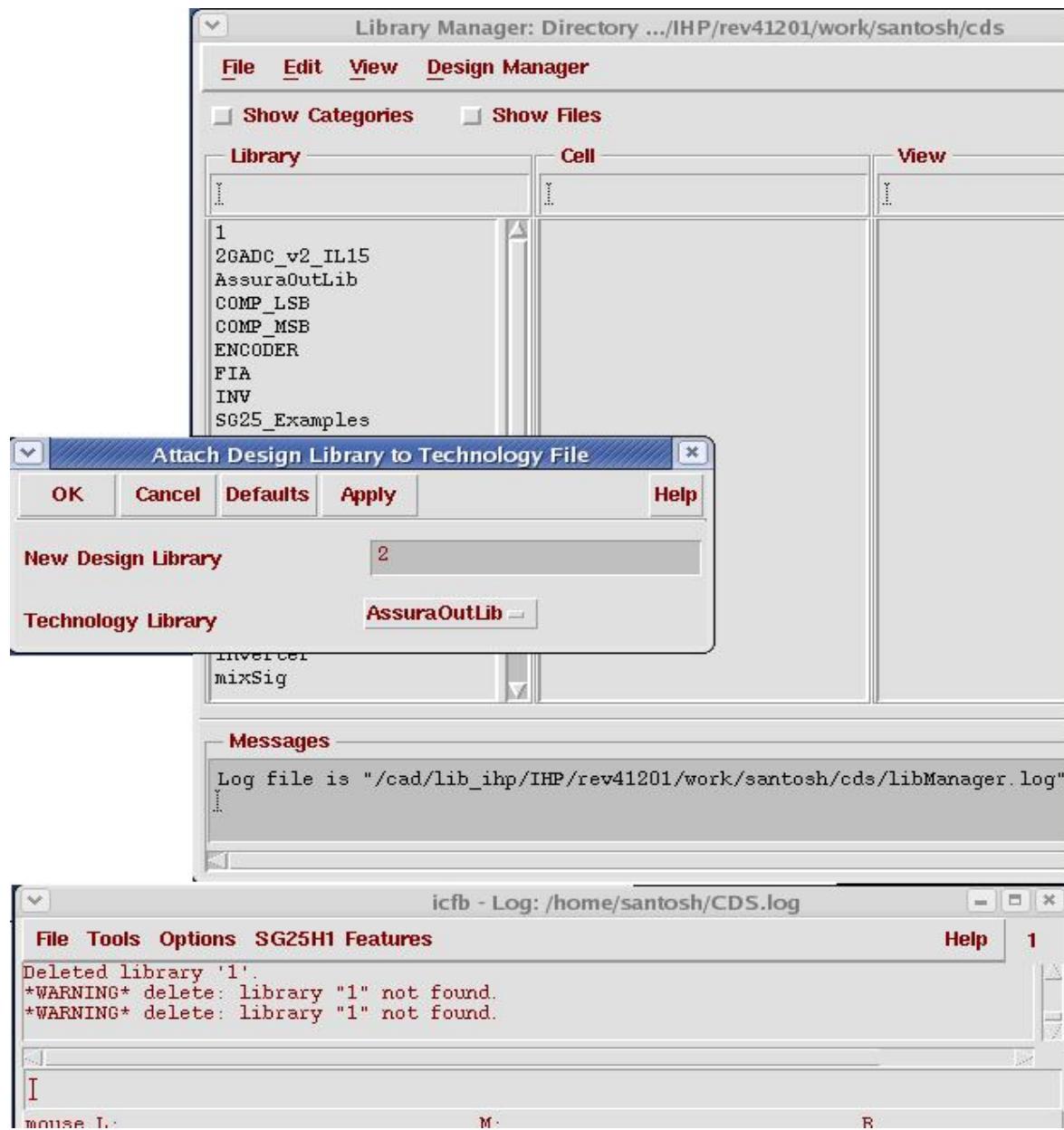


Fig 6

Change the Technology Library to SG25\_dev as shown in Fig 7:

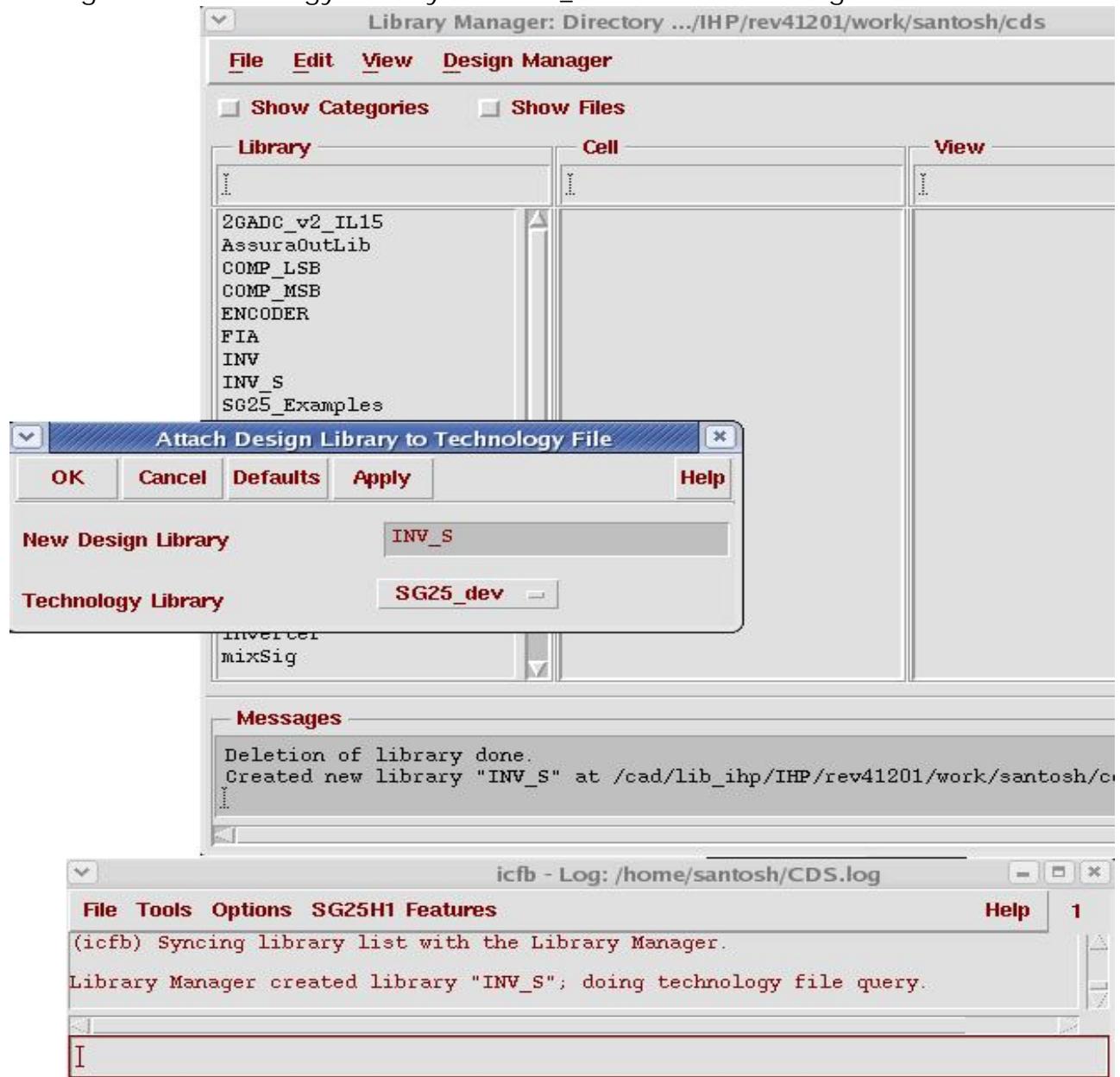


Fig 7

Then press ok.

This will create a library INV\_S as shown in Fig 8:

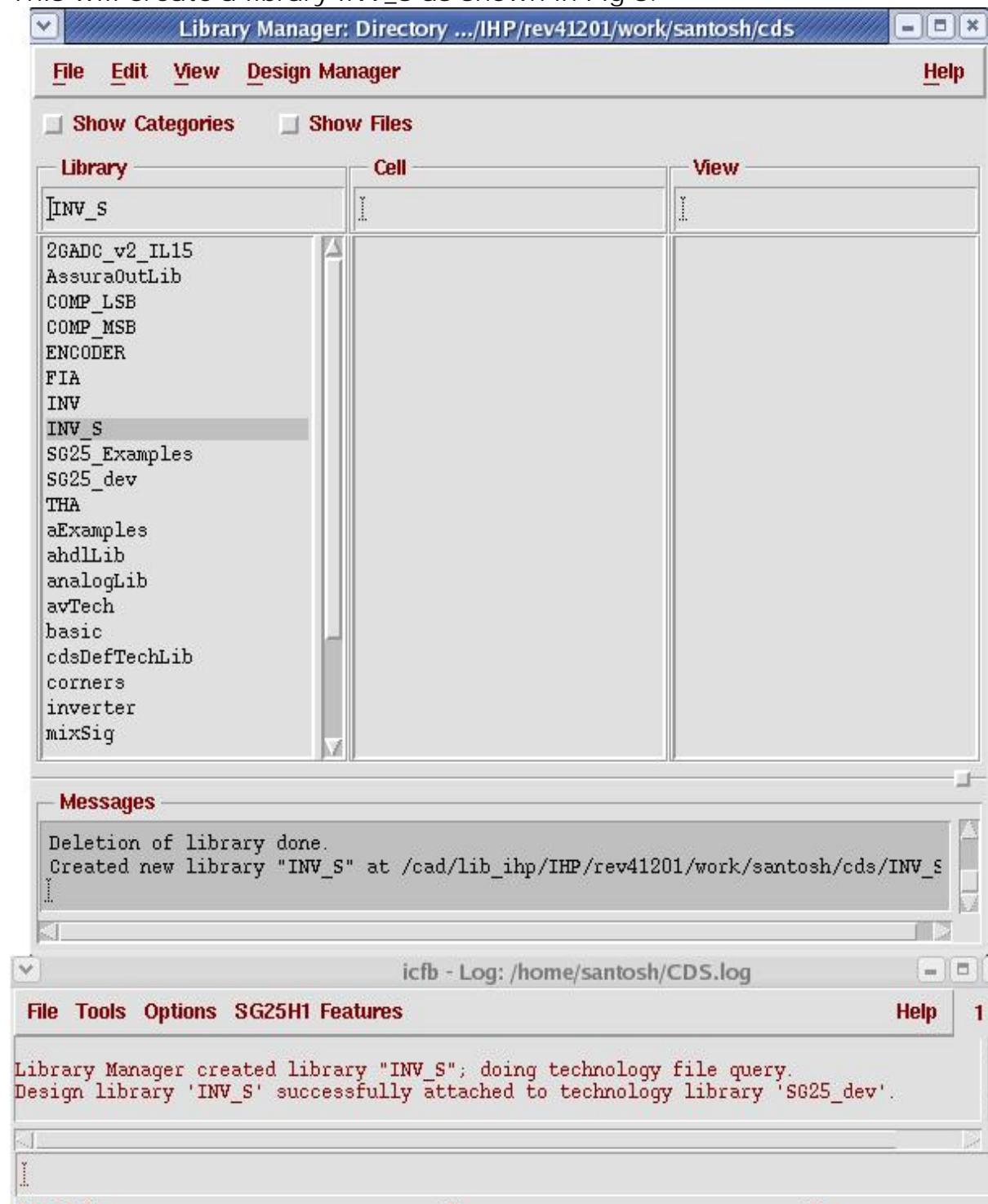


Fig 8

Now, go to Library manager->file->New->cell view. One window will open as shown in Fig 9:

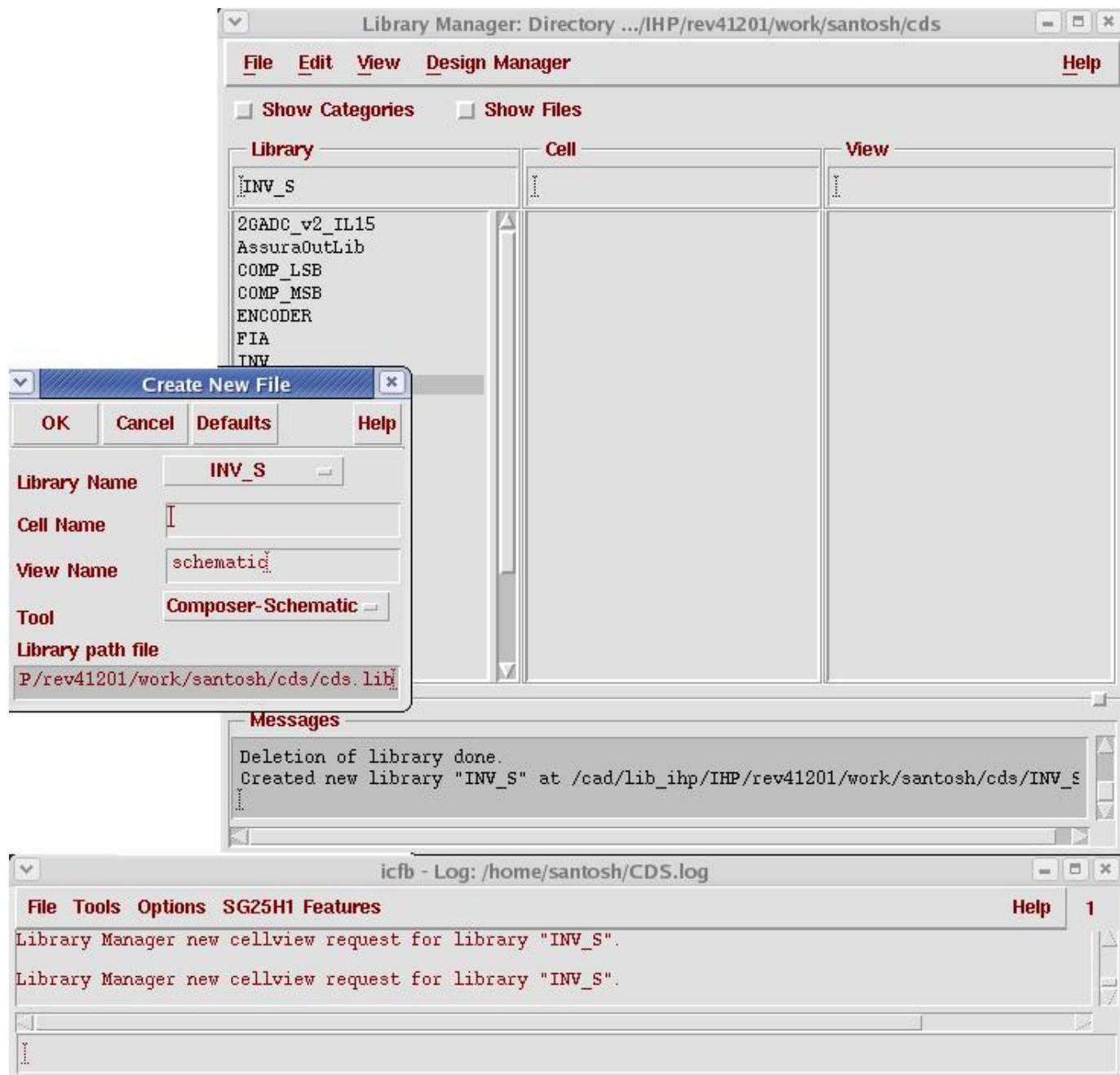


Fig 9

Give the cell name as "inv". Set the Tool to "Composer-Schematic", then press ok. Now the Virtuoso schematic editor will open as shown in Fig 10:

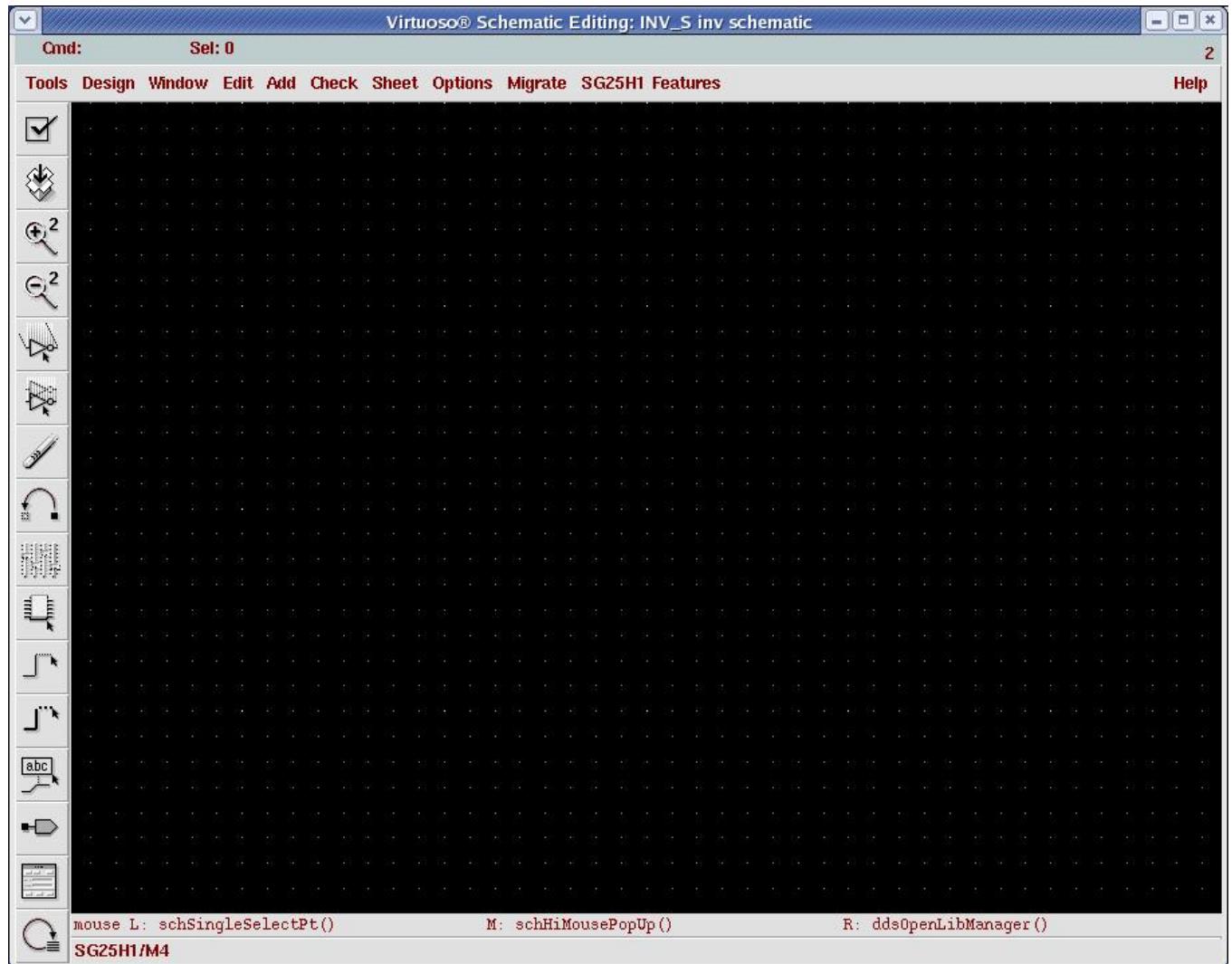


Fig 10

Now go to Add->instance. This will open a window as shown in Fig 11:

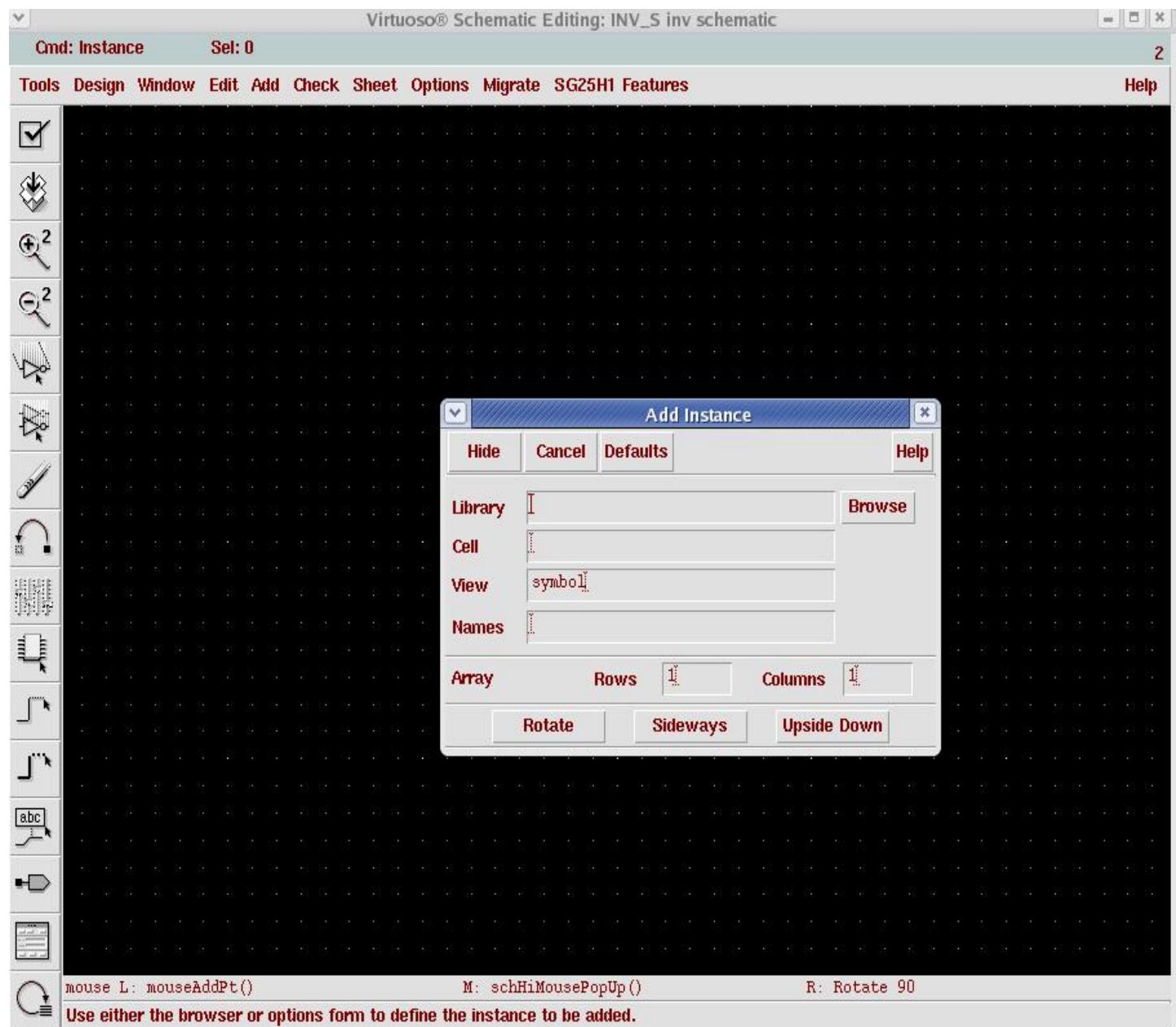


Fig 11

Now press the browse button, this will take you to Library browse window as shown in Fig 12:

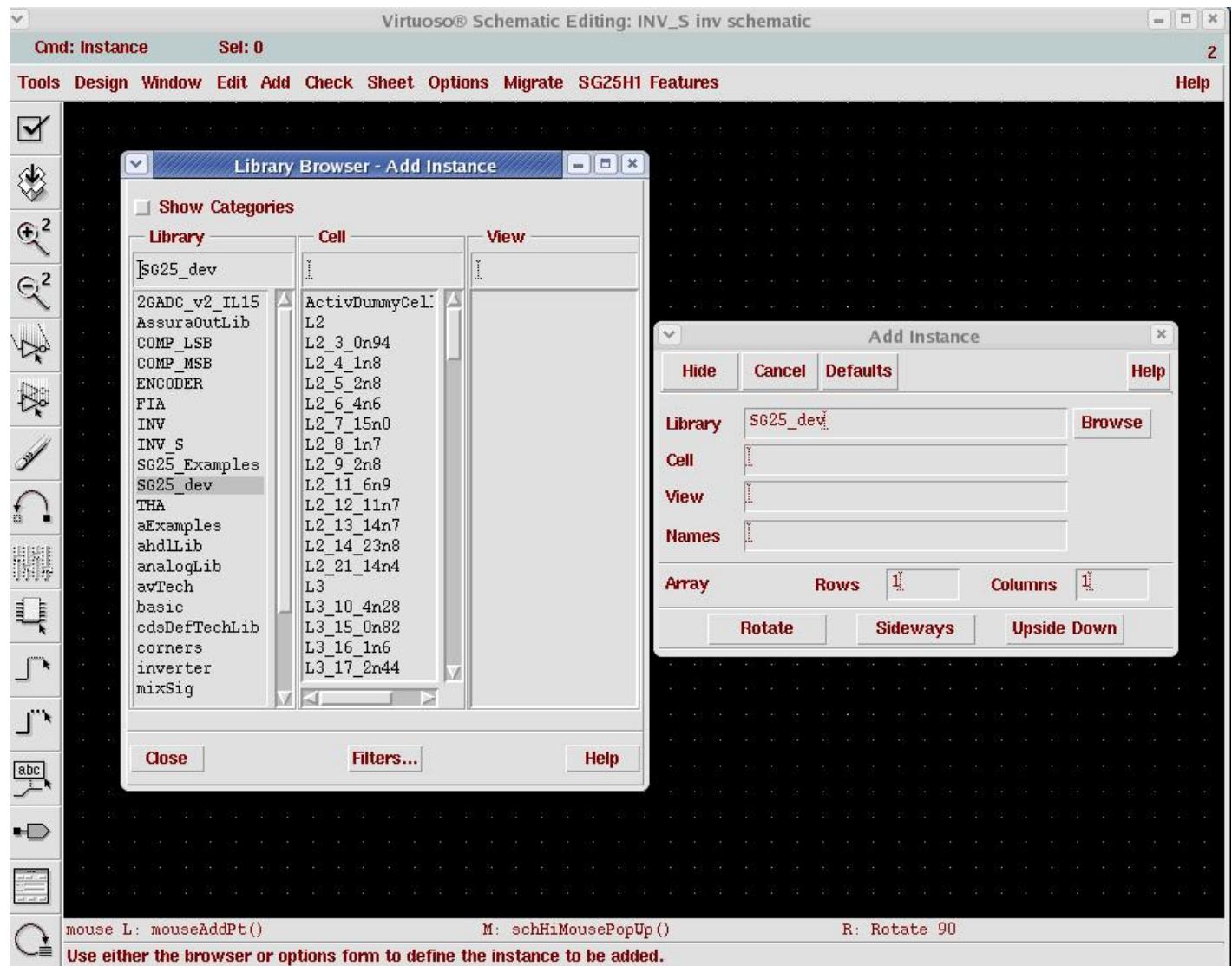


Fig 12

Select the SG25\_dev library, the search for pmos as shown in Fig 13:

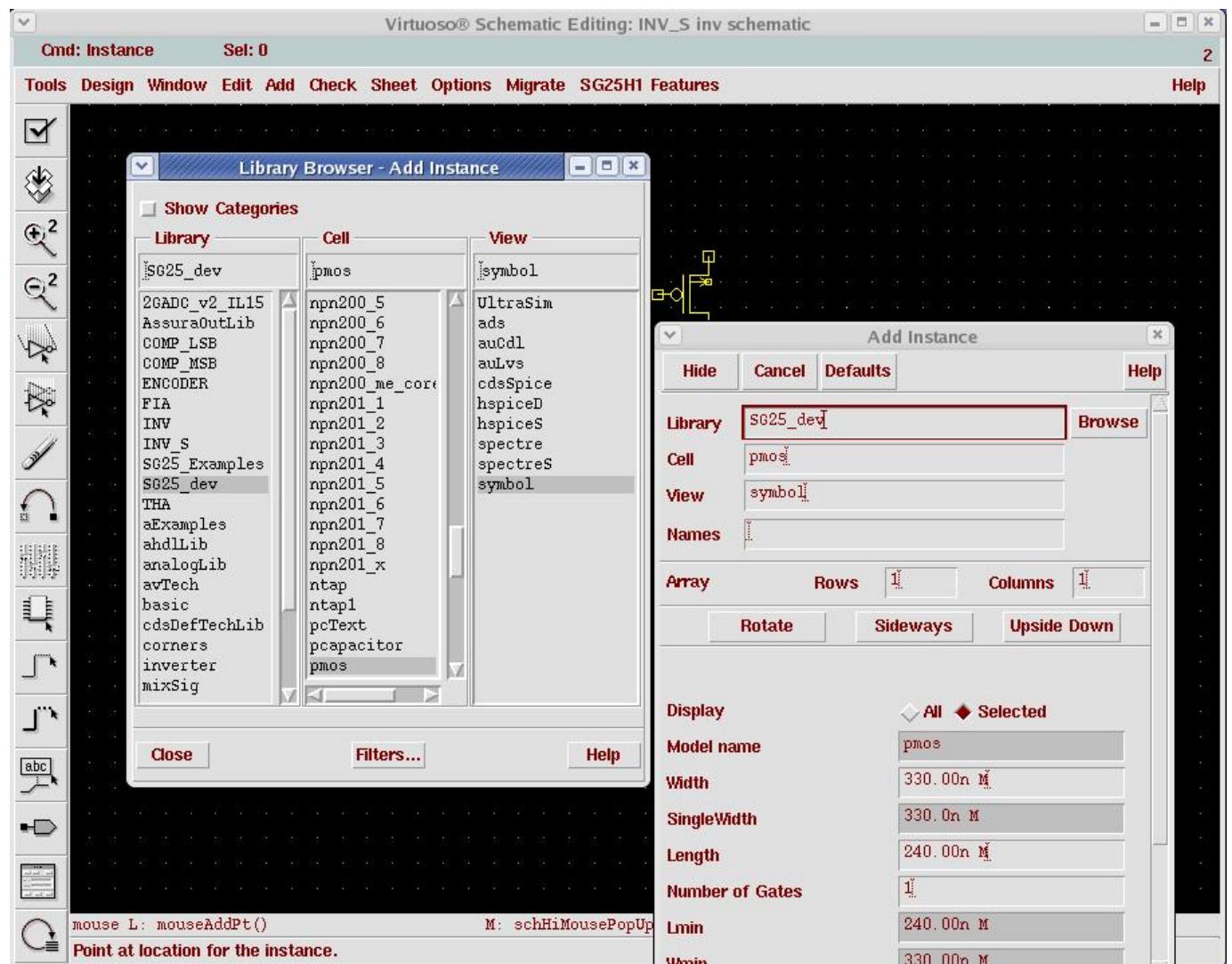


Fig 13

Now close the Library browser window, hide the Add instance window, and place the pmos on the schematic editor as shown in Fig 14:

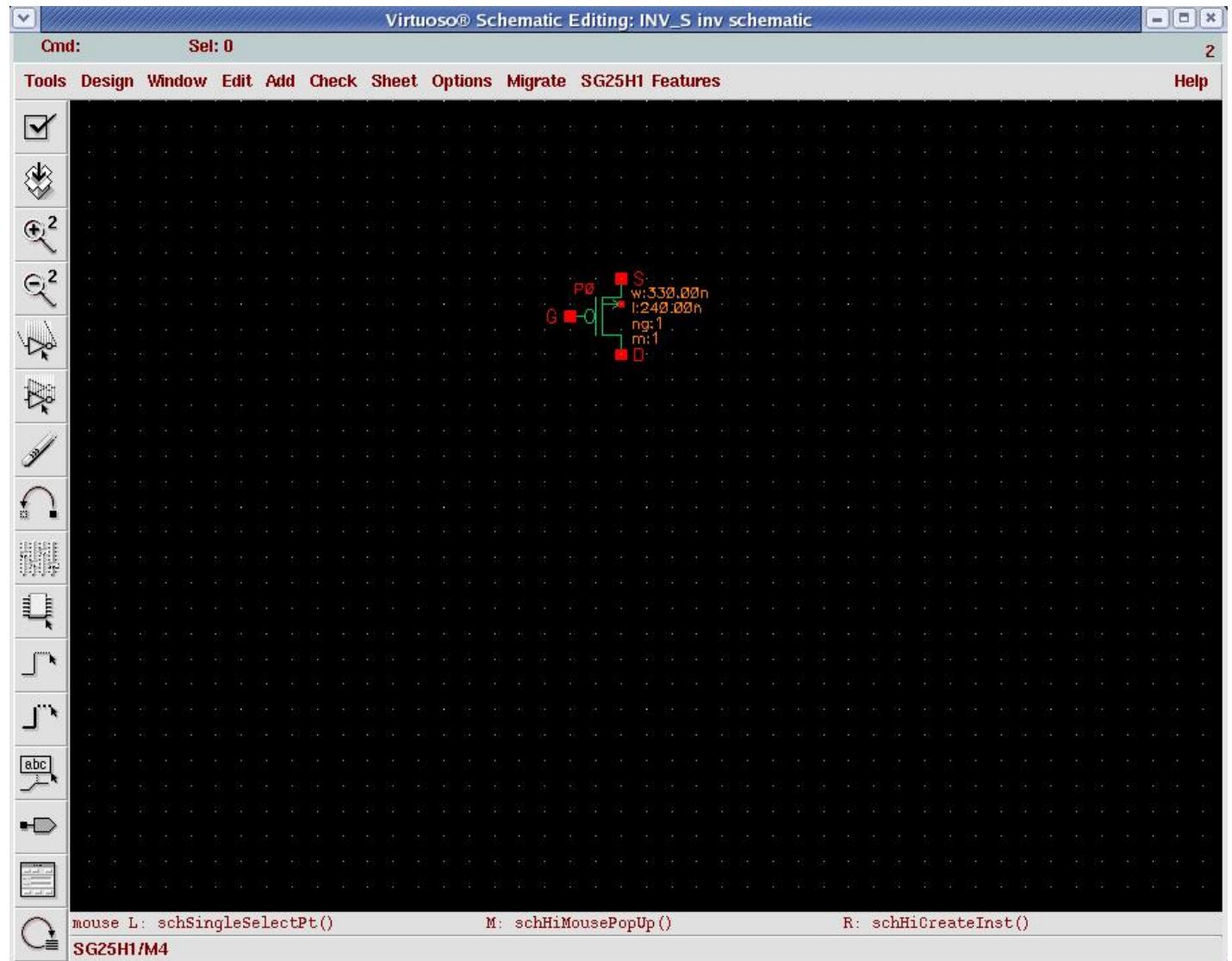


Fig 14  
Then press "Esc" button.

Short cuts

Zoom in -> ]

Zoom out -> [

Fit -> f

The same you can go for nmos transistor. Now press w for wire and do the connection as shown in Fig 15:

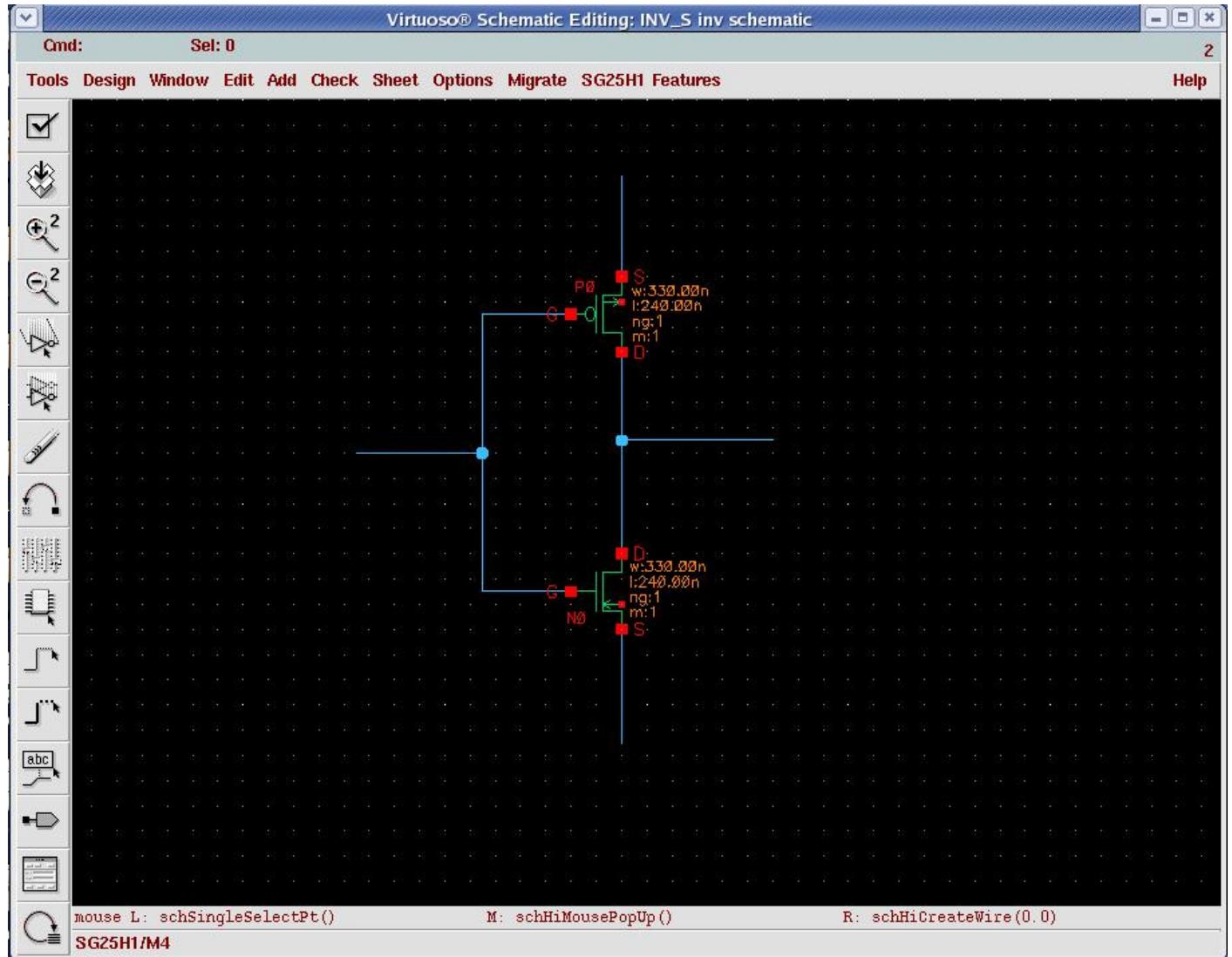


Fig 15

Now, you have to go for vdd, vcd, gnd, and vpulse. These things are available in analogLib. Then, place these components as shown Fig 16:

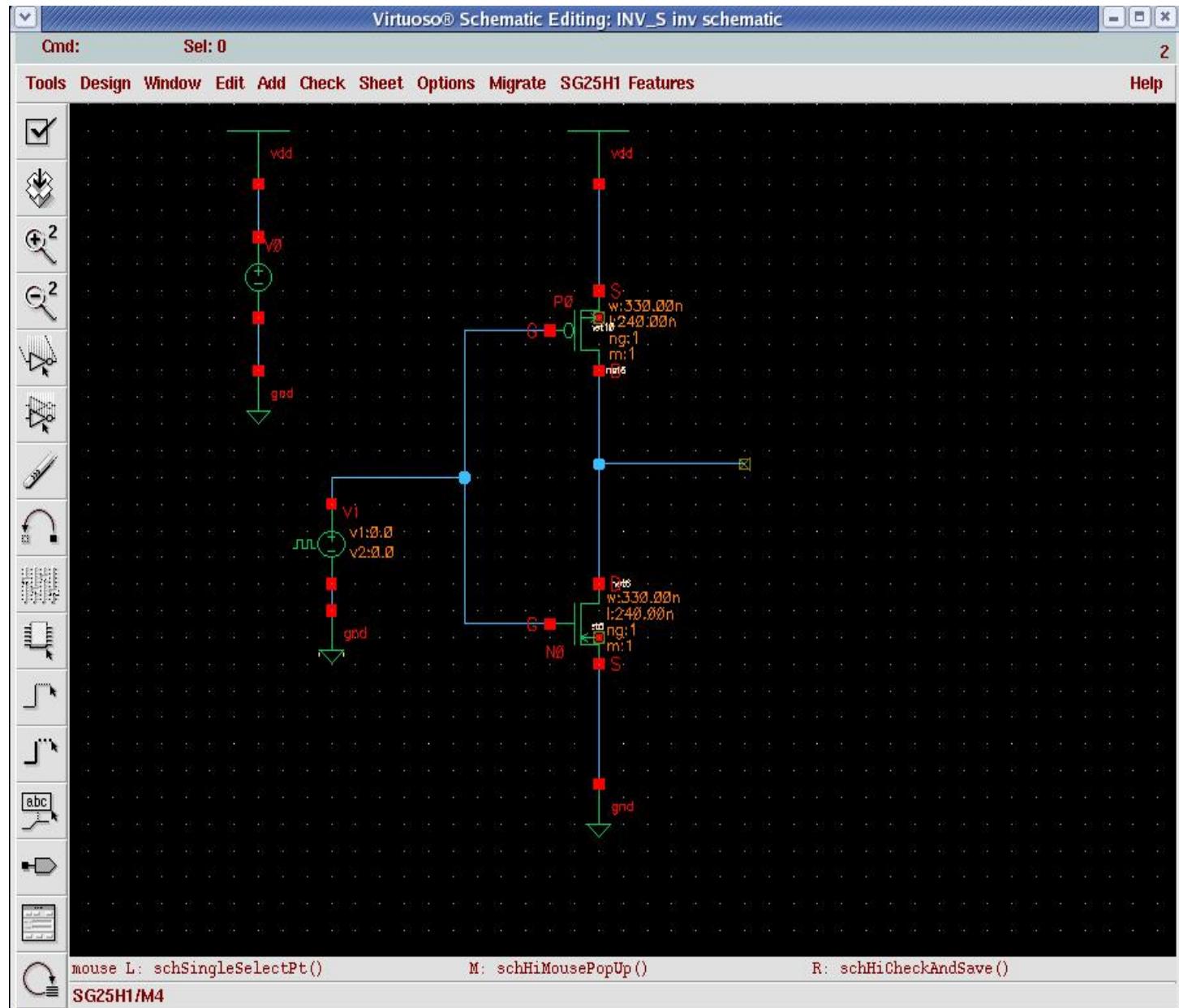


Fig 16

Connect the substrate and nwell to "sub", ptap1, ntap1 (SG25\_dev). Also connect the output to a pin. This is as shown Fig 17:

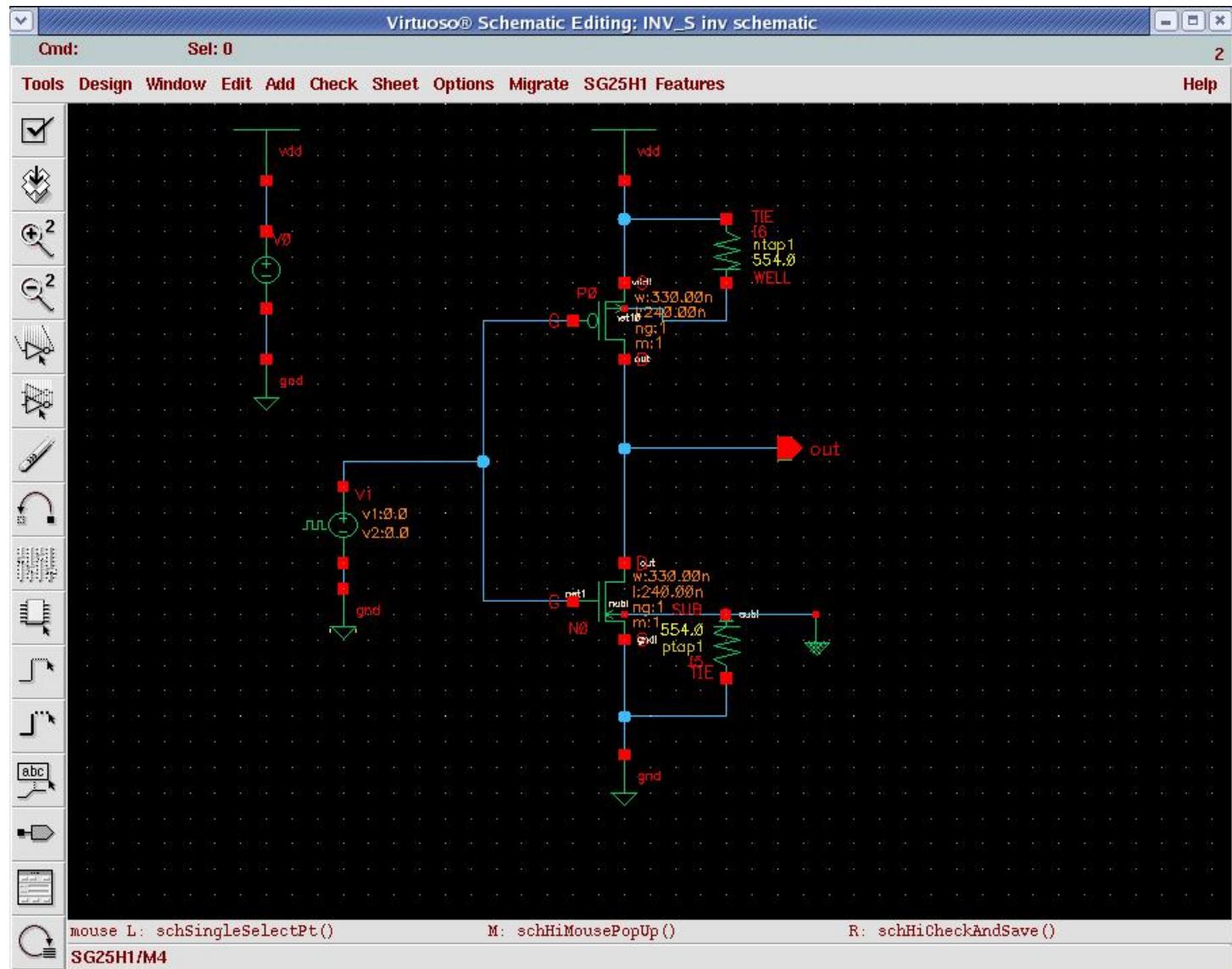


Fig 17

Now to set the pulse value, select the instances, then go to edit->property-object. This will open the following window:  
Set the values as shown in Fig 18.

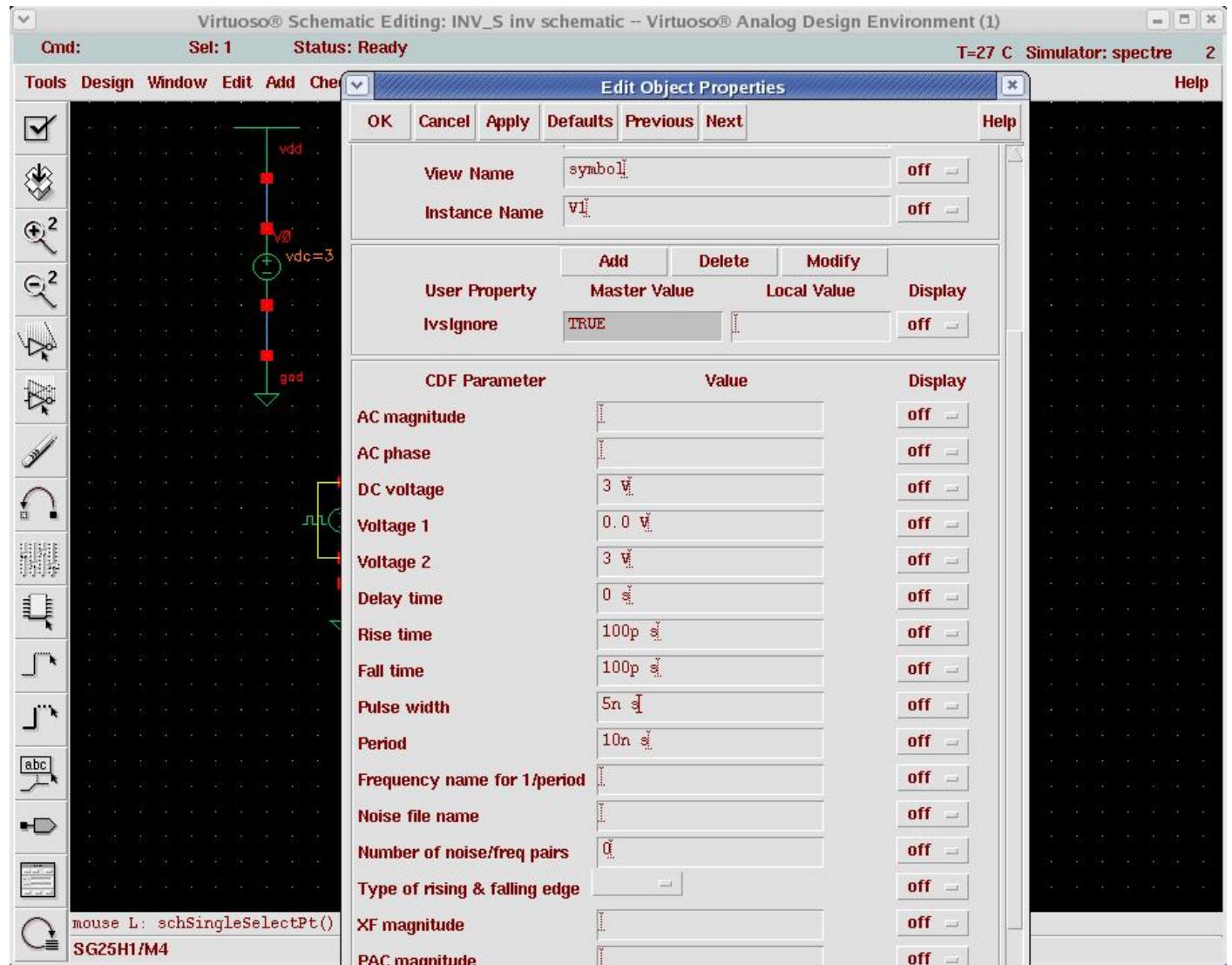


Fig 18

Same way you can set the dc value and width of pmos and nmos as shown in Fig 19, Fig 20, and Fig 21:

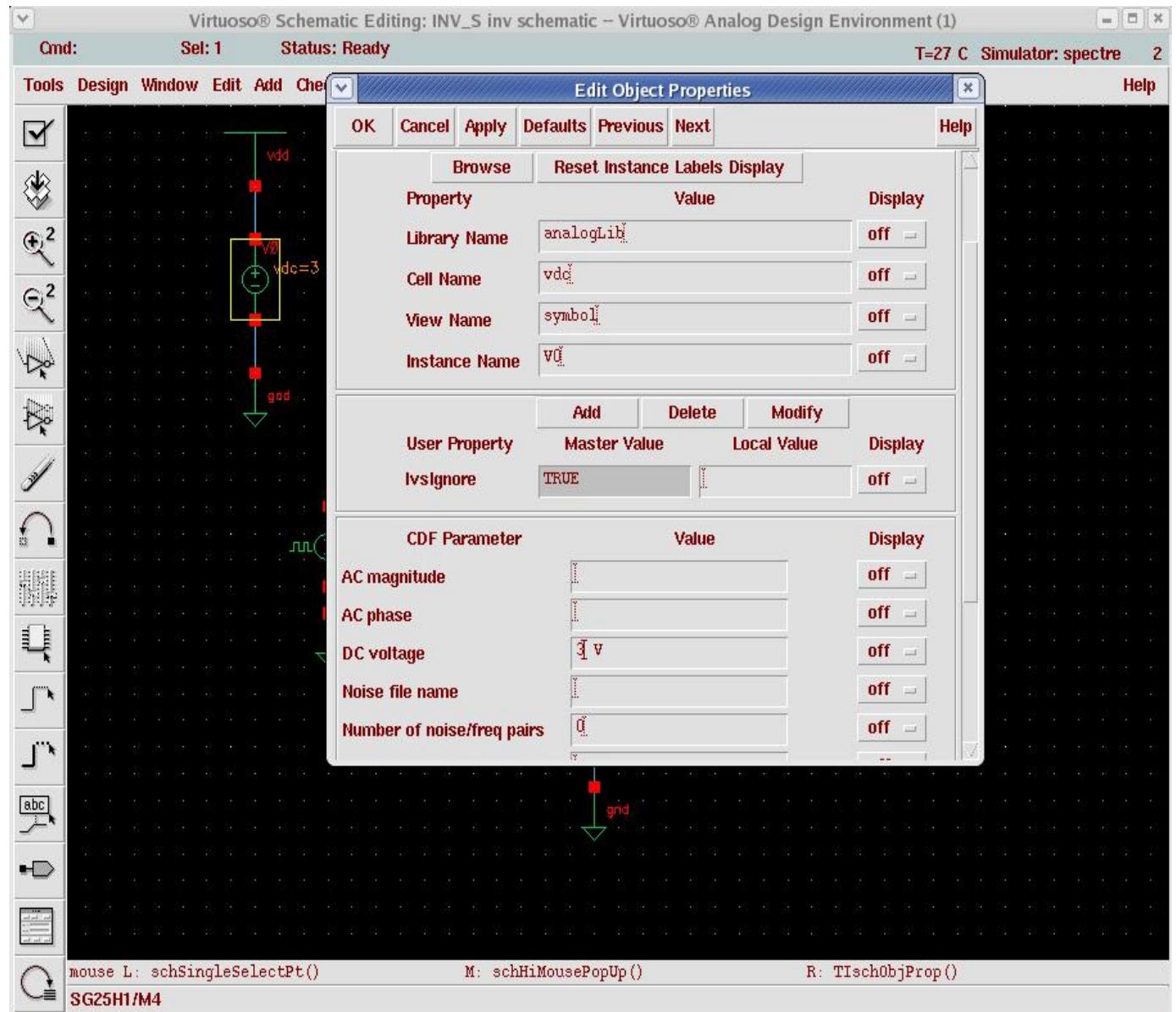


Fig 19

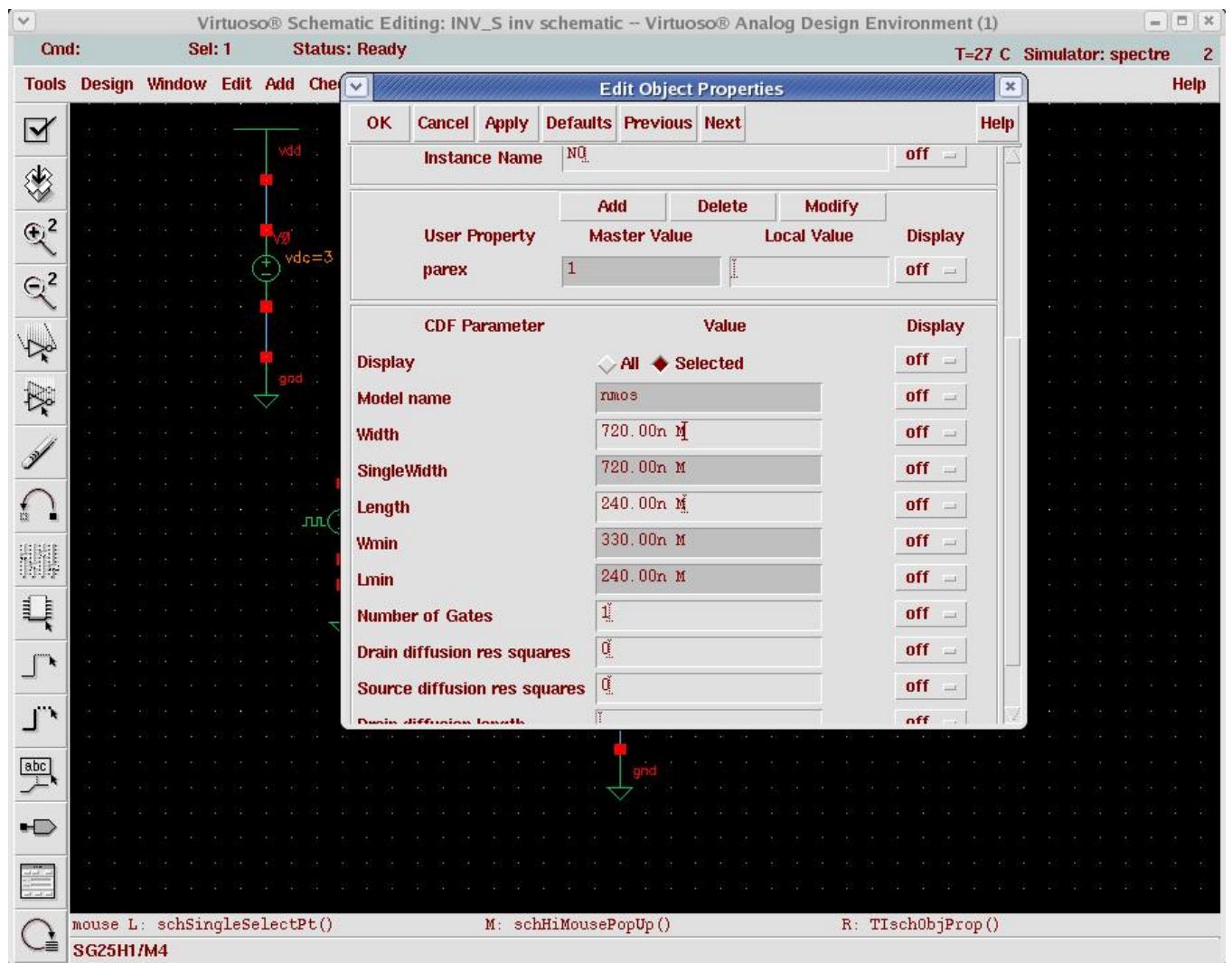


Fig 20

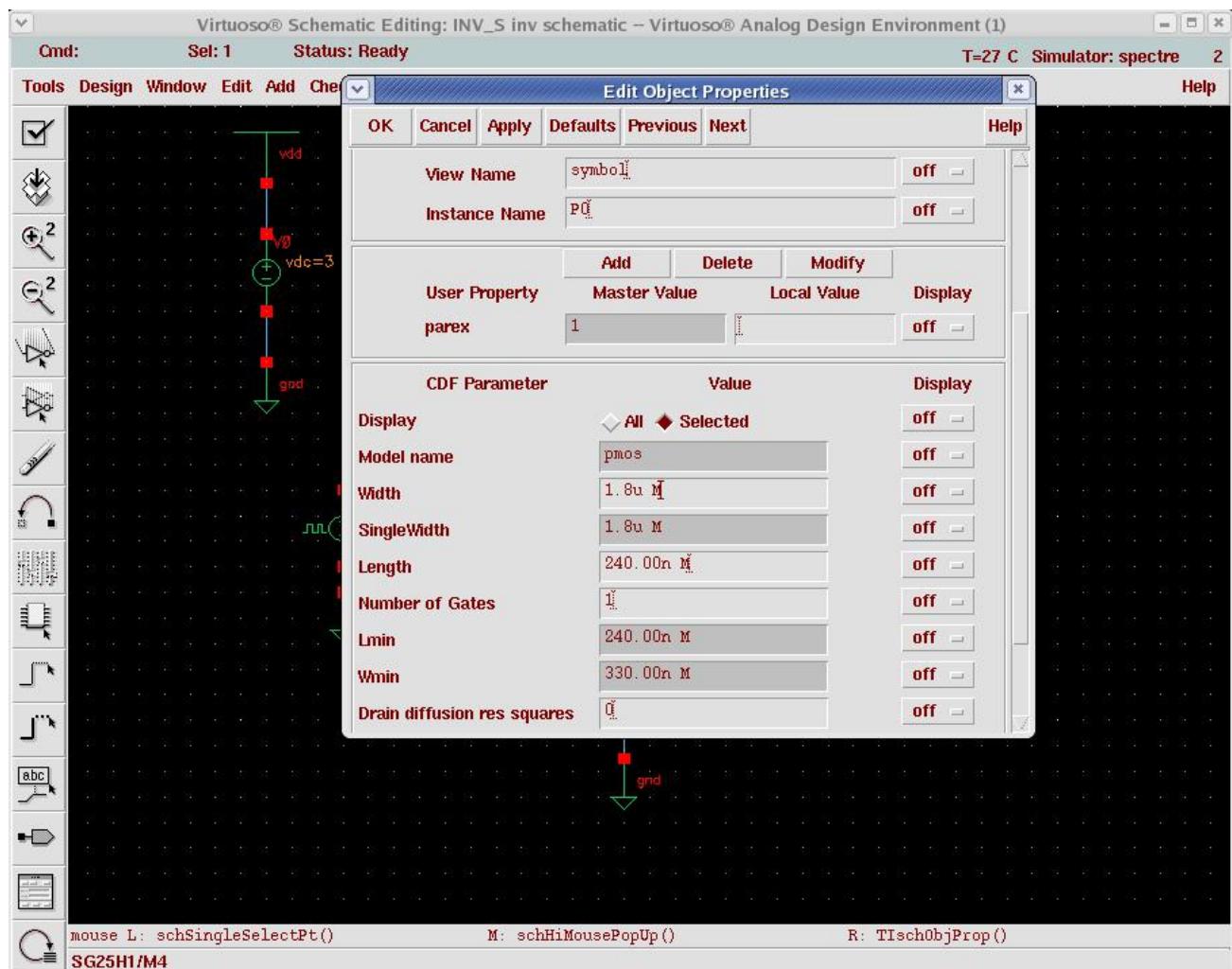


Fig 21

Then go to Design->Check and Save.

This completes your schematic.

## Simulation :

Once your schematic is checked and saved without any warning and error, you can go for simulation.

For simulation, go to Tools->Analog Environment. This will open a window as shown in Fig 22:

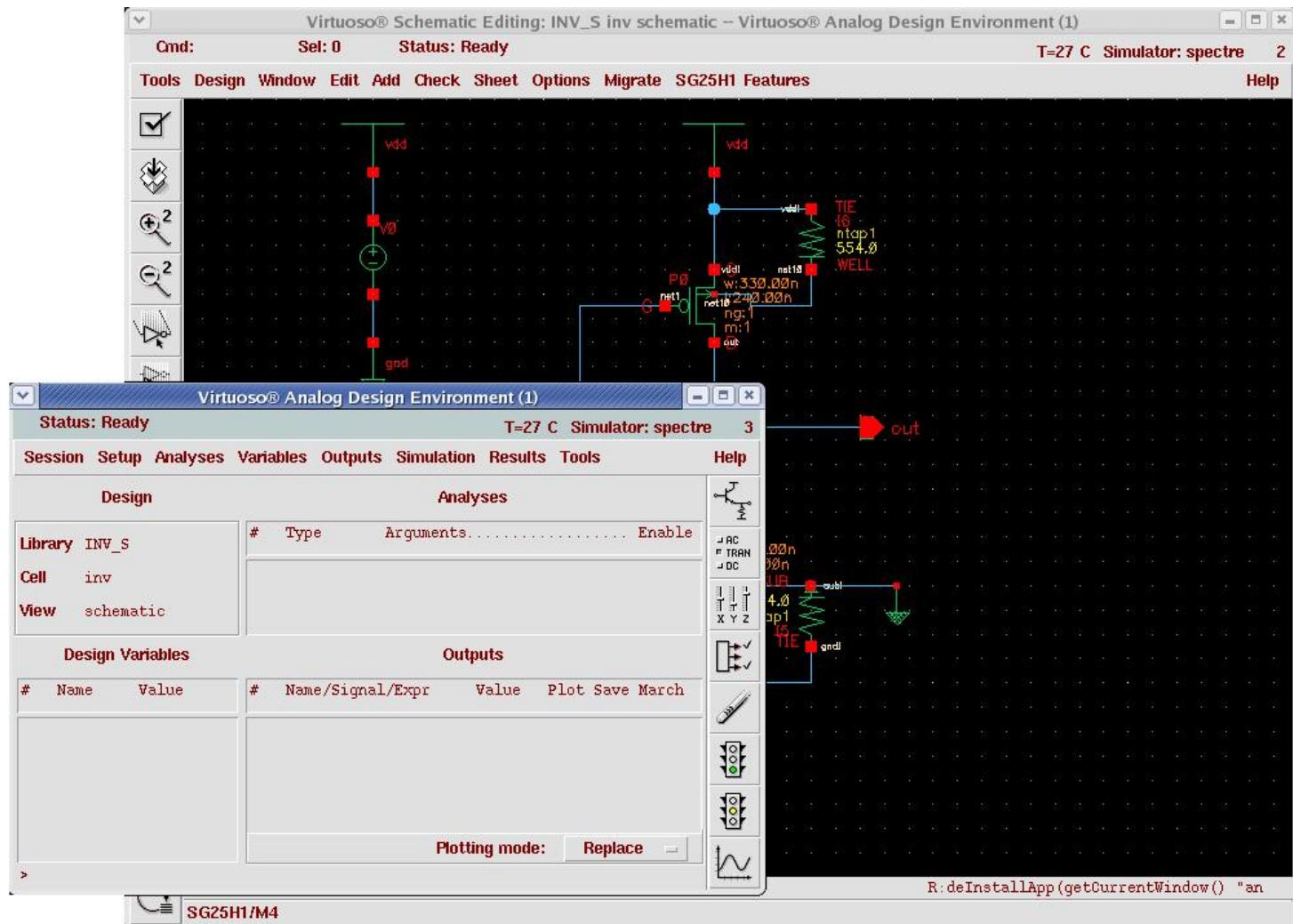


Fig 22

Now go to Analysis->Choose. You will see a window as shown in Fig 23:

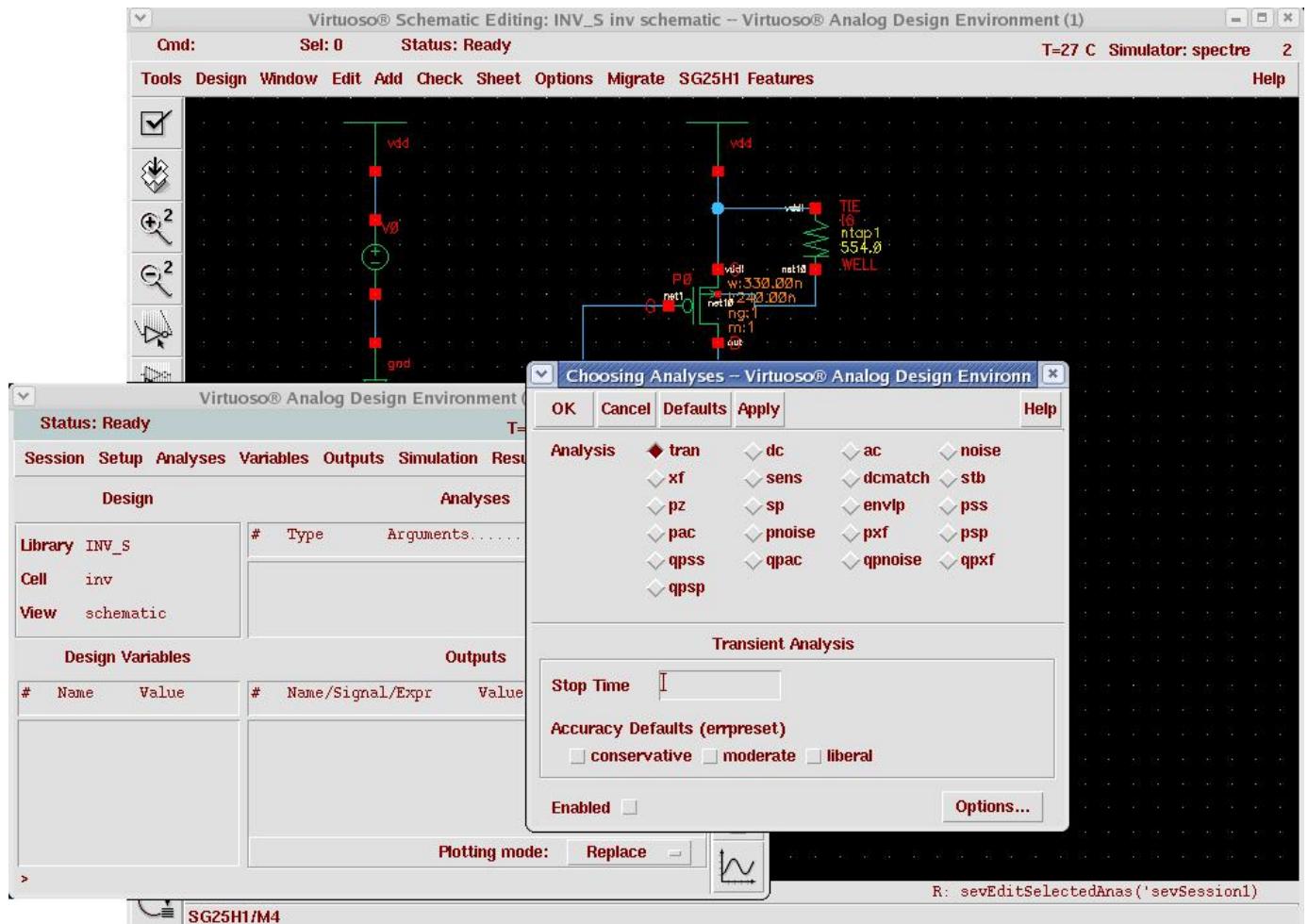


Fig 23

Select the **tran** option and set the stop time as 100n (n-nano second). Then press ok.

Now go to Outputs->To be plotted, select the nets on the schematic where you want to see the signal.

The final setup for simulation will look as shown in Fig 24:

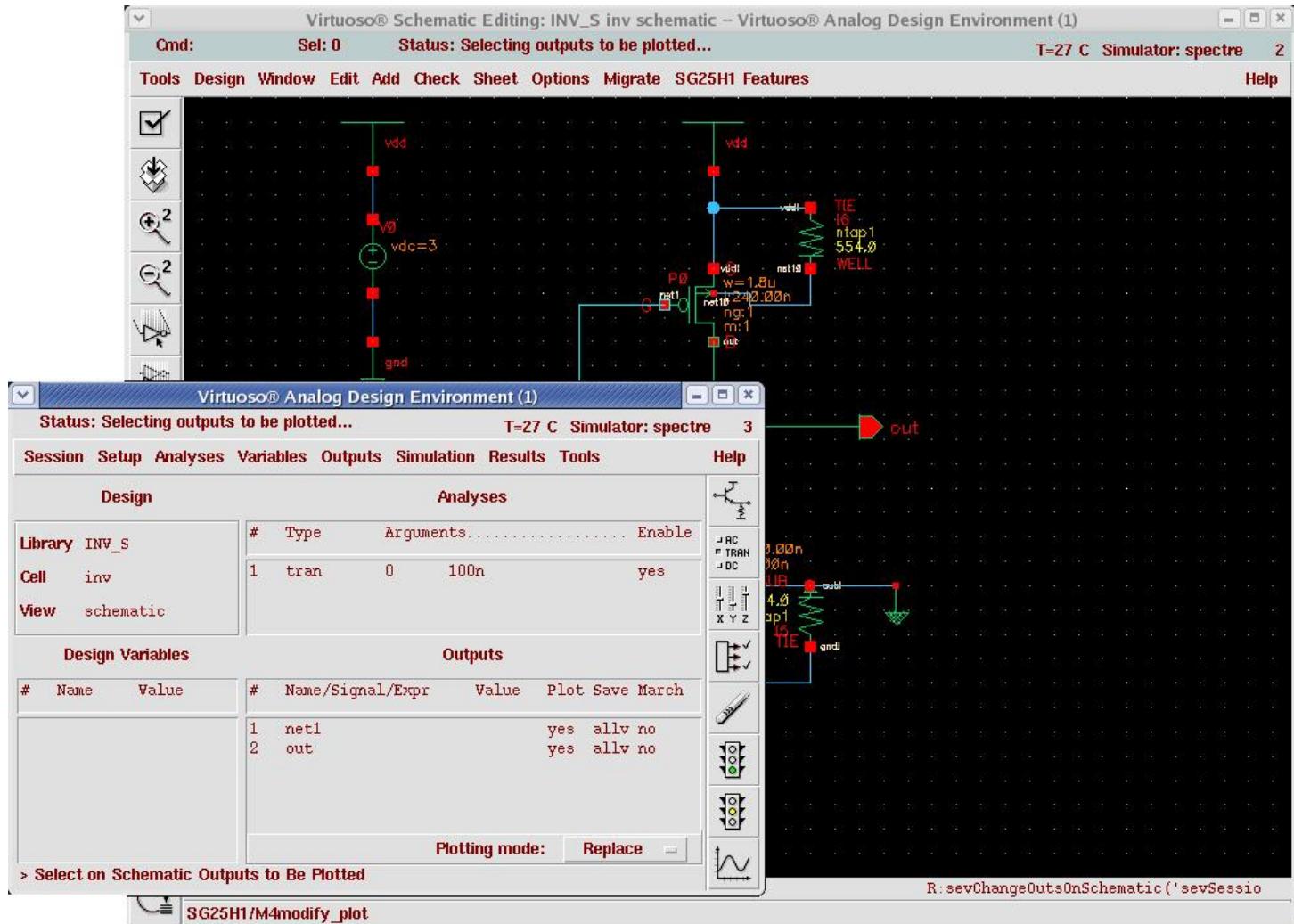


Fig 24

Now press the **Green signal button** for running the simulation.

This will open a window, which will show you the run details. This is as shown in Fig 25:

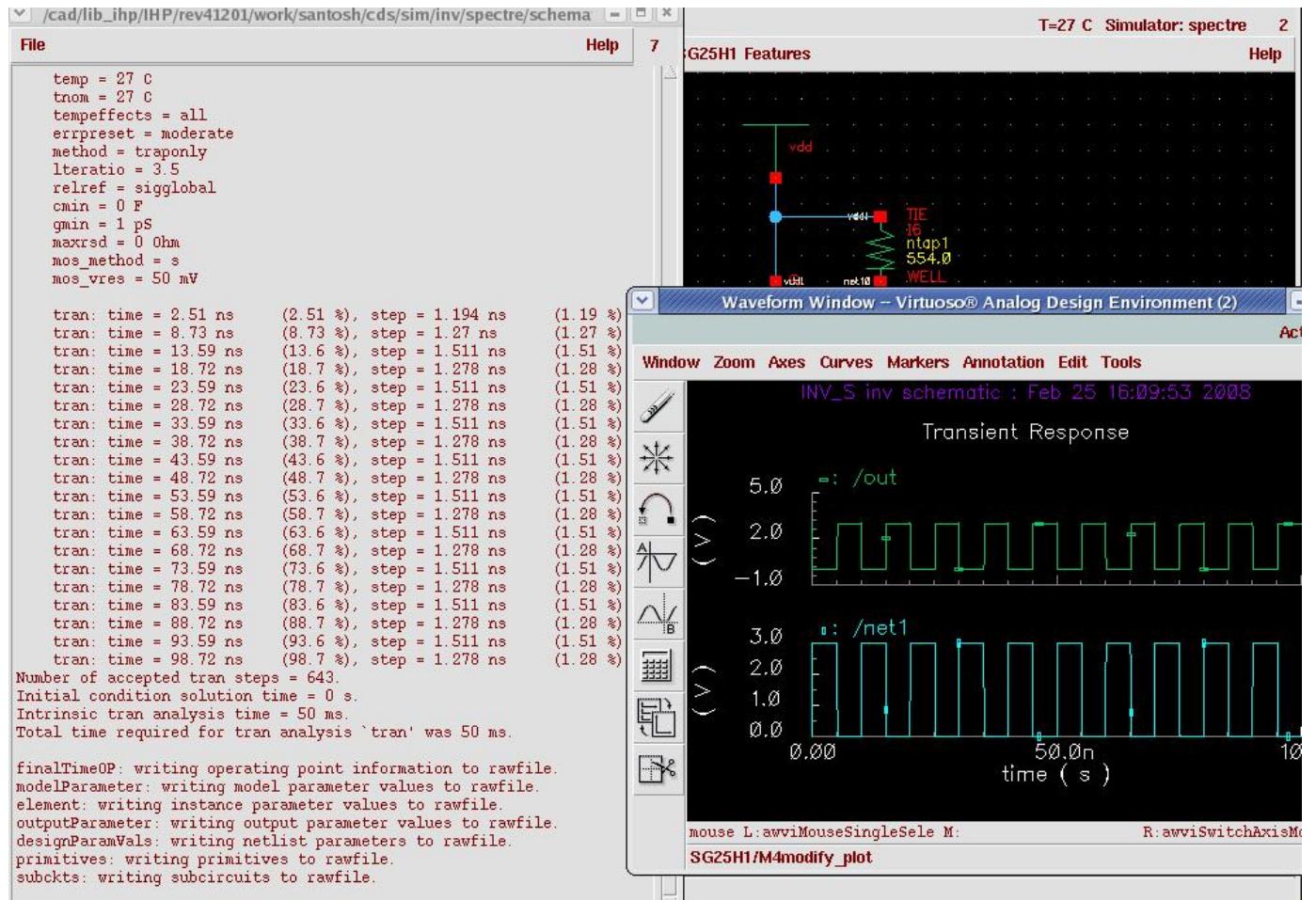


Fig 25

Once your simulation will over, you can see the waveform as shown above.

### Symbol creation:

First of all, remove all the sources (Voltage, Current) and connect the pins to all the terminals as shown in Fig 26:

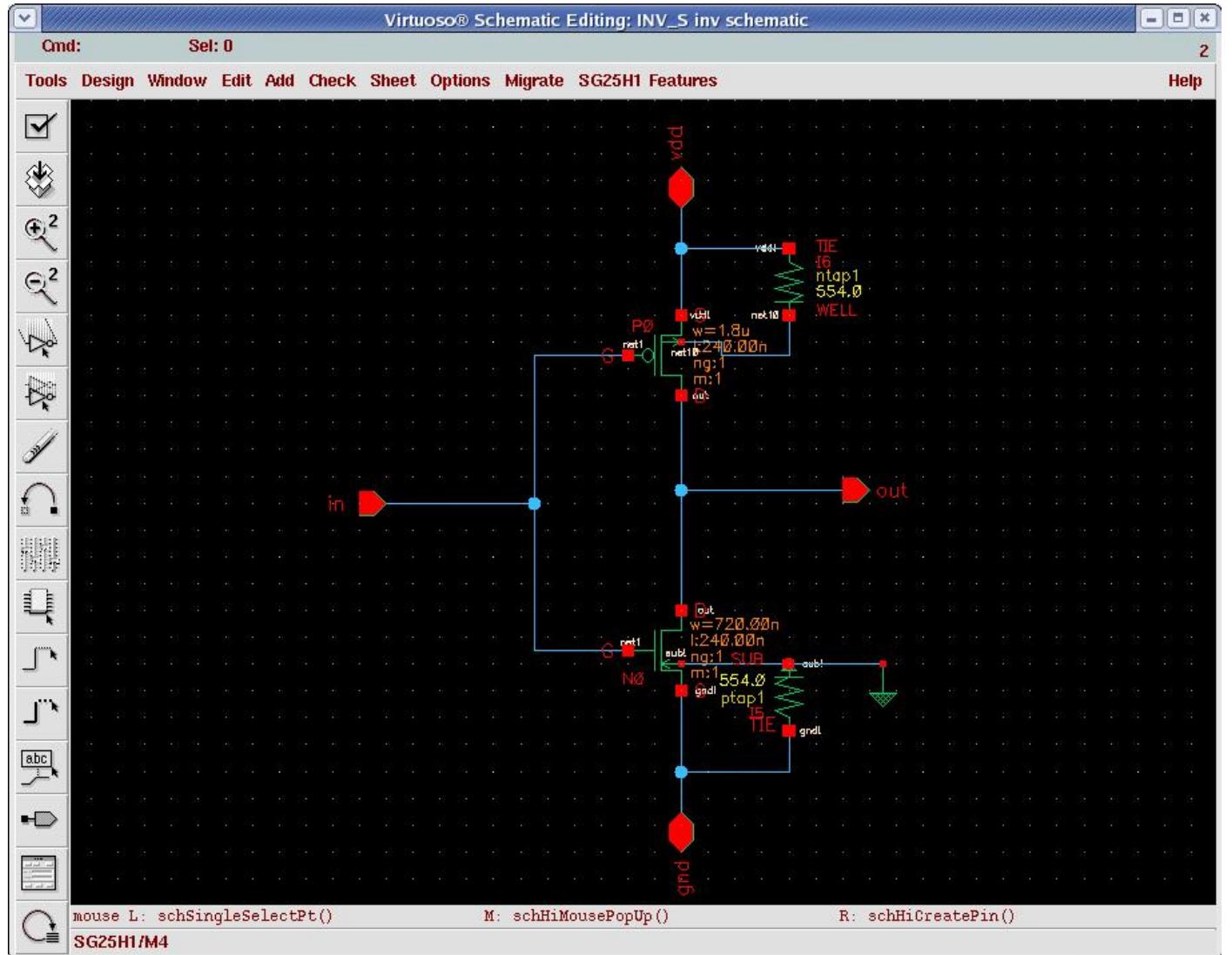


Fig 26

Now go to Design->Create cellview->From Cellview. This will open the window shown in Fig 27:

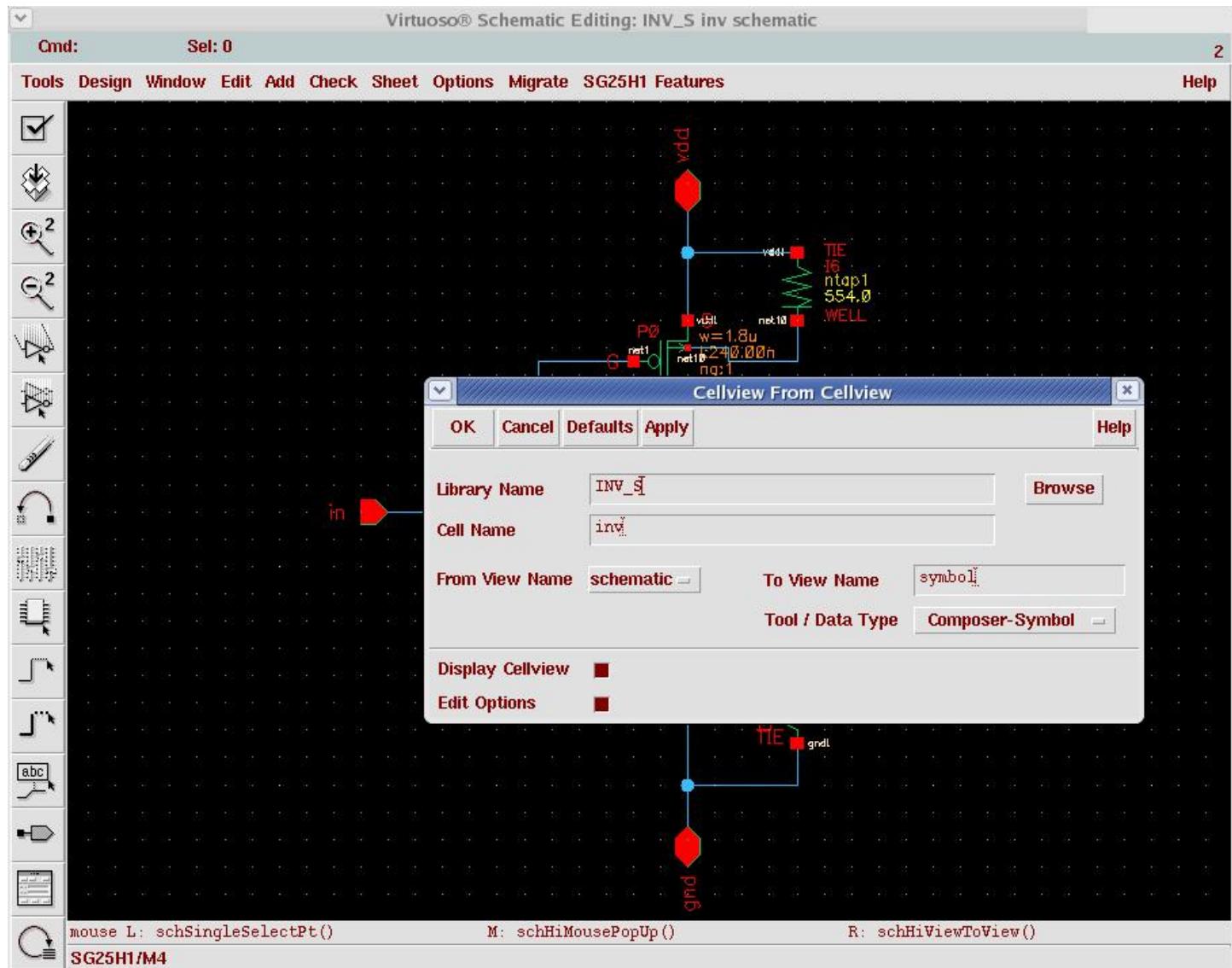


Fig 27

Just press ok to see the symbol generation window.

Now change the gnd pin from Top pins to Bottom pins, then press ok. This will create a symbol as shown in Fig 28:

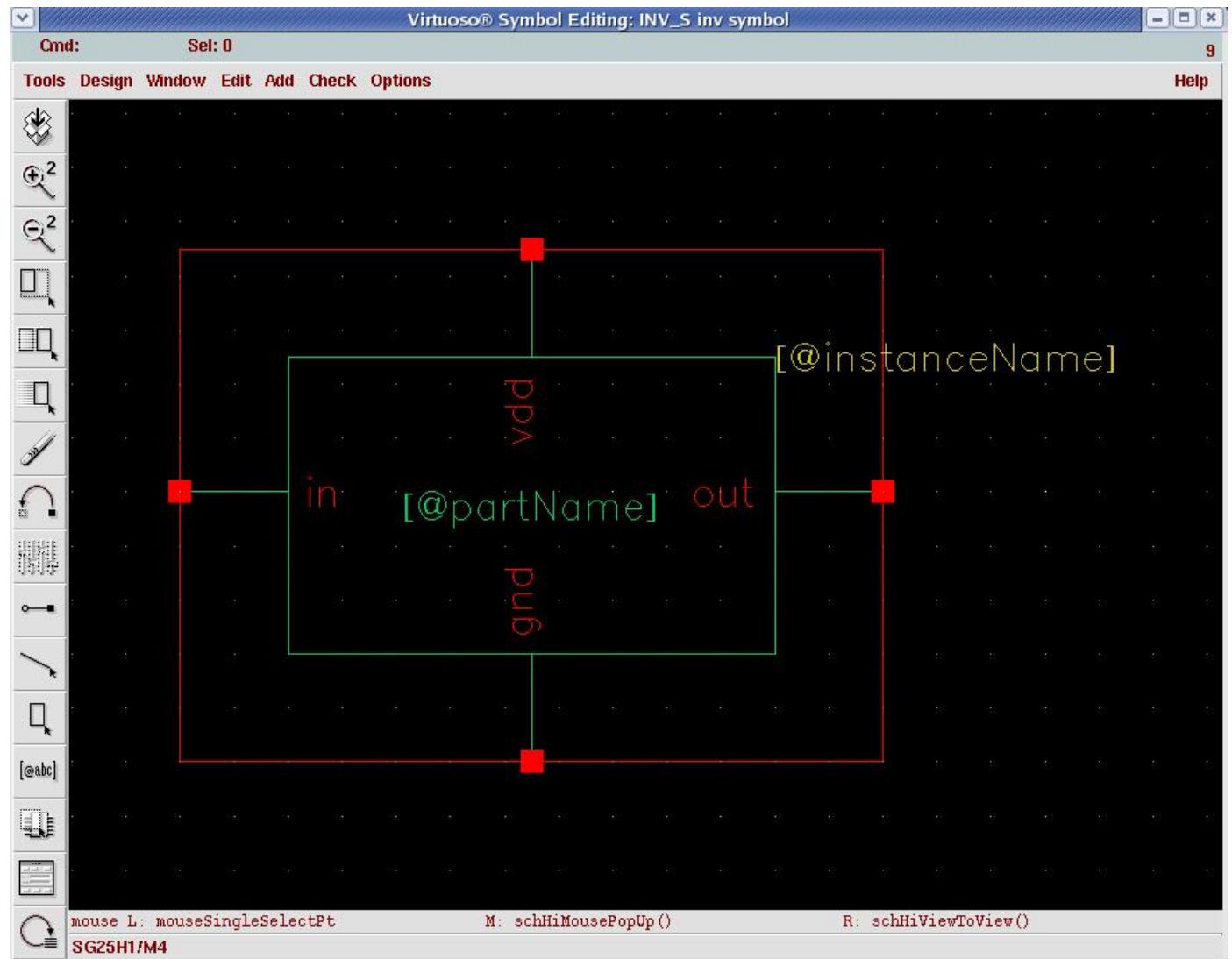


Fig 28

Now go to design->check and save. Then close this window.

---

## Schematic driven Layout:

In the schematic window select Tools->Design Synthesis->Layout XL. This will open a window as shown in Fig 29:

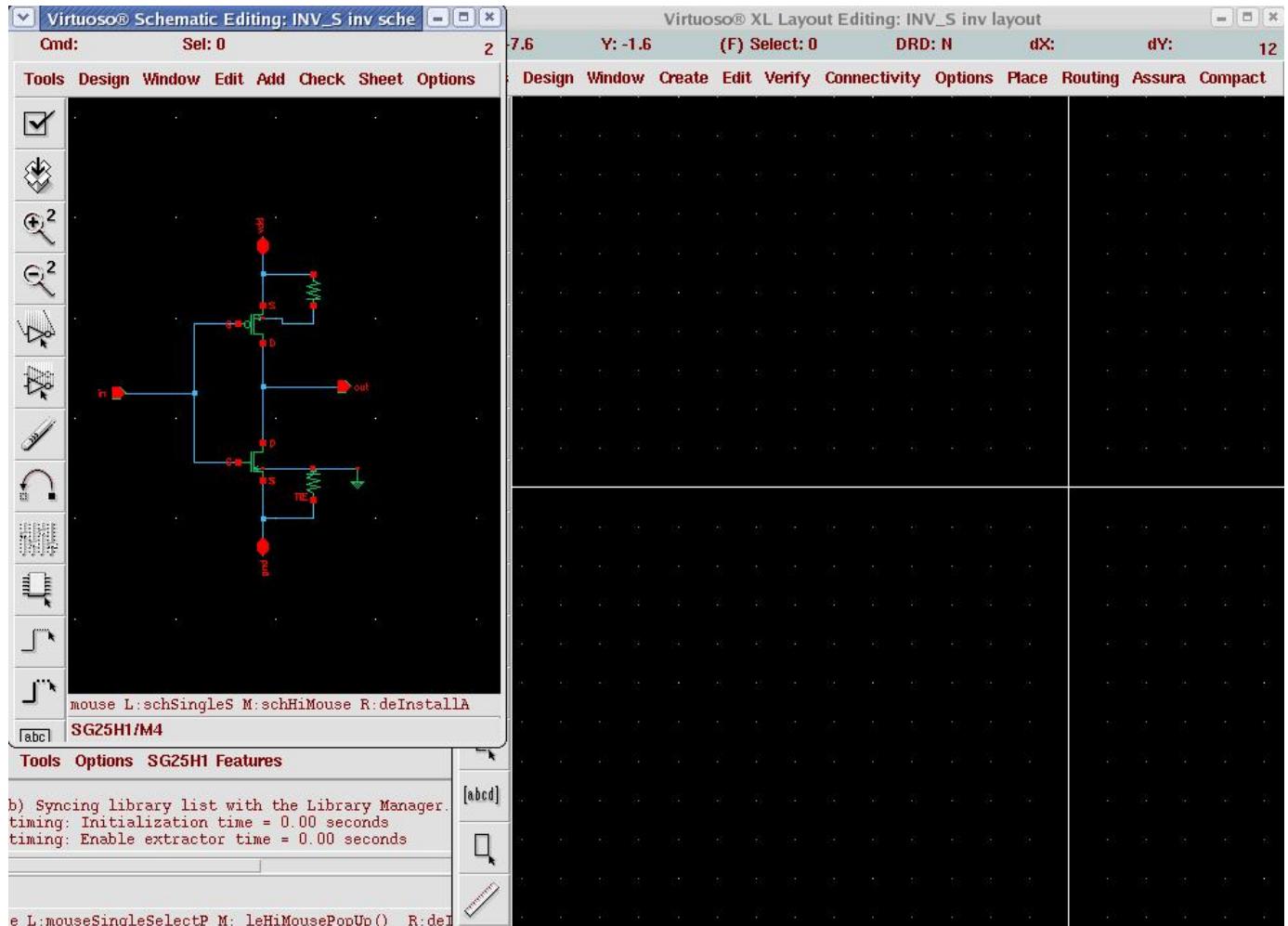


Fig 29

Select the option "create new" and press ok. Then a "create new file window" will open. Just press ok.

This will open the Virtuoso XL Layout Editor as shown in Fig 30:

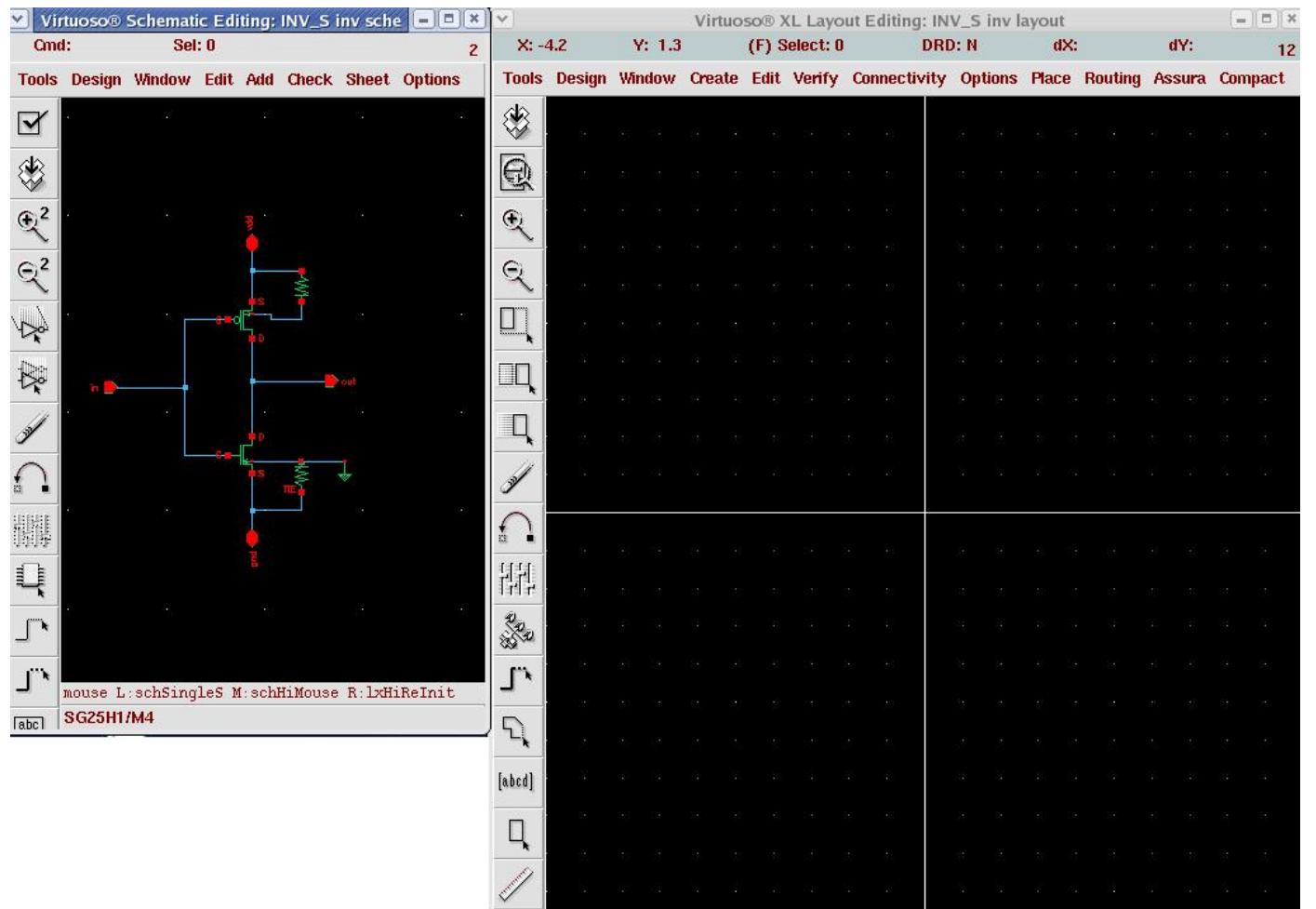


Fig 30

Now go to this Layout editor-> Design->Gen from source. This will open a window as shown in Fig 31:

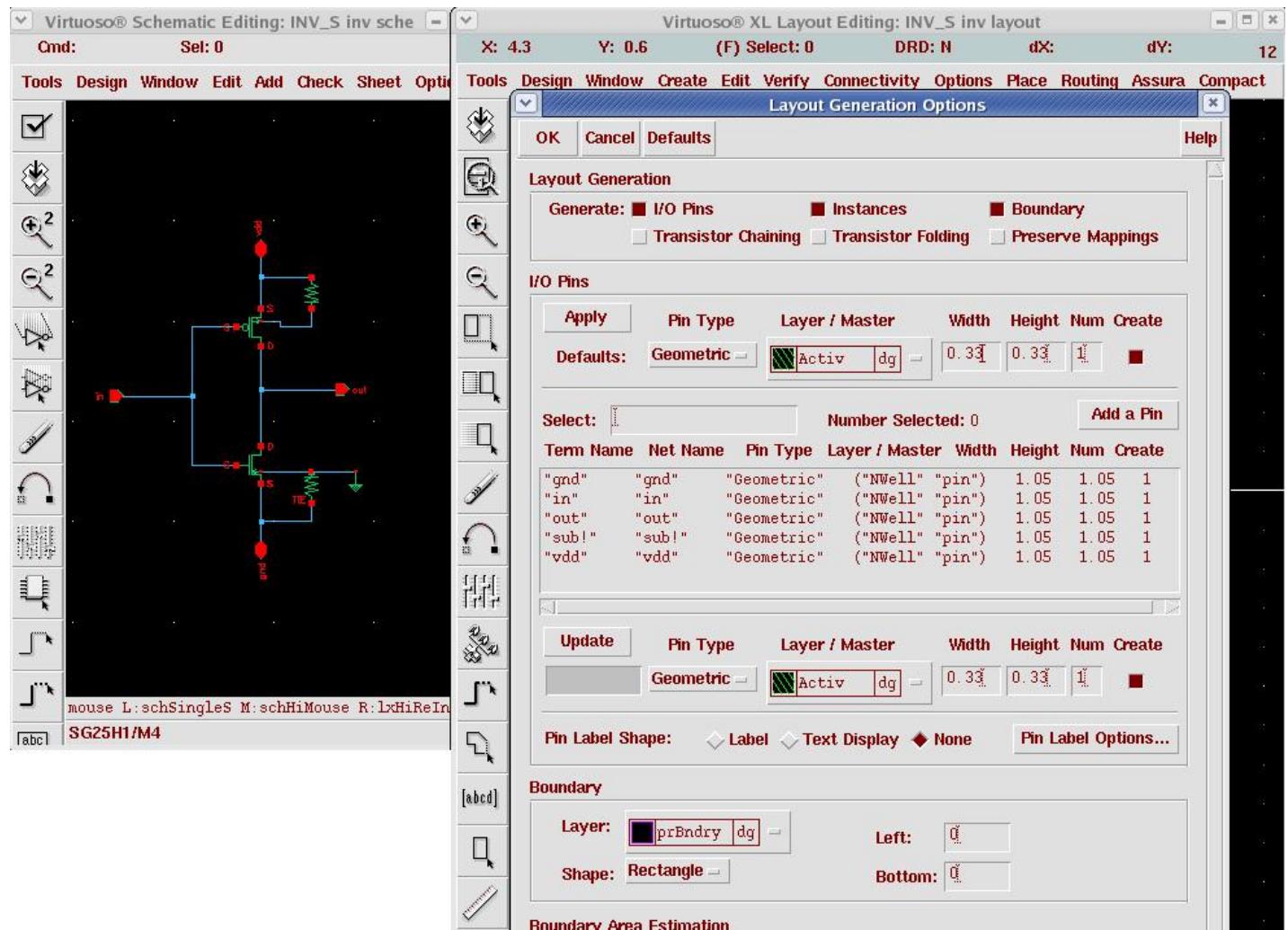


Fig 31

In the I/O pins option, change the Active dg to Metal pn as shown in Fig 32:

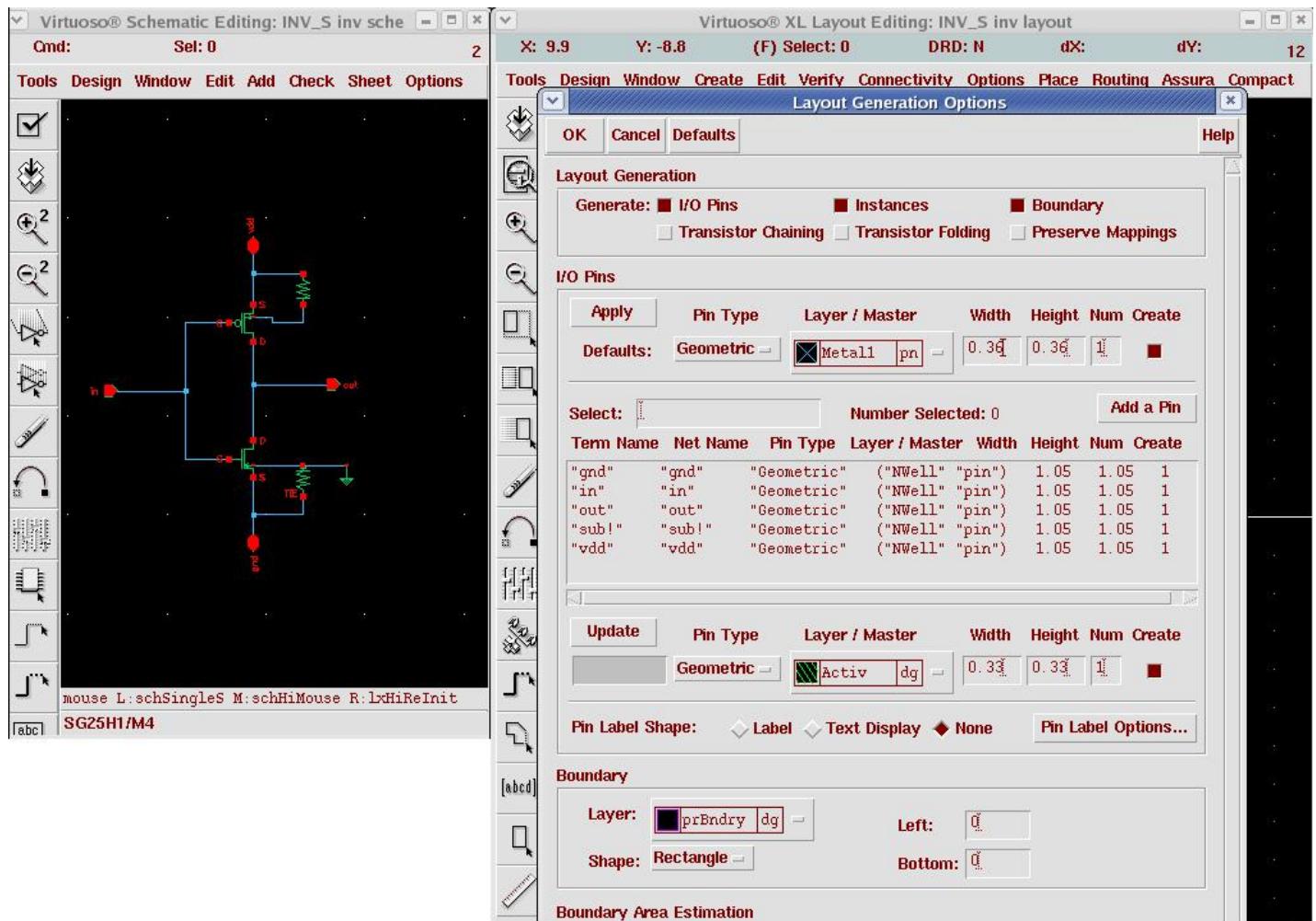


Fig 32

Then press "apply" and "ok". Now you can see the components in the layout editor as shown in Fig 33:

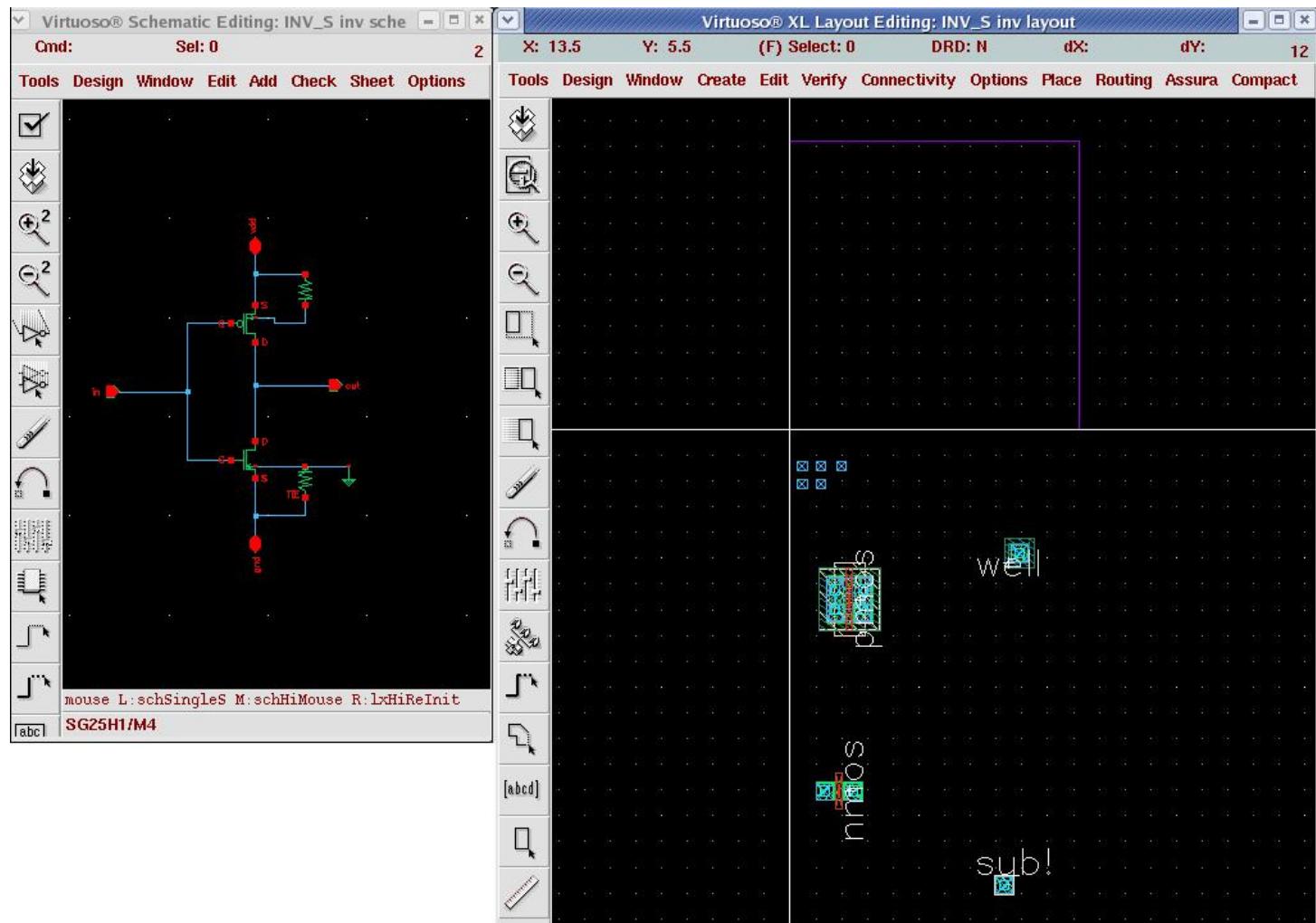


Fig 33

Now drag these components and place as in schematic. This is shown in Fig 34:

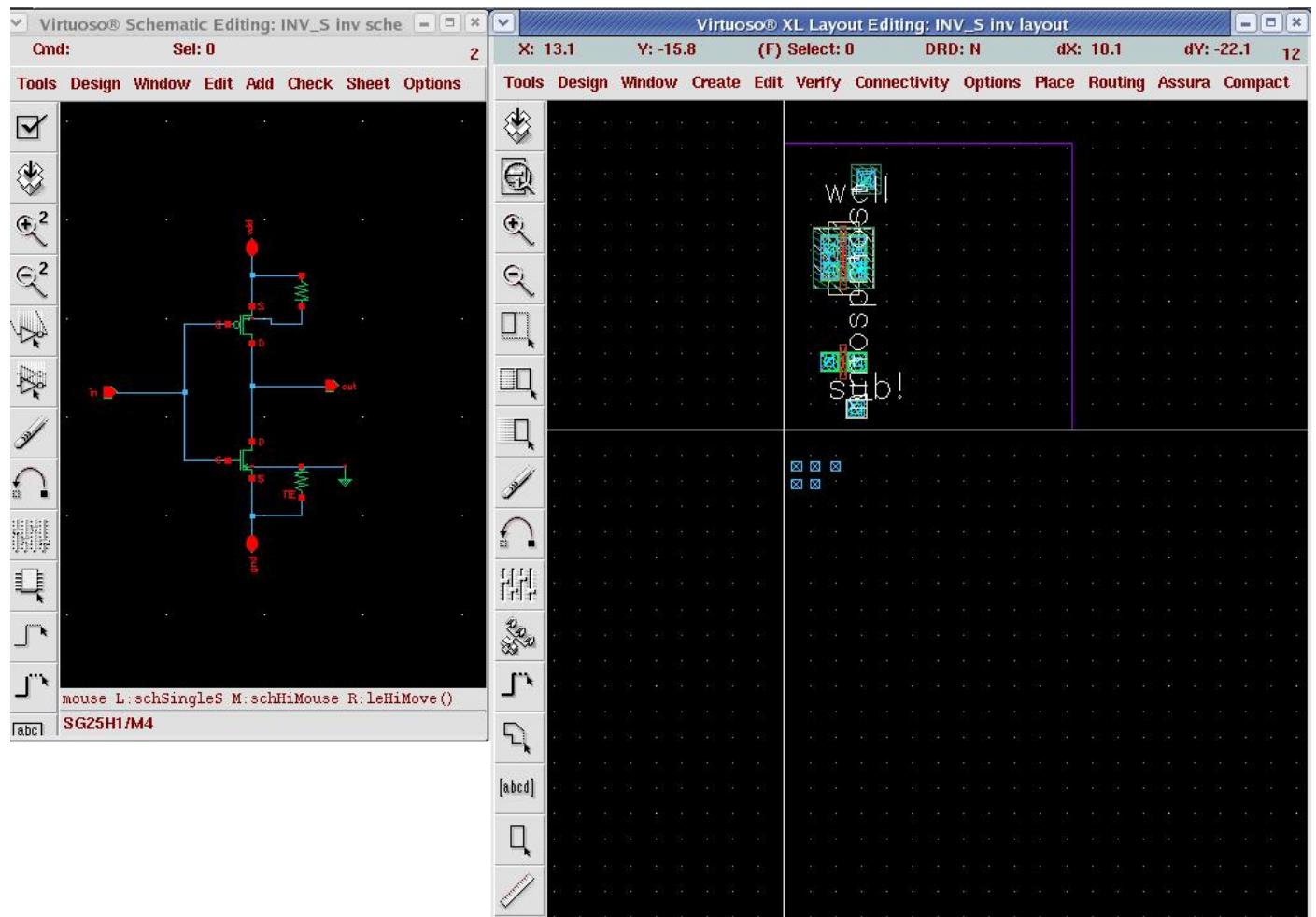


Fig 34

To move the components, first select the component, then press "m" then drag it.

Now set the grid to 0.01 micron. For this, go to Option->Display. This will open a window as shown in Fig 35:

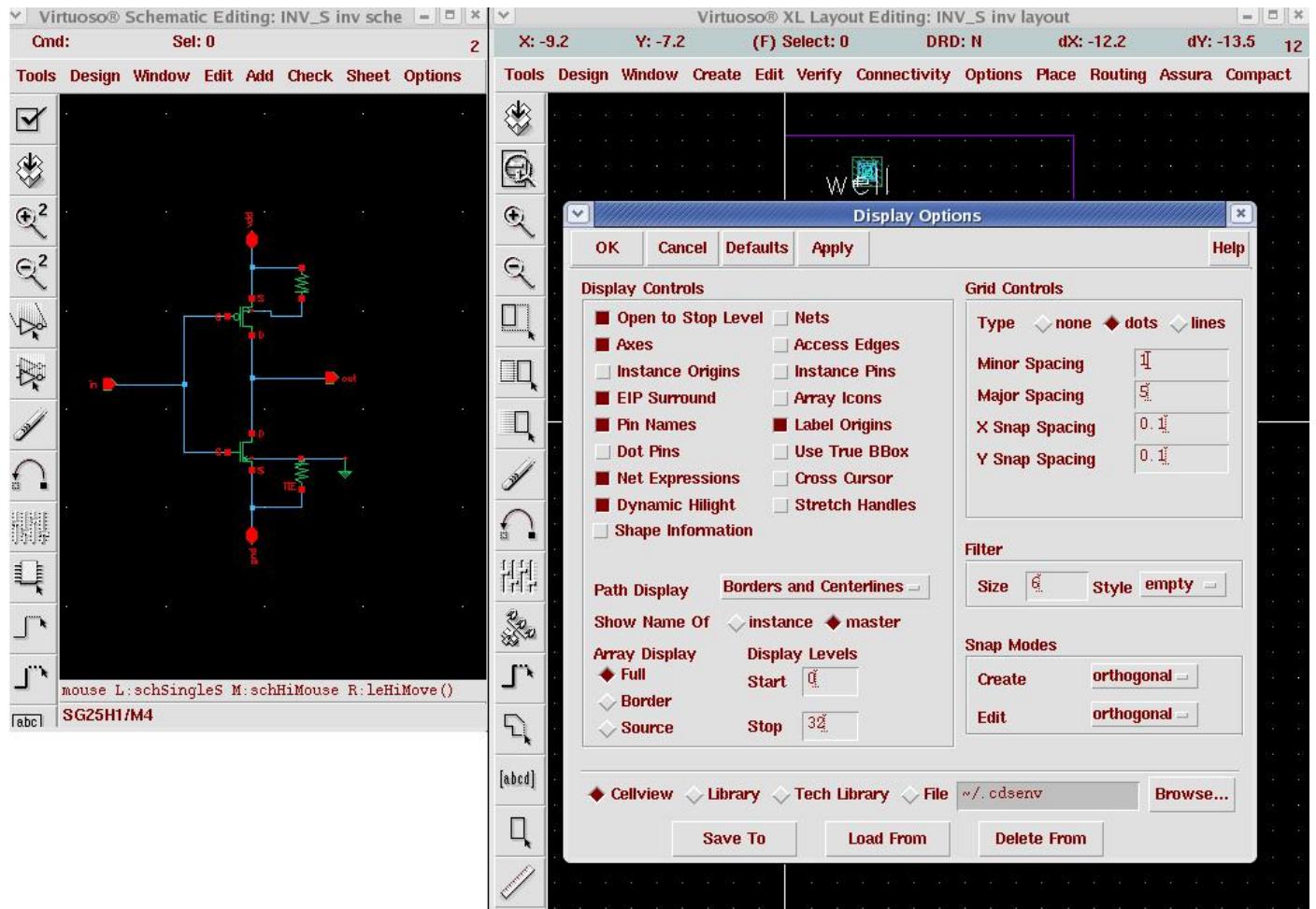


Fig 35

Now set the X Snap Spacing to 0.01 and Y Snap Spacing to 0.01. Then press apply and ok.

#### Short cuts

Zoom in : Ctrl z

Zoom out : Shft z

Fit : f

Now do the interconnections with different layers as shown in Fig 36:

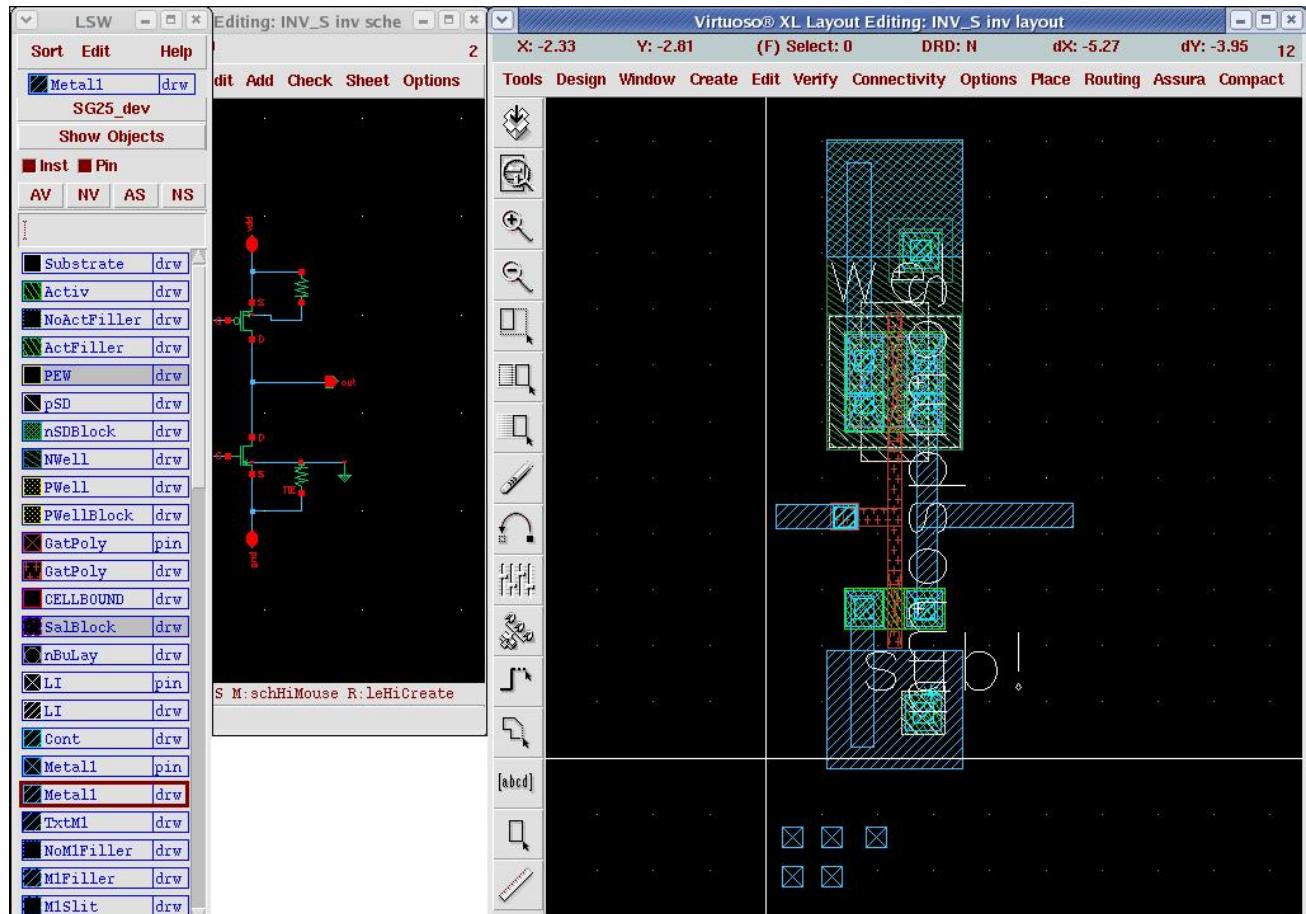


Fig 36

Follow the design rules properly while doing the layout.

For creating the contact, go to create contact. This will open a window as shown in Fig 37:

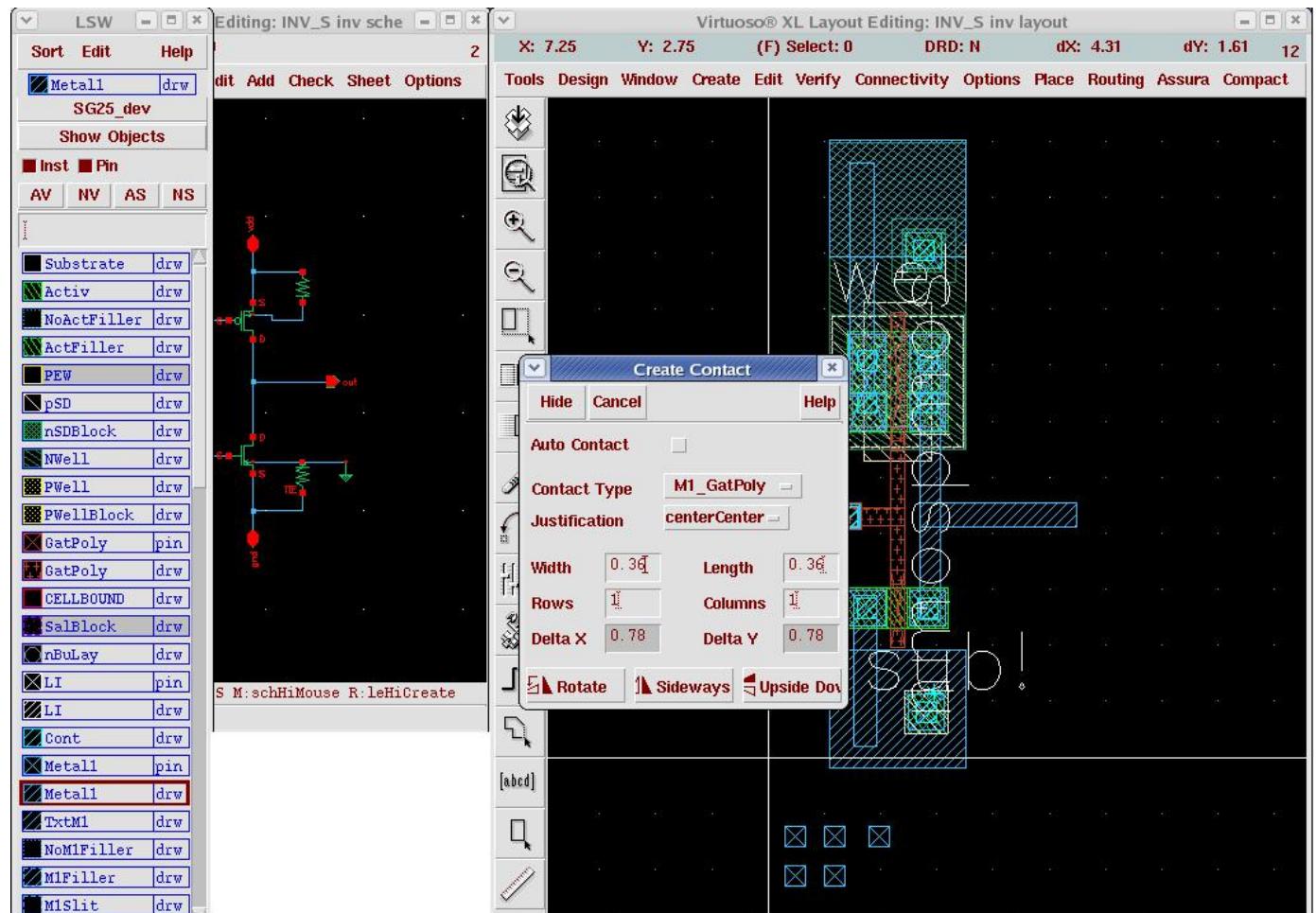


Fig 37

Select the proper contact type required for your design.

Now you have to place the pins at the appropriate place. This is as shown in Fig 38:

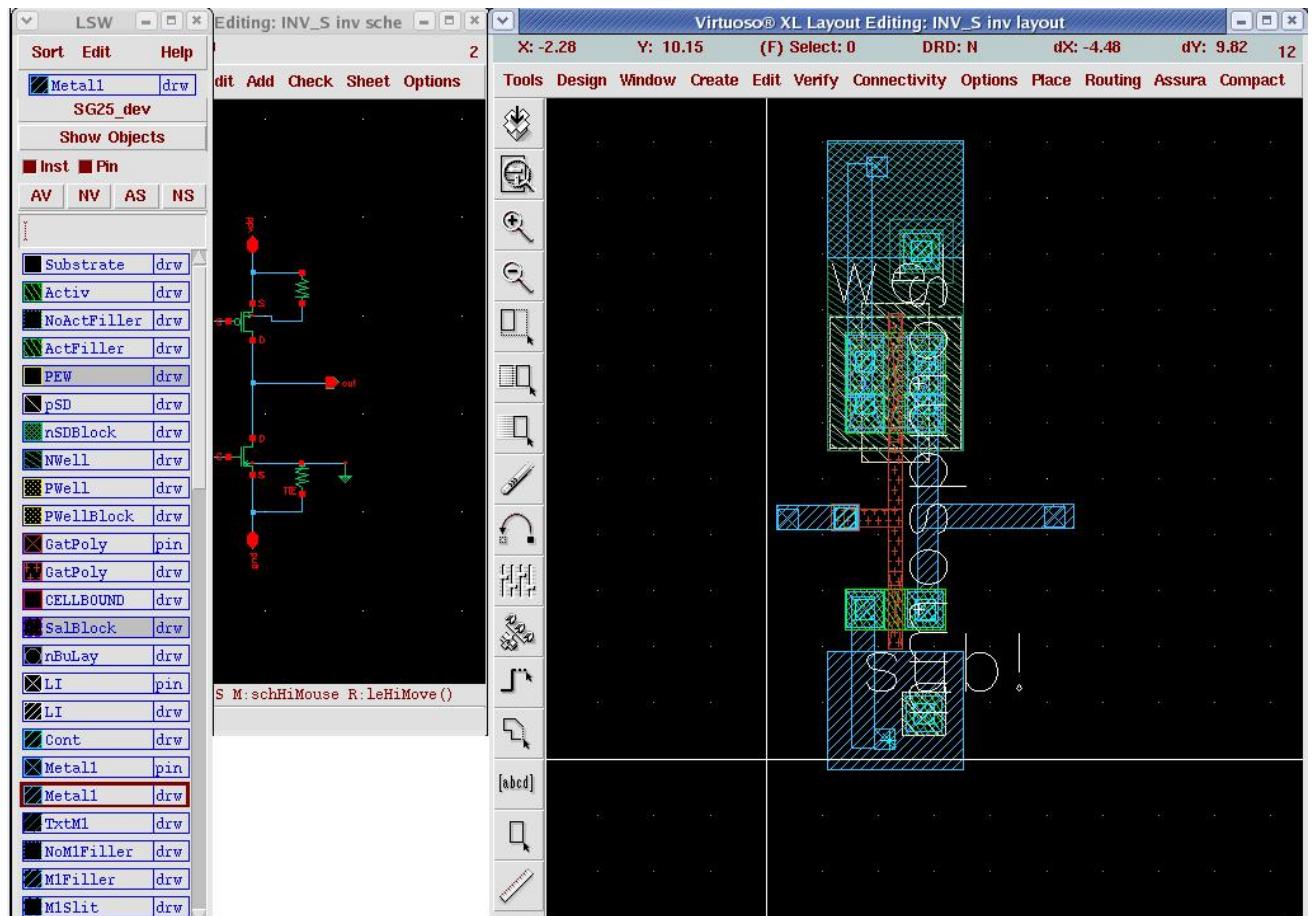


Fig 38

Here "sub!" pin is not required, so just delete it.

Now your Layout is ready. For more readability, just give the levels to all the pins as shown in Fig 39:

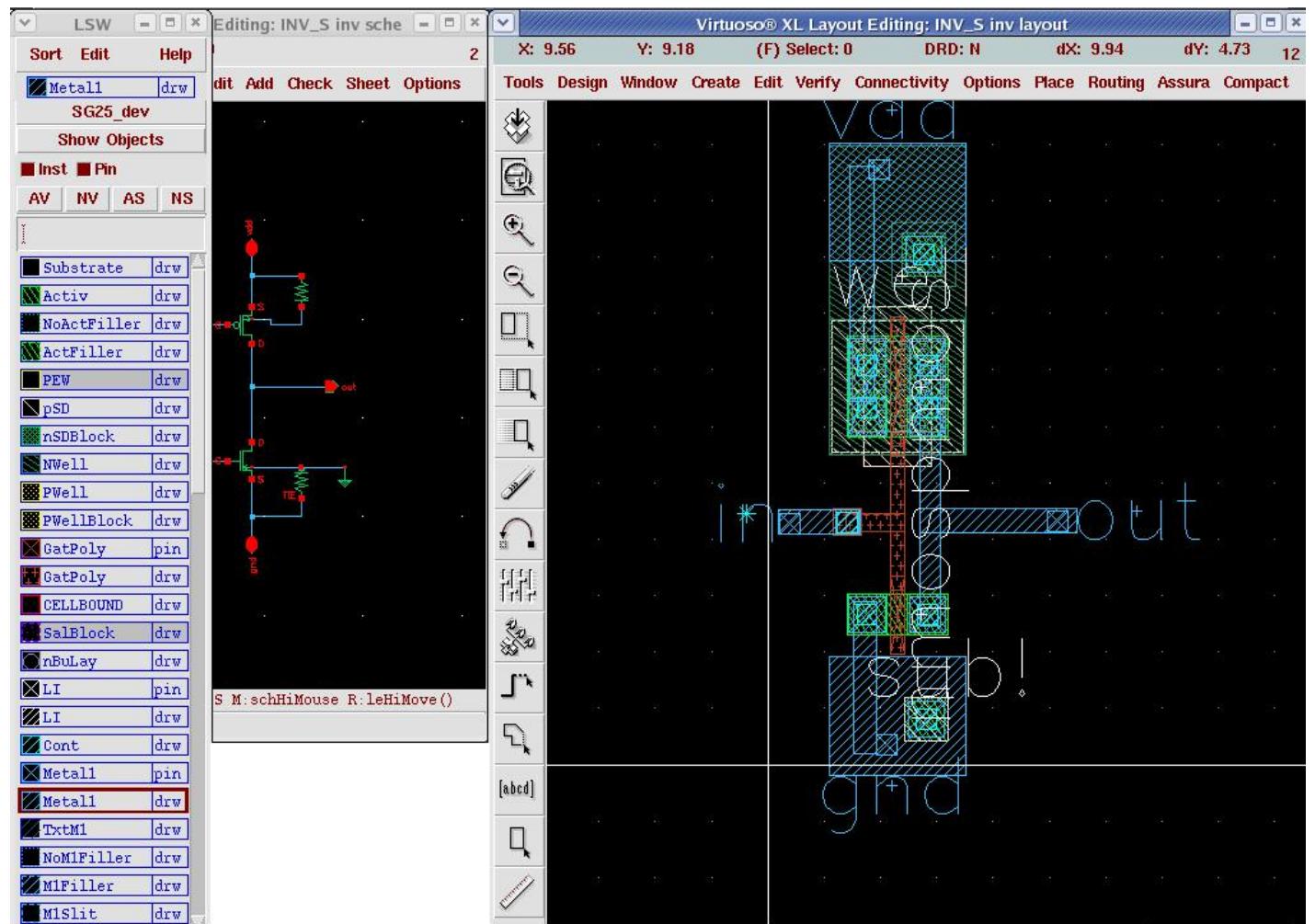


Fig 39

Now save the layout.

---

## DRC: (Design Rule Check)

For checking DRC, go to Assura->RUN DRC. This will open a window as shown in Fig 40:

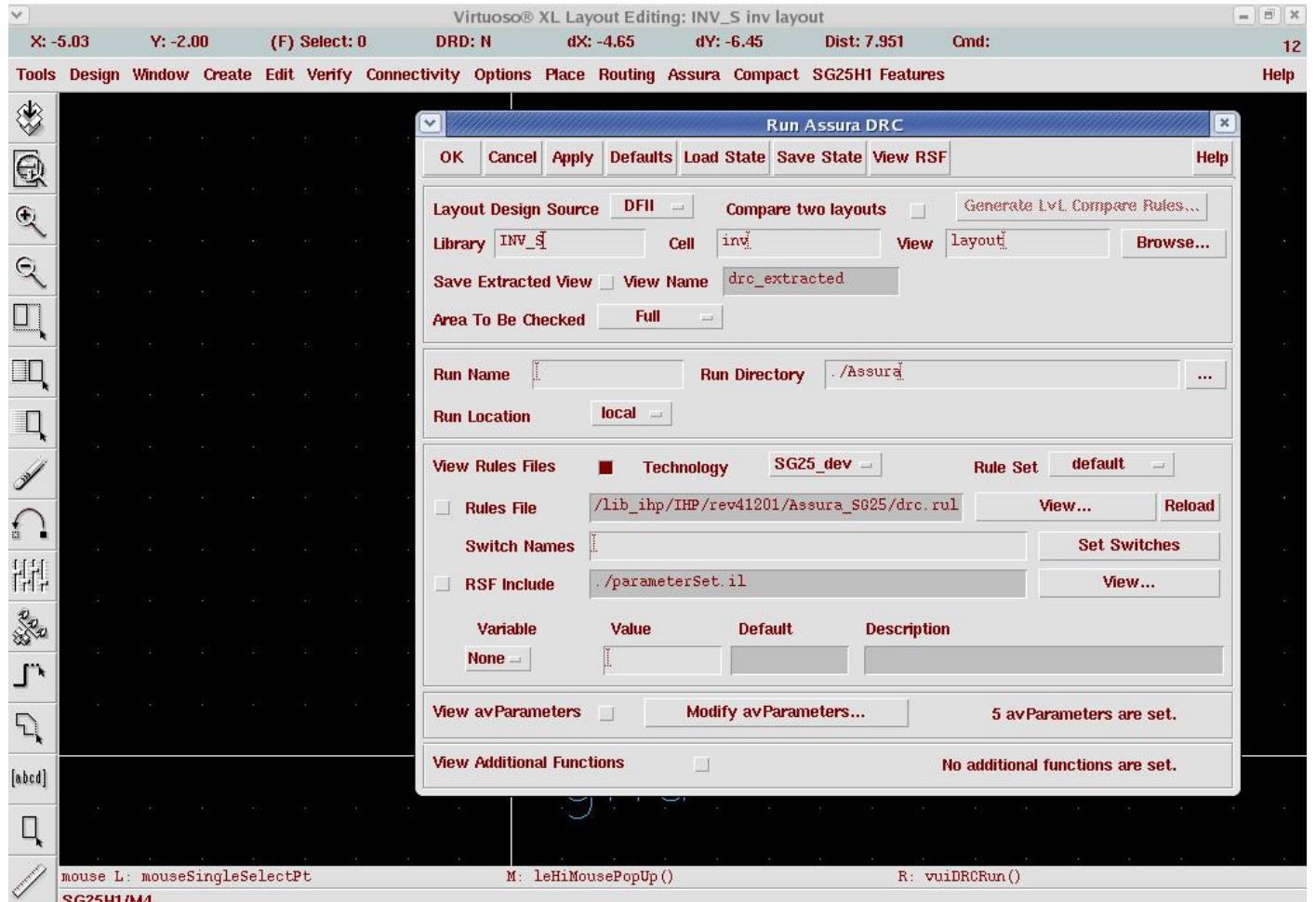


Fig 40

Press ok to run the DRC. If the layout is done perfectly, then it will show no drc errors.

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## LVS: (Layout Vs Schematic)

To run the LVS, go to Assura->RUN LVS. This will open a window as shown in Fig 41:

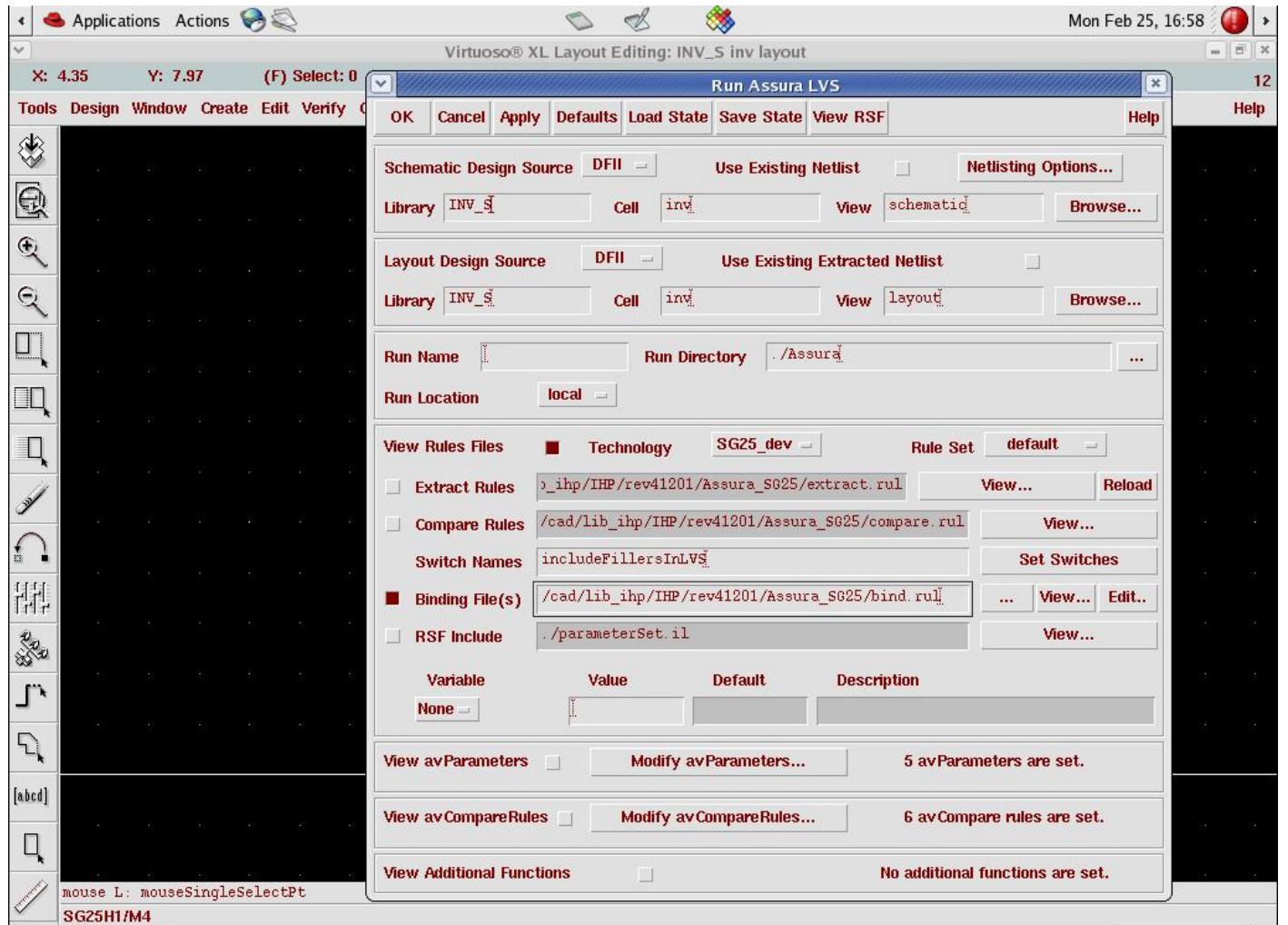


Fig 41

Press ok to run the LVS. If all the connections and components in schematic and layout are matched properly, then this LVS run show that schematic and layout are matched.

## RCX: (Parasitic Extraction)

To run the parasitic extraction, go to Assurs->RUN RCX. This will open a window as shown in Fig 42:

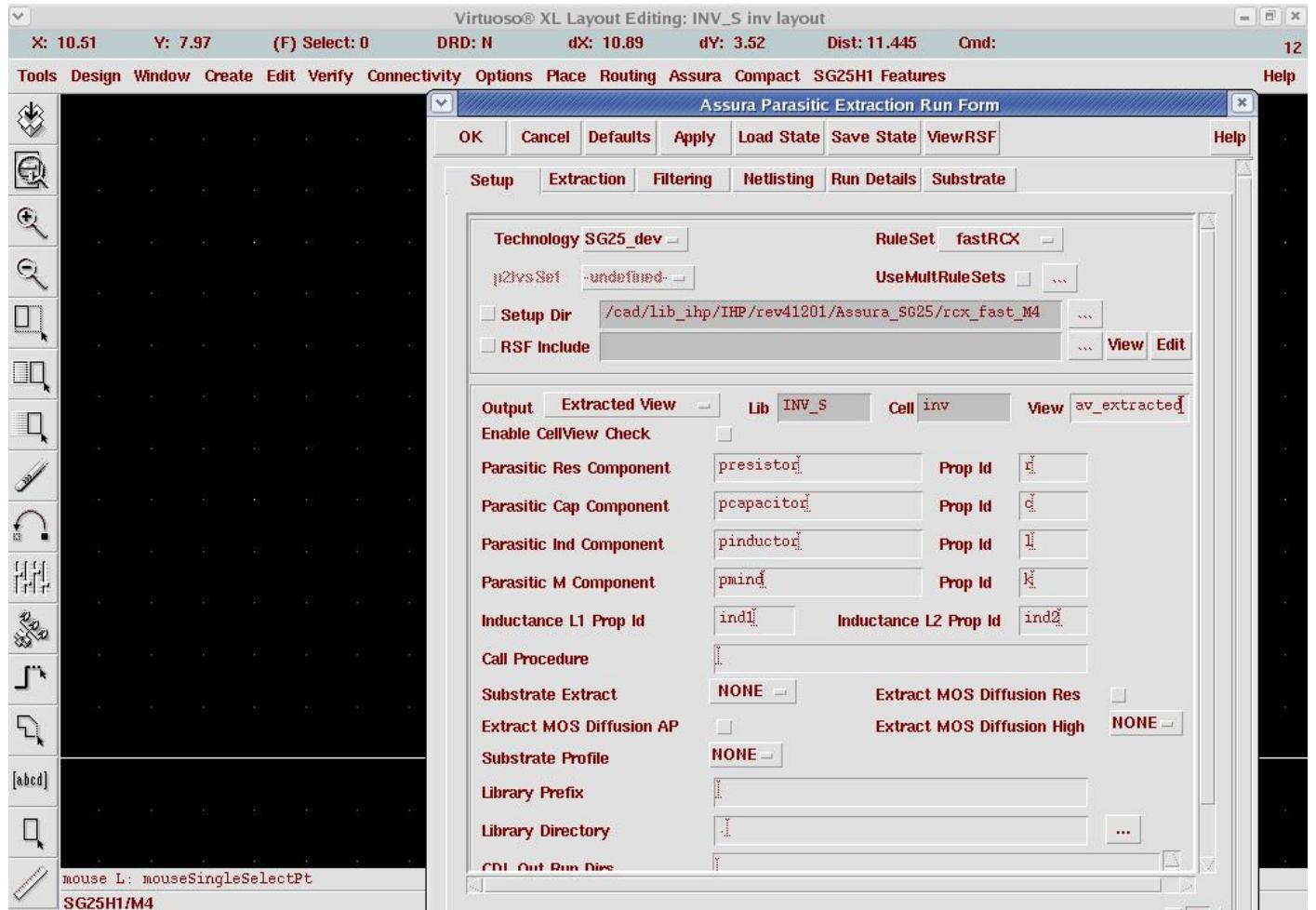


Fig 42

Now go to the Extraction option, set the Extraction mode to RC. Then press ok to run the RCX.

Once it will be completed successfully, it will show a message as shown in Fig 43:

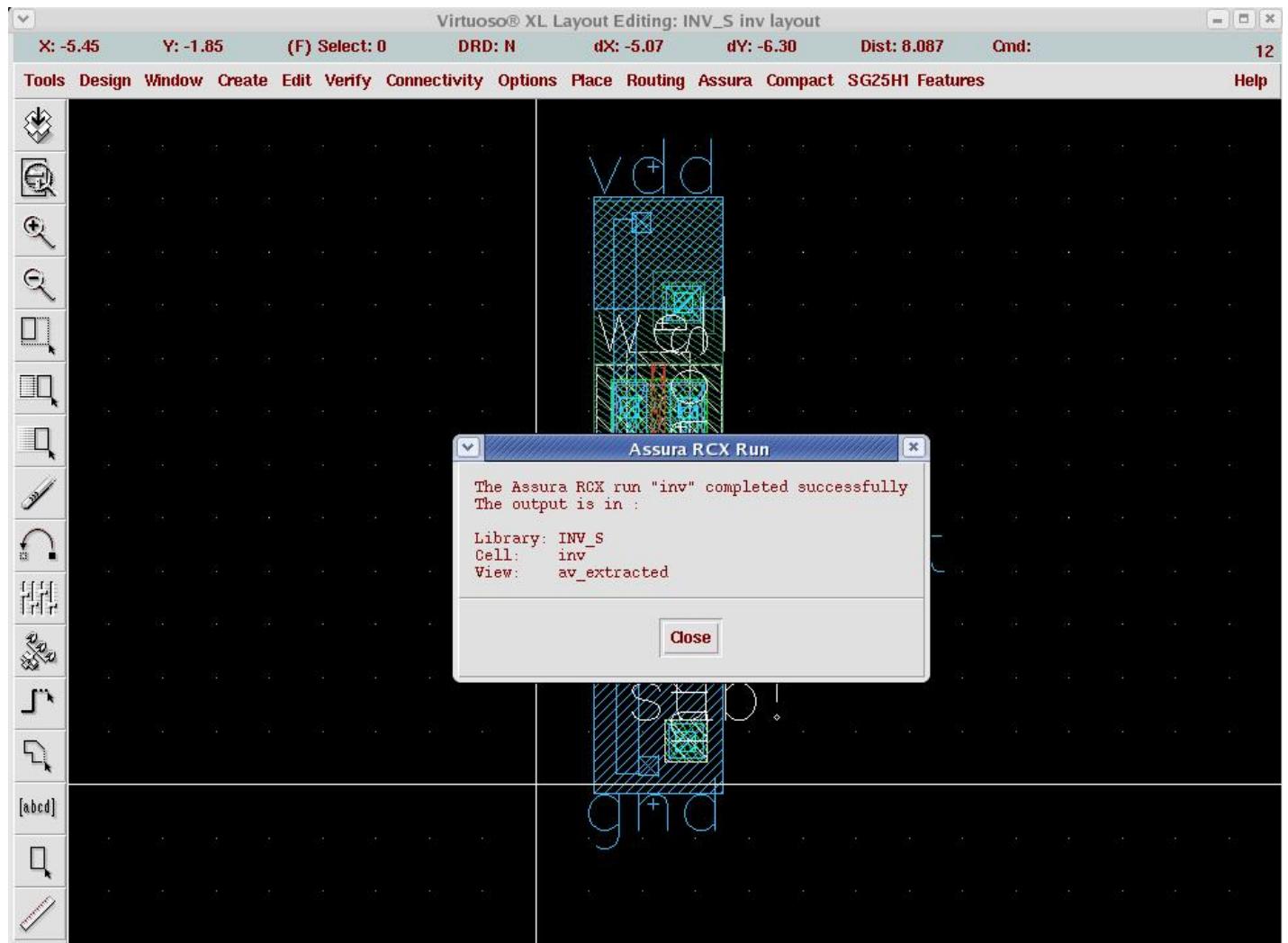


Fig 43

Close the layout Editor.

---

### Post layout Simulation:

Open the Library manager window. Select INV\_S. Go to File->New->Cell View. Give the Cell name as inv\_test. Set the tool to Composer\_Schematic and then press ok. This will open a schematic window.

Now go to Add->instance and select the library as INV\_S and cell as inv, then place the symbol as shown in Fig 44:

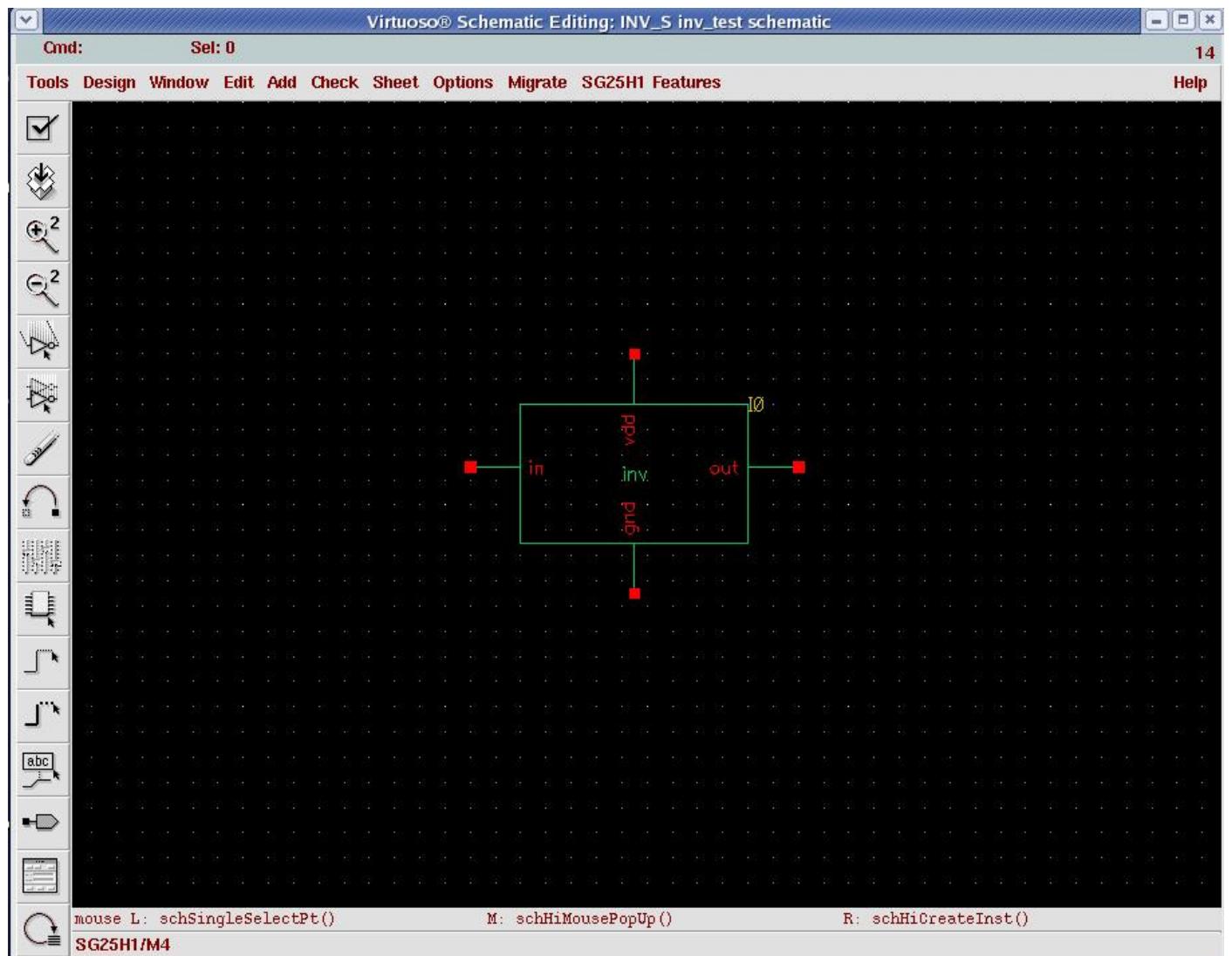


Fig 44

Do the connections as shown in Fig 45:

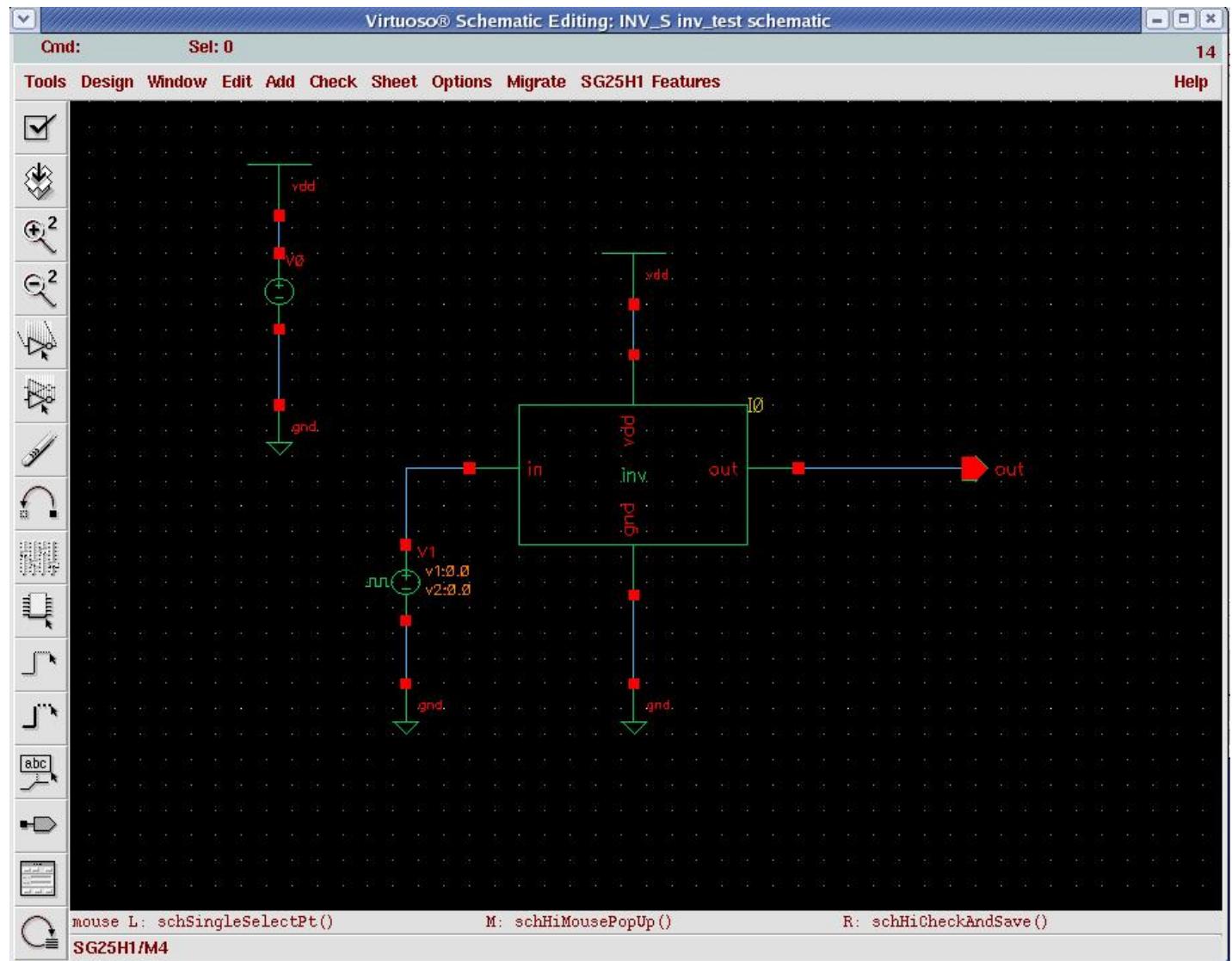


Fig 45

Edit the values of  $vdd$  and  $vpulse$  as you did in schematic. Then check and save. Close this window.

Go to library manager. Select INV\_S library, inv\_test cell, go to File->New->Cell view. Set the tool to Hierarchy-Editor, press ok. This will open a window as shown in Fig 46:

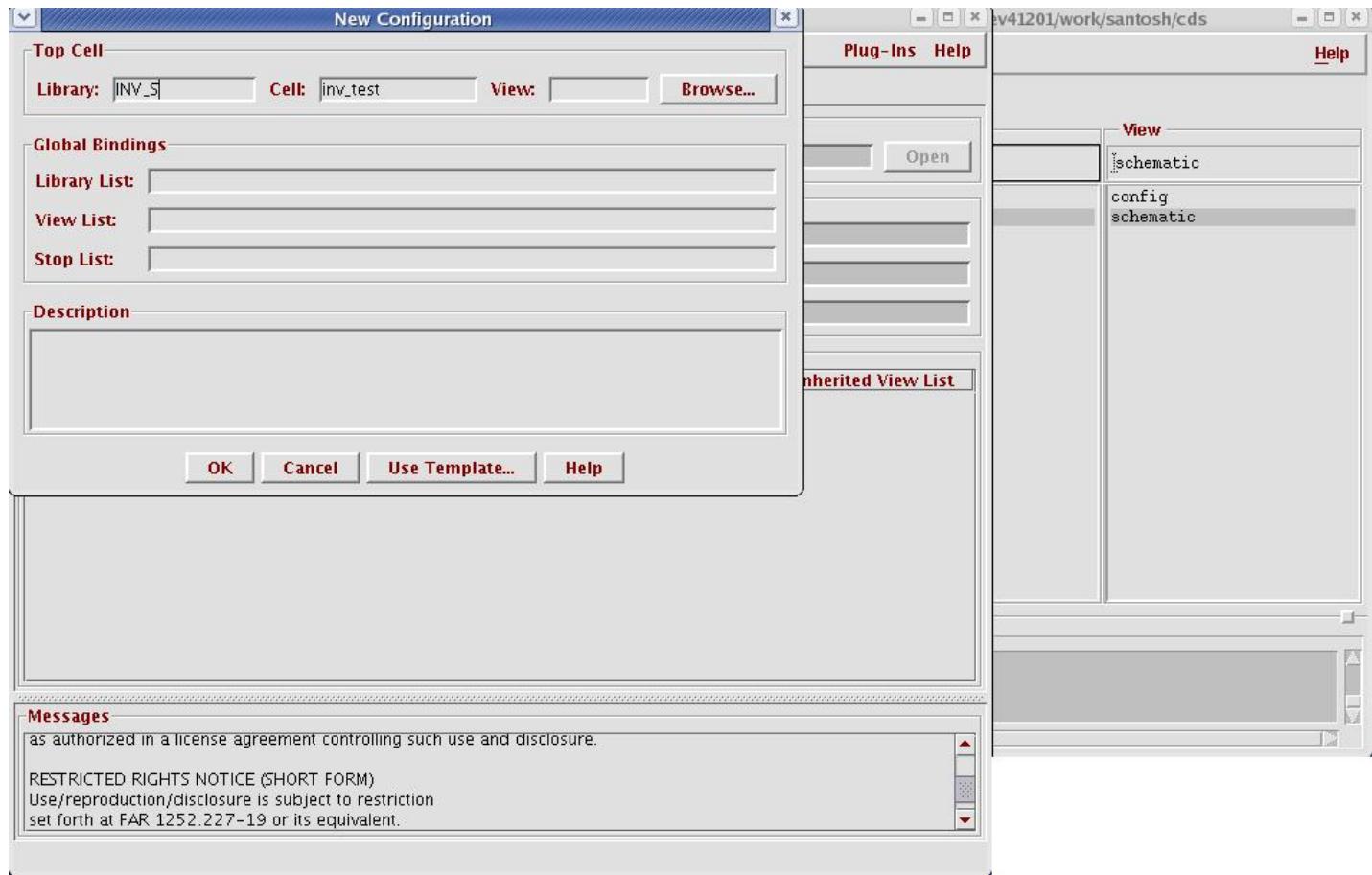


Fig 46

In the view of New Configuration Window, write schematic, and then press use Template button. This will open the Use Template window. Set the name to spectre, then press "apply" and "ok". Press the ok button in the New Configuration Window. In the hierarchy editor, go to view->update. Then Save it and close the window.

Now in the library Manager, under inv\_test, you will find config. Open this. The window will look as shown in Fig 47:

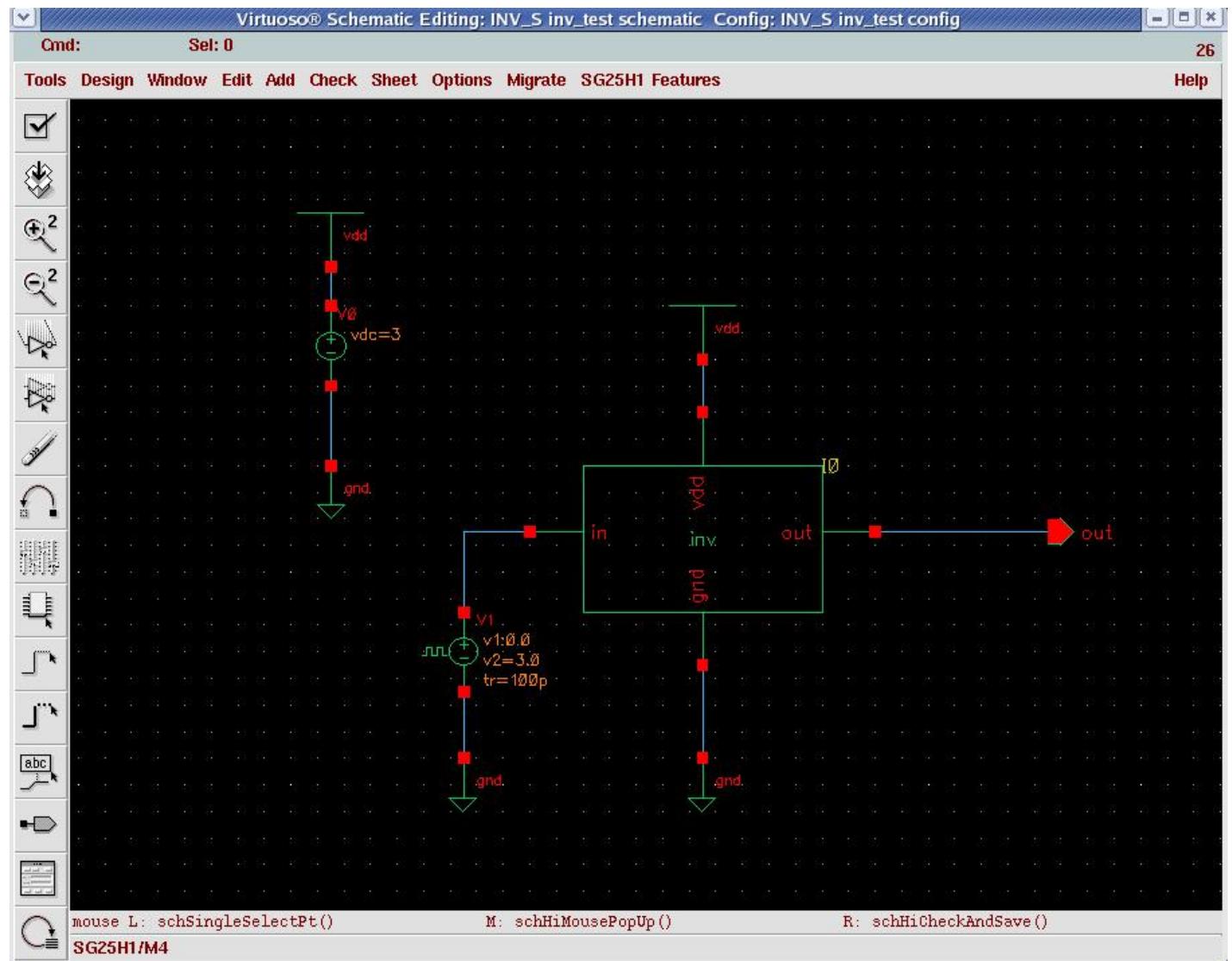


Fig 47

Now go to tools->Hierarchy Editor. This will come on the top menu bar. Now select the symbol and go to Hierarchy Editor->Set Instance Binding. This will open a window as shown in Fig 48:

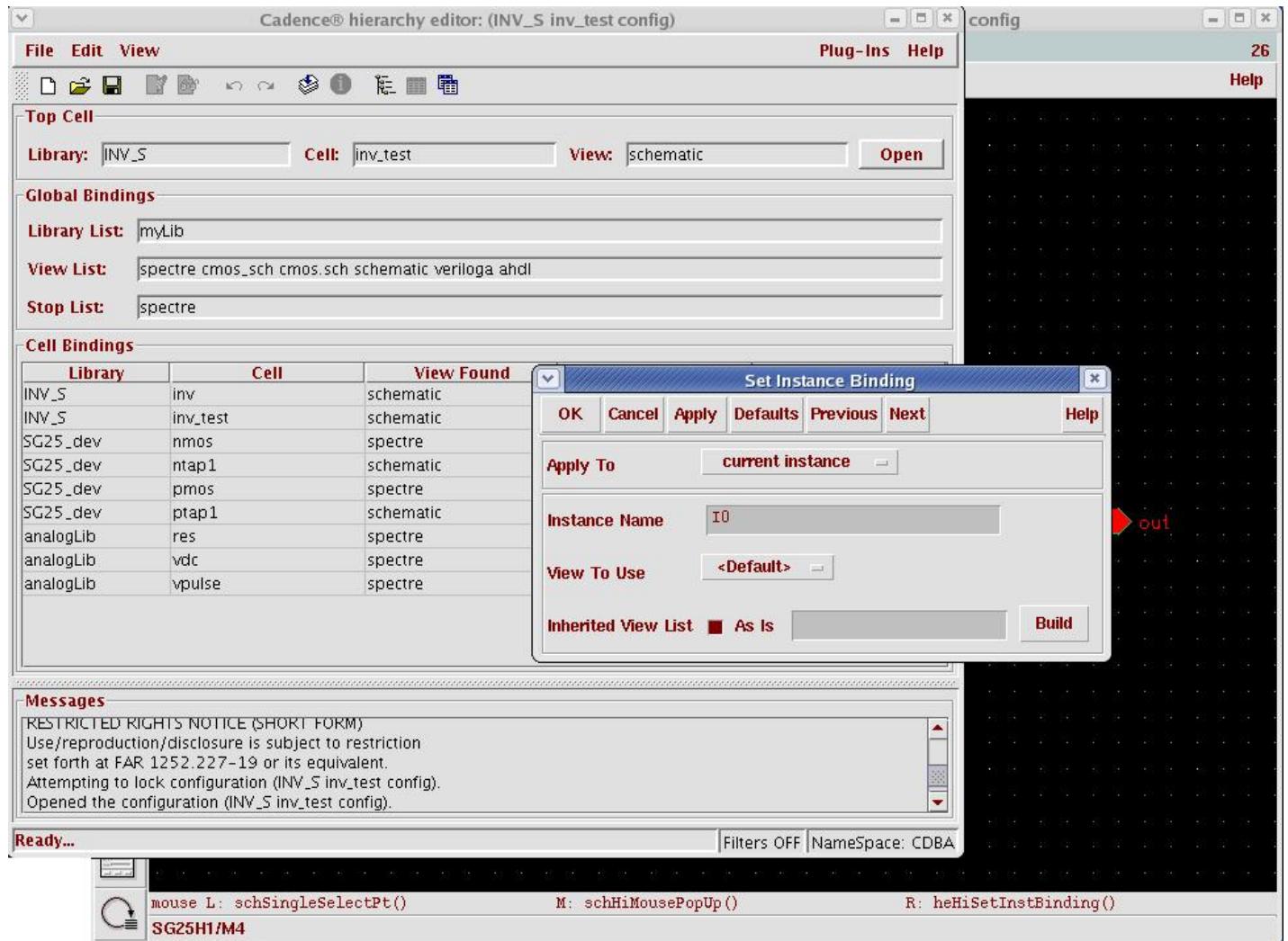


Fig 48

In the View to use option select av\_extracted, and then press ok. Then in the Hierarchy editor go to view->Update. Then save and close this hierarchy window.

Now if you want to see, what is behind the symbol, just select the symbol, the press shift-e. This will show you the extracted view as shown in Fig 49:

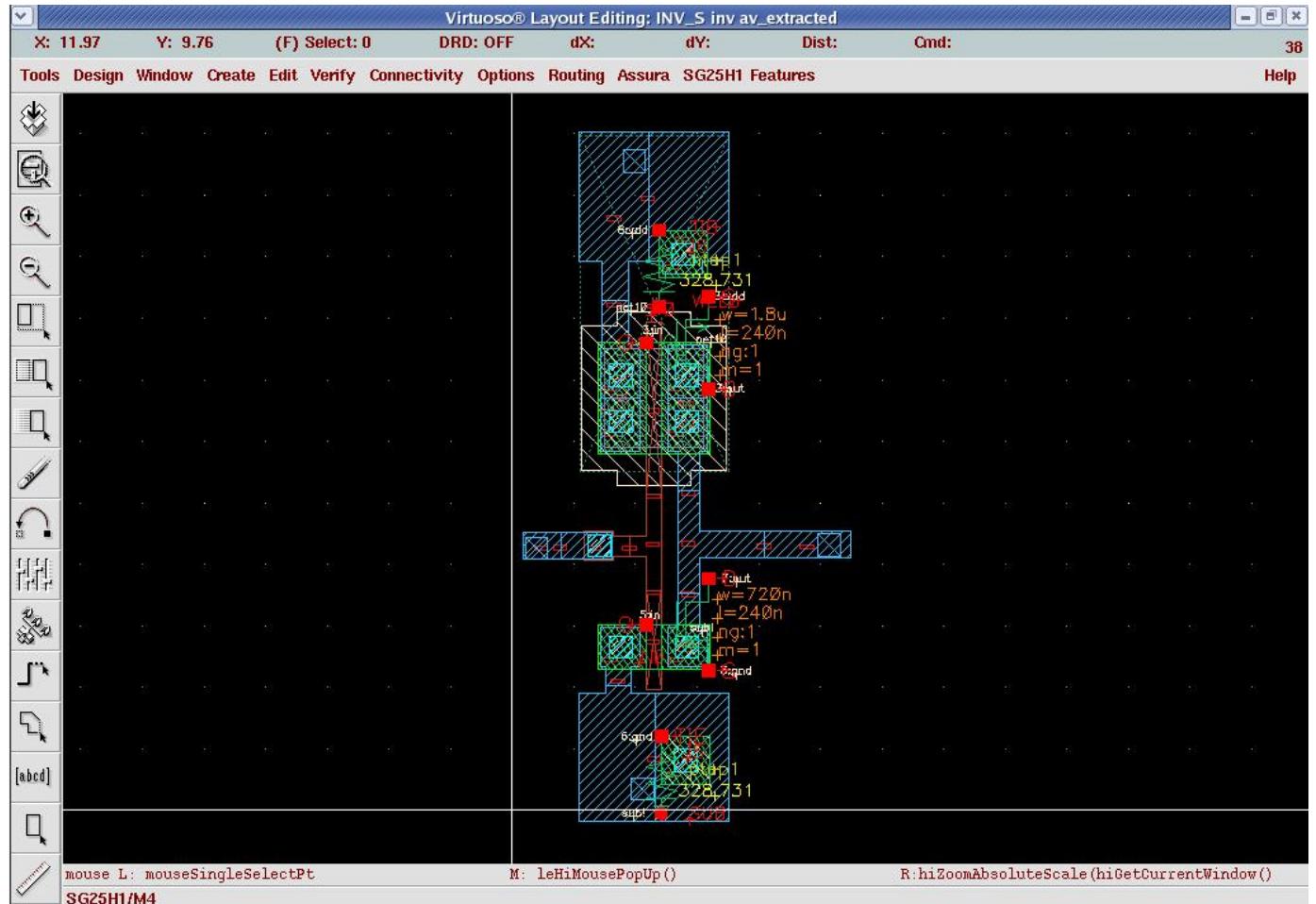


Fig 49

Then close the extracted view window. Open the config again, go to tool->Analog Environment. Then do the simulation as you did in schematic.

## GDS File Creation:

In the icfb window shown below, go to file->Export->Stream..



Fig 50

This will open a window as shown in Fig 51:

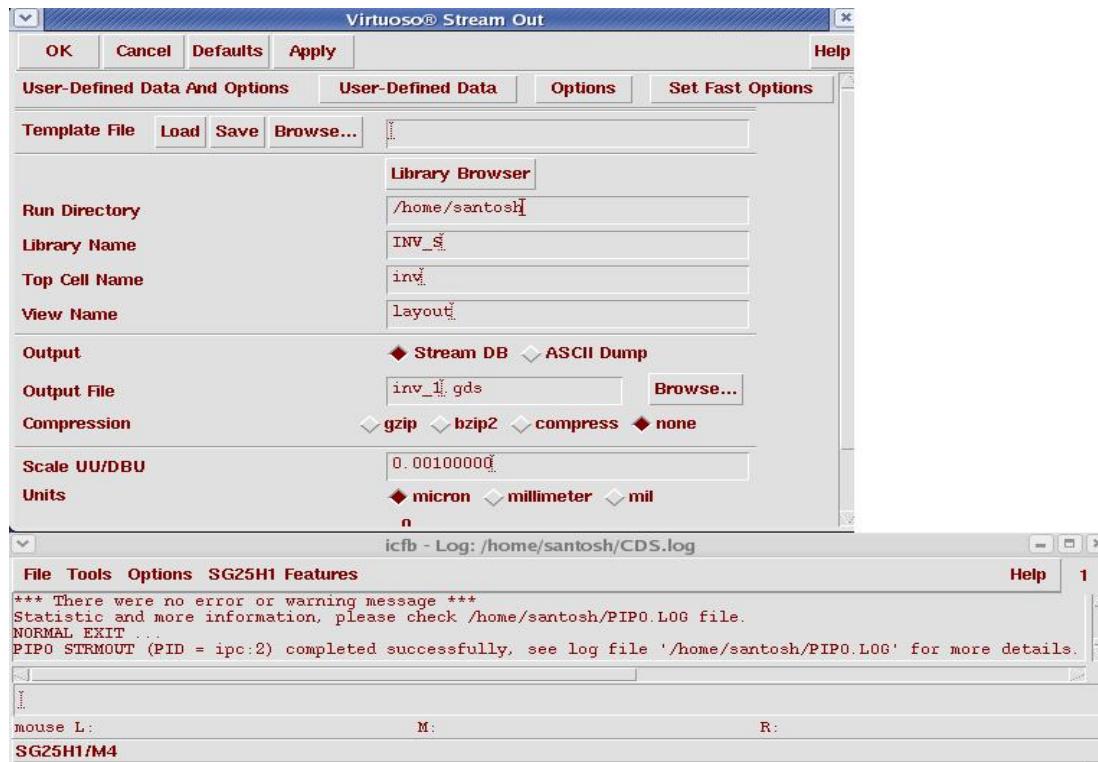


Fig 51

Set the fields as shown above. Then press ok. It might take some time to create the GDS file. Once it will be created, you can find it in your home directory.

<<<<<<<<<<< ALL THE BEST >>>>>>>>>>