

# **Induction Motor Control Using FPGA-Based Variable Frequency Drive**

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towards successful completion of

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by

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## DECLARATION

We hereby *declare* that the Major Project Work Report entitled "***Induction Motor Control Using FPGA-Based Variable Frequency Drive***" , which is being submitted to the **National Institute of Technology Karnataka, Surathkal**, for the award of the Degree of Bachelor of Technology in Electrical and Electronics Engineering, is a *bonafide report of the work carried out by us*. The material contained in this Report has not been submitted to any University or Institution for the award of any degree.

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# CERTIFICATE

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# ABSTRACT

This report presents an overview of induction motor control using FPGA-based Variable Frequency Drives (VFDs) for efficient and flexible motor operation. The primary focus is on the speed control techniques employed, including the Volts per Hertz (V/f) method and Sinusoidal Pulse Width Modulation (SPWM), which are key in achieving smooth and energy-efficient motor control. The V/f method is used to maintain a constant motor flux by adjusting the voltage proportionally with the frequency, while SPWM ensures the generation of a high-quality sinusoidal waveform to minimize harmonic distortion.

The report delves into the use of Field Programmable Gate Arrays (FPGAs) for motor control applications, with an emphasis on the Basys 3 FPGA board and its specifications. Replacing microcontrollers with FPGAs offers several advantages, such as enhanced speed, parallel processing capabilities, and flexibility in designing custom control algorithms. Additionally, the Verilog Hardware Description Language (HDL) is explored for the design and simulation of the control system, where different modules such as sine wave generation, clock dividers, and frequency selectors are discussed.

The design considerations for an open-loop control system are presented, including detailed descriptions of the various modules and their integration. Furthermore, the implementation and testing phases are covered, with a focus on constraints files, testing the SPWM output, and filtering the generated signal to obtain the desired motor control characteristics.

In conclusion, the combination of V/f control, SPWM, and FPGA technology offers a powerful solution for efficient and adaptable induction motor control. This report highlights the importance of these methods and technologies in improving motor performance, energy efficiency, and system reliability in a variety of industrial applications.

**Keywords-** Variable Frequency Drives, SPWM, FPGA, Basys3

# 1 INTRODUCTION

Variable Frequency Drives (VFDs) have become essential in modern motor control systems due to their versatility and efficiency. They enable precise speed regulation of induction motors, which is critical in applications like conveyor belts, pumps, fans, and other industrial machinery where the motor's speed must adapt to varying load conditions. VFDs achieve this by dynamically adjusting the frequency and voltage supplied to the motor, offering benefits such as variable speed operation, soft starting and stopping to reduce mechanical stress, and significant energy savings by operating motors at only the required speed rather than at full capacity.

Traditional motor control solutions often rely on microcontrollers, which, while effective in simpler applications, face challenges in handling precise timing and managing complex control algorithms. Microcontrollers are inherently sequential in operation, limiting their ability to manage multiple real-time tasks efficiently, such as generating high-frequency pulse-width modulation (PWM) signals and monitoring inputs simultaneously. Furthermore, their fixed hardware architecture makes it challenging to customize them for specific control needs.

In this context, Field-Programmable Gate Arrays (FPGAs) offer a compelling alternative. FPGAs provide parallel processing capabilities, allowing multiple tasks to execute simultaneously, which is critical for precise motor control. They enable the implementation of custom logic tailored to specific control strategies, such as Sinusoidal Pulse Width Modulation (SPWM) and the V/f control method.

This report focuses on the design, implementation, and testing of an FPGA-based VFD using the Basys 3 FPGA board. The implementation emphasizes an open-loop control strategy, where motor speed is regulated by adjusting the supply voltage and frequency without feedback. The report also delves into SPWM, a widely used technique for generating smooth, variable-frequency outputs essential for controlling motor speed and torque efficiently.

By leveraging FPGA technology, this project demonstrates how advanced hardware can overcome the limitations of traditional microcontroller-based systems, offering precise, high-performance motor control suitable for modern industrial applications.

## 2 Induction Motor Speed Control

### 2.1 V/f Method of Speed Control

The V/f method, also known as the Volts per Hertz control, is a widely used technique for controlling the speed of induction motors. This method is based on the principle that the synchronous speed of an induction motor is directly proportional to the supply frequency. The synchronous speed  $N_s$  is given by:

$$N_s = \frac{120 \cdot f}{p}$$

where:

- $N_s$ : Synchronous speed (RPM)
- $f$ : Supply frequency (Hz)
- $p$ : Number of poles of the motor

In this method, the applied voltage is varied in proportion to the frequency to maintain a constant magnetic flux in the motor. This ensures efficient operation and prevents issues like magnetic saturation or under-fluxing. The relationship can be expressed as:

$$\frac{V}{f} = \text{constant}$$

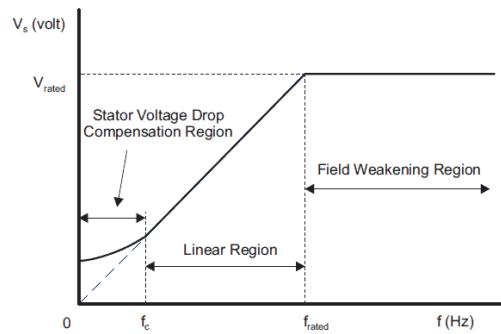


Figure 4. Stator Voltage Versus Frequency Profile Under V/Hz Control

Figure 1: Constant V/f Control.

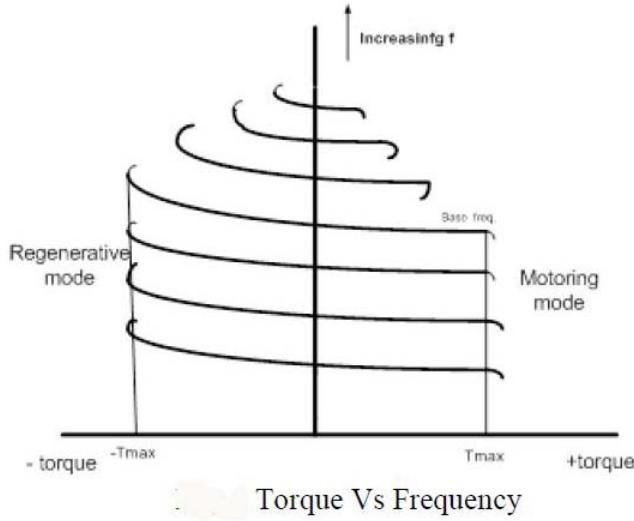


Figure 2: Constant V/f Control.

This proportionality ensures a constant torque operation over a wide range of speeds. The V/f method is particularly effective for applications requiring smooth speed control and minimal mechanical stress, such as fans, pumps, and conveyors. However, this method lacks feedback and operates in an open-loop configuration, which means it does not compensate for disturbances or changes in load conditions.

## 2.2 Sinusoidal Pulse Width Modulation (SPWM)

SPWM, or Sinusoidal Pulse Width Modulation, is a key technique in power electronics used to control the output voltage and frequency of inverters, which are integral to Variable Frequency Drives (VFDs). SPWM generates a waveform that approximates a sinusoidal signal by modulating the width of its pulses in correspondence with the amplitude of a reference sinusoidal signal.

The SPWM process involves:

1. **Reference Wave:** A sinusoidal waveform of the desired output frequency ( $f_r$ ).
2. **Carrier Wave:** A high-frequency triangular waveform ( $f_c$ ) serves as the comparison baseline.
3. **Pulse Generation:** The reference wave's amplitude is compared to the carrier wave. When the reference amplitude exceeds the carrier, the output is set high (logic 1); otherwise, it is set low (logic 0).

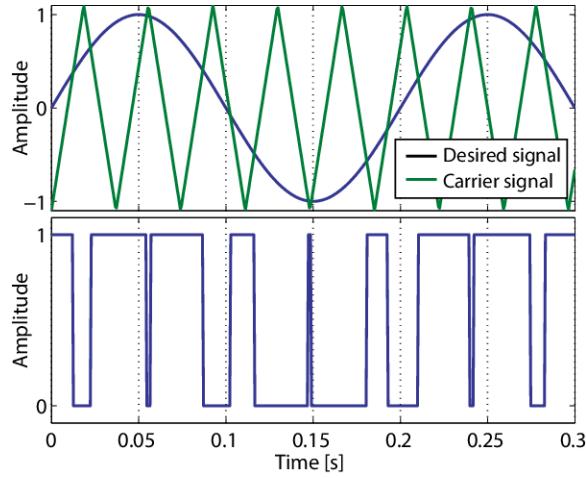


Figure 3: SPWM Modulation.

This modulation technique has several advantages:

- Reduces harmonic distortion in the output waveform.
- Enables precise control over the output frequency and voltage.
- Ensures compatibility with the V/f method by adjusting the modulation index ( $m_a$ ) to regulate voltage.

The relationship between the modulation index and the line-to-line RMS voltage ( $V_{L-L}$ ) is given by:

$$V_{L-L} = 0.612 \cdot m_a \cdot V_{dc}$$

Here,  $V_{dc}$  is the DC bus voltage, and  $m_a$  is the modulation index, which controls the amplitude of the output voltage.

SPWM plays a critical role in ensuring the smooth and efficient operation of induction motors by providing a high-quality sinusoidal output from an inverter. It is widely adopted in industrial drives and motor control systems.

### 3 Variable Speed Operation

#### 3.1 Variable Speed Operation Using SPWM

Variable speed operation using Sinusoidal Pulse Width Modulation (SPWM) is a versatile and efficient method to control the speed of induction motors. This approach enables precise speed regulation by varying the output frequency and voltage of the inverter while maintaining a constant volts-per-hertz (V/f) ratio.

The frequency of the sinusoidal reference wave ( $f_r$ ) directly influences the inverter's output frequency. By increasing or decreasing  $f_r$ , the synchronous speed of the motor ( $N_s$ ) is adjusted proportionally. The synchronous speed is defined as:

$$N_s = \frac{120 \cdot f}{p}$$

where:

- $f$ : Supply frequency in Hz
- $p$ : Number of poles in the motor

**Control of Output Voltage** To maintain consistent motor torque and prevent under-fluxing or saturation, the voltage ( $V$ ) is varied proportionally with the frequency ( $f$ ). This is achieved through constant V/f control, ensuring optimal motor operation across varying speeds.

The modulation index ( $m_a$ ) in SPWM determines the amplitude of the inverter's output voltage. Adjusting  $m_a$  ensures that the required V/f ratio is maintained for various speed settings.

This method is particularly effective for industrial applications requiring dynamic speed adjustments, such as conveyor belts, pumps, and fans. It ensures energy efficiency, smooth acceleration, and reduced mechanical stress.

## 3.2 Open-Loop Control

Open-loop control is a straightforward approach for managing induction motor operation without using feedback mechanisms. In this method, the input parameters—voltage and frequency—are predefined and applied to the motor, and the system does not adjust these parameters based on the motor's performance or external conditions.

### 3.2.1 Characteristics of Open-Loop Control

- 1. No Feedback Mechanism:** The system does not monitor or respond to the motor's actual speed, torque, or load conditions.
- 2. Simplicity:** The design and implementation of open-loop systems are simple, making them cost-effective and easy to maintain.
- 3. Fixed V/f Ratio:** The V/f control method is commonly used in open-loop systems to maintain constant magnetic flux and ensure stable operation.

#### Advantages:

- Easy to implement and configure.
- Suitable for applications with minimal load variations or where high precision is not critical.
- Cost-effective for basic motor control tasks.

#### Disadvantages:

- Inability to compensate for disturbances or load changes.
- Reduced efficiency and performance in variable load scenarios.
- Risk of instability under significant load fluctuations.

#### Applications:

- Fans and blowers
- Pumps with consistent operating conditions
- Low-power motor drives where precision is not a primary requirement.

Despite its limitations, open-loop control remains a valuable option for simple motor control tasks, providing an efficient and economical solution for specific industrial applications.

## 4 Field Programmable Gate Arrays (FPGAs)

### 4.1 Overview of FPGAs

Field Programmable Gate Arrays (FPGAs) are integrated circuits designed to be configured by the user after manufacturing. Unlike application-specific integrated circuits (ASICs), which are tailored to specific tasks during fabrication, FPGAs offer post-manufacture programmability, making them versatile for various applications.

FPGAs consist of:

- **Configurable Logic Blocks (CLBs):** Provide the basic building blocks for implementing logic functions.
- **Programmable Interconnects:** Enable flexible connections between CLBs and input/output blocks.
- **On-Chip Resources:** Include memory blocks, digital signal processing (DSP) slices, and clock management systems.

Applications of FPGAs: FPGAs are used in diverse domains, such as:

1. Digital signal processing.
2. Aerospace and defense systems.
3. Industrial automation.
4. Prototyping for ASICs.

FPGAs offer parallel processing capabilities, low latency, and reusability, making them highly suitable for dynamic environments requiring rapid prototyping and hardware customization.

## 4.2 Selecting an Appropriate FPGA Board

Choosing the right FPGA board depends on project requirements and available resources. Some critical factors to consider include:

1. **Performance Needs:** The logic capacity, speed grade, and on-chip resources should align with the project's computational demands. High-performance applications may require advanced boards like the AMD Virtex series, while entry-level projects can use boards such as Basys 3.
2. **Interfaces and Peripherals:** Boards must support essential I/O interfaces, including UART, GPIO, and specialized connectors like PMOD or FMC.
3. **Logic Capacity and Resource Utilization:** Evaluate the number of logic elements, DSP slices, and block RAM available. For projects involving complex algorithms or data-intensive tasks, higher capacity is essential.
4. **On-Chip Features:** Additional features like analog-to-digital converters, clock generators, and embedded processors can significantly impact the board's suitability.

Based on these considerations, the Basys 3 FPGA board was chosen for its cost-effectiveness, compatibility with AMD Vivado tools, and suitability for educational and basic digital design projects.

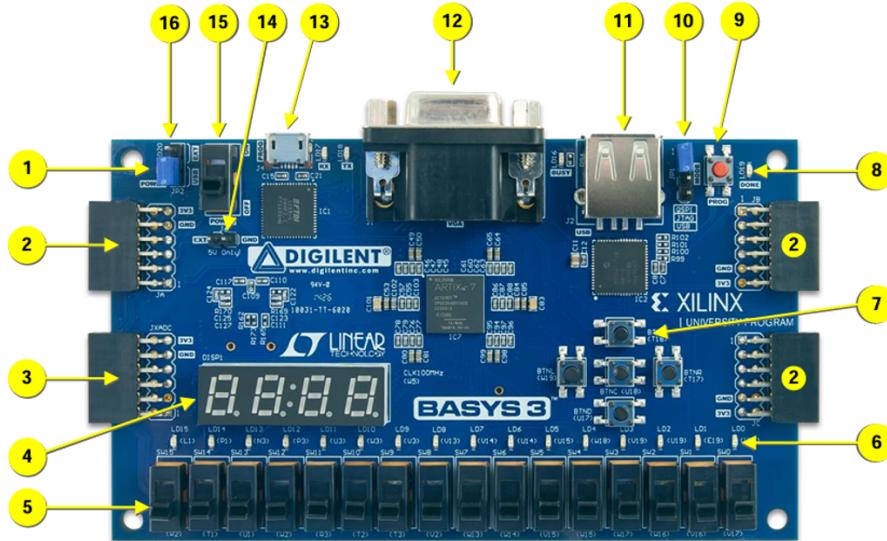


Figure 4: BASYS-3 FPGA board with AMD artix-7 Chip

## 4.3 Basys 3 FPGA Board and Specifications

The Basys 3 FPGA board, based on AMD Artix-7 architecture, is a beginner-friendly and affordable development platform designed for educational and entry-level digital design projects. Below are its key specifications:

### Hardware Features:

- **FPGA Chip:** XC7A35T-1CPG236C.
- **Logic Cells:** 33,280 across 5200 slices.
- **Block RAM:** 1800 Kbits.
- **DSP Slices:** 90 for arithmetic operations.
- **Clock Speed:** 100 MHz internal clock.

### Connectivity and I/O:

- 16 LEDs and 16 switches for general I/O.
- A 4-digit, 7-segment display for output visualization.
- PMOD connectors for external peripherals.
- USB interface for programming and data exchange.

### Advantages:

- Entry-level pricing, making it accessible to students and hobbyists.
- Compatibility with the AMD Vivado Design Suite for efficient development.
- Adequate resources for implementing basic control systems and digital designs.

The Basys 3 board is an excellent choice for projects involving FPGA-based induction motor control, providing sufficient flexibility and performance at a reasonable cost.

## 5 Replacing Microcontrollers with FPGAs

### 5.1 Advantages of Using FPGAs Over Microcontrollers

Field Programmable Gate Arrays (FPGAs) offer several advantages over traditional microcontrollers, particularly in applications requiring high performance, flexibility, and precise timing control.

1. **Parallel Processing:** Unlike microcontrollers, which execute tasks sequentially using a fixed architecture, FPGAs allow for parallel execution of multiple operations. This makes FPGAs ideal for real-time applications like generating multiple PWM signals, handling various input/output operations, and monitoring system parameters concurrently.
2. **Customizable Hardware:** FPGAs provide the ability to design custom logic circuits tailored to specific requirements. This flexibility enables the optimization of hardware for particular motor control algorithms, making them highly versatile in diverse applications.
3. **Low Latency:** Since FPGAs process operations in hardware rather than software, they exhibit minimal latency. This characteristic is crucial for applications demanding rapid response times, such as motor speed control or real-time signal processing.
4. **Adaptability:** FPGAs can be reprogrammed to accommodate changes in control schemes or motor types without requiring hardware modifications. This adaptability simplifies prototyping and future-proofing of designs.
5. **High Precision and Deterministic Performance:** By operating on dedicated hardware circuits, FPGAs provide predictable and precise timing, ensuring accurate control over motor functions.

These advantages make FPGAs particularly valuable in industrial automation, robotics, and complex motor control applications.

# 6 Verilog Hardware Description Language (HDL)

## 6.1 Verilog HDL Modules

Verilog Hardware Description Language (HDL) is a high-level programming language used to describe the design and behavior of digital systems. It is widely utilized in the design and simulation of circuits for Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs).

In Verilog, designs are composed of modules, which are building blocks representing different functionalities. Each module can have:

- **Inputs:** Define the signals that the module receives.
- **Outputs:** Represent the signals the module produces.
- **Internal Logic:** Specifies the operations performed inside the module.

Modules allow for hierarchical design, where complex systems are built by combining simpler modules. This modularity promotes code reuse and simplifies debugging.

```
module AND_Gate {  
    input: wire A, wire B  
    output: wire Y  
    logic: Y = A & B  (Logical AND operation)  
    endmodule
```

## 7 Design Considerations

### 7.1 Open-Loop Control Design Considerations

Open-loop control refers to a system where the input signals, such as voltage and frequency, are applied to the motor without any feedback to monitor or adjust its performance. This approach is straightforward and cost-effective, making it suitable for applications where precise control is not critical.

Key considerations for open-loop control design include:

1. **Voltage and Frequency Control:** Maintaining a constant  $V/f$  ratio is crucial to ensure proper magnetic flux in the motor.
2. **Timing and Sequencing:** The SPWM signal generation, voltage modulation, and inverter switching need to be carefully synchronized to avoid excessive harmonic distortion.
3. **Simplicity:** Open-loop systems are simple to design and implement but are sensitive to load variations and disturbances.

While open-loop control is effective in specific scenarios, it has limitations such as an inability to compensate for changes in load or disturbances, making it less robust compared to closed-loop systems.

### 7.2 Module Descriptions

#### 7.2.1 Sine Wave Generation (LUT Method)

The sine wave generation module employs a lookup table (LUT) containing 4096 precomputed samples representing one full period of a sine wave. To ensure the waveform remains entirely positive, the sine values were amplitude-shifted upward by 128 units. As a result, the output sine wave varies between 0 and 255, with the original bipolar waveform (ranging from -127 to +127) transformed into a unipolar form suitable for digital systems.

##### Features:

- The ROM dimensions are defined by the resolution required.
- A counter increments addresses to fetch the sine wave values.

This method ensures high precision and eliminates runtime computation, making it efficient for FPGA-based designs.

### **7.2.2 Clock Divider (Sine and Triangular Waves)**

Clock dividers are used to reduce the internal FPGA clock frequency to generate waveforms with the required frequency. This is achieved by toggling the output clock signal after a specific count.

#### **Key Points:**

- Ensures compatibility with motor operational frequency.
- Reduces power consumption by optimizing clock usage.

### **7.2.3 MUX (Frequency Selector)**

The multiplexer (MUX) module selects between different input frequencies based on a select line signal. It enables the system to switch dynamically between predefined operational modes.

### **7.2.4 Triangular Wave Generation**

The triangular wave generation module produces a waveform that linearly increases and decreases between a defined range. This wave is essential for SPWM signal generation.

#### **Mechanism:**

- A counter is incremented or decremented based on the current direction of the wave.
- The waveform's amplitude is confined to the specified range.

### **7.2.5 Modulation Index Module and Amplitude Modulator**

The modulation index module adjusts the amplitude of the sine wave by multiplying it with a modulation factor. This modulated amplitude ensures that the  $V/f$  ratio is maintained.

#### **Steps:**

1. Take input sine wave samples.
2. Multiply with modulation index to scale amplitude.
3. Output scaled waveform for further processing.

### 7.2.6 Comparator and Top Module

The comparator module generates SPWM signals by comparing the modulated sine wave with the triangular carrier wave. The top module integrates all submodules and ensures synchronization between them.

#### Key Outputs:

- Pulse Width Modulated (PWM) signals for inverter control.
- Synchronized operation of sine and triangular wave generators.

## 7.3 Complete Schematic

The complete schematic integrates all modules into a single cohesive system. It includes:

1. **SPWM Signal Generation:** The sine wave and triangular wave modules work together to produce SPWM signals.
2. **Inverter Control:** The SPWM signals are fed to an inverter to control the motor's voltage and frequency.
3. **Synchronization:** The system ensures precise timing and coordination between modules.

The schematic provides a detailed representation of interconnections between the FPGA ports and external components such as the motor and inverter. It acts as a blueprint for hardware implementation and testing.

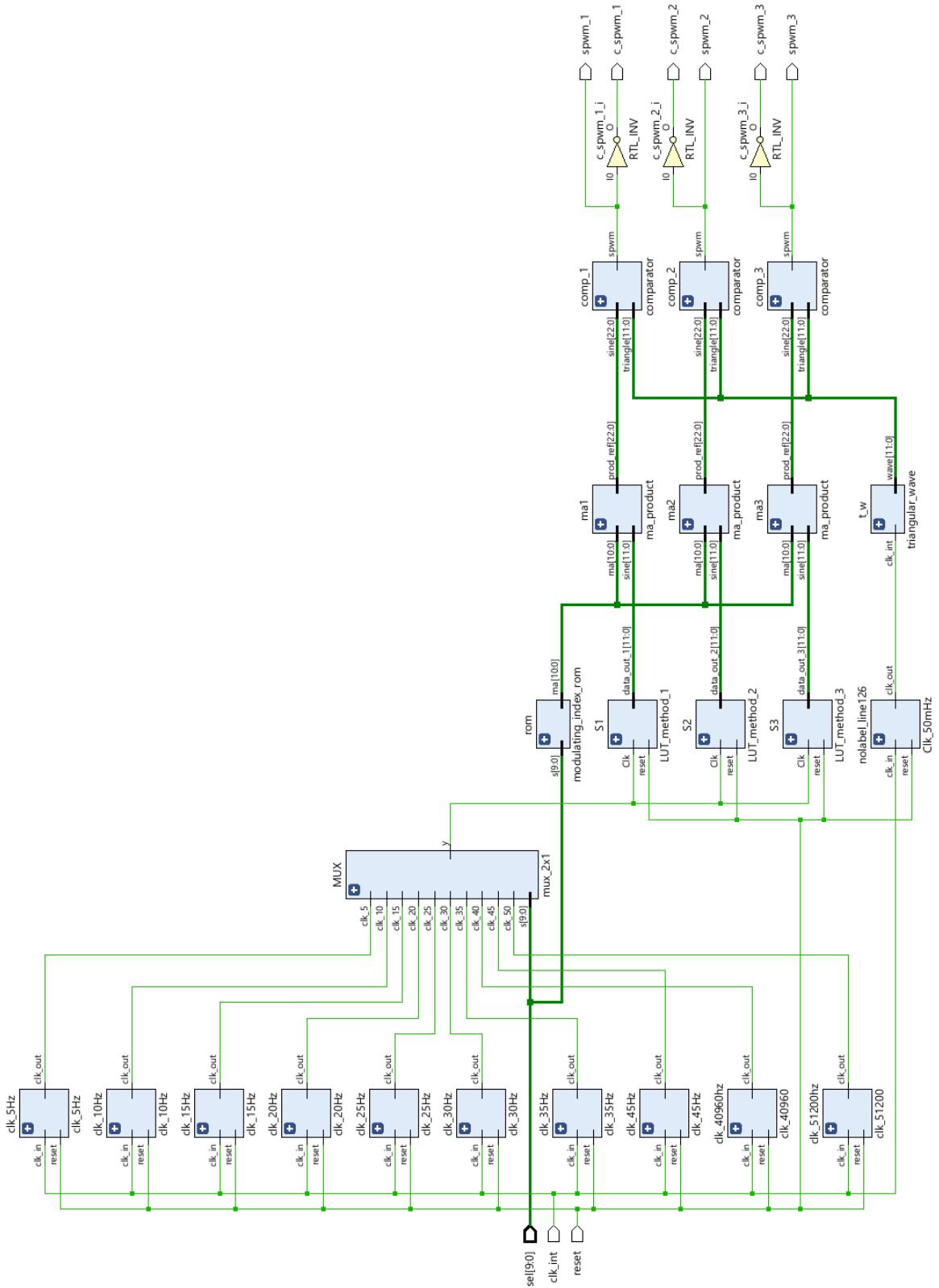


Figure 5: Complete schematic with all modules

# 8 Implementation and Testing

## 8.1 Constraints File and Ports Used

During the implementation phase, a constraints file was used to define the necessary physical pin mappings and other essential configurations for the FPGA. The constraints file is crucial for proper operation, as it ensures that the design is correctly mapped to the FPGA hardware. The file is typically in ‘xdc’ format for Xilinx FPGAs, and it specifies parameters such as the clock frequency, pin assignments, and timing requirements.

In this project, the key ports used in the design were:

- **W5:** Internal Clock of 100 MHz — This clock drives the entire FPGA design.
- **R2:** Switch for Reset Signal — Used to initialize the system.
- **V17,V16,W16,W17,W15,V15,W14,W13,V2,T3:** Switch for MUX Select Line Signal and modulating index selection — Selects between the ten different frequencies for the sine wave generation and selecting the appropriate modulating index
- **K17:** SPWM output with phase shift 0 degree.
- **M18:** SPWM output with phase shift 120 degree.
- **N17:** SPWM output with phase shift -120 degree.
- **L17:** SPWM complemented output with phase shift 0 degree.
- **M19:** SPWM complemented output with phase shift 120 degree.
- **P17:** SPWM complemented output with phase shift -120 degree.

These ports were connected to the FPGA board’s I/O pins to facilitate real-time testing and signal verification. Additionally, the constraints file ensures that all timing constraints, such as the clock period and input/output delays, are adhered to during the synthesis and implementation processes. Proper configuration of the constraints file is essential to ensure the functionality of the system, as it directly affects the operation of the FPGA and the accuracy of the output signals.

## 8.2 Design of RC Low Pass Filter for SPWM Signal

The design and purpose of an RC (Resistor-Capacitor) Low Pass Filter (LPF) for smoothing an SPWM (Sinusoidal Pulse Width Modulation) signal is presented. The SPWM technique is widely used in inverter circuits to generate sinusoidal waveforms by modulating a high-frequency PWM signal. However, the output of an SPWM signal directly from an inverter contains high-frequency switching components that must be filtered to recover the desired sinusoidal waveform. An RC low pass filter is one of the simplest and most effective ways to achieve this.

The SPWM signal generated by the FPGA switches at a high carrier frequency, typically in the range of several kilohertz, while the fundamental frequency of the desired sinusoidal waveform (output to the motor or load) lies between 0 Hz and 50 Hz. The goal of the RC low pass filter is to attenuate the high-frequency components (mainly the PWM carrier) and allow the low-frequency (fundamental) sinusoidal component to pass through with minimal distortion.

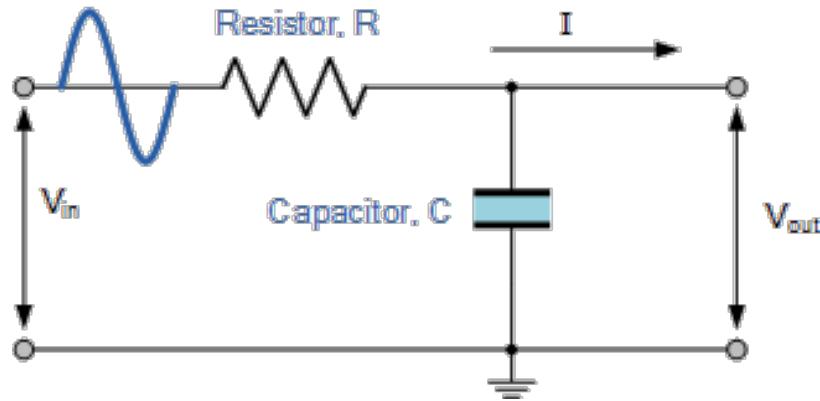


Figure 6: RC Low Pass Filter

The cutoff frequency ( $f_c$ ) of a RC low-pass filter is given by the formula:

$$f_c = \frac{1}{2\pi RC}$$

For this design, the required cutoff frequency was chosen to be 1 kHz, ensuring adequate attenuation of the high-frequency SPWM components while preserving the fundamental waveform. A standard capacitor value of 0.1 F was selected based on availability. Substituting into the cutoff frequency formula:

$$R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi \times 1000 \times 0.1 \times 10^{-6}} \approx 1.6 k\Omega$$

Thus, a resistor value of approximately 1.6 k $\Omega$  was chosen to pair with the 0.1 F capacitor, forming the RC low-pass filter.

### 8.3 Filtered SPWM Signal Observations (7th Sem)

After the SPWM signal was passed through a low-pass filter, the resulting waveform was analyzed to assess its quality. The purpose of the low-pass filter is to eliminate high-frequency components from the SPWM signal, producing a smooth output that approximates a pure sine wave.

However, the filtered output revealed that the waveform was not perfectly sinusoidal. This deviation is likely due to the absence of a sign bit in the FPGA's signal processing, which impacts the precision of the PWM output. Although the waveform retained a generally sinusoidal shape, noticeable distortions were present.

Further improvements in output frequency and amplitude tuning could enhance waveform quality. Key observations from the filtered output include:

- **Slightly reduced amplitude:** The peak amplitude was lower than expected, likely due to inaccuracies in the amplitude modulation process.
- **Inverted negative half-cycle:** The negative portion of the sine wave appeared inverted, potentially resulting from the lack of a sign bit in the signal representation.

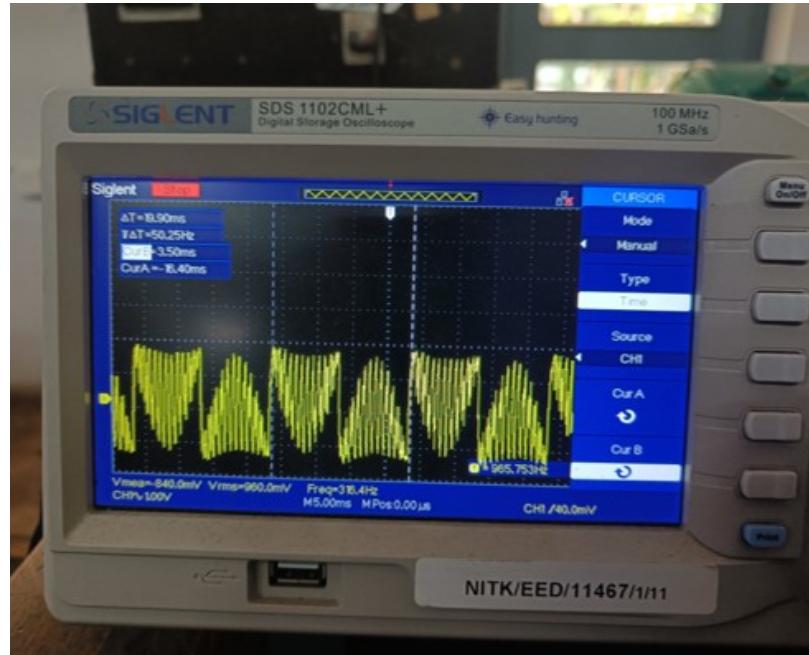


Figure 7: Filtered SPWM signal

## 8.4 Filtered SPWM Signal Observations (8th Sem)

Based on observations and analysis of the previously inaccurate SPWM output, several modifications were made to achieve a more accurate and properly filtered sinusoidal waveform:

- **Increased waveform resolution:** The number of samples per period for both the sine and triangular waves was increased from 1024 to 4096, enhancing the resolution of the SPWM signal.
- **Amplitude shifting:** Both sine and triangular waves were converted to unipolar form by applying a positive amplitude shift, simplifying the comparison process during SPWM generation.

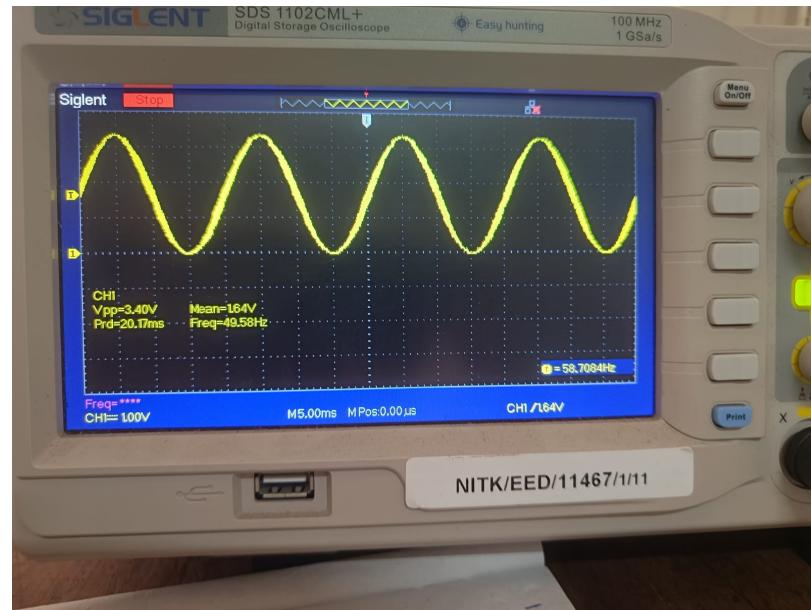


Figure 8: Filtered SPWM signal with 1000Hz cutoff frequency low-pass filter

After achieving a clean SPWM output, further enhancements were implemented to support V/f control:

- **Expanded frequency range:** Additional input frequencies were introduced, ranging from 5 Hz to 50 Hz in 5 Hz increments.
- **Three-phase SPWM generation:** The single-phase SPWM logic was replicated to generate three-phase SPWM signals, each phase-shifted by 120°.
- **Complementary signals:** Complementary SPWM waveforms were generated to enable proper triggering of the inverter switches.

## 8.5 Hardware implementation using Inverter and R Load

After verifying the FPGA code by using a low pass filter and observing the output on a DSO, we move forward to give this SPWM signal to an inverter and check voltage waveform for a R-Load.

Two complementary PWM signals were taken for two-sets of switches of a H-bridge inverter. Each leg consisted of two switching devices (IGBTs), forming the upper and lower arms. A single full H-bridge inverter topology was used, comprising two legs with a total of four switching devices. The H-bridge configuration enabled the generation of a bipolar AC output across the load by alternately applying the positive and negative terminals of the DC supply.

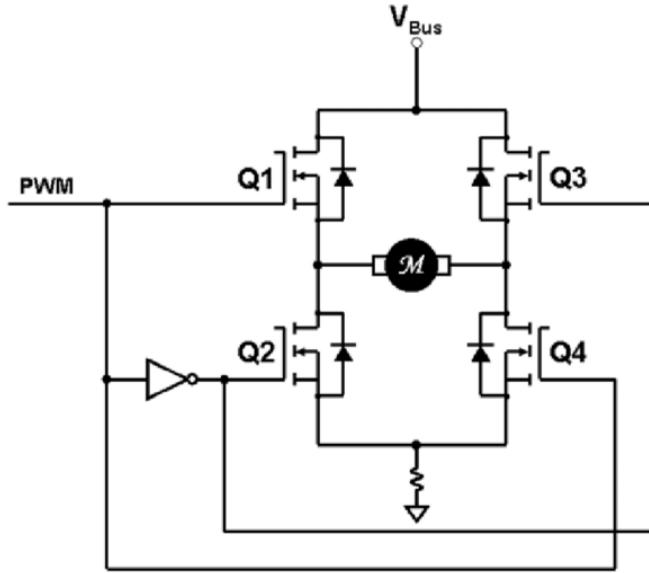


Figure 9: Circuit for Single phase H-bridge inverter

The gate driver inputs were connected to the FPGA's SPWM outputs to control the switches of the H-Bridge inverter as follows:

- **Leg A (Left Leg – Q1 and Q2):** The upper switch (Q1) was driven directly by the SPWM signal generated by the FPGA. The lower switch (Q2) was driven by the complement of the same SPWM signal. This complementary control ensures that Q1 and Q2 are never on at the same time.
- **Leg B (Right Leg – Q3 and Q4):** The same complementary logic was used, but with the control signals inverted in terms of their assignment. Here, the lower switch (Q4) was driven by the SPWM signal, while the upper switch (Q3) was driven by its complement. This reversal creates a  $180^\circ$  phase shift between

Leg A and Leg B, which is necessary to produce the correct bipolar output across the load.

The inverter circuit was powered using a 26V regulated DC power supply connected across the H-bridge's high-side and low-side rails:

- The positive terminal of the DC source was connected to the drain of the upper switches (Q1 and Q3).
- The negative terminal (ground) was connected to the source of the lower switches (Q2 and Q4).

The output terminals of the H-bridge inverter (i.e., the junction between Q1/Q2 and Q3/Q4) were connected across a resistive load using a variable rheostat. The rheostat was adjusted to its full resistance setting, providing a purely resistive load to ensure that the output waveform was not distorted by reactive components.

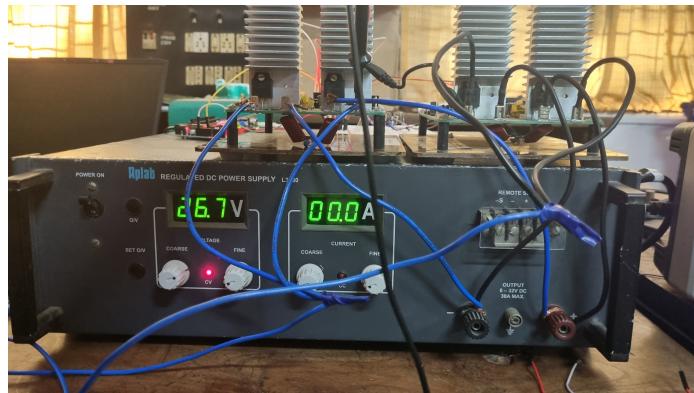


Figure 10: Regulated DC supply



Figure 11: R-Load

The voltage waveform across the rheostat was monitored using a digital storage oscilloscope (DSO). Two frequency conditions were tested:

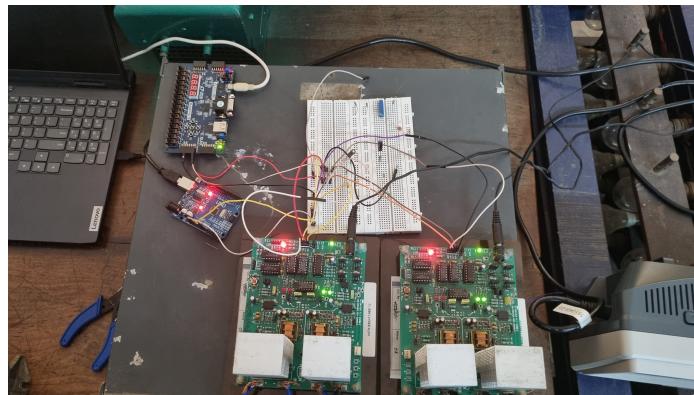


Figure 12: Hardware Implementation using Inverter

- 50 Hz SPWM signal
- 60 Hz SPWM signal

In both cases, the inverter successfully synthesized sinusoidal waveforms across the R load, with clean transitions and expected frequency characteristics.

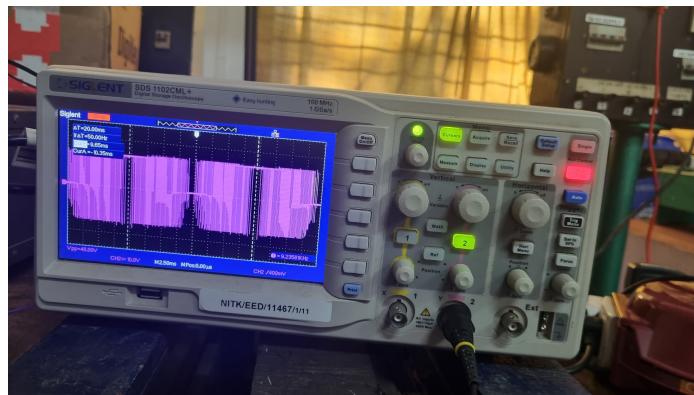


Figure 13: Voltage across R - Load (50 Hz)

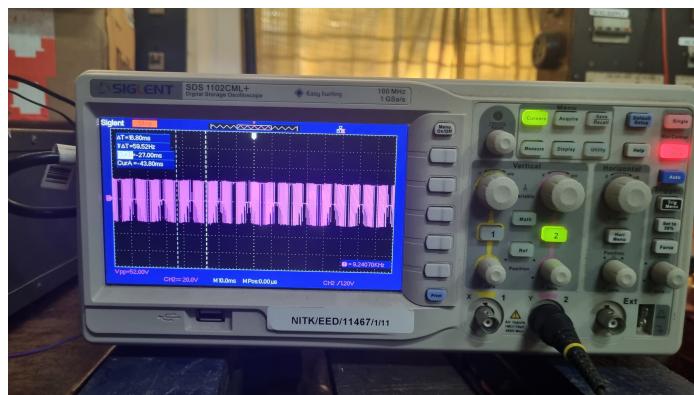


Figure 14: Voltage across R - Load (60 Hz)

## 8.6 V/f implementation and control

### 1. Principle of Constant V/f Ratio:

- In a 3-phase induction motor, torque is approximately proportional to the voltage-to-frequency ratio (V/f).
- To maintain optimal magnetic flux and torque, this V/f ratio is kept constant while varying the speed.

### 2. Speed Control Mechanism:

- Synchronous speed of the motor is given by:

$$N_s = \frac{120 \times f}{P}$$

where  $f$  is the frequency and  $P$  is the number of poles.

- By increasing or decreasing the stator frequency, the motor speed is controlled.

### 3. Voltage Adjustment:

- As frequency increases, stator voltage is also increased proportionally to maintain a constant V/f ratio.
- This prevents magnetic saturation at low frequencies and flux weakening at high frequencies.

### 4. Implementation via Inverter:

- A PWM-controlled inverter converts a fixed DC source into variable voltage and frequency AC.
- The FPGA generates PWM signals based on desired speed and ensures voltage and frequency scale together.

### 5. Typical V/f Profile:

- Up to the base frequency (e.g., 50/60 Hz), voltage is linearly increased with frequency.
- Beyond base frequency, voltage is held constant ( $V_{max}$ ), entering the flux weakening region.

### 6. DIP Switch-Based Frequency Selection:

- Output frequency is controlled via DIP switches on the FPGA board.
- Each DIP switch combination corresponds to a predefined frequency (e.g., 5 Hz to 50 Hz).
- Allows discrete motor speed selection without dynamic inputs.

## 7. FPGA Control Logic:

- FPGA monitors DIP switch inputs in real time.
- Based on selected frequency:
  - Adjusts PWM frequency to match desired motor speed.
  - Modifies duty cycle to proportionally control output voltage.

## 8. PWM Waveform Generation:

- FPGA generates sinusoidal PWM (SPWM) signals based on DIP switch settings.
- These signals are fed to gate drivers of the inverter, which drive the motor with appropriate voltage and frequency.

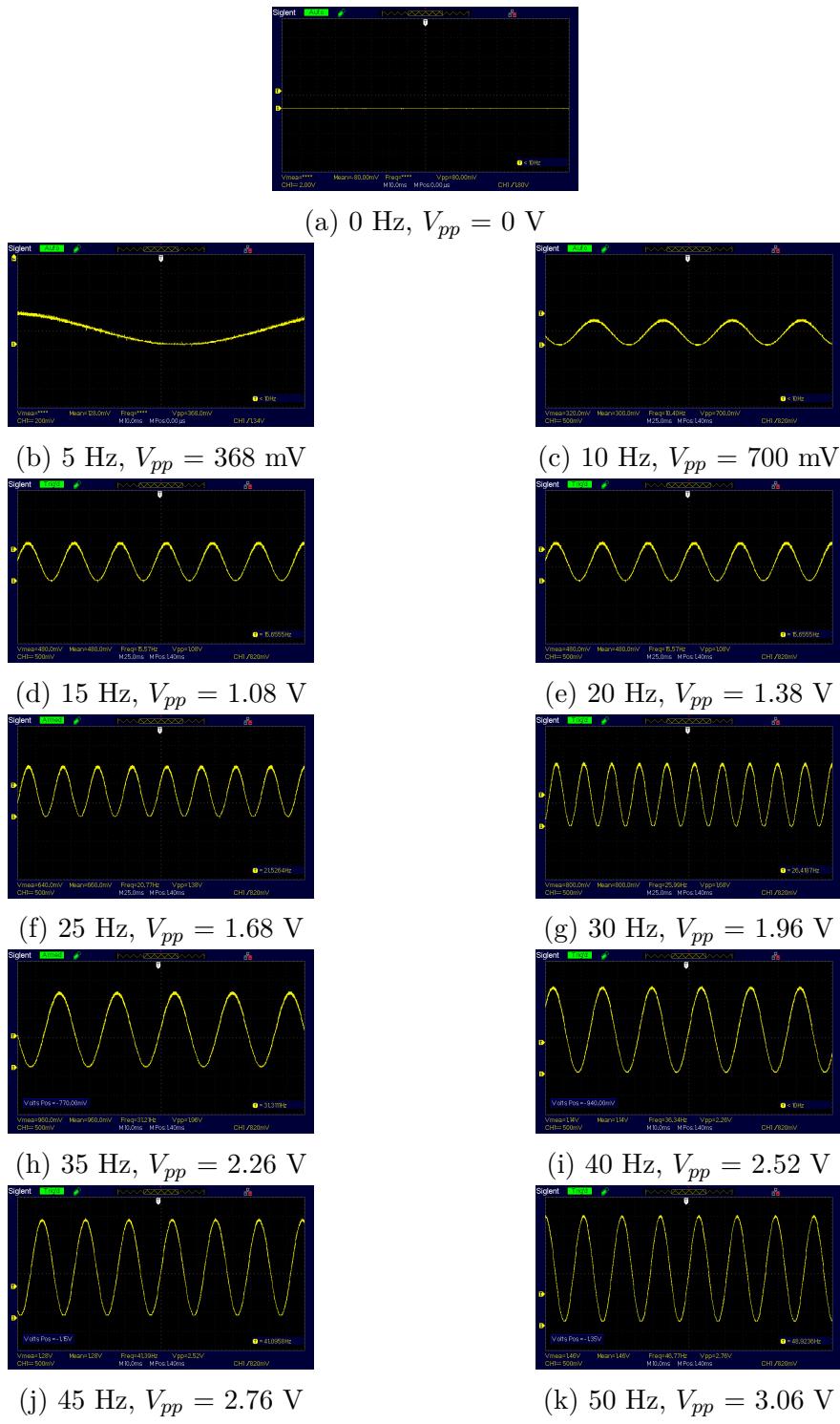


Figure 15: Voltage waveforms corresponding to frequencies observed on a DSO

## 9 Conclusion

This project successfully demonstrates the open-loop implementation of V/f (Voltage/Frequency) control for a three-phase inverter system using FPGA-generated Sinusoidal Pulse Width Modulation (SPWM). The main objective was to control the output voltage and frequency of the inverter in such a way that their ratio remains constant, thereby maintaining the desired magnetic flux in a three-phase induction motor under variable speed conditions. Although a motor was not used, the control strategy was validated using a resistive (R) load.

The FPGA was used to generate three-phase SPWM signals with precise 120° phase shifts, enabling control of a three-phase inverter. These SPWM waveforms were synthesized digitally and sent to the inverter's gate driver circuit, which converted a fixed DC input into a variable-frequency and variable-voltage AC output. By keeping the V/f ratio constant, the system emulates the expected behavior of an open-loop induction motor drive.

Frequency control was implemented through DIP switch configurations on the FPGA board, allowing discrete frequency steps from 0 Hz to 50 Hz in 5 Hz intervals. For each frequency step, the modulation index was dynamically adjusted within the FPGA to ensure that the output voltage scaled proportionally with frequency, thus maintaining the desired constant V/f profile. This method helps prevent issues such as magnetic saturation at low frequencies and flux weakening at higher speeds (within the linear region).

The hardware implementation on a resistive load confirmed the effectiveness of the generated SPWM signals. The results verified that the system can reliably modulate both frequency and amplitude in an open-loop configuration without feedback.

In summary, this project establishes a foundational open-loop V/f control system using FPGA for inverter-based applications. It offers a scalable and reconfigurable platform suitable for further developments such as closed-loop control, actual motor integration, and advanced modulation techniques.

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