Shubham Shrivastava

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Summary

Design for Test (DFT) Engineer with 3+ years of experience, currently working at Marvell Semiconductors in the Data Center Engineering BU. Skilled in end-to-end DFT implementation and test methodologies across 3nm, 5nm, and 7nm technology nodes, with strong problem-solving abilities.

Experience

Senior Digital IC Design Engineer, Marvell India Pvt. Ltd. – Bengaluru, Karnataka June 2022 – Present

- DFT End-to-End Execution:
  - Led a partition in a Chiplet-based project, ensuring high-quality and timely delivery of all hierarchical blocks.
  - Performed various DFT tasks including MBIST, EDT-OCC, Scan insertion, ATPG, and simulations.
  - Collaborated with the chip lead to implement layout-aware SSN, IJTAG, and BISR architecture.
  - Responsible for achieving ATPG coverage targets across all hierarchical blocks within the partition.
  - Performed re-targeting and extest pattern generation at the partition level.
  - Generated flat-SDC at the partition level to deliver reliable DFT constraints.
  - Debugged multiple MBIST simulation failures using Cadence tools.
  - Collaborated with cross-functional teams to align DFT implementation with RTL and PD requirements.
- DFT Methodology:
  - Developed a robust end-to-end Clock Mesh DFT solution using Tessent, improving scalability for large-die, high-frequency designs.
  - Developed automation to support tile-based designs for controlling the memory margin pins, with detailed documentation.
  - Enhanced methodology by evaluating and integrating custom MBIST patterns for multiple memory vendors.

Digital IC Design Intern, Marvell India Pvt. Ltd. – Bengaluru, Karnataka June 2021 – May 2022

- Worked on a test chip project (Viraj) and performed end-to-end DFT execution on a hierarchical block.
- Delivered VCDs for ATPG and MBIST patterns to assist the power team's correlation activities.
- Developed a custom TCL script to automate "delete no fault" operations on memory instance pins.

Education

Visvesvaraya National Institute of Technology, Nagpur Sept 2020 – June 2022

- MTech in Communication Systems | CGPA: 7.4/10.0

Government Engineering College, Raipur Aug 2014 – June 2018

- BE in Electronics and Telecommunication | CGPA: 8.0/10.0

Skills

Languages: TCL, Verilog, Python(Basic)

Tools: Tessent, Xcelium, Design Compiler, Formality, Defacto, Spyglass, JIRA, MS-Office

Achievements:

- Published a paper titled *"Methods and Apparatus to Support Multiple Synchronous Clocks with a Single Clock Mesh"* at the **IEEE 33rd Asian Test Symposium (ATS), 2024.** Paper Link
- Presented on "DFT Implementation Challenges for Clock Mesh/Grid-based Clocking Architecture" at the invite-only **Industry Test-Challenges session, ITC India 2025.**
- Received the Gold Award for timely delivery of a floorplan-aware partition to the Physical Design team, contributing to successful project milestones.