SHUBHAM SHRIVASTAVA

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SUMMARY:

Design for Test (DFT) Engineer with nearly 4 years of experience, currently at Marvell Semiconductors. Skilled in end-to-end DFT execution, test methodology, and delivering high-quality silicon through strong leadership and problem-solving abilities.

EXPERIENCE:

Marvell India Pvt. Ltd.: Senior Digital IC Design Engineer
June 2022 - Present

1. **DFT End-to-End Execution:**
   - Led a partition in a Chiplet-based project, ensuring high-quality and timely delivery of all hierarchical blocks to the PD team.
   - Performed various DFT tasks including MBIST, EDT-OCC, Scan insertion, ATPG, and simulations.
   - Collaborated with the chip lead to implement layout-aware SSN, IJTAG, and BISR architecture.
   - Responsible for achieving ATPG coverage targets across all hierarchical blocks within the partition.
   - Performed re-targeting and extest pattern generation at the partition level.
   - Generated flat-SDC at the partition level to deliver reliable DFT constraints.
   - Debugged multiple MBIST simulation failures using Cadence tools.
   - Collaborated with Physical Design and Timing teams to align DFT implementation with design constraints and timing requirements.
2. **DFT Methodology:**
   - Implemented end-to-end Clock Mesh DFT architecture from MBIST to ATPG using Tessent, enabling support for high-frequency designs with larger die sizes.
   - Evaluated and integrated MBIST custom patterns into the DFT flow.

INTERNSHIP:

Marvell India Pvt. Ltd.: Digital IC Design Intern
June 2021 - May 2022

- Worked on a test chip project (Viraj) and performed end-to-end DFT execution on a hierarchical block using Tessent.
- Performed power correlation between pre-silicon and post-silicon by coordinating with the power team and generating VCDs for multiple ATPG and MBIST patterns.
- Developed a custom TCL script to automate "delete no fault" operations on memory instance pins.

SKILLS:

Languages: TCL, Verilog, Python(Basic), LaTeX

Tools: Tessent, Xcelium, Simvision, JIRA, Design Compiler, Formality, Defacto

EDUCATION:

Qualification	Institution	Year	CGPA/%
M.Tech(Comm.System)	VNIT,Nagpur	2020-22	7.4
B.E.(ECE)	Govt.Engineering College,Raipur	2014-18	8.0
XII Board - CBSE	Holy Cross Sr. Sec. School Kapa,Raipur	2014	81%
X Board - CBSE	Holy Cross Sr. Sec. School Kapa,Raipur	2012	8.2

COURSES:

1. Hardware Modeling using Verilog Course by NPTEL
2. Programming for Everybody (Getting Started with Python) by University of Michigan on Coursera.
3. Programming in C++ Course by NPTEL.
4. Course on VLSI Design & Embedded System for one month at MNNIT, Allahabad.

PUBLICATION:

- Published a paper titled *"Methods and Apparatus to Support Multiple Synchronous Clocks with a Single Clock Mesh"* at the **IEEE 33rd Asian Test Symposium (ATS), 2024.**Link

ACHIEVEMENTS:

1. Selected to present "*DFT Implementation Challenges for Clock Mesh/Grid-based Clocking Architecture*" at the invite-only **ITC-India 2025** Industry Test-Challenges session.
2. Received the Silver Award in recognition of my support in MBIST activities, contributing to the successful execution and delivery of the project.
3. Recognized as 'DFT Trailblazer of the Month' for advancing EMA methodology and actively contributing to Marvell Internal Forums.

Hobbies: Badminton, Diary Writing, Swimming