Shubham Shrivastava

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Summary

Design for Test (DFT) Engineer with 3 years of experience, currently working at Marvell Semiconductors in the Data Center Engineering BU. Skilled in end-to-end DFT implementation and test methodologies across 3nm, 5nm, and 7nm technology nodes, with strong leadership and problem-solving abilities.

Experience

Senior Digital IC Design Engineer, Marvell India Pvt. Ltd. – Bengaluru, Karnataka June 2022 – Present

- DFT End-to-End Execution:
  - Led a partition in a Chiplet-based project, ensuring high-quality and timely delivery of all hierarchical blocks to the PD team.
  - Performed various DFT tasks including MBIST, EDT-OCC, Scan insertion, ATPG, and simulations.
  - Collaborated with the chip lead to implement layout-aware SSN, IJTAG, and BISR architecture.
  - Responsible for achieving ATPG coverage targets across all hierarchical blocks within the partition.
  - Generated flat-SDC at the partition level to deliver reliable DFT constraints.
  - Debugged multiple MBIST simulation failures using Cadence tools.
  - Collaborated with Physical Design and Timing teams to align DFT implementation with design constraints and timing requirements.
- DFT Methodology:
  - Implemented end-to-end Clock Mesh DFT architecture from MBIST to ATPG using Tessent, enabling support for high-frequency designs with larger die sizes.
  - Evaluated and integrated MBIST custom patterns into the DFT flow.

Digital IC Design Intern, Marvell India Pvt. Ltd. – Bengaluru, Karnataka June 2021 – May 2022

- Worked on a test chip project (Viraj) and performed end-to-end DFT execution on a hierarchical block using Tessent.
- Performed power correlation between pre-silicon and post-silicon by coordinating with the power team and generating VCDs for multiple ATPG and MBIST patterns.
- Developed a custom TCL script to automate "delete no fault" operations on memory instance pins.

Education

Visvesvaraya National Institute of Technology, Nagpur Sept 2020 – June 2022

- MTech in Communication Systems | CGPA: 7.4/10.0

Government Engineering College, Raipur Aug 2014 – June 2018

- BE in Electronics and Telecommunication | CGPA: 8.0/10.0

Skills

Languages: TCL, Verilog, Python(Basic), LaTeX

Tools: Tessent, Xcelium, Simvision, JIRA, Design Compiler, Formality, Defacto, MS-Office

Courses

- Hardware Modeling using Verilog Course by NPTEL.
- Programming for Everybody (Getting Started with Python) by University of Michigan on Coursera.
- Course on VLSI Design & Embedded System for one month at MNNIT, Allahabad.

Publications

- Published a paper titled *"Methods and Apparatus to Support Multiple Synchronous Clocks with a Single Clock Mesh"* at the **IEEE 33rd Asian Test Symposium (ATS), 2024.** Paper Link

Achievements & Extra-Curricular:

- Presented on "DFT Implementation Challenges for Clock Mesh/Grid-based Clocking Architecture" at the invite-only **Industry Test-Challenges session, ITC India 2025.**
- Received the Silver Award in recognition of my support in MBIST activities, contributing to the successful execution and delivery of the project.
- Recognized as 'DFT Trailblazer of the Month' for advancing EMA methodology and actively contributing to Marvell Internal Forum.

Hobbies: Badminton, Diary Writing, Swimming