Shubham Kumar

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Professional Summary

B. Tech Electrical Engineering student at IIT Jodhpur specializing in hardware-software co-design, embedded systems, and performance optimization. Experienced in VLSI design, FPGA programming, real-time embedded systems, and systems-level programming with strong foundations in computer architecture and parallel computing.

EDUCATION

2022 - 2026 B.Tech in Electrical Engineering at IIT Jodhpur (CGPA: 7.68/10.0)

Technical Skills

Systems & Hardware Embedded Systems (STM32, Arduino, FPGA), Verilog, Computer Architecture, ARM/x86/

MIPS Assembly

Programming Languages C++, C, Python, Java, Rust, SQL

Parallel & Performance OpenMP, MPI, CUDA (learning), Hardware Acceleration, Optimization

EDA & Circuit Tools Cadence Virtuoso, LTspice, Vivado, Simulink, MATLAB

Software Development Git, Flutter, Firebase, Django, REST APIs

ML Frameworks TensorFlow, OpenCV, Scikit-learn, Pandas, NumPy (familiarity)

EXPERIENCE

Inter-IIT Tech Meet 12.0

Dec 2023

Quantum Computing Project

IIT Madras, Chennai

GitHub Link

Team Rank: Top 10% among 23 IITs

- Developed a Streamlit interface for rescheduling 20+ flights using D-Wave's hybrid quantum solvers.
- Optimized rerouting efficiency with < 10% deviation from classical baselines under real-time constraints.
- Integrated backend quantum solver with dynamic UI handling 15+ parameters, improving airline usability.
- Presented live demo to Mphasis and IIT panel, securing top 10% rank among 23+ participating IIT teams.

Technical Projects

CUDA-Accelerated Image Processing Toolkit

[In Development]

GPU Computing, Performance Optimization

- Building parallel GPU-accelerated image filters (Gaussian blur, edge detection, brightness adjustment) using CUDA C++
- Implementing performance comparison framework measuring CPU vs GPU execution times with speedup analysis for various image sizes
- Optimizing CUDA kernel configurations (block/grid dimensions) and memory transfers for maximum throughput

Multifunctional Digital Clock

GitHub — YouTube Demo

PYNQ-Z2 FPGA, Verilog — Digital Design, HDL

- Designed and implemented complete digital system in Verilog with 4 operational modes: clock, timer, stopwatch, and alarm functionality
- Achieved precise timing control with ± 1 -second accuracy through careful clock division and synchronization logic
- Optimized display multiplexing: drove four seven-segment displays using single output port to minimize I/O pin usage

Real-Time Analog Signal Visualizer

STM32F429 Discovery Board — Embedded Systems, Real-Time Programming

- Developed a full-featured digital oscilloscope on ARM Cortex-M4 with custom LCD driver and touchscreen interface.
- Implemented real-time ADC sampling, signal processing, and waveform visualization with adjustable timebase (1-500 ms) and gain control.
- Integrated ADC, LCD(LTDC/DMA2D), I2C touchscreen & UART modules to achieve low-latency system performance.

Relevant Coursework

Core Systems Data Structures & Algorithms, Computer Architecture, Embedded Systems, Digital Design

Hardware Design VLSI Design, Analog Electronics, Semiconductor Devices, Control Systems

Mathematics & Theory Linear Algebra, Probability & Statistics

Pattern Recognition & Machine Learning, Computer Vision, Artificial Intelligence ML/AI (Exposure)

Leadership & Extracurriculars

Class Representative — Electrical Engineering Batch 2026, IIT Jodhpur Aug 2023 - Present

Core Member — DevlUp Labs (Open Source Organization), IIT Jodhpur

Core Member — RAID (AI/ML/DL Club), IIT Jodhpur

Assistant Head — Prometeo'24 & Varchas'23 (College Technical & Sports Fests), IIT Jodhpur