Experiment No: 3

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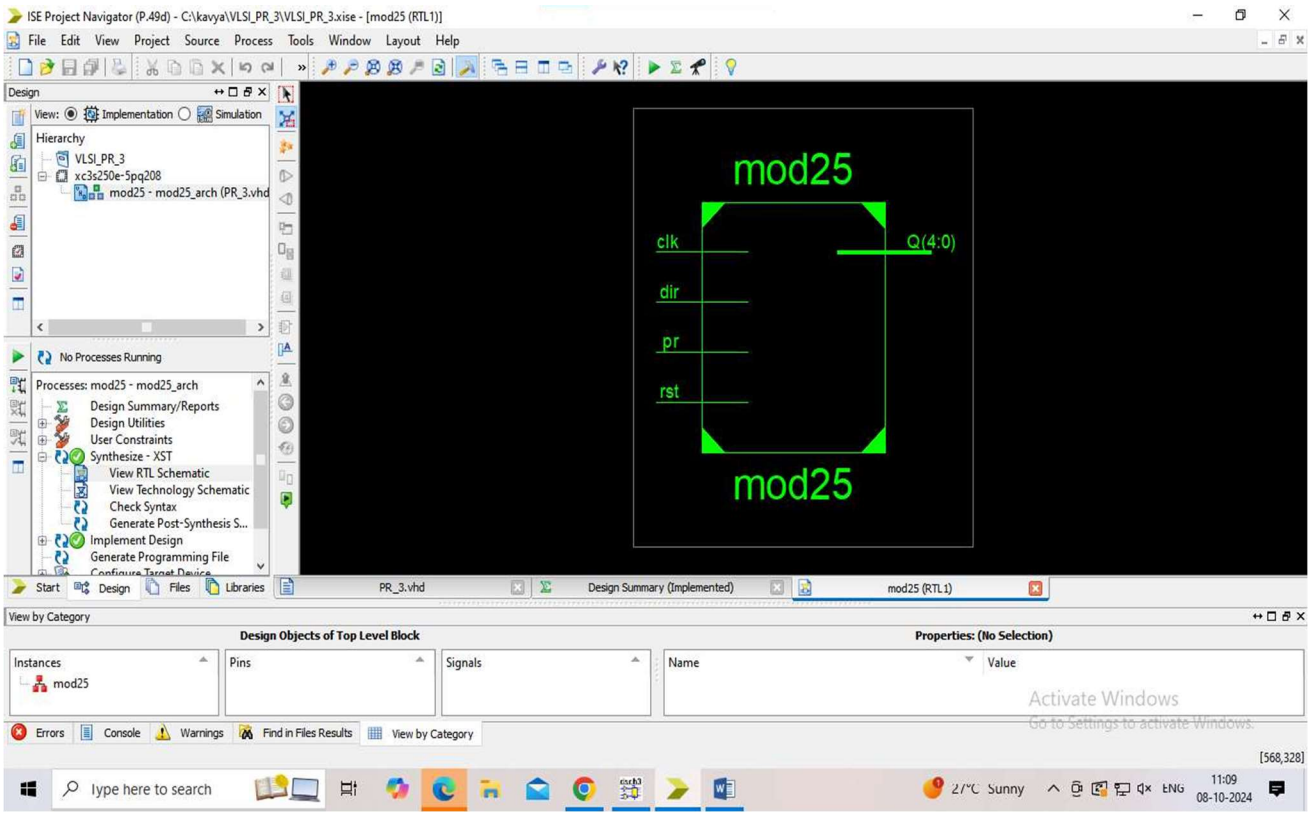
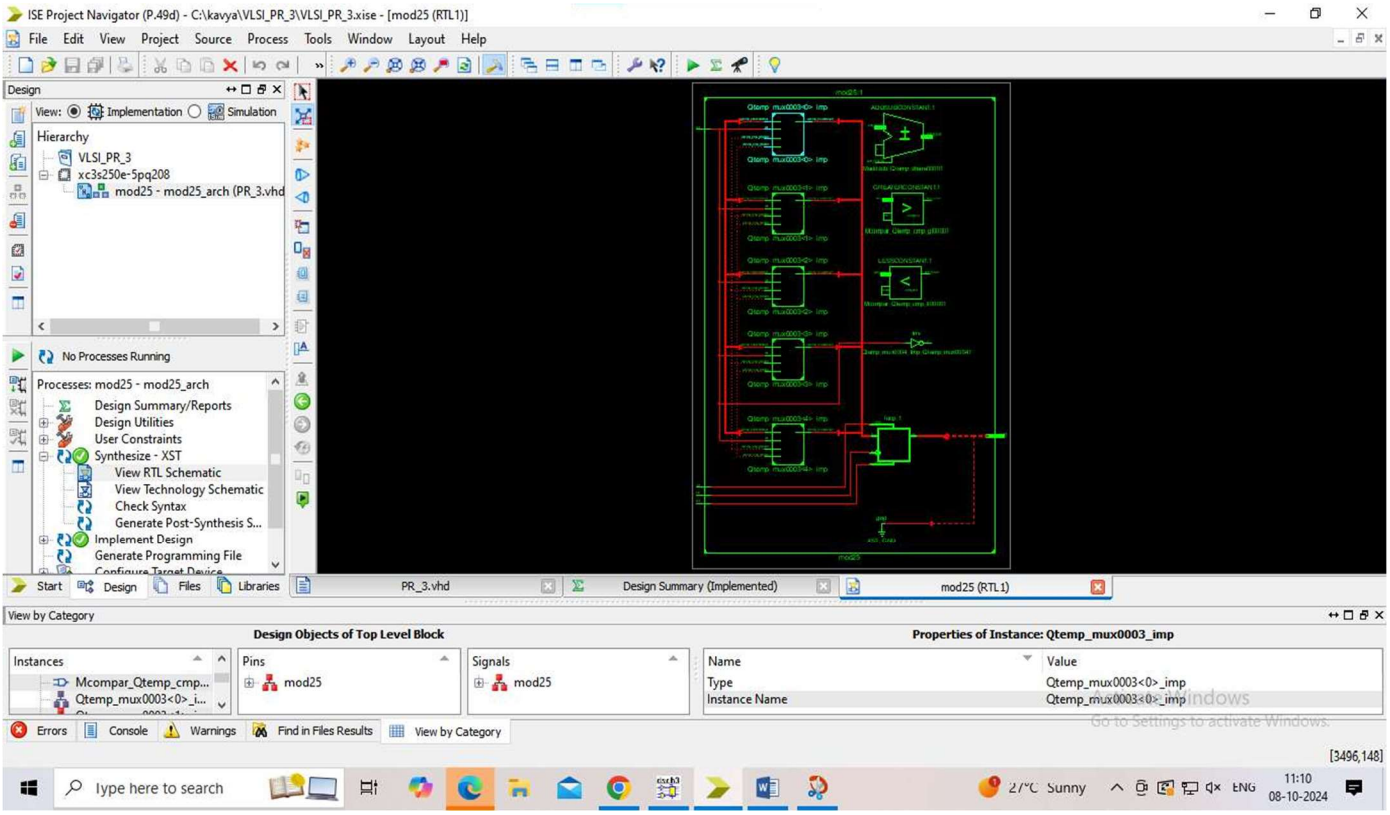
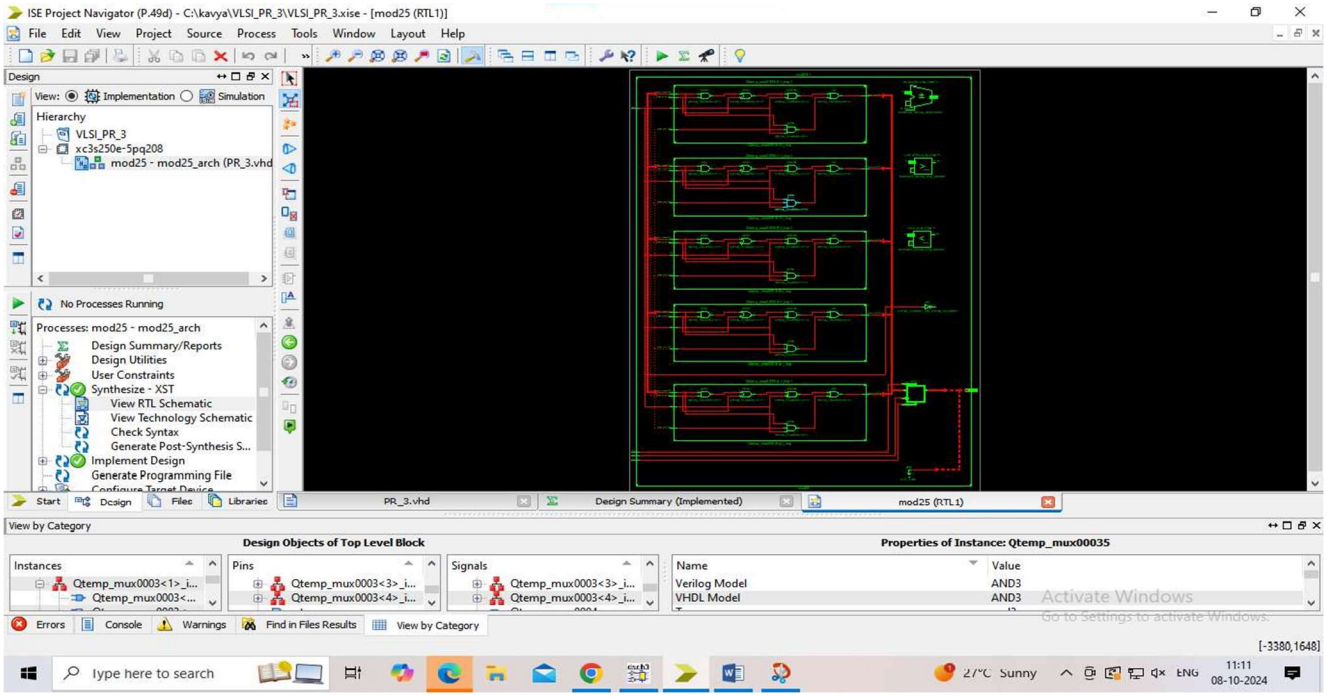
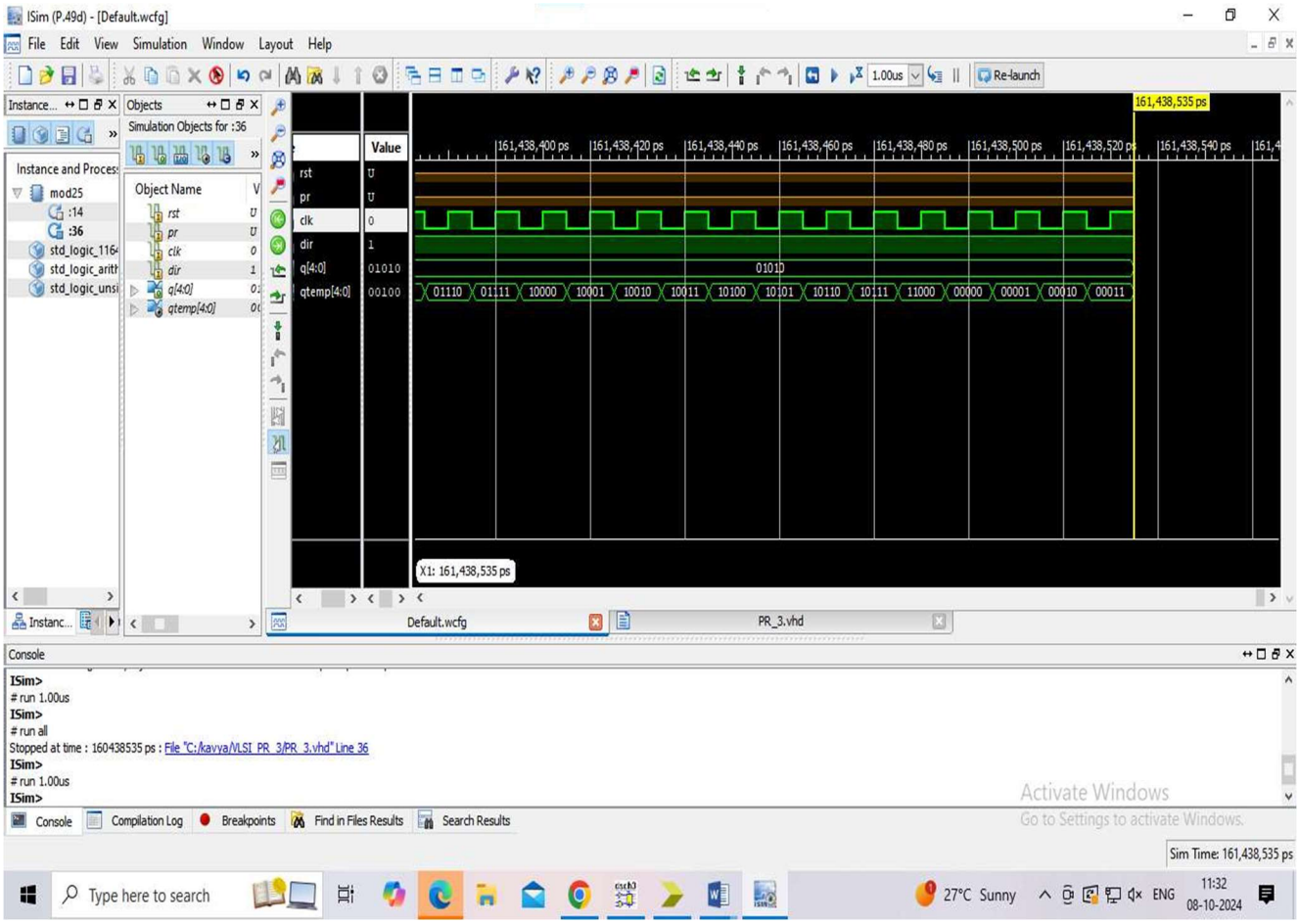
Roll No.: E42067

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity mod25 is
 Port ( rst : in STD_LOGIC; pr : in STD_LOGIC;
 clk : in STD_LOGIC; dir : in STD_LOGIC;
 Q : out STD_LOGIC_VECTOR (4 downto 0)); end mod25;
architecture mod25_arch of mod25 is
signal Qtemp : STD_LOGIC_VECTOR (4 downto 0) := "00000"; begin
 process(rst,pr,clk,dir) begin
 if rst ='1' then
 Qtemp <= (OTHERS =>'0');
 elsif pr='1' then
 Qtemp <= (OTHERS =>'1');
 elsif falling_edge(clk) then if dir = '1' then
 if Qtemp < 24 then Qtemp <= Qtemp + 1; else
 Qtemp <= "00000";
 end if; else
 if Qtemp > 7 then Qtemp <= Qtemp - 1; else
 Qtemp <= "11111";
end if;
 end if;
end if;
end process;
 Q<=Qtemp;
end mod25_arch;
```


ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
mod25
clk
dir
pr
rst
Q(4:0)
mod25
Start Design Files Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
mod25
Pins
Signals
Name
Value
Activate Windows
Go to Settings to activate Windows.
Errors Console Warnings Find in Files Results View by Category
[568,328]
Type here to search
27°C Sunny
ENG
11:09
08-10-2024


ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
Start Design Files Libraries
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: Qtemp_mux0003_imp
Instances
Mcompar_Qtemp_cmp...
Qtemp_mux0003<0>_i...
Pins
mod25
Signals
mod25
Name
Value
Type
Qtemp_mux0003<0>_imp
Instance Name
Qtemp_mux0003<0>_imp
Errors Console Warnings Find in Files Results View by Category
[3496,148]
Type here to search
27°C Sunny
ENG
11:10
08-10-2024


ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [mod25 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
VLSI_PR_3
xc3s250e-5pq208
mod25 - mod25_arch (PR_3.vhd
No Processes Running
Processes: mod25 - mod25_arch
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Generate Programming File
PR_3.vhd
Design Summary (Implemented)
mod25 (RTL1)
View by Category
Design Objects of Top Level Block
Properties of Instance: Qtemp_mux00035
Instances
Pins
Signals
Name
Value
Verilog Model
AND3
VHDL Model
AND3
Activate Windows
Errors
Console
Warnings
Find in Files Results
View by Category
[-3380,1648]
Type here to search
27°C Sunny
ENG
11:11
08-10-2024


ISim (P.49d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
1.00us
Instance and Proces
mod25
:14
:36
std_logic_116
std_logic_arith
std_logic_unsi
Objects
Simulation Objects for :36
Object Name
rst
pr
clk
dir
q[4:0]
qtemp[4:0]
Value
0
1
01010
00100
161,438,535 ps
161,438,400 ps
161,438,420 ps
161,438,440 ps
161,438,460 ps
161,438,480 ps
161,438,500 ps
161,438,520 ps
161,438,540 ps
01010
01110
01111
10000
10001
10010
10011
10100
10101
10110
10111
11000
00000
00001
00010
00011
X1: 161,438,535 ps
Default.wcfg
PR_3.vhd
Console
ISim>
run 1.00us
ISim>
run all
Stopped at time : 160438535 ps : File "C:/kavya/VLSI_PR_3/PR_3.vhd" Line 36
ISim>
run 1.00us
ISim>
Activate Windows
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 161,438,535 ps
Type here to search
27°C Sunny
ENG
11:32
08-10-2024

ISE Project Navigator (P.49d) - C:\kavya\VLSI_PR_3\VLSI_PR_3.xise - [PR_3a.ucf]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

VLSI_PR_3

xc3s250e-5pq208

mod25 - mod25_arch (PR_3.vhd

No Processes Running

Processes: mod25 - mod25_arch

Design Summary/Reports

Design Utilities

User Constraints

Synthesize - XST

Implement Design

Translate

Map

Place & Route

Generate Programming File

Configure Target Device

```
1  NET "Q[4]" LOC = P164;
2  NET "Q[3]" LOC = P162;
3  NET "Q[2]" LOC = P161;
4  NET "Q[1]" LOC = P160;
5  NET "Q[0]" LOC = P153;
6  NET "clk" LOC = P132;
7  NET "dir" LOC = P202;
8  NET "pr" LOC = P204;
9  NET "rst" LOC = P194;
```

Start Design Files Libraries PR_3.vhd Design Summary (Implemented) mod25 (RTL) PR_3a.ucf

View by Category

Design Objects of Top Level Block

Instances: Qtemp_mux0003<1>_i... Qtemp_mux0003<...

Pins: Qtemp_mux0003<3>_i... Qtemp_mux0003<4>_i...

Signals: Qtemp_mux0003<3>_i... Qtemp_mux0003<4>_i...

Properties of Instance: Qtemp_mux00035

Name	Value
Verilog Model	AND3
VHDL Model	AND3

Activate Windows

Go to Settings to activate Windows.

Errors Console Warnings Find in Files Results View by Category

Ln 9 Col 23 UCF

Type here to search 27°C Sunny ENG 11:16 08-10-2024