Experiment No: 2

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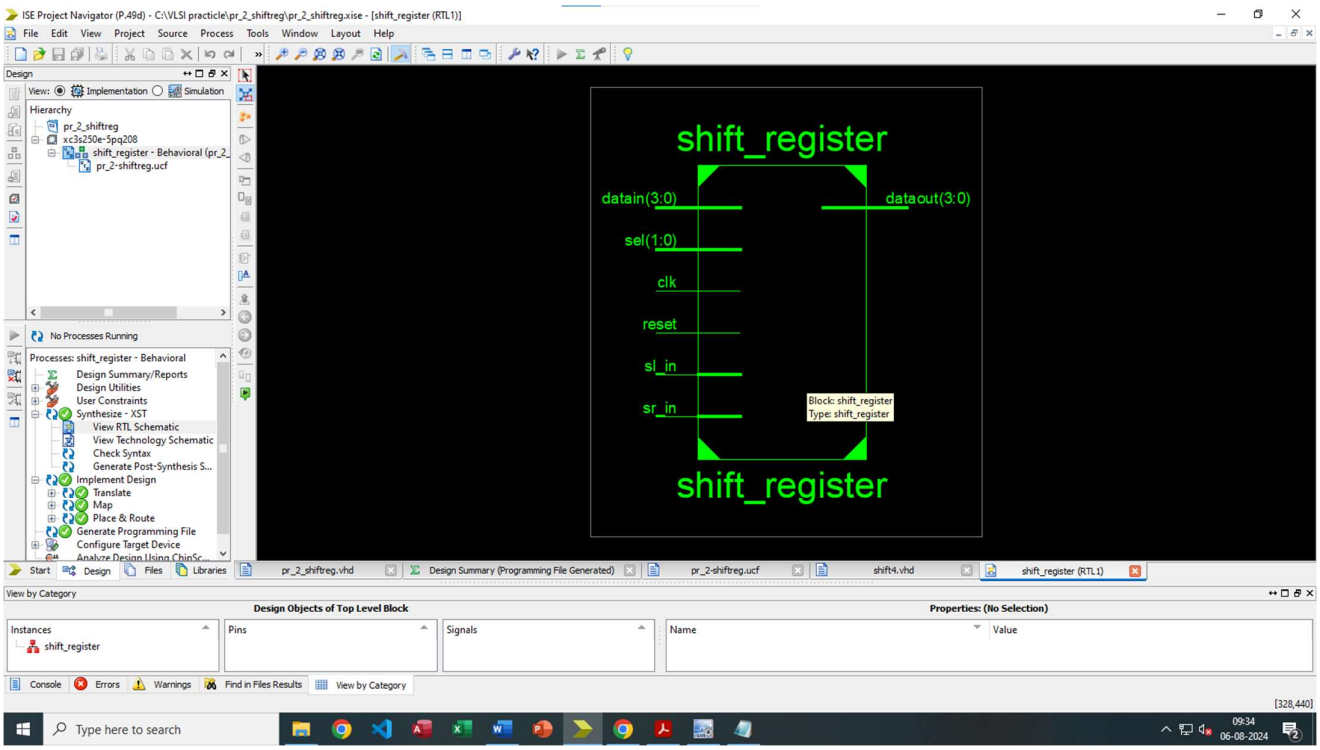
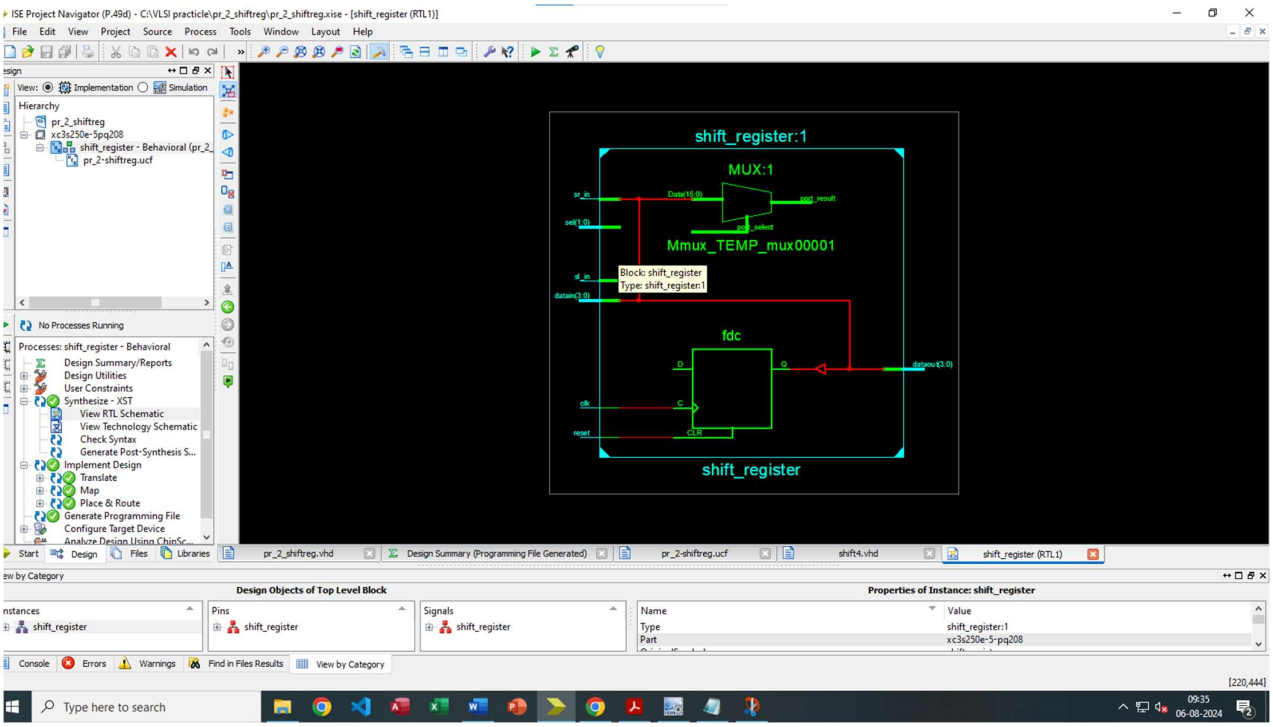
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity shift_register is
Port ( clk : in STD_LOGIC;
reset: in STD_LOGIC;
datain: in STD_LOGIC_VECTOR (3 downto 0);
sel: in STD_LOGIC_VECTOR (1 downto 0);
sl_in: in STD_LOGIC;
sr_in: in STD_LOGIC;
dataout: out STD_LOGIC_VECTOR (3 downto 0));
end shift_register;
architecture Behavioral of shift_register is
begin
Process (reset, clk, sel, sl_in, sr_in, datain)
variable TEMP : STD_LOGIC_VECTOR (3 downto 0);
begin if reset = '1' then TEMP := "0000";
elsif clk'event and clk = '1' then case Sel is when "11" => TEMP := datain;
when "01" => TEMP := TEMP(2 downto 0) & sl_in;
when "10" => TEMP := sr_in & TEMP(3 downto 1);
when others => NULL;
end case;
end if;
dataout <= TEMP;
end process;
end Behavioral;
```


ISE Project Navigator (P.49d) - C:\VLSI practicle\pr_2_shiftreg\pr_2_shiftreg.xise - [shift_register (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
pr_2_shiftreg
xc3s250e-5pq208
shift_register - Behavioral (pr_2_
pr_2-shiftreg.ucf
No Processes Running
Processes: shift_register - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Translate
Map
Place & Route
Generate Programming File
Configure Target Device
shift_register
datain(3:0)
sel(1:0)
clk
reset
sl_in
sr_in
dataout(3:0)
Block: shift_register
Type: shift_register
shift_register
Start Design Files Libraries
pr_2_shiftreg.vhd
Design Summary (Programming File Generated)
pr_2-shiftreg.ucf
shift4.vhd
shift_register (RTL1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
shift_register
Pins
Signals
Name
Value
Console Errors Warnings Find in Files Results View by Category
[328,440]
Type here to search
09:34
06-08-2024


ISE Project Navigator (P.49d) - C:\VLSI practicle\pr_2_shiftreg\pr_2_shiftreg.xise - [shift_register (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Hierarchy
pr_2_shiftreg
xc3s250e-5pq208
shift_register - Behavioral (pr_2_
pr_2-shiftreg.ucf
No Processes Running
Processes: shift_register - Behavioral
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis S...
Implement Design
Translate
Map
Place & Route
Generate Programming File
Configure Target Device
shift_register:1
MUX:1
sr_in
Data(16,0)
sel(1:0)
Mmux_TEMP_mux00001
sl_in
datain(3:0)
Block: shift_register
Type: shift_register:1
fdc
D
Q
dataout(3:0)
clk
C
reset
CLR
shift_register
Start Design Files Libraries
pr_2_shiftreg.vhd
Design Summary (Programming File Generated)
pr_2-shiftreg.ucf
shift4.vhd
shift_register (RTL1)
Design Objects of Top Level Block
Properties of Instance: shift_register
shift_register
Pins
Signals
Name
Value
Type
shift_register:1
Part
xc3s250e-5-pq208
Console Errors Warnings Find in Files Results View by Category
[220,444]
Type here to search
09:35
06-08-2024

NET "clk" LOC = P132;

NET "reset" LOC = P204;

NET "sl_in" LOC = P179;

NET "sr_in" LOC = P180;

NET "sel<0>" LOC = P165;

NET "sel<1>" LOC = P167;

NET "datain<0>" LOC = P192;

NET "datain<1>" LOC = P193;

NET "datain<2>" LOC = P189;

NET "datain<3>" LOC = P190;

NET "dataout<0>" LOC = P205;

NET "dataout<1>" LOC = P206;

NET "dataout<2>" LOC = P203;

NET "dataout<3>" LOC = P200;