Akhil Jain - 14CS10003

Shubham Jain - 14CS10043

OP-CODE encoding

<table>
<tr><th rowspan="2">0th bit (Jump/ Non-Jump)</th><th colspan="4">(1-6)bits</th></tr>
<tr><th colspan="2">(1-3)bits
fsel(ALU)/load/store</th><th colspan="2">(4-6)bits
Addressing Modes</th></tr>
<tr><td rowspan="8">0</td><td>add</td><td>000</td><td>register</td><td>000</td></tr>
<tr><td>sub</td><td>001</td><td>immediate</td><td>001</td></tr>
<tr><td>and</td><td>010</td><td rowspan="2">Base-indexed addressing</td><td rowspan="2">010</td></tr>
<tr><td>or</td><td>011</td></tr>
<tr><td>mns</td><td>100</td><td rowspan="2">Base addressing</td><td rowspan="2">011</td></tr>
<tr><td>cmp</td><td>101</td></tr>
<tr><td>ld</td><td>110</td><td>Indirect</td><td>100</td></tr>
<tr><td>sw</td><td>111</td><td>PC relative</td><td>101</td></tr>
<tr><td rowspan="13">1
(Jumps)</td><td colspan="2">j</td><td colspan="2">0000xx</td></tr>
<tr><td colspan="2">jz</td><td colspan="2">0001xx</td></tr>
<tr><td colspan="2">jnz</td><td colspan="2">0010xx</td></tr>
<tr><td colspan="2">jc</td><td colspan="2">0011xx</td></tr>
<tr><td colspan="2">jnc</td><td colspan="2">0100xx</td></tr>
<tr><td colspan="2">jv</td><td colspan="2">0101xx</td></tr>
<tr><td colspan="2">jnv</td><td colspan="2">0110xx</td></tr>
<tr><td colspan="2">jm</td><td colspan="2">0111xx</td></tr>
<tr><td colspan="2">jnm</td><td colspan="2">1000xx</td></tr>
<tr><td colspan="2">jal</td><td colspan="2">1001xx</td></tr>
<tr><td colspan="2">jr</td><td colspan="2">1010xx</td></tr>
</table>

The remaining 9-bits (7-15) are for the registers.

If we require the next 16-bit depending upon the addressing modes then all the 16-bits are storing the required 16-bits.