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Instruction Interpretation

Instruction	Op-code	Interpretation	RTL level Interpretation
addr (Add - Register mode)	0 000 000	r1 <= r1 + r2	r1 <= r1 + r2
subi (Sub - Immediate mode)	0 001 001	r1 <= r1 + M[PC]	MAR <= PC PC <= PC + 2 MDR <= M[MAR] r1 <= r1 - MDR
andx (And - Base Indexed Addressing mode)	0 010 010	r1 <= r1 & M[r2 + r3 + M[PC]]	MAR <= PC PC <= PC + 2 MDR <= M[MAR] temp <= r2 + MDR MAR <= r3 + temp MDR <= M[MAR] r1 <= r1 & MDR
ora (Or - Base Addressing mode)	0 011 011	r1 <= r1 | M[r2 + r3]	MAR <= r2 + r3 MDR <= M[MAR] r1 <= r1 | MDR
mnsn (Minus - Indirect mode)	0 100 100	Z <= r1 - M[M[r2 + r3 + M[PC]]]	MAR <= PC PC <= PC + 2 MDR <= M[MAR] temp <= r2 + MDR MAR <= r3 + temp MDR <= M[MAR] MAR <= MDR MDR <= M[MAR] Z <= r1 - MDR
ldn (Load - Indirect mode)	0 110 100	r1 <= M[M[r2 + r3 + M[PC]]]	MAR <= PC PC <= PC + 2 MDR <= M[MAR] temp <= r2 + MDR MAR <= r3 + temp MDR <= M[MAR] MAR <= MDR MDR <= M[MAR] r1 <= MDR
stx (Store - Base Indexed Addressing mode)	0 111 010	M[r1 + r2 + M[PC]] <= r3	MAR <= PC PC <= PC + 2 MDR <= M[MAR] temp <= r2 + MDR MAR <= r1 + temp MDR <= r3 M[MAR] <= MDR
j (Jump - PC relative)	1 0000xx	PC <= PC + M[PC]	MAR <= PC PC <= PC + 2 MDR <= M[MAR] PC <= PC + MDR

PC : Program Counter Register
MAR : Memory Address Register
temp : Temporary Register
M[A] : Data from memory at the address A
MDR : Memory Data Register
ri : Register from Register bank given by operand i