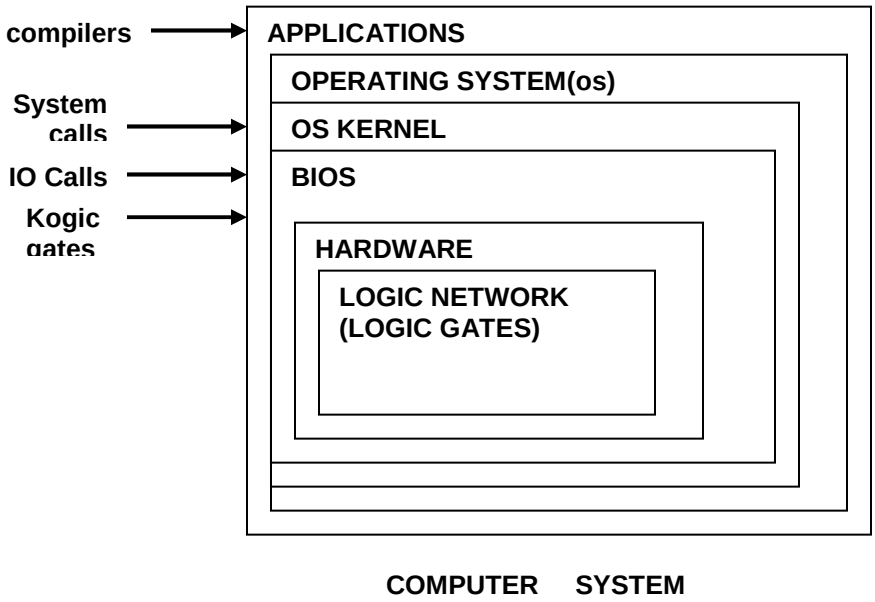
# CS 210 LOGIC DESIGN and
# CS 288 logic Design Lab
# Course Objectives and contents

Prof M R Bhujade




COMPUTER SYSTEM

## Lecture 1 COURSE OBJECTIVES AND MOTIVATION

### Objectives

- This course along with a lab forms a foundation for computer hardware design.

- It imparts basic theory and practice required to master the art of Designing Digital Systems which are part any automation we see today.

- The course also has objective to make you familiar with Computer Aided Design of Logic
- (Introduces most recent trends in the design by making you work with CAD tools which are used by chip designers.

- The knowledge imparted in this course is used extensively in the course computer organisation and microprocessor s and many others related to hardware/VLSI/architecture courses.
- At the end of course you will be able to design small automations/controls, understand the computer hardware building blocks and be literate to handle VHDL based designs

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**COURSE CONTENTS**

- **Module 1:Introduction to logic and switching functions.** Introduction to number system, Boolean algebra and switching functions**representation and properties of switching functions and their realizations using gates and switches.**

- **Module 2 Computer aided Design tools**
- Design automation tools introduction, introduction to VHDL (more of it in labs on VHDL)

**Module 3 Digital Systems Building Blocks**

Adders, Decoders/Encoders, Multiplexes/ Demultiplexers, Flip flops, Registers,Shift Registers and counters , error detection and correction logic

**Module 4 Combinational Logic Optimization**
Optimal Design of logic circuits using Minimization, Design with PLAs Minimization of Boolean functions using K Maps Quine Mckluskey algorithm.

**Module 5: Sequential Logic Design**
Finite State machines, Synchronous sequential circuits, State diagram and state table, Machine minimization. State assignments and realization of FSMs. Incompletely specified machines, FSM as a controller.

**Module 6: Asynchronous Sequential Circuits**
Fundamental mode circuits, Primitive flow table Minimization of flow tables, Minimization, race free state assignments and realisation.

**Module 7: Linear Machines**
Introduction to linear machines, transfer functions, inverse machines, application for error detection.

**Module 8 Advanced Topics**

**REFERENCE/TEXT BOOKS**


1. Bhujade, M.R. "**Digital computer design principles."** Pitamber, New Delhi. 1995
2. Unger, S.H. **Essence of logic circuits.** Publisher: Englesood Cliffs, Prentice-Hall, 1989.

3. Kohavi, Zwi **Switching and finite automata theory. 2nd ed** : Tata McGraw Hill, New Delhi, 1986
4. M R Bhujade**,** **VHDL Lecture Notes**, 1998.
5. Yalamanchili, Sudhakar **VHDL starter's guide** Upper Saddle River : Prentice-Hall, 1998
6. Stefan Sjoho;m and Lennart Lindh , "VHDL for Designers", Prentice Hall 1997

**Scheme of Assessment**
**Attendance not satisfactory XX**
**Satisfactory attendance**
**End sem 50%**
**Midsem 30%**
**2 QUIZES 20%**
**ONE WITH DATE ANNOUNCED IN ADVANCE , OTHER QUIZ ON NOT AVANCE ANNOUCEMENT DATE**

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**Email :** mrb@cse
**Course Web page :** www.cse.iitb.ac.in/~mrb**/ld** **top pane contains various course links**
**Office ; SIA112 1ST FLOOR A BLOCK KR BUILDING**

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**CS 288 LOGIC DESIGN LAB WILL BE BASED ON THE MATERIAL COVERED IN THE CLASS. And based on VHDL based design experiments to be completed in the lab time (Monday 2 to 5 pm in old software lab) and assessmed at the end ofd the lab time(at 4.30 pm)**