Experiment No. 6

Title: To prepare CMOS layout for 2:1 multiplexer using transmission gates. Simulate with and without capacitive load,comment on rise, and fall times.and fall times.

PROBLEM STATEMENT:

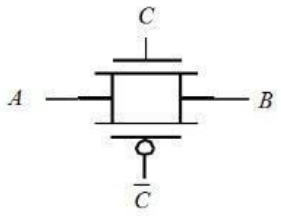
To prepare CMOS layout for 2:1 MUX using
transmission gate and compare the performance in terms of speed, space and power

OBJECTIVE:

1. To Study Logic gate implementation using conventionalapproach.
2. To Study Logic gate implementation using transmission gateapproach.
3. To compare the performance among the design.

THEORY:

A transmission gate has three inputs, called *source*, *n-gate*, and *p-gate*; and it has one output, called *drain*. When diagrammed, the *source* input and *drain* output are drawn connected by two plates. The two *gate* inputs are drawn as lines connected to plates parallel to each of the plates connecting *source* to *drain*. The *p-gate* input's line has a circle, while the *n-gate* input's line does not.



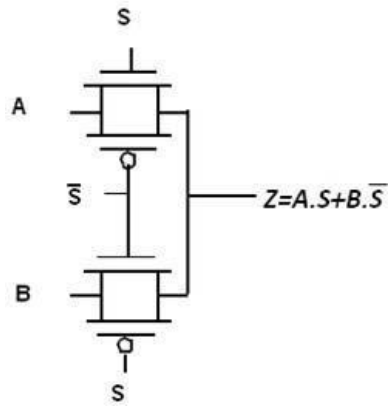
The transmission gate is simply the combination of two complementary transistors. The values at *n-gate* and *p-gate* are expected to be opposite to each other. If *p-gate* is 0 while *n-gate* is 1, then the value found at *source* is transmitted to *drain*. If *p-gate* is 1 while *p-gate* is 0, then the connection is broken, so the value at *drain* is left floating. In all other cases, *drain* receives an error output — unless *source* is floating, in which case *drain* is floating as well. This behavior is summarized by the following table.

p-gate	***n-gate***	***drain***
0	0	X*
0	1	*source*
1	0	Z
1	1	X*
X/Z	*any*	X*
any	X/Z	X*

** If source is Z, drain is Z; otherwise drain is X.*

If the Data Bits attribute is more than 1, each gate input is still a single bit, but the gate values are applied simultaneously to each of the source input's bits.

The transmission gate acts as a bidirectional switch controlled by the gate signal *C*. When *C=1*, both MOSFETs are on, allowing the signal to pass through the gate. In short, *A=B, if C=1*. On the other hand, *C=0*, places both transistors in cut-off, creating an open circuit between nodes *A* and *B*. Fig.5 shows the implementation of a 2:1 MUX using transmission gate logic.



Here, the transmission gates selects input *A* or *B* on the basis of the value of the control signal *S*. When *S=0, Z=A* and when *S=1, Z=B*.

PLATFORM USED:

1. Microwind 3.1

FAQ:

Why PMOS and NMOS are sized equally in a Transmission Gates?

In Transmission Gate, PMOS and NMOS aid each other rather competing with each other. That's the reason why we need not size them like in CMOS. In CMOS design we have NMOS and PMOS competing which is the reason we try to size them proportional to their mobility.

Why don't we use just one NMOS or PMOS transistor as a transmission gate?

NMOS passes a good 0 and a degraded 1, whereas PMOS passes a good 1 and bad 0. for pass transistor, both voltage levels need to be passed and hence both NMOS and PMOS need to be used.

CONCLUSION: