Experiment No. 5

Title: To prepare CMOS layout for Inverter Simulatewith and without capacitive load, comment on rise,

PROBLEM STATEMENT:

To prepare CMOS layout for Inverter, with and without capacitive load, comment on rise and fall time.

OBJECTIVE:

1. To manually design the mask layout of CMOS inverter
2. To check the design for design rule errors.
3. To check the functionality using simulation with the built-insimulator.
4. Measure propagation delay

THEORY:

MICROWIND program allows to design and simulate an integrated circuit. The package itself contains a library of common logic and analog ICs to view and simulate. MICROWIND includes all the commands for a mask editor as well as new original tools never gathered before in a single module. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

A specific command displays the characteristics of pMOS and nMOS, where the size of the device and the process parameters can be very easily changed. Altering the MOS model parameters and, then, seeing the effects on the Vds and Ids curves constitutes a good interactive tutorial on devices.

The MOS device

The MOS symbols are reported below. The n-channel MOS is built using polysilicon as the gate material and N+ diffusion to build the source and drain. The p-channel MOS is built using polysilicon as the gate material and P+ diffusion to build the source and drain.

CMOS Inverter:

CMOS configuration is called complementary MOS. Thecircuit topology is complementary push-pull in the sense that for high input, the NMOS transistor drives (pull- down), the output node, while the PMOS transistor act as the load, and for the low input the PMOS transistor drives (pull-up), output node, while NMOS acts as load. Consequently both devices contribute equally to the circuit operation characteristics.

The CMOS inverter has 2 input advantages over the other inverter configuration. The trend of increasing sub threshold leakage current in deep sub-micron technologies causes great design challenges. in all other inverter structures examined so far ,a non-zero steady state current is drown from the power source when the driver transistor is turned-on, which result in a significant dc power consumption. The other advantages of CMOS configuration are that the voltage swing between 0v and VDD and that the Vth is usually very sharp.

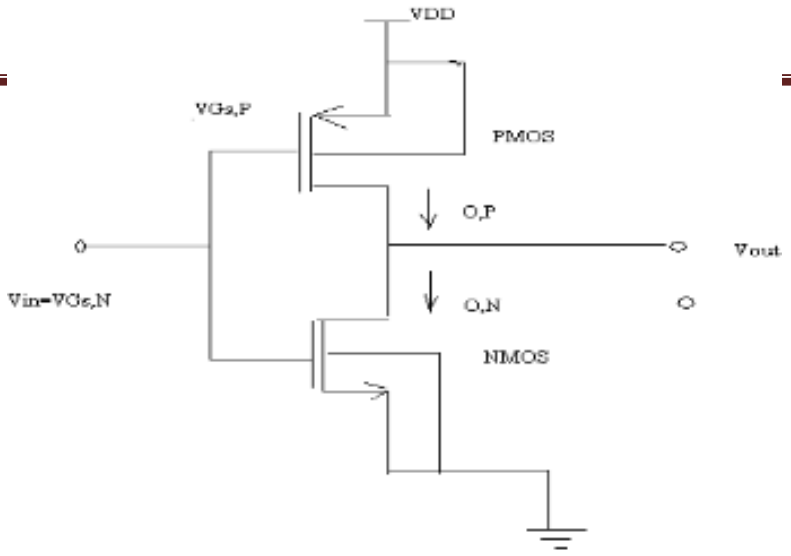

FIG. 1. CMOS INVERTER CIRCUIT

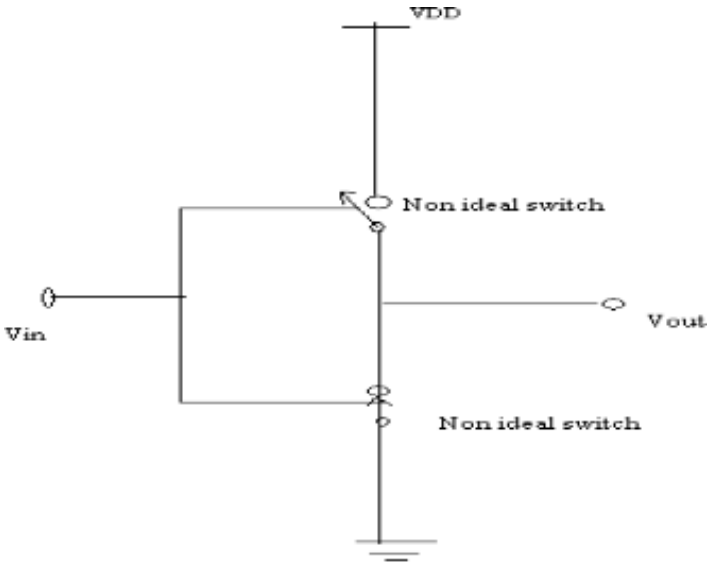

FIG 2.SIMPLIFIED VIEW OF CMOS

CONCLUSION: