VHDL CODE:

```
Library IEEE;
Use ieee.std_logic_1164.all;
entity HA is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           sum : out  STD_LOGIC;
           carry : out  STD_LOGIC);
end HA;
architecture Structural of HA is
component XOR22
port(X,Y:in std_logic;
     z:out std_logic);
 end component;
component AND22
port(P,Q:in std_logic;
     R:out std_logic);
 end component;
begin
X1:XOR22 port map (A,B,sum);
X2:AND22 port map (A,B,carry);
end Structural;
```