Experiment No. 7

Title: To prepare CMOS layout for NAND, NOR gates. Simulate with and without capacitive load, comment on rise and fall time

PROBLEM STATEMENT:

To prepare CMOS layout for NAND and NOR gate with and without capacitive load, comment on rise and fall time.

OBJECTIVE:

1. To manually design the mask layout of NAND, NOR gates
2. To check the design for design rule errors.
3. To check the functionality using simulation with the built-insimulator.
4. Measure propagation delay

THEORY:

MICROWIND program allows to design and simulate an integrated circuit. The package itself contains a library of common logic and analog ICs to view and simulate. MICROWIND includes all the commands for a mask editor as well as new original tools never gathered before in a single module. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

A specific command displays the characteristics of pMOS and nMOS, where the size of the device and the process parameters can be very easily changed. Altering the MOS model parameters and, then, seeing the effects on the Vds and Ids curves constitutes a good interactive tutorial on devices.

The MOS device

The MOS symbols are reported below. The n-channel MOS is built using polysilicon as the gate material and N+ diffusion to build the source and drain. The p-channel MOS is built using polysilicon as the gate material and P+ diffusion to build the source and drain.

NAND and NOR Theory:

A two-input NAND gate ($F = A \cdot B$). The PDN network consists of two NMOS devices in series that conduct when both A and B are high. The PUN is the dual network, and consists of two parallel PMOS transistors. This means that F is 1 if $A = 0$ or $B = 0$, which is equivalent to $F = A \cdot B$. The truth table for the simple two input NAND gate is given in Table 1. It can be verified that the output F is always connected to either VDD or GND, but never to both at the same time.

Table no 1: Operating regions of CMOS Inverter

REGION	Vin	Vout	NMOS	PMOS
A	<VTO,n	VoH	Cut-off	linear
B	ViL	High~VoH	saturation	linear
C	VtH	VtH	saturation	saturation
D	ViH	Low~VoL	linear	saturation
E	>(VDD+VTo,p)	VoL	linear	Cut-off

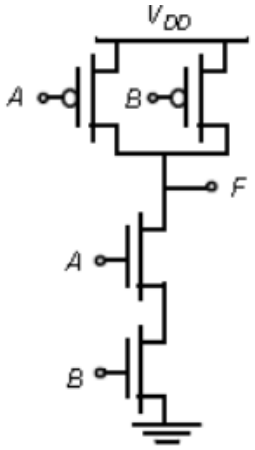
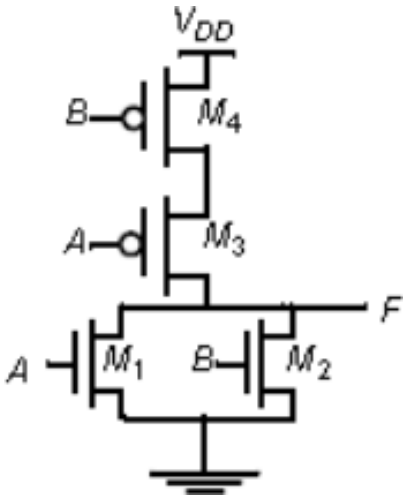


Fig 1: Two-input NAND gate in complementary static CMOS style.

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: Truth Table for 2 input NAND

The first step in the synthesis of the logic gate is to derive the pull-down network. The fact is that NMOS devices in series implements the AND function and parallel device implements the OR function. The next step is to use duality to derive the PUN in a hierarchical fashion. The PDN network is broken into smaller networks (i.e., subset of the PDN) called sub-nets that simplify the derivation of the PUN.



Design Consideration: The important point to take away from is that the noise margins are input pattern dependent. A smaller input glitch will cause a transition at the output if only one of the inputs does not represent the worst-case static behavior. The data dependencies should be carefully modeled.

The output of this NOR network is high, if and only if both inputs A and B are low. The worst-case pull-down transition happens when only one of the NMOS devices turns on (i.e., if either A or B is high). Since the pull-down path in the worst case is a single device, the NMOS devices (M1and M2) can have the same device widths as the NMOS device in the inverter. For the output to be pulled high, both devices must be turned on. Since the resistances add, the devices must be made twotimes larger compared to the PMOS in the inverter. Since PMOS devices have a lower mobility relative to NMOS devices, stacking devices in series must be avoided as much as possible. A NAND implementation is clearly preferred over a NOR implementation for implementing generic logic

PLATFORM USED:

1. Microwind

CONCLUSION: