Experiment 9

Aim: Write a Verilog code to implement shift register and verify the functionality using test bench.

Theory:

A shift register is a digital circuit that stores and shifts data serially. It is commonly used for applications like data storage, data manipulation, and serial data transmission. A shift register is a sequential digital circuit that stores data in a linear fashion, and the data can be shifted in or out one bit at a time. It typically consists of flip-flops connected in series. There are two main types of shift registers: serial-in, serial-out (SISO) and serial-in, parallel-out (SIPO).

Serial-In, Serial-Out (SISO) Shift Register: In a Serial-In, Serial-Out (SISO) shift register, data is entered serially (one bit at a time) at one end, and it is shifted through the register until it reaches the other end. This type of shift register is often used for applications like delay lines and time-domain signal processing.

Serial-In, Parallel-Out (SIPO) Shift Register: In a Serial-In, Parallel-Out (SIPO) shift register, data is entered serially but can be read out in parallel. It's often used for applications like data conversion and interfacing serial data to parallel data.

Parallel-In, Serial-Out (PISO) Shift Register: In a Parallel-In, Serial-Out (PISO) shift register, data is entered in parallel and shifted out serially. This type is useful for parallel-to-serial data conversion.

Parallel-In, Parallel-Out (PIPO) Shift Register: A Parallel-In, Parallel-Out (PIPO) shift register allows data to be entered and read out in parallel. It can be used for various parallel data processing tasks.

The behaviour of a shift register is described by its control signals, such as clock (for shifting), clear (for clearing the register), and data inputs (for loading data). Depending on the specific type and configuration of the shift register, data can be shifted left or right, and the number of stages determines how many bits can be stored.

Code:

Behavioural

```
module shift_register_4bit (
   input CLK,
   input SI,
   output SO,
   output [3:0] Q
);

reg SO;
reg [3:0] Q;

always @(posedge CLK) begin
   Q <= {Q[2:0], SI};
```

```
    SO <= Q[0];
end

endmodule
```

Test bench

```
module testbench;

    reg CLK;
    reg SI;
    wire SO;
    wire [3:0] Q;

    shift_register_4bit uut (
        .CLK(CLK),
        .SI(SI),
        .SO(SO),
        .Q(Q)
    );

initial begin
    CLK = 0;
    SI = 0;
    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;
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    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;
    #5 SI = 0;
    #5 SI = 1;

    #5 $finish;
end
```
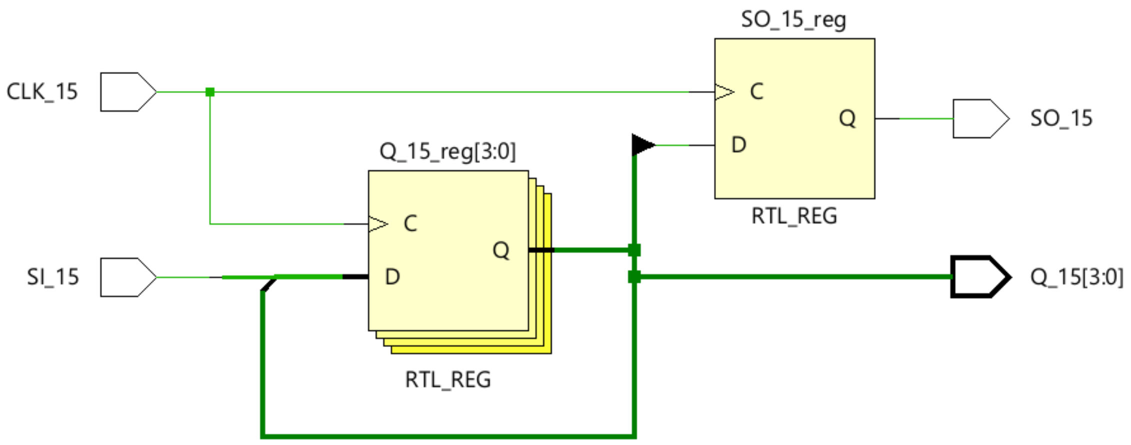
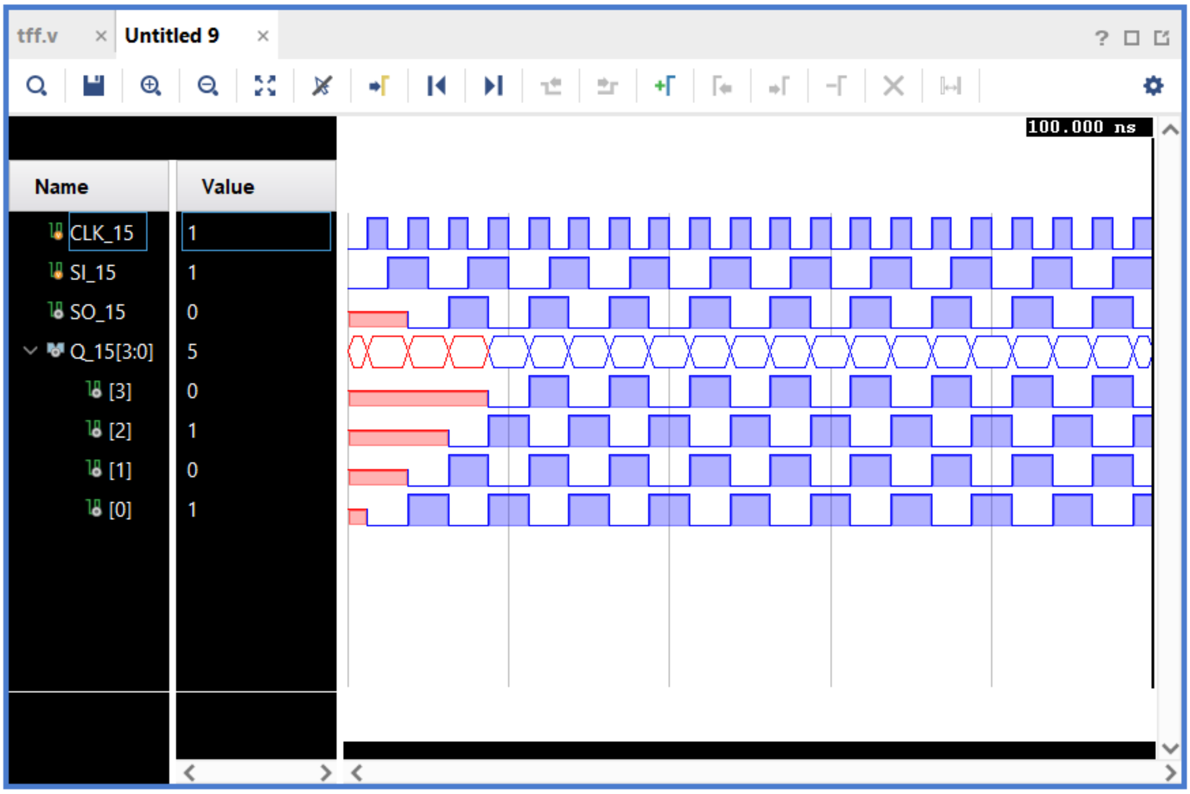

```
always begin
   #2.5 CLK = ~CLK;
end

endmodule
```

RTL Schematic:

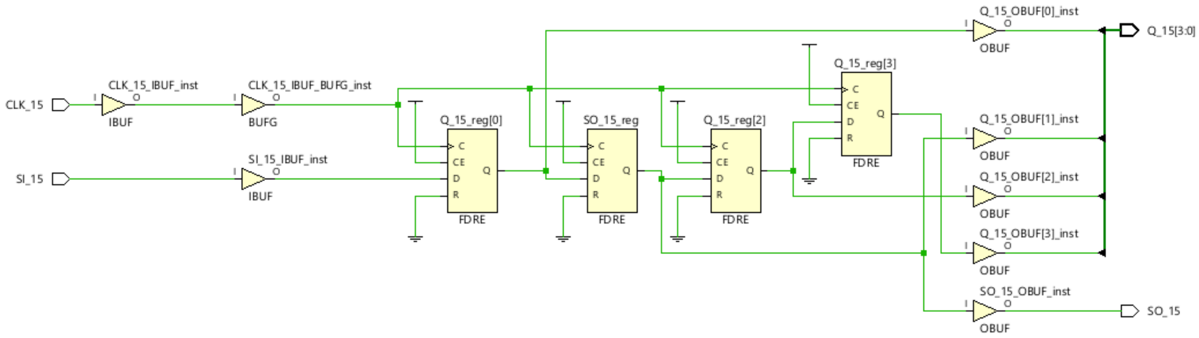


Function Verification:

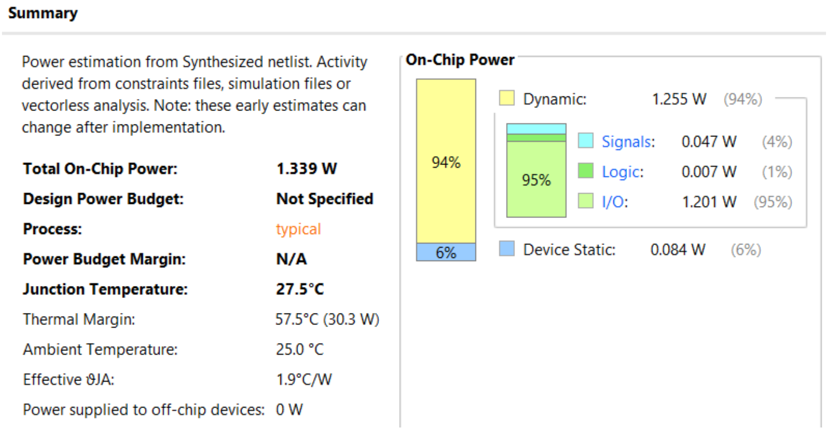


Name	Value
CLK_15	1
SI_15	1
SO_15	0
Q_15[3:0]	5
[3]	0
[2]	1
[1]	0
[0]	1

Post synthesis schematic:



Post power report:



Summary

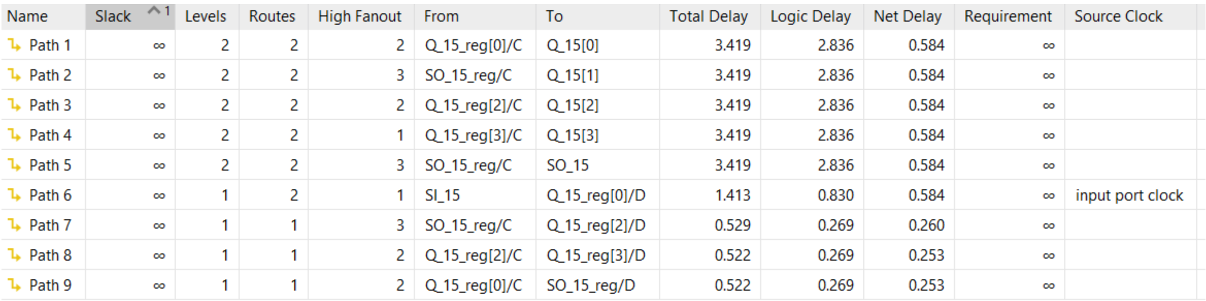
Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.339 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.5°C**
Thermal Margin:	57.5°C (30.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

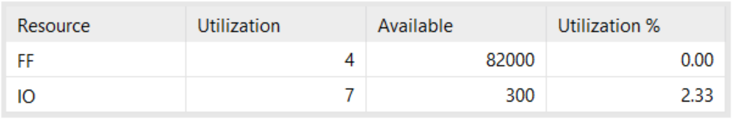
Dynamic:	1.255 W	(94%)
Signals:	0.047 W	(4%)
Logic:	0.007 W	(1%)
I/O:	1.201 W	(95%)
Device Static:	0.084 W	(6%)

Post synthesis timing summary:

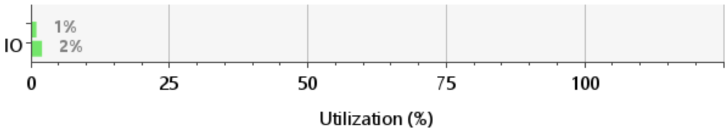


Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	2	Q_15_reg[0]/C	Q_15[0]	3.419	2.836	0.584	∞	
Path 2	∞	2	2	3	SO_15_reg/C	Q_15[1]	3.419	2.836	0.584	∞	
Path 3	∞	2	2	2	Q_15_reg[2]/C	Q_15[2]	3.419	2.836	0.584	∞	
Path 4	∞	2	2	1	Q_15_reg[3]/C	Q_15[3]	3.419	2.836	0.584	∞	
Path 5	∞	2	2	3	SO_15_reg/C	SO_15	3.419	2.836	0.584	∞	
Path 6	∞	1	2	1	SI_15	Q_15_reg[0]/D	1.413	0.830	0.584	∞	input port clock
Path 7	∞	1	1	3	SO_15_reg/C	Q_15_reg[2]/D	0.529	0.269	0.260	∞	
Path 8	∞	1	1	2	Q_15_reg[2]/C	Q_15_reg[3]/D	0.522	0.269	0.253	∞	
Path 9	∞	1	1	2	Q_15_reg[0]/C	SO_15_reg/D	0.522	0.269	0.253	∞	

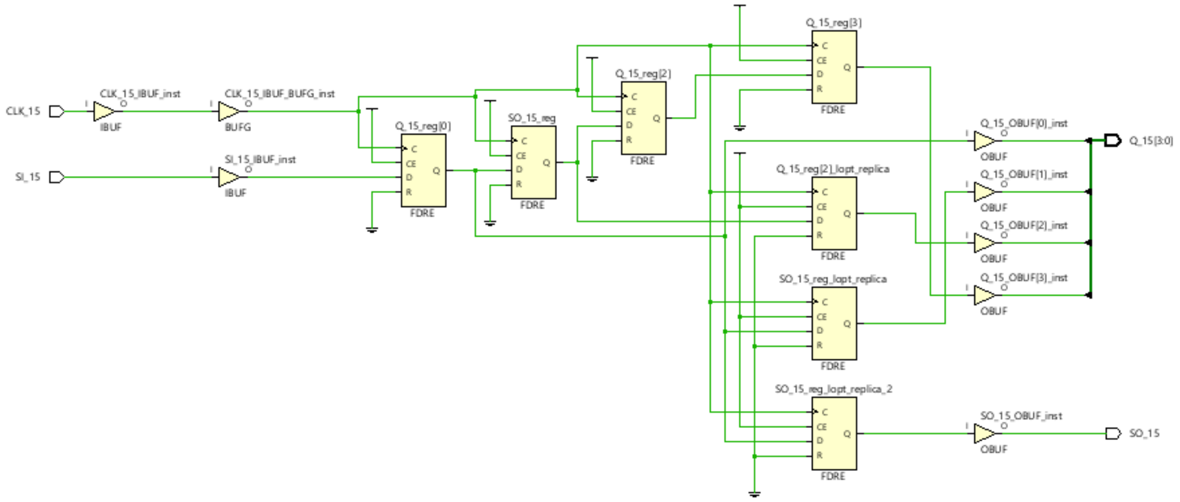
Post utilization/ area summary:



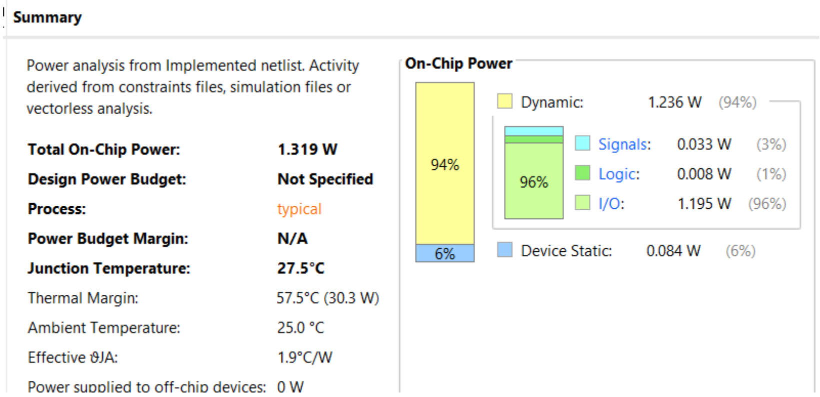
Resource	Utilization	Available	Utilization %
FF	4	82000	0.00
IO	7	300	2.33



Post implementation schematic:



Post implementation power report:



Summary

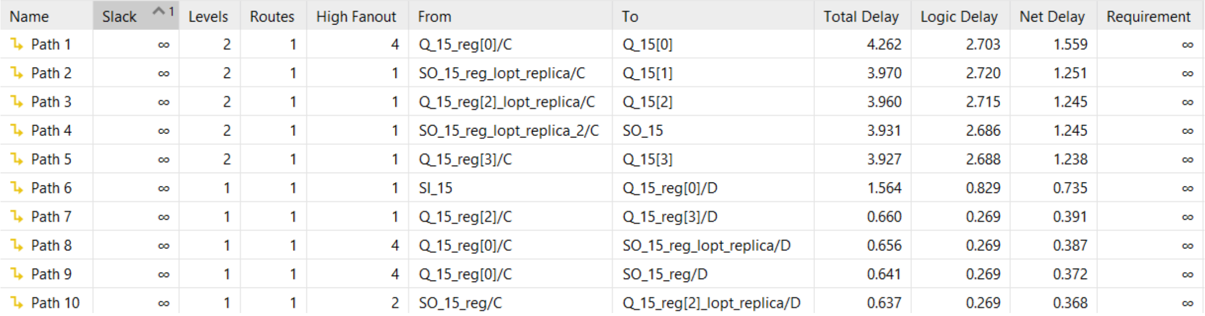
Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.319 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**27.5°C**
Thermal Margin:	57.5°C (30.3 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

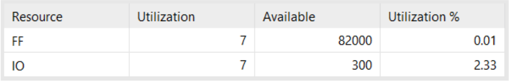
Dynamic:	1.236 W	(94%)
Signals:	0.033 W	(3%)
Logic:	0.008 W	(1%)
I/O:	1.195 W	(96%)
Device Static:	0.084 W	(6%)

Post implementation timing summary:

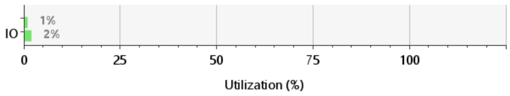


Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	2	1	4	Q_15_reg[0]/C	Q_15[0]	4.262	2.703	1.559	∞
Path 2	∞	2	1	1	SO_15_reg_lopt_replica/C	Q_15[1]	3.970	2.720	1.251	∞
Path 3	∞	2	1	1	Q_15_reg[2]_lopt_replica/C	Q_15[2]	3.960	2.715	1.245	∞
Path 4	∞	2	1	1	SO_15_reg_lopt_replica_2/C	SO_15	3.931	2.686	1.245	∞
Path 5	∞	2	1	1	Q_15_reg[3]/C	Q_15[3]	3.927	2.688	1.238	∞
Path 6	∞	1	1	1	SI_15	Q_15_reg[0]/D	1.564	0.829	0.735	∞
Path 7	∞	1	1	1	Q_15_reg[2]/C	Q_15_reg[3]/D	0.660	0.269	0.391	∞
Path 8	∞	1	1	4	Q_15_reg[0]/C	SO_15_reg_lopt_replica/D	0.656	0.269	0.387	∞
Path 9	∞	1	1	4	Q_15_reg[0]/C	SO_15_reg/D	0.641	0.269	0.372	∞
Path 10	∞	1	1	2	SO_15_reg/C	Q_15_reg[2]_lopt_replica/D	0.637	0.269	0.368	∞

Post implementation utilization/ area summary:



Resource	Utilization	Available	Utilization %
FF	7	82000	0.01
IO	7	300	2.33



Conclusion:

- In this experiment, we written Verilog code for a circuit of SISO shift register and verified its output and Schematic using its test bench and we got desired output.