DATE: 11/08/2023

Experiment 2

Aim:

a) Write Verilog codes for implementing **half-adder** having structural, data flow and behavioural model and perform synthesis by generating different synthesis and timing waveforms.
b) Write Verilog codes for implementing **full-adder using half-adder** having structural, data flow and behavioural model and perform synthesis by generating different synthesis and timing waveforms.

Theory:

Half Adder:

A half adder is a digital circuit that performs binary addition of two inputs (A and B), generating a sum (S) and a carry (Cout).

A	B	Sum (S)	Carry (Cout)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder:

A full adder is a digital circuit that performs binary addition of three inputs (A, B, and Cin), generating a sum (S) and a carry out (Cout).

Truth Table:

A	B	Cin	Sum (S)	Carry Out (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Code for Half-adder:

1) Structural

```
module halfAdder_s(
   input a, b,
   output c, s
   );
   and(c,a,b);
   xor(s,a,b);
endmodule
```

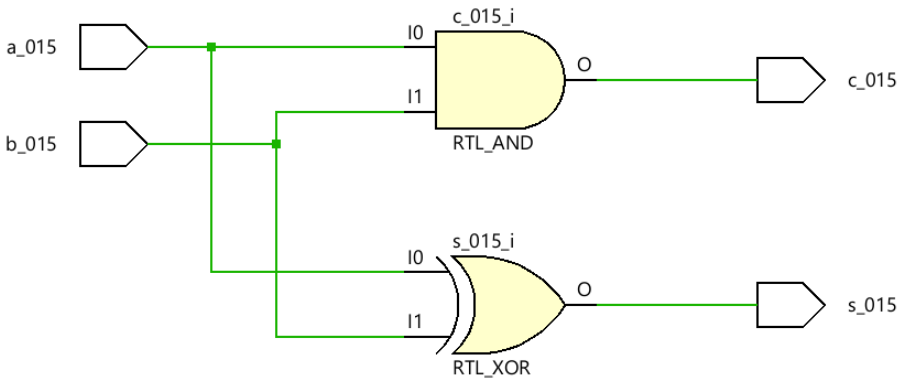
2) Data Flow

```
module halfAdder_d(
   input a, b,
   output c, s
   );
   assign c = a & b;
   assign s = a^b;
endmodule
```

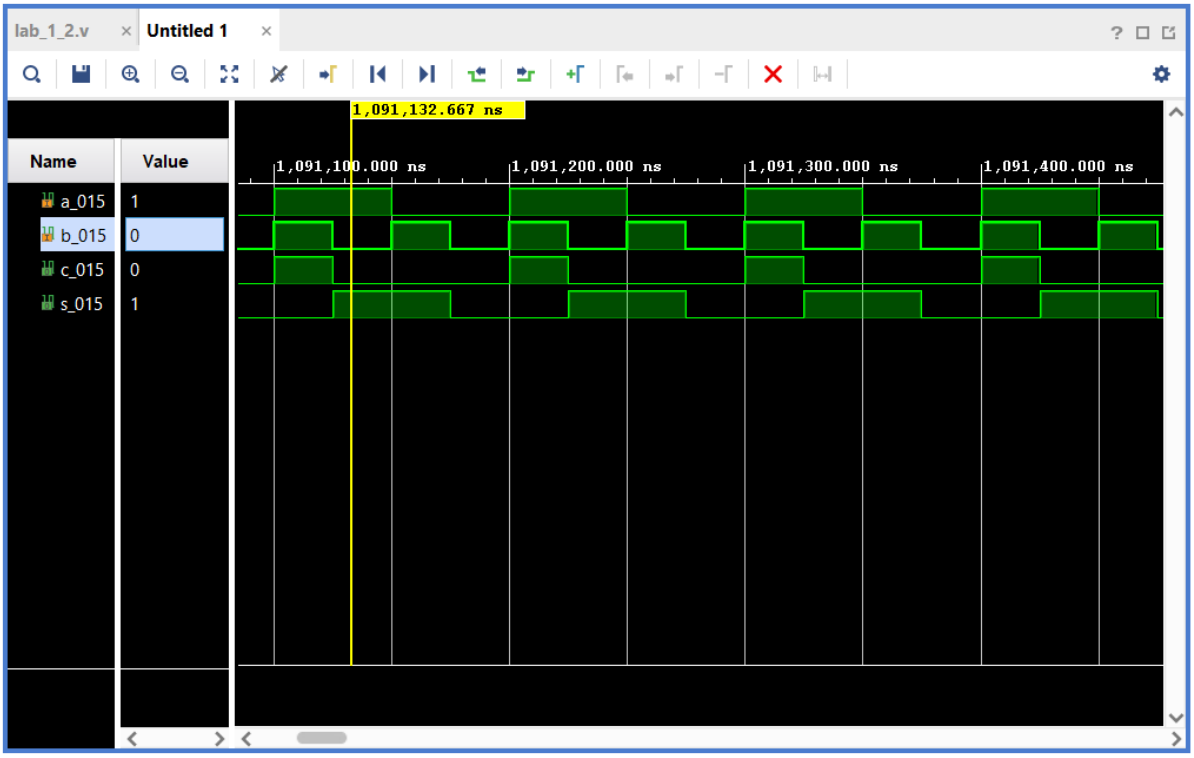
3) Behavioural

```
module halfAdder_b(
   input a, b,
   output reg c, s
   );
   always @(a, b)
   begin
   c = a & b;
   s = a ^ b;
   end
endmodule
```

RTL Schematic:



Function Verification:

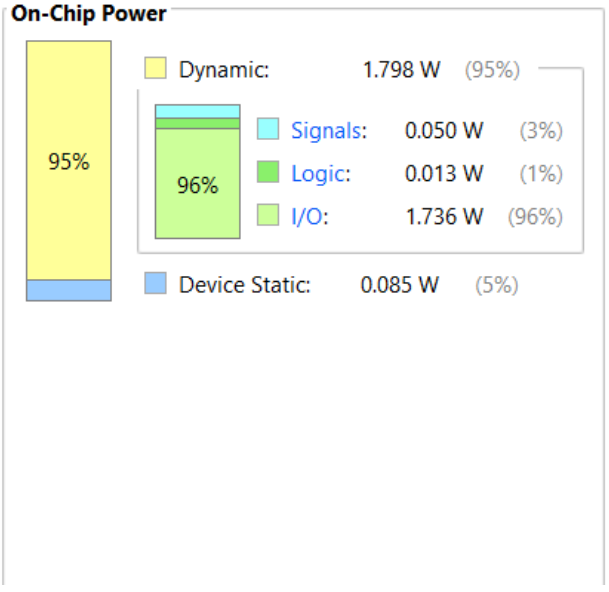


Post power report:

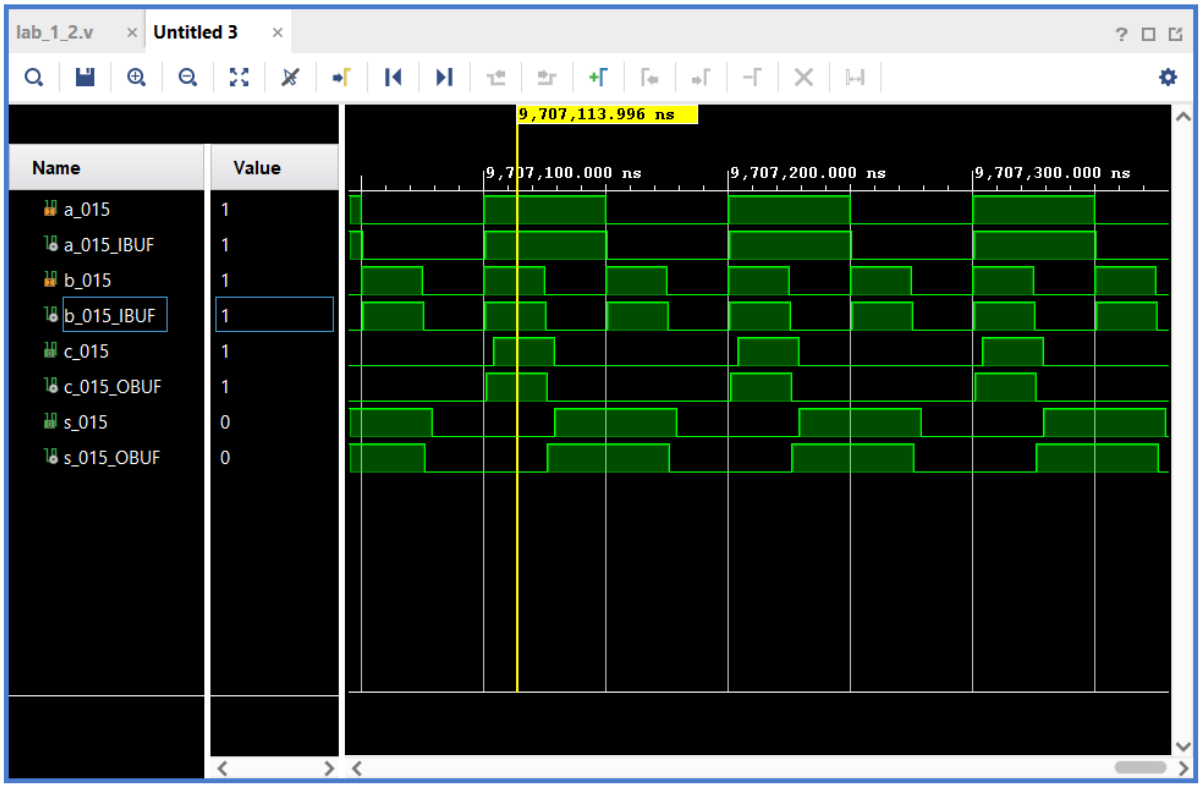
Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

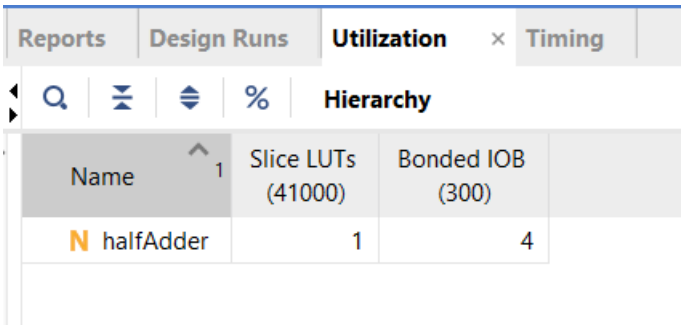
Total On-Chip Power:	**1.883 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.5°C**
Thermal Margin:	56.5°C (29.8 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



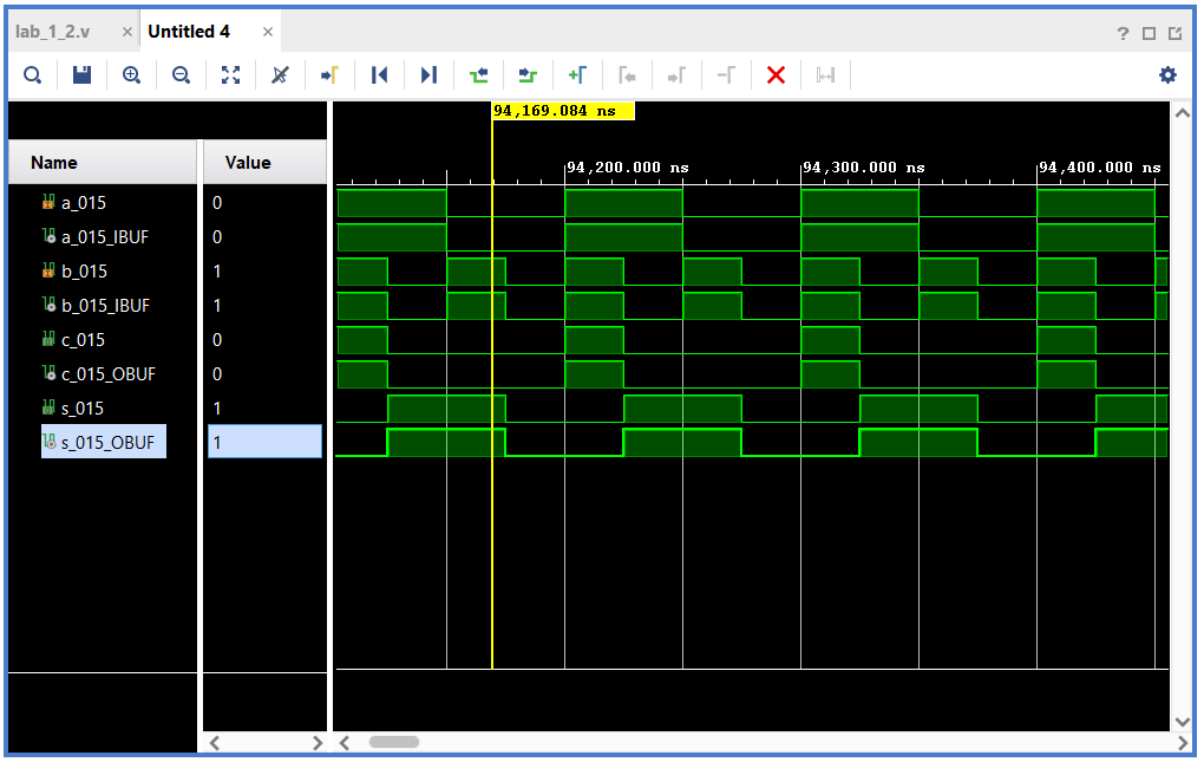
Post synthesis timing summary:



Post utilization/ area summary:



Post implementation schematic:



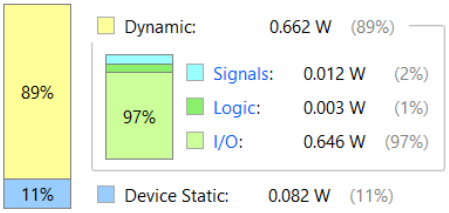
Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.744 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.4°C**
Thermal Margin:	58.6°C (30.9 W)
Ambient Temperature:	25.0 °C
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

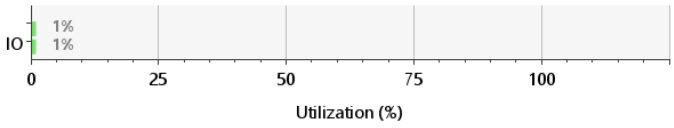
On-Chip Power



Post implementation utilization/ area summary:

Summary

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
IO	4	300	1.33



Code for Full adder using Half-adder:

1) Structural

```
module halfadder_s(
   input a, b,
   output c, s
   );
   and(c,a,b);
   xor(s,a,b);
endmodule

module full_half_s(
   input a, b, c,
   output sum, carry
   );
   wire w1, w2, w3;
   halfadder h1(.a(a), .b(b), .c(w2), .s(w1));
   halfadder h2(.a(w1), .b(c), .c(w3), .s(sum));
   or(carry, w2, w3);
endmodule
```

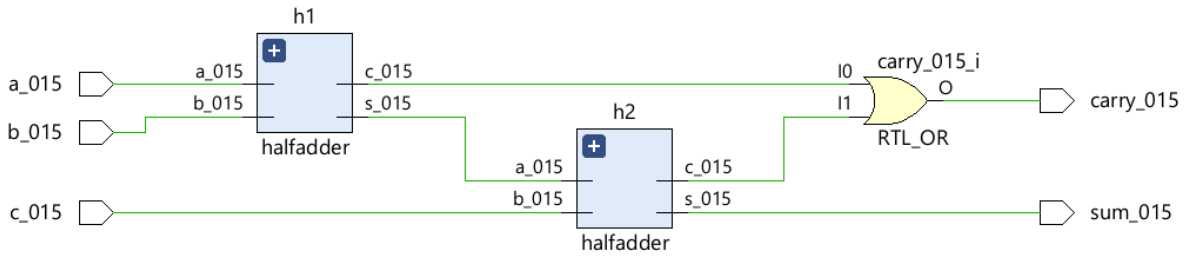
2) Data Flow

```
module halfadder_d(
   input a, b,
   output c, s
   );
   assign {c, s} = a + b;
endmodule

module full_half_d(
   input a, b, c,
   output sum, carry
   );
   wire w1, w2, w3;
   halfadder h1(.a(a), .b(b), .c(w2), .s(w1));
   halfadder h2(.a(w1), .b(c), .c(w3), .s(sum));
   or(carry, w2, w3);
endmodule
```

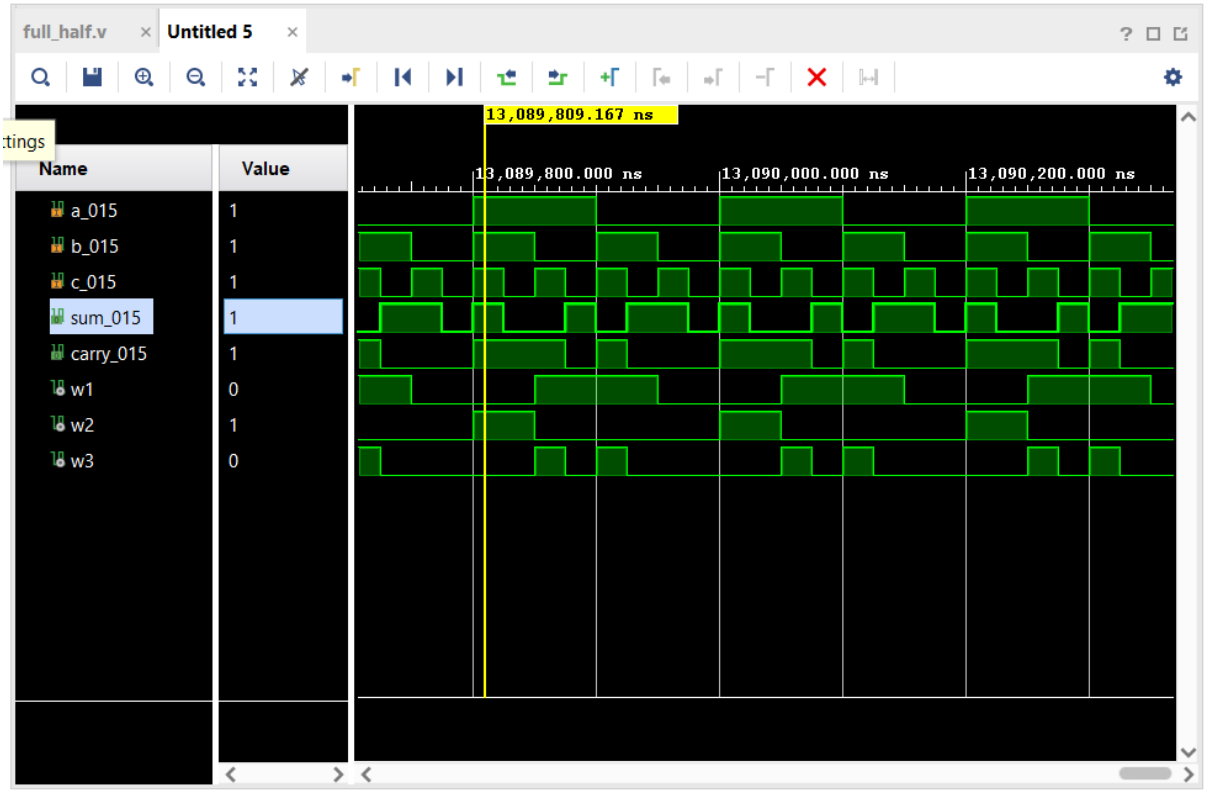
3) Behavioural

```
module halfadder_b(
    input a, b,
    output reg c, s
    );
    always @(a, b)
    begin
    c = a & b;
    s = a ^ b;
    end
endmodule

module full_half_b(
    input a, b, c,
    output sum, carry
    );
    wire w1, w2, w3;
    halfadder h1(.a(a), .b(b), .c(w2), .s(w1));
    halfadder h2(.a(w1), .b(c), .c(w3), .s(sum));
    or(carry, w2, w3);
endmodule
```

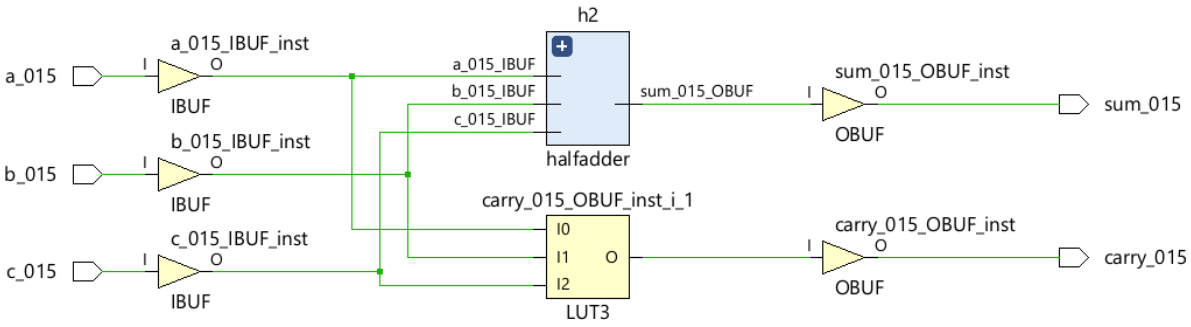
RTL Schematic:



Function Verification:



Post synthesis schematic:

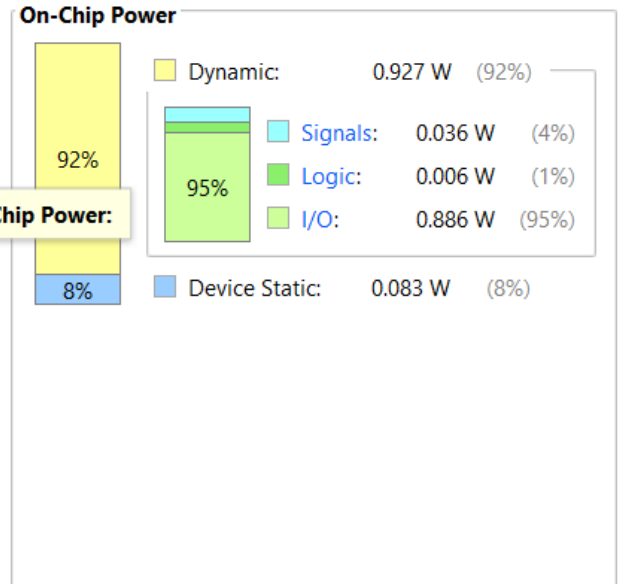


Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.01 W**
Design Power Budget:	**Not**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (30.7 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



Post synthesis timing summary:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	4	2	c_015	carry_015	4.512	3.345	1.167	∞	input port clock
Path 2	∞	3	4	2	c_015	sum_015	4.512	3.345	1.167	∞	input port clock

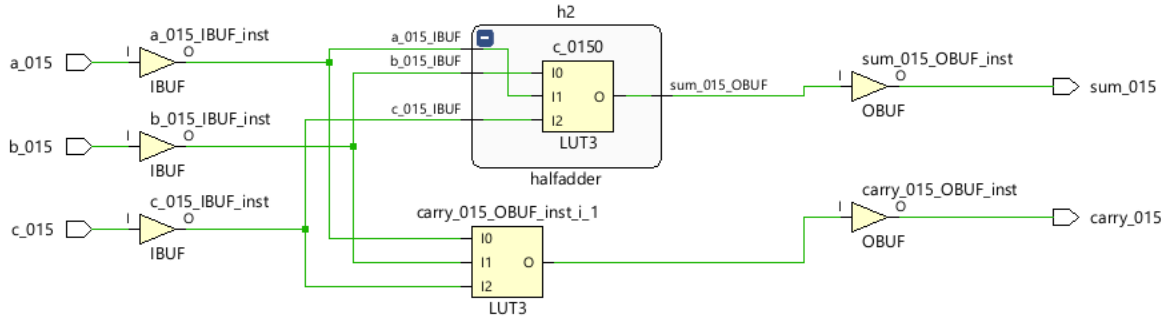
Post utilization/ area summary:

Reports | Design Runs | Timing | Power | **Utilization**

Hierarchy

Name	Slice LUTs (41000)	Bonded IOB (300)
N full_half	2	5
h2 (halfadder)	1	0

Post implementation schematic:

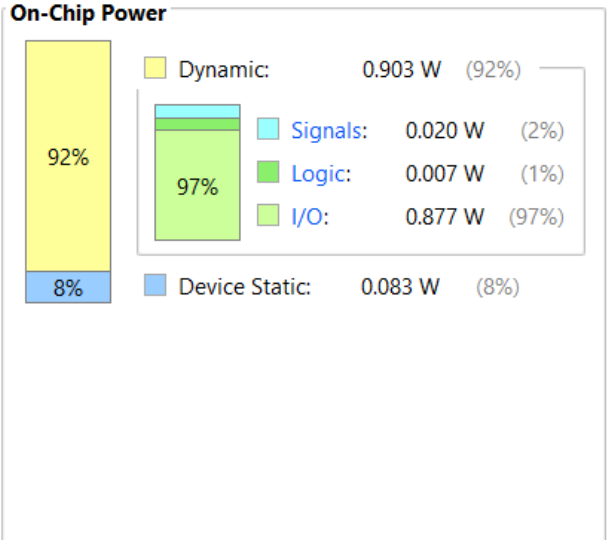


Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.986 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (30.7 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low



Post implementation timing summary:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	2	a_015	sum_015	5.625	3.272	2.353	∞	input port clock
Path 2	∞	3	2	2	a_015	carry_015	5.622	3.274	2.348	∞	input port clock

Post implementation utilization/ area summary:

Reports | Design Runs | DRC | Power | Timing | **Utilization**

Hierarchy

Name	Slice LUTs (41000)	Slice (10250)	LUT as Logic (41000)	Bonded IOB (300)
full_half	2	1	2	5
h2 (halfadder)	1	1	1	0