Experiment 5

Aim:

- Design a circuit which works as a half subtractor when select line is 1 and a Half adder when select line is 0.
- Design a circuit which works as a full subtractor when select line is 1 and a full adder when select line is 0.

Theory:

Half Subtracter and Half Adder Circuit:

A half subtractor subtracts two binary bits (A and B) and produces two outputs: a difference (D) and a borrow (B_out). A half adder adds two binary bits and produces a sum (S) and a carry (C_out).

To create a circuit that functions as a half subtractor when the select line is 1 and a half adder when the select line is 0, you can use multiplexers (MUX). Here's the circuit theory:

When the select line is 1, pass inputs A and B through the half subtractor.

When the select line is 0, pass inputs A and B through the half adder.

Truth Tables:

For the half subtractor:

A	B	D	B_out
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

For the half adder:

A	B	S	C_out
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Subtracter and Full Adder Circuit:

A full subtractor subtracts three binary bits (A, B, and Bin) and produces two outputs: a difference (D) and a borrow (B_out). A full adder adds three binary bits (A, B, and Cin) and produces two outputs: a sum (S) and a carry (C_out).

To create a circuit that functions as a full subtractor when the select line is 1 and a full adder when the select line is 0, you can use multiplexers (MUX). Here's the circuit theory:

When the select line is 1, pass inputs A, B, and Bin through the full subtractor.

When the select line is 0, pass inputs A, B, and Cin through the full adder.

Truth Tables:

For the full subtractor:

A	B	Bin	D	B_out
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

For the full adder:

A	B	Cin	S	C_out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

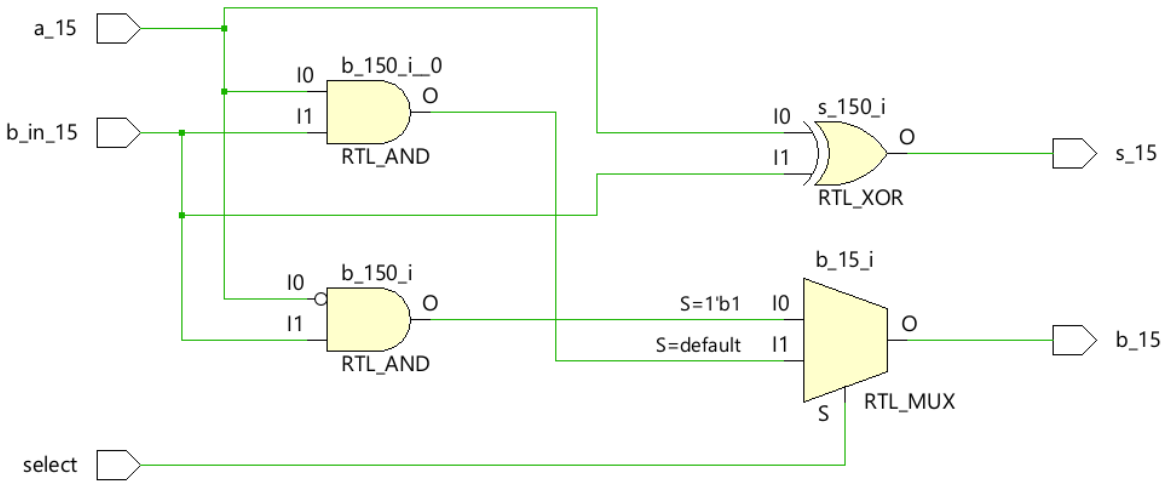
Code for Half_Adder_Subtractor:

Behavioural

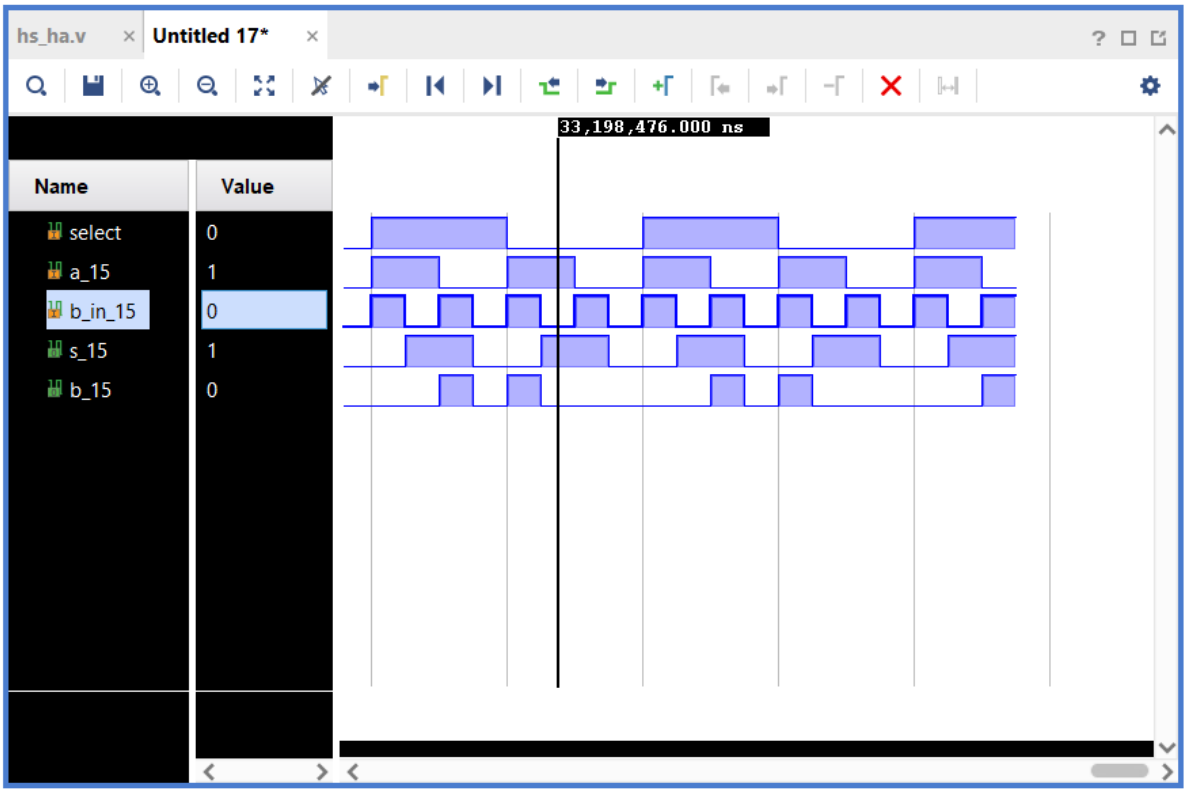
```
module Half_Adder_Subtractor (
   output reg s, // Sum
   output reg b, // Borrow or Difference
   input a,      // Operand A
   input b_in,   // Operand B or Borrow-in
   input select  // Select line (1 for subtraction, 0 for addition)
);

always@(a, b_in, select)
begin
   if (select == 1'b1) // Subtraction
   begin
      s= a ^ b_in; // Difference
      b = ~a & b_in;
   end
```

```
    else // Addition
    begin
        s= a ^ b_in; // Sum
        b = a & b_in; // Carry
    end
end

endmodule
```

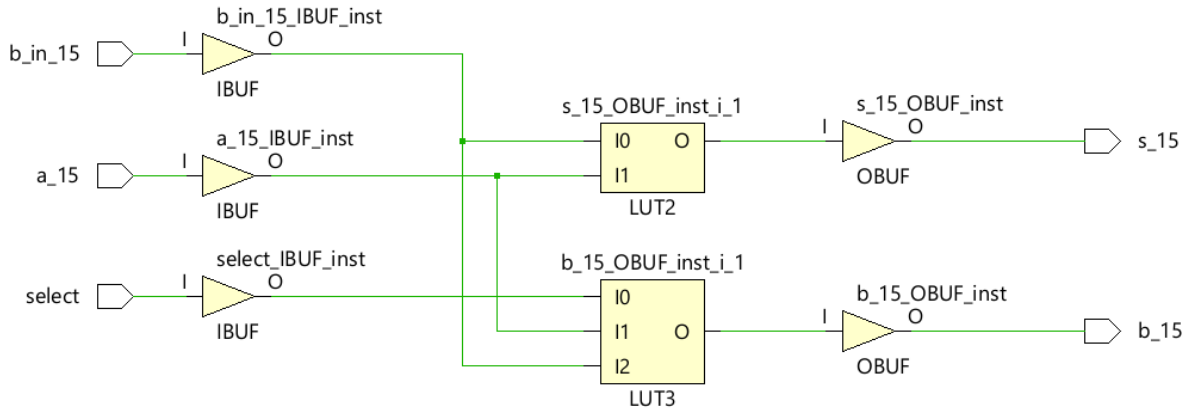
RTL Schematic:



Function Verification:



Post synthesis schematic:



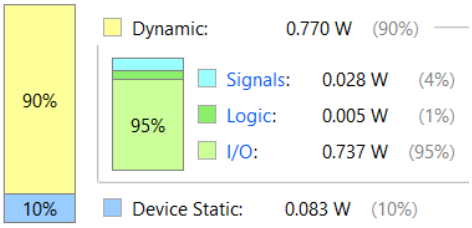
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.853 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.6°C**
Thermal Margin:	58.4°C (30.8 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power



Post synthesis timing summary:

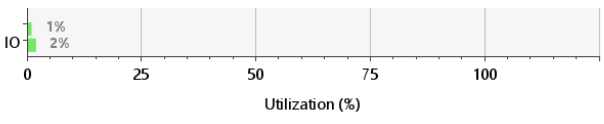
Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	4	2	b_in_15	s_15	4.524	3.357	1.167	∞	input port clock
Path 2	∞	3	4	2	b_in_15	b_15	4.512	3.345	1.167	∞	input port clock

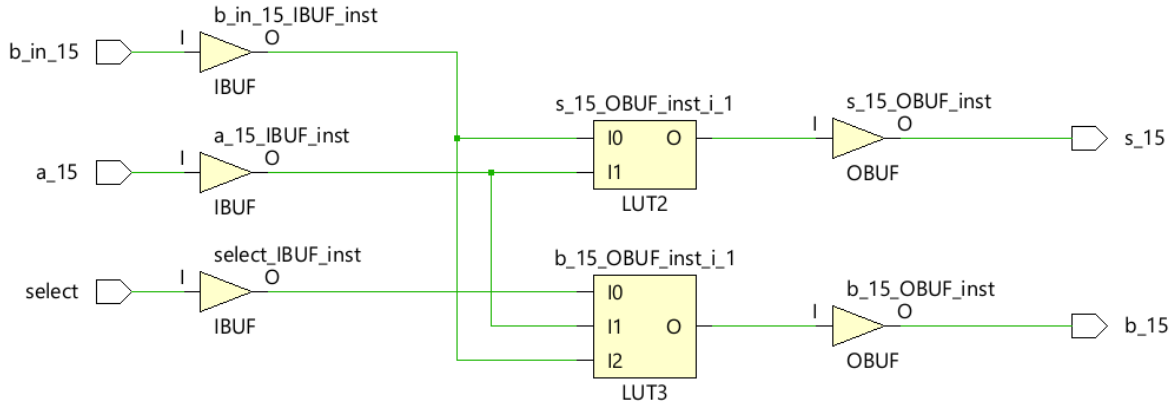
Post utilization/ area summary:

Summary

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
IO	5	300	1.67



Post implementation schematic:



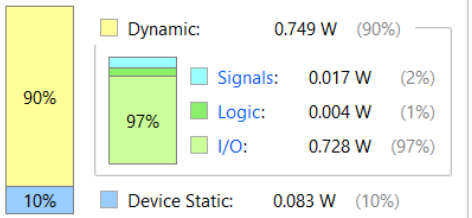
Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.832 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.6°C**
Thermal Margin:	58.4°C (30.8 W)
Ambient Temperature:	25.0 °C
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

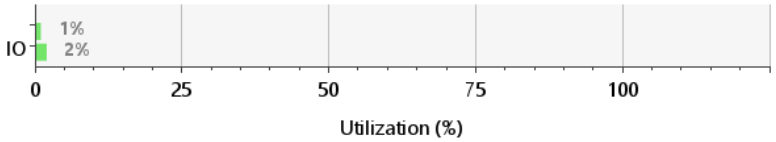


Post implementation timing summary:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	2	b_in_15	b_15	5.602	3.420	2.182	∞	input port clock
Path 2	∞	3	2	2	b_in_15	s_15	5.462	3.289	2.173	∞	input port clock

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
IO	5	300	1.67

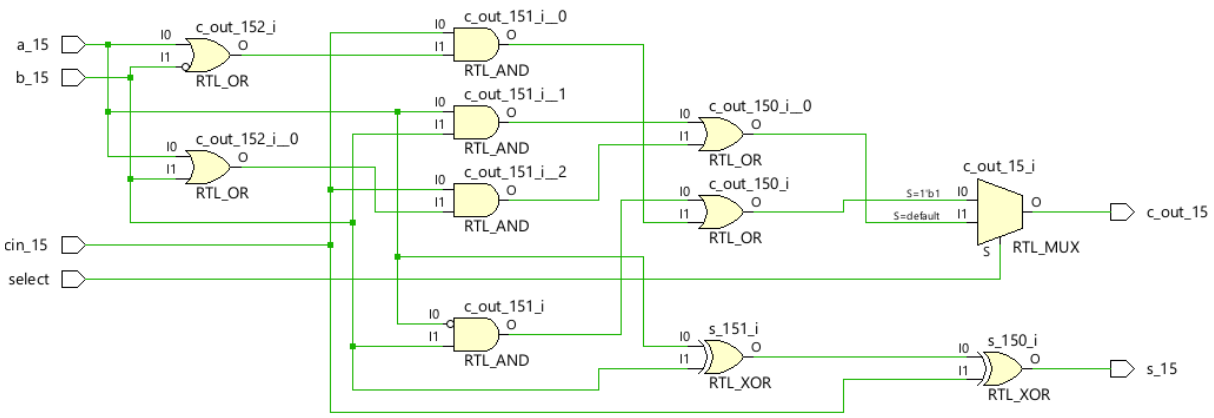


Code for Full_Adder_Subtractor:

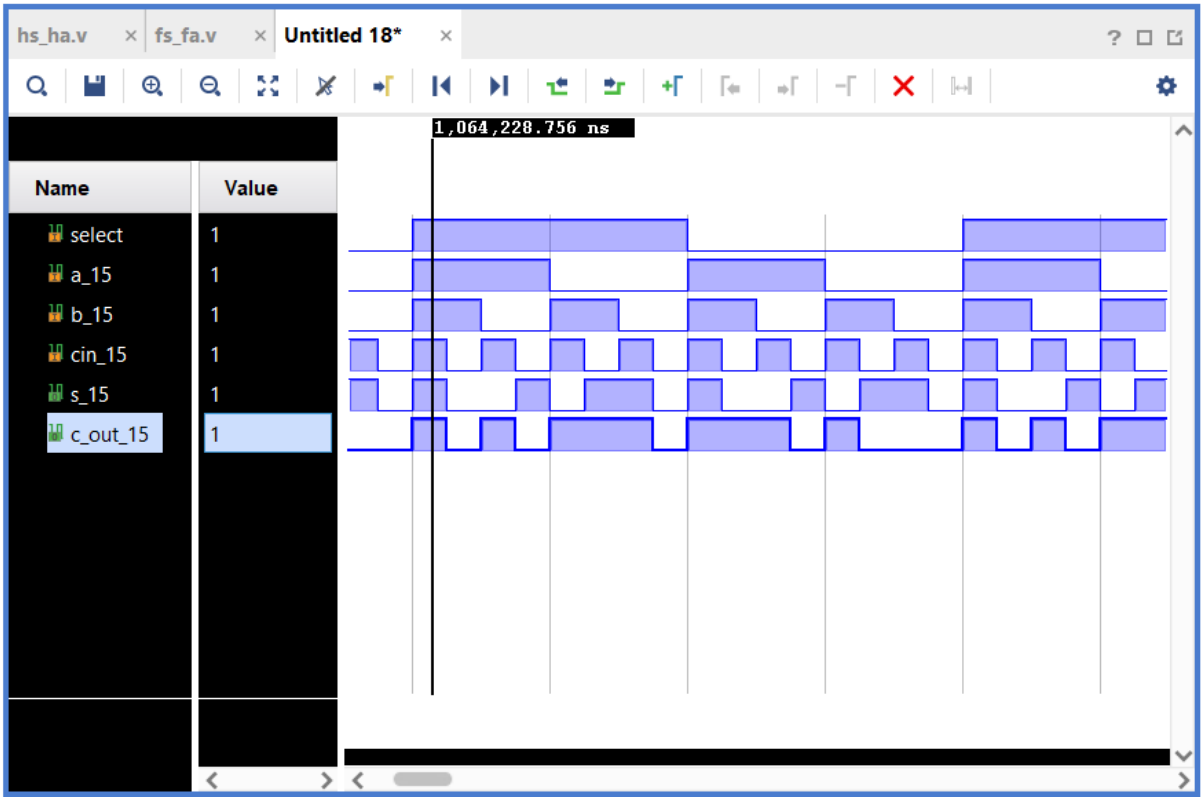
Behavioural

```
module Full_Adder_Subtractor (
    output reg s, // Sum
    output reg c_out, // Carry-out or Borrow-out
    input a,      // Operand A
    input b,      // Operand B
    input cin,    // Carry-in or Borrow-in
    input select  // Select line (1 for subtraction, 0 for addition)
);

always @(a, b, cin, select)
begin
    if (select == 1'b1) // Subtraction
    begin
        s = a ^ b ^ cin; // Difference
        c_out = (~a & b) | (cin & (a | ~b));
    end
    else // Addition
    begin
        s = a ^ b ^ cin; // Sum
        c_out = (a & b) | (cin & (a | b));
    end
end

endmodule
```

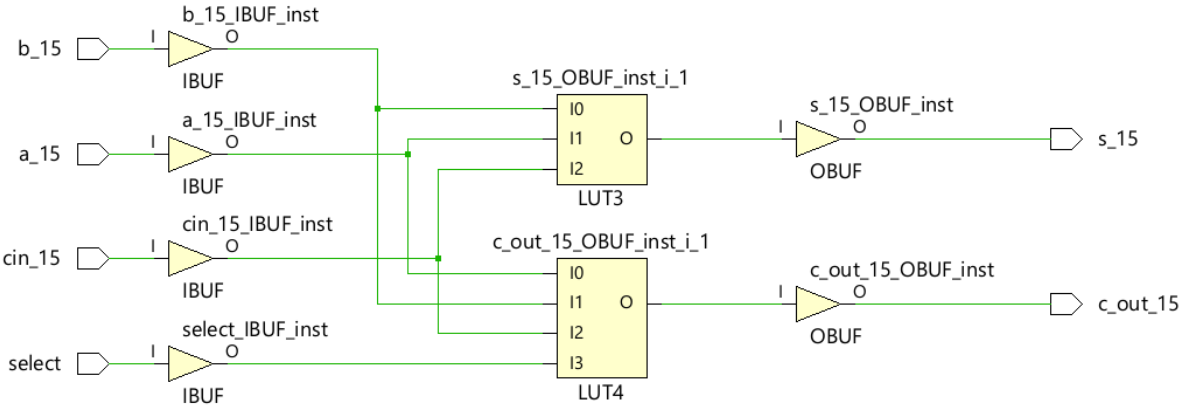
RTL Schematic:



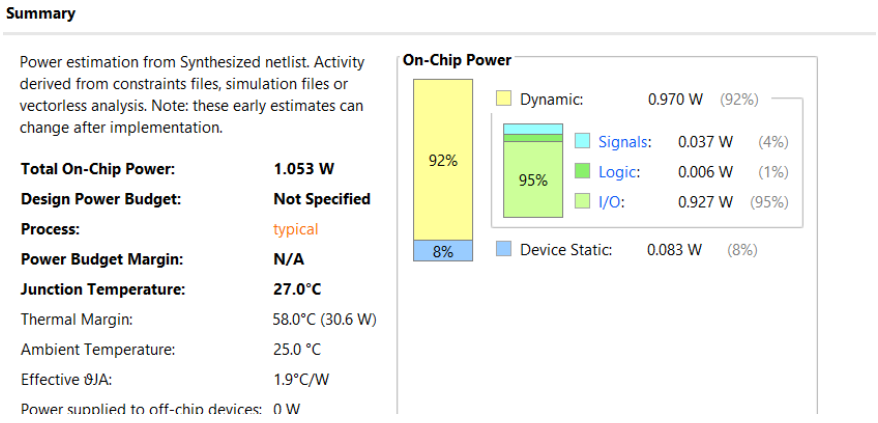
Function Verification:



Post synthesis schematic:



Post power report:

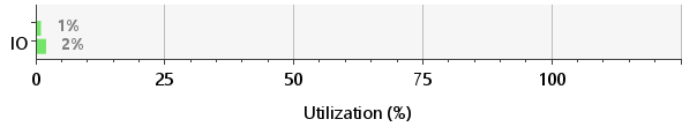


Post synthesis timing summary:

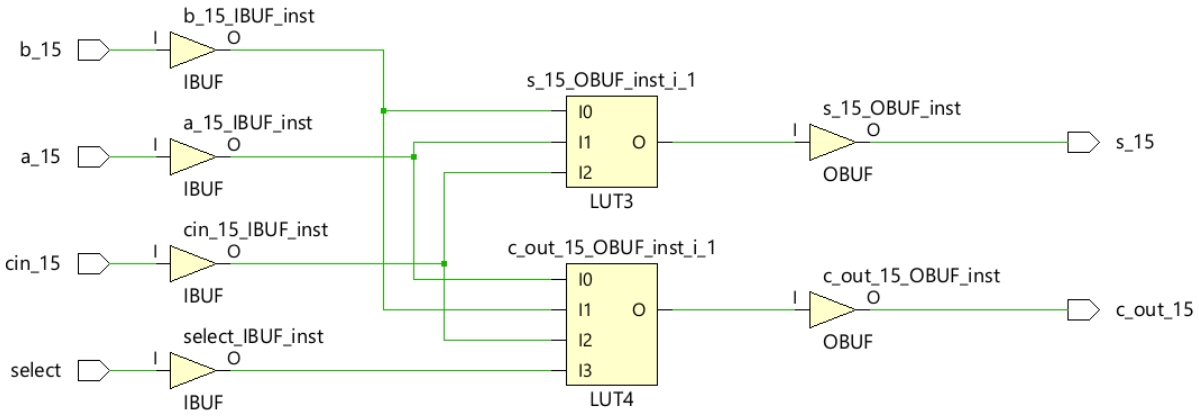
Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	4	2	b_15	s_15	4.526	3.359	1.167	∞	input port clock
Path 2	∞	3	4	1	select	c_out_15	4.512	3.345	1.167	∞	input port clock

Post utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
IO	6	300	2.00



Post implementation schematic:

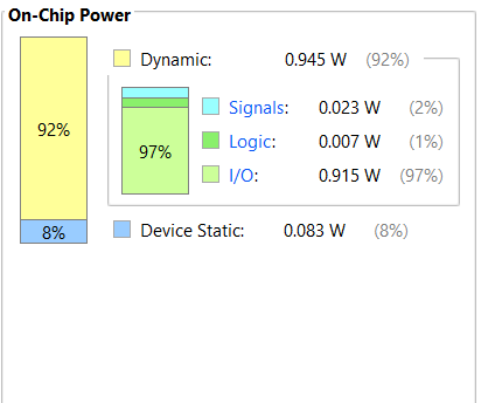


Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.028 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.9°C**
Thermal Margin:	58.1°C (30.6 W)
Ambient Temperature:	25.0 °C
Effective θJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

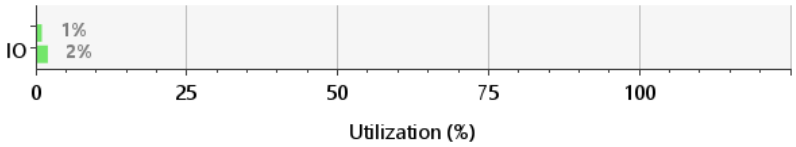


Post implementation timing summary:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	2	a_15	c_out_15	5.836	3.399	2.437	∞	input port clock
Path 2	∞	3	2	2	a_15	s_15	5.700	3.315	2.384	∞	input port clock

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
IO	6	300	2.00



Conclusion:

- In this experiment, we written Verilog code for a circuit which works as a half subtractor when select line is 1 and a Half adder when select line is 0.
- We have also design a circuit which works as a full subtractor when select line is 1 and a full adder when select line is 0 and verified its output and Schematic.