Experiment 8

Aim: Write a Verilog code to implement 8 bit ring oscillator and verify the functionality using test bench.

Theory:

A ring oscillator consists of an odd number of inverter stages connected in a closed loop. The output of each inverter is connected to the input of the next inverter in the ring. The simplest configuration is a 3-stage ring oscillator, but for an 8-bit ring oscillator, we would use 8 inverters.

Here's how it works:

1. When we apply a logic high (1) at the input of the first inverter, it will produce a logic low (0) at its output.
2. This logic low is then inverted by the second inverter, producing a logic high at its output.
3. This process continues through all the stages, with the logic level alternating between high and low as it propagates through the inverters.
4. The output of the last inverter is then fed back to the input of the first inverter, closing the loop.
5. The delay introduced by each inverter stage is what causes the oscillation. The total delay around the loop must be an odd number of inverter delays for sustained oscillation to occur.

Code:

Behavioural for 8 bit ring oscillator

```
module ring_counter_8bit (
   input CLK,
   output [7:0] Q
);

reg [7:0] Q = 8'b10000000;

   always @(posedge CLK) begin
      Q <= {Q[6:0], Q[7]};
   end

endmodule
```

Test bench

```
module testbench;
        reg CLK;
```

```
    wire [7:0] Q;

    ring_counter_8bit uut (
        .CLK(CLK),
        .Q(Q)
    );

initial begin
    CLK = 0;
    #5 CLK = 1;
    #5 CLK = 0;
    #5 CLK = 1;
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    #5 CLK = 0;
    #5 CLK = 1;
    #5 CLK = 0;
    #5 $finish;
end

always begin
    #5 CLK = ~CLK;
end

endmodule
```
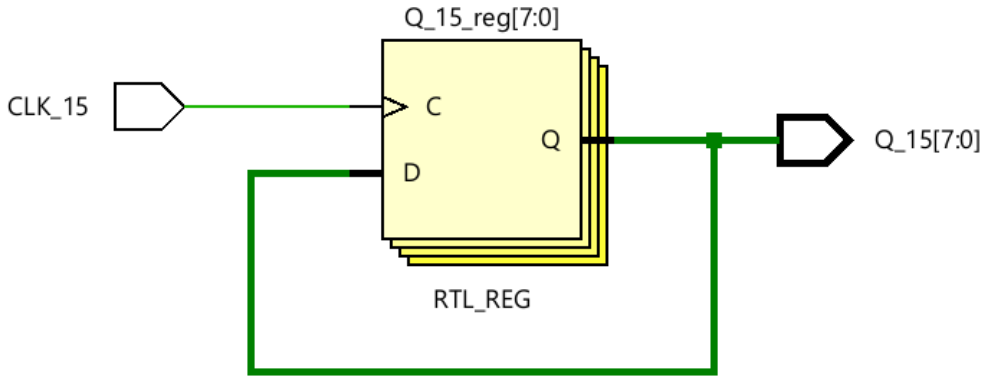
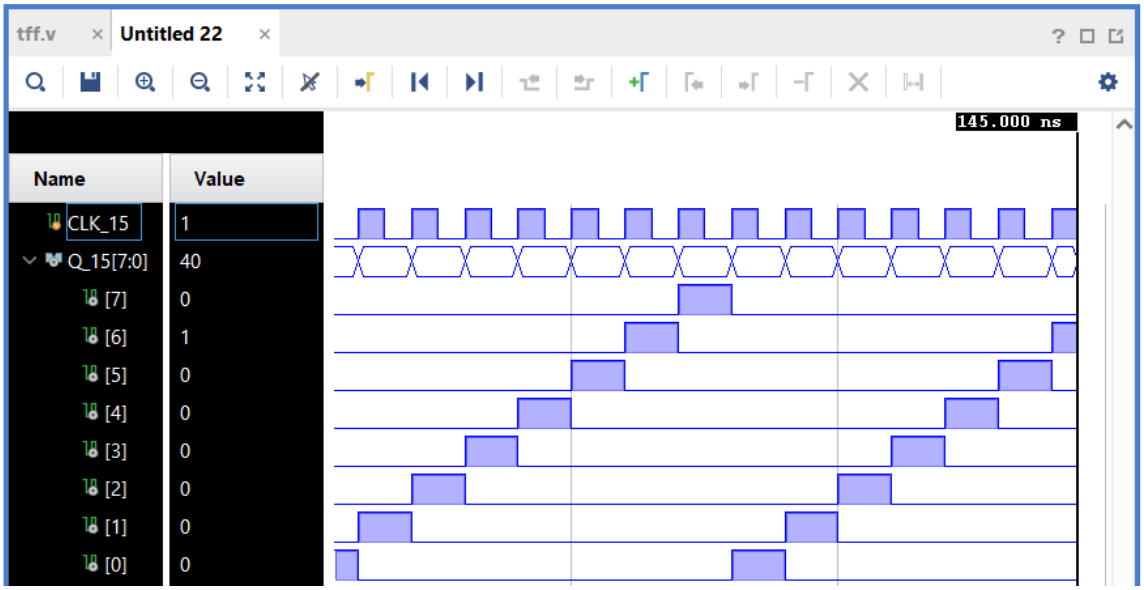
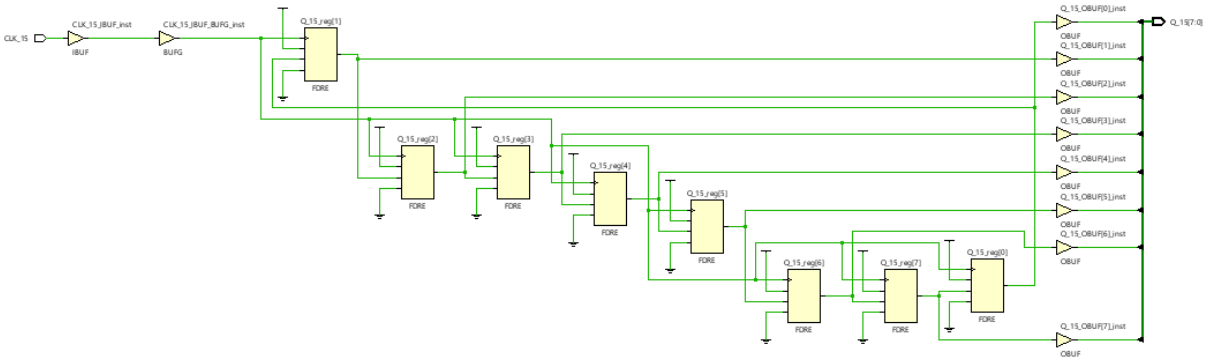

RTL Schematic:



Function Verification:



Post synthesis schematic:



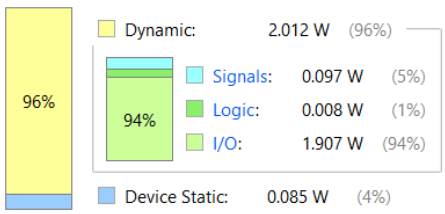
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.097 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.9°C**
Thermal Margin:	56.1°C (29.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

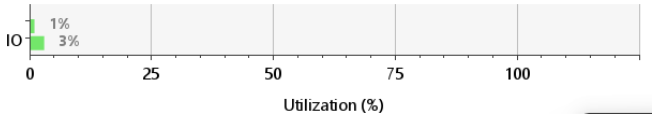


Post synthesis timing summary:

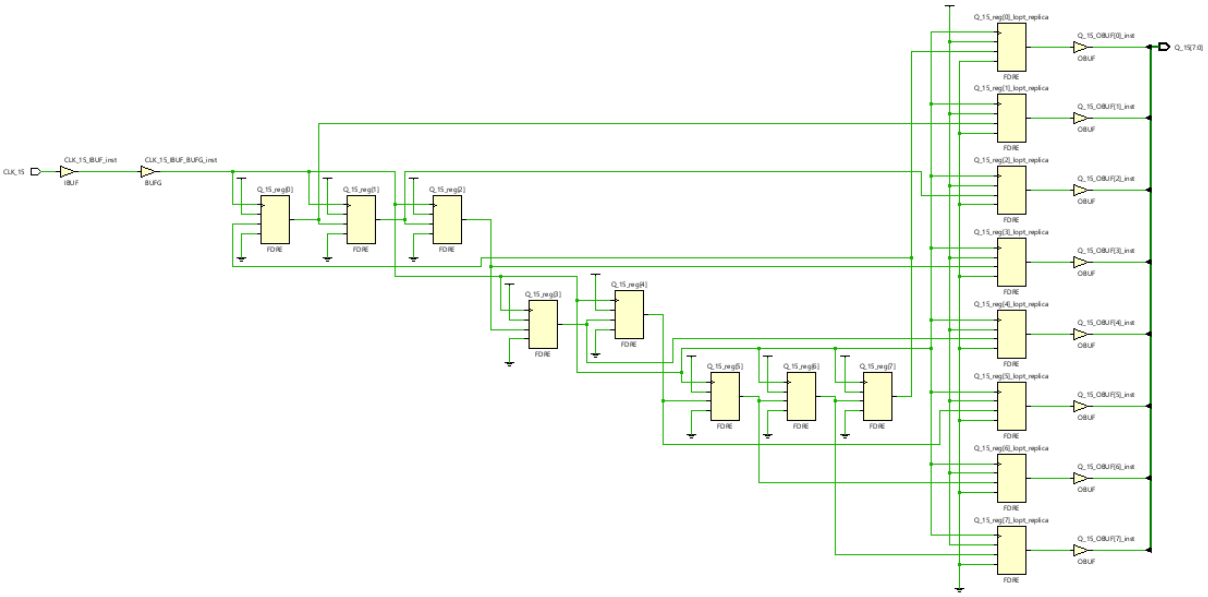
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	2	2	2	Q_15_reg[0]/C	Q_15[0]	3.419	2.836	0.584	∞
Path 2	∞	2	2	2	Q_15_reg[1]/C	Q_15[1]	3.419	2.836	0.584	∞
Path 3	∞	2	2	2	Q_15_reg[2]/C	Q_15[2]	3.419	2.836	0.584	∞
Path 4	∞	2	2	2	Q_15_reg[3]/C	Q_15[3]	3.419	2.836	0.584	∞
Path 5	∞	2	2	2	Q_15_reg[4]/C	Q_15[4]	3.419	2.836	0.584	∞
Path 6	∞	2	2	2	Q_15_reg[5]/C	Q_15[5]	3.419	2.836	0.584	∞
Path 7	∞	2	2	2	Q_15_reg[6]/C	Q_15[6]	3.419	2.836	0.584	∞
Path 8	∞	2	2	2	Q_15_reg[7]/C	Q_15[7]	3.419	2.836	0.584	∞
Path 9	∞	1	1	2	Q_15_reg[7]/C	Q_15_reg[0]/D	0.522	0.269	0.253	∞
Path 10	∞	1	1	2	Q_15_reg[0]/C	Q_15_reg[1]/D	0.522	0.269	0.253	∞

Post utilization/ area summary:

Resource	Utilization	Available	Utilization %
FF	8	82000	0.01
IO	9	300	3.00



Post implementation schematic:



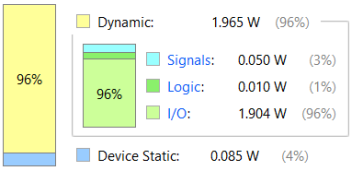
Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.05 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.9°C**
Thermal Margin:	56.1°C (29.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

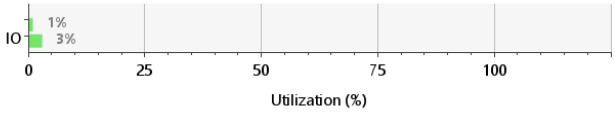


Post implementation timing summary:

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	2	1	1	Q_15_reg[0]_lopt_replica/C	Q_15[0]	4.020	2.703	1.318	∞
Path 2	∞	2	1	1	Q_15_reg[5]_lopt_replica/C	Q_15[5]	3.981	2.730	1.251	∞
Path 3	∞	2	1	1	Q_15_reg[6]_lopt_replica/C	Q_15[6]	3.969	2.729	1.240	∞
Path 4	∞	2	1	1	Q_15_reg[2]_lopt_replica/C	Q_15[2]	3.966	2.715	1.251	∞
Path 5	∞	2	1	1	Q_15_reg[1]_lopt_replica/C	Q_15[1]	3.959	2.720	1.239	∞
Path 6	∞	2	1	1	Q_15_reg[7]_lopt_replica/C	Q_15[7]	3.955	2.710	1.245	∞
Path 7	∞	2	1	1	Q_15_reg[4]_lopt_replica/C	Q_15[4]	3.931	2.686	1.245	∞
Path 8	∞	2	1	1	Q_15_reg[3]_lopt_replica/C	Q_15[3]	3.928	2.688	1.240	∞
Path 9	∞	1	1	2	Q_15_reg[1]/C	Q_15_reg[2]/D	0.892	0.269	0.623	∞
Path 10	∞	1	1	2	Q_15_reg[4]/C	Q_15_reg[5]/D	0.892	0.269	0.623	∞

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
FF	16	82000	0.02
IO	9	300	3.00



Conclusion:

- In this experiment, we written Verilog code for a circuit of 8-bit ring oscillator verified its output and Schematic using its test bench and we got desired output.