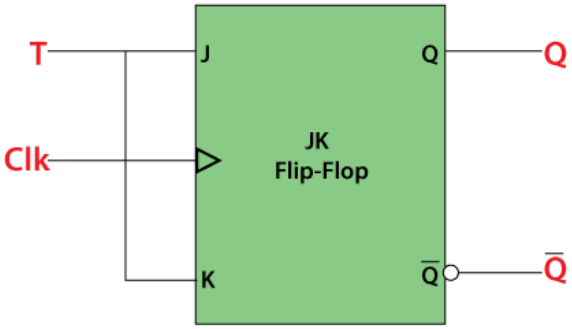
Experiment 7

Aim: Write Verilog codes to create T flip flop, SR flip flop, D flip flop and verify it using a testbench.

Theory:

T Flip-Flop (Toggle Flip-Flop):

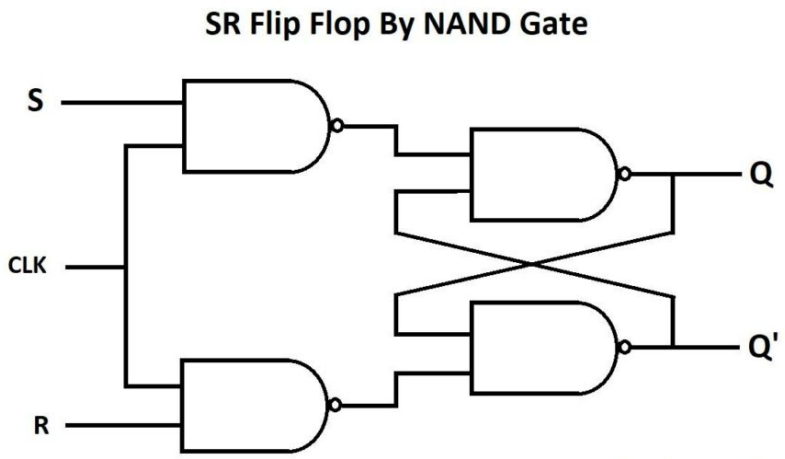
The T flip-flop is also known as a toggle flip-flop because it toggles its output (Q) based on the input (T). Here's the truth table for a T flip-flop:



	Previous		Next	
T	Q	Q'	Q	Q'
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	0	1

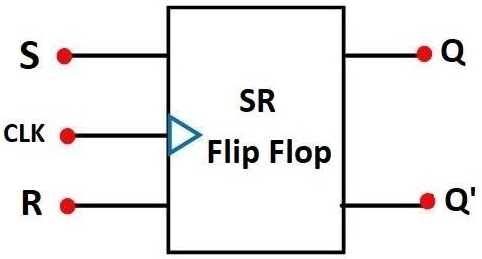
SR Flip-Flop (Set-Reset Flip-Flop):

The SR flip-flop has two inputs, S (Set) and R (Reset). It can be used to set (S=1) or reset (R=1) the flip-flop. Here's the truth table:



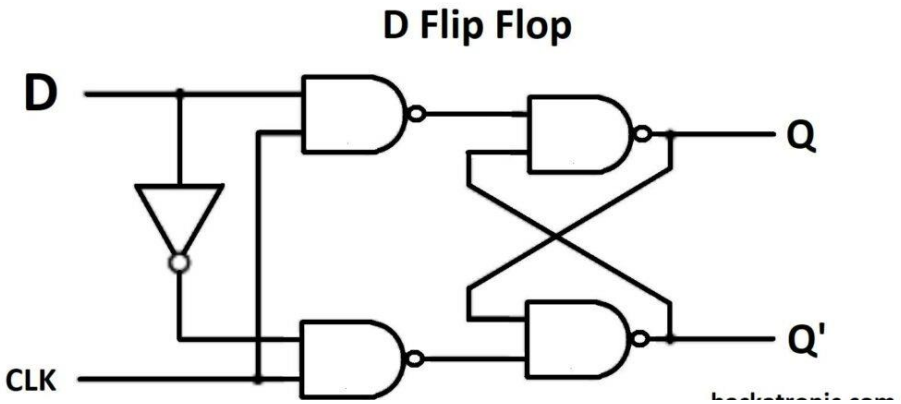
Truth Table of SR Flip Flop

S	R	Q	Q`
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞



D Flip-Flop (Data Flip-Flop):

The D flip-flop has a single data input (D) and a clock input (CLK). It stores the value of the D input on the rising edge of the clock signal. Here's the truth table:



Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

Code:

Behavioural Verilog code for T flip flop:

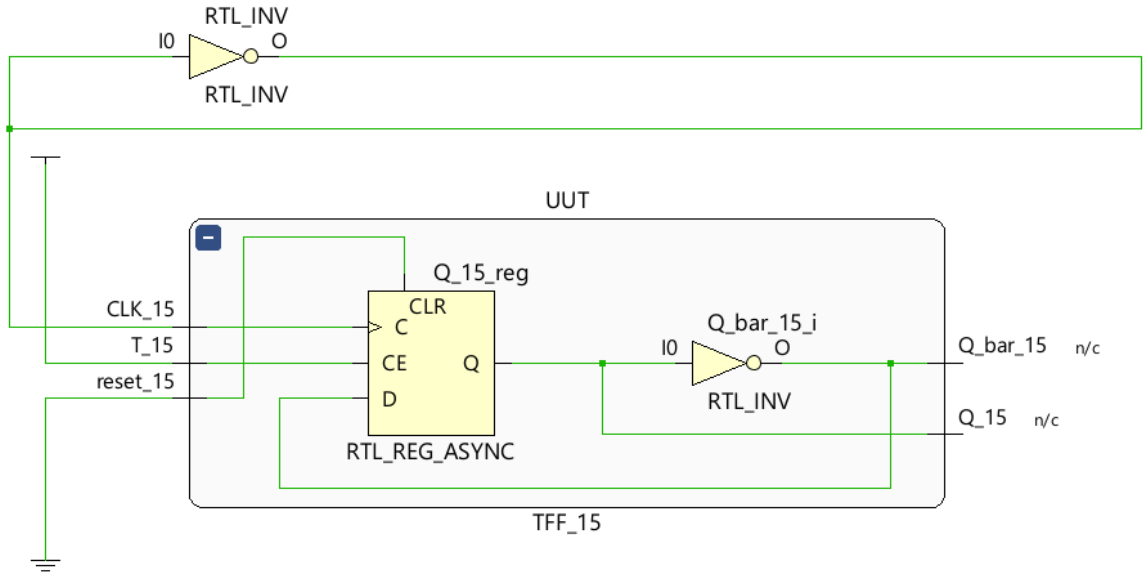
```
module TFF(
   input CLK,
   input T,
   input reset,
   output Q,
   output Q_bar
);

   reg Q, Q_next;

   always @(posedge CLK or posedge reset) begin
      if (reset) begin
         Q <= 1'b0;
      end else begin
         Q <= T ? ~Q : Q;
      end
   end

   assign Q_bar = ~Q;

endmodule
```

Testbench for T flip flop:

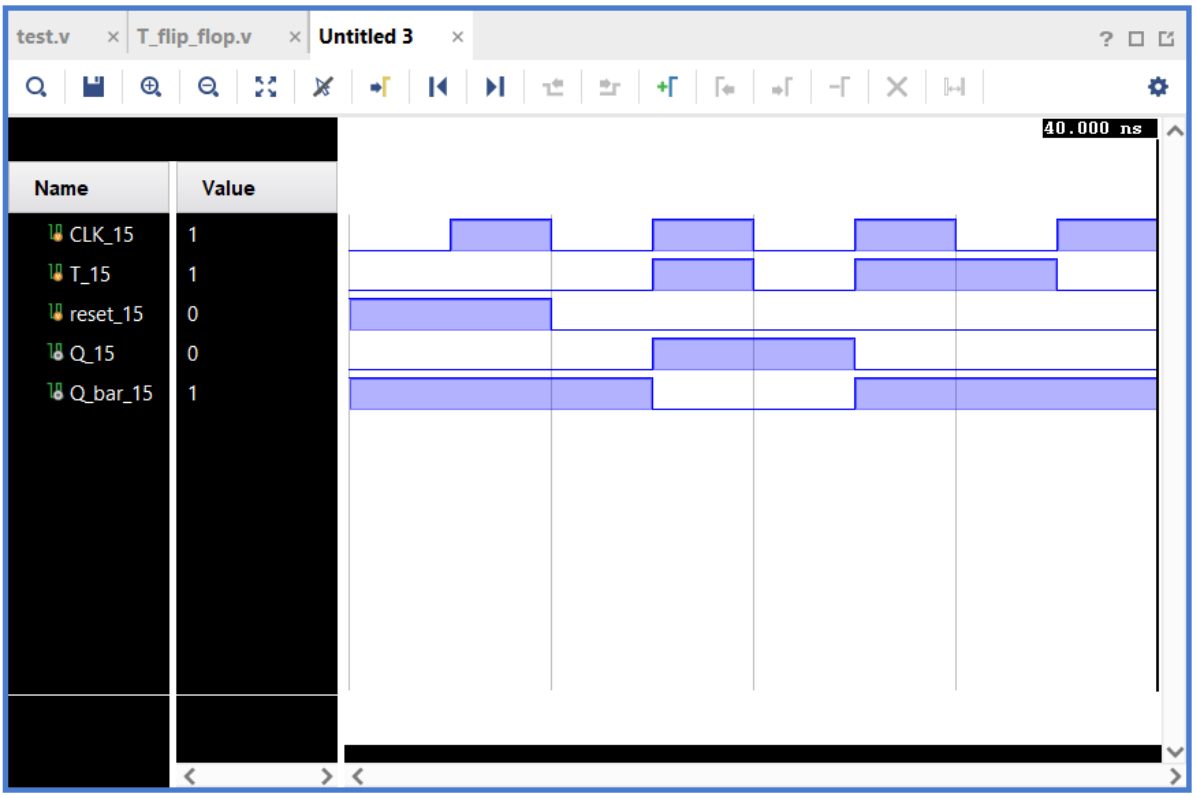
```
module testbench_TFF;

reg CLK;
reg T;
reg reset;
wire Q;
wire Q_bar;

// Instantiate the T flip-flop
TFF UUT (
   .CLK(CLK),
   .T(T),
   .reset(reset),
   .Q(Q),
   .Q_bar(Q_bar)
);

initial begin
   // Initialize inputs
```

```
    CLK = 0;
    T = 0;
    reset = 0;

    // Apply a reset pulse
    reset = 1;
    #10 reset = 0;

    // Test cases
    #5 T = 1; // Toggling input, Q should change
    #5 T = 0; // T is 0, Q should remain the same
    #5 T = 1; // Toggling input again, Q should change

    // Test cases
    #5 T = 1; // Toggling input, Q should change
    #5 T = 0;
    #5 T = 1;
    $finish;
end

always begin
    #5 CLK = ~CLK; // Toggle the clock every 5 time units
end

endmodule
```

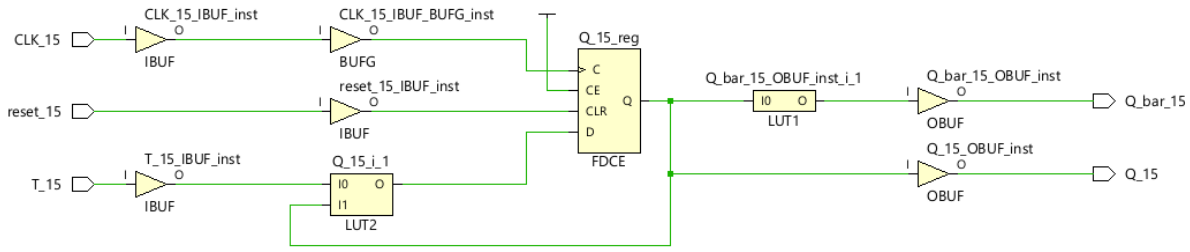
RTL Schematic:



Function Verification:



Post synthesis schematic:



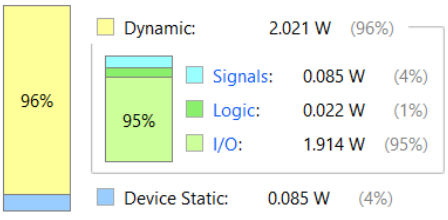
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**2.106 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**29.0°C**
Thermal Margin:	56.0°C (29.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power



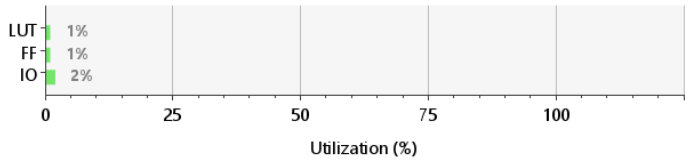
Post synthesis timing summary:

Unconstrained Paths - NONE - NONE - Setup

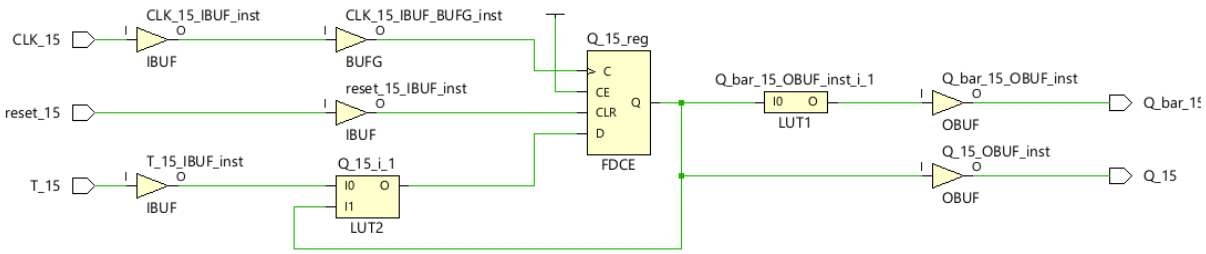
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	3	3	Q_15_reg/C	Q_bar_15	3.730	2.887	0.844	∞	
Path 2	∞	2	2	3	Q_15_reg/C	Q_15	3.419	2.836	0.584	∞	
Path 3	∞	2	3	1	T_15	Q_15_reg/D	1.466	0.883	0.584	∞	input port clock
Path 4	∞	1	2	1	reset_15	Q_15_reg/CLR	1.413	0.830	0.584	∞	input port clock

Post utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
FF	1	82000	0.00
IO	5	300	1.67



Post implementation schematic:

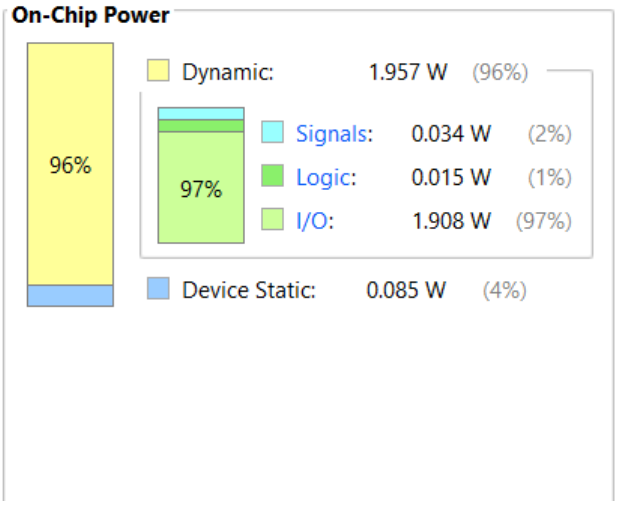


Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**2.042 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.8°C**
Thermal Margin:	56.2°C (29.6 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W



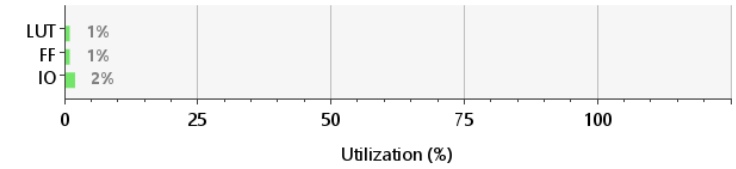
Post implementation timing summary:

Unconstrained Paths - NONE - NONE - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	3	Q_15_reg/C	Q_bar_15	4.367	2.773	1.595	∞	
Path 2	∞	2	1	3	Q_15_reg/C	Q_15	4.008	2.703	1.305	∞	
Path 3	∞	1	1	1	reset_15	Q_15_reg/CLR	1.644	0.787	0.856	∞	input port clock
Path 4	∞	2	1	1	T_15	Q_15_reg/D	1.559	0.870	0.689	∞	input port clock

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
FF	1	82000	0.00
IO	5	300	1.67



Code:

Behavioural Verilog code for SR flip flop:

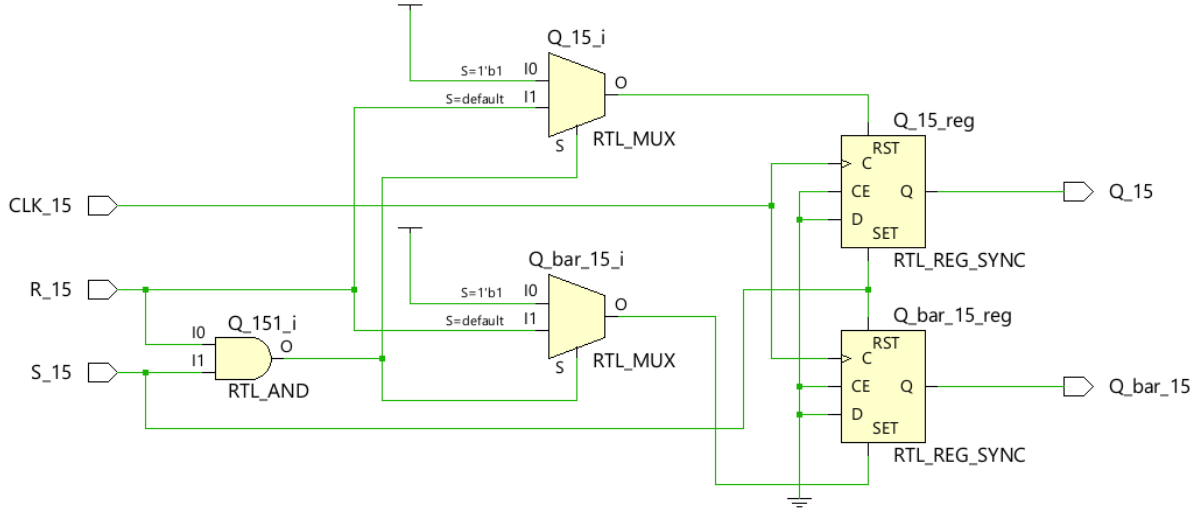
```
module sr_flip_flop (
    input CLK,
    input S,
    input R,
    output Q,
    output Q_bar
);

reg Q, Q_bar;

always @(posedge CLK) begin
    if (R && S) begin
        // Invalid condition, both set and reset are active
        Q <= 1'b0;
        Q_bar <= 1'b1;
    end else if (R) begin
        // Reset is active
        Q <= 1'b0;
        Q_bar <= 1'b1;
    end else if (S) begin
        // Set is active
        Q <= 1'b1;
        Q_bar <= 1'b0;
    end else begin
        // No action
```

```
        Q <= Q;
        Q_bar <= Q_bar;
    end
end

endmodule
```

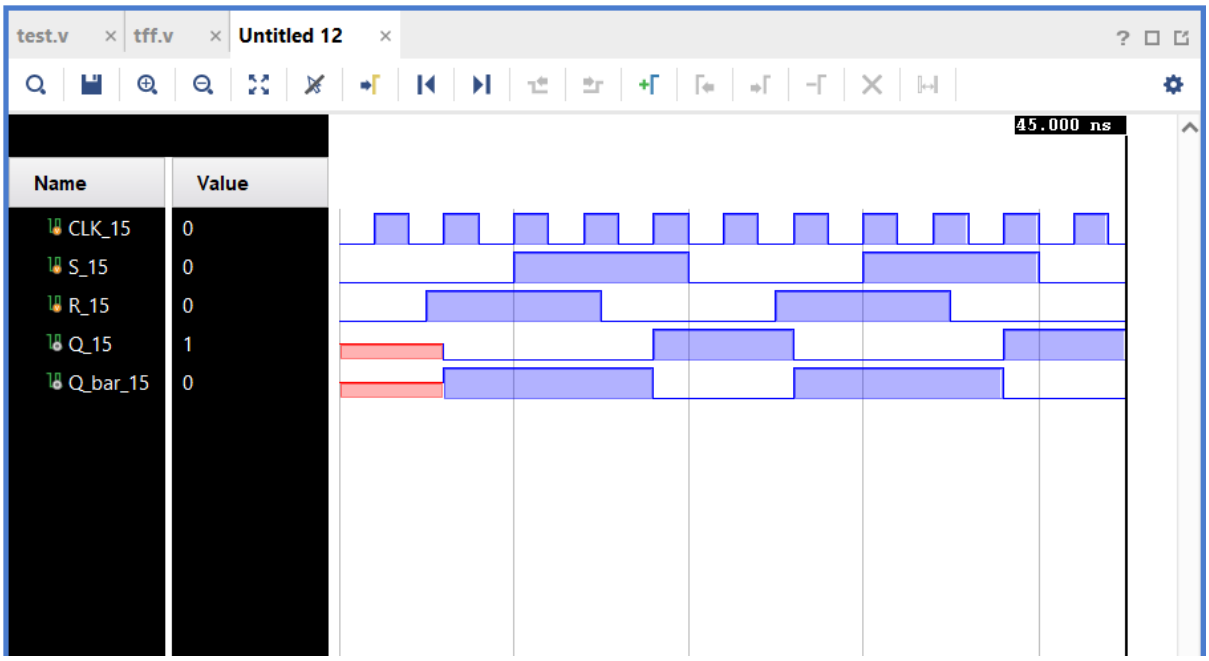
Testbench for SR flip flop:

```
module testbench;

reg CLK;
reg S;
reg R;
wire Q;
wire Q_bar;

sr_flip_flop uut (
    .CLK(CLK),
    .S(S),
    .R(R),
    .Q(Q),
    .Q_bar(Q_bar)
);

initial begin
    CLK = 0;
    S = 0;
    R = 0;
    #5 R = 1;
    #5 S = 1;
    #5 R = 0;
    #5 S = 0;
    #5 R = 1;
    #5 S = 1;
    #5 R = 0;
    #5 S = 0;
    #5 $finish;
end

always begin
    #2 CLK = ~CLK;
end

endmodule
```

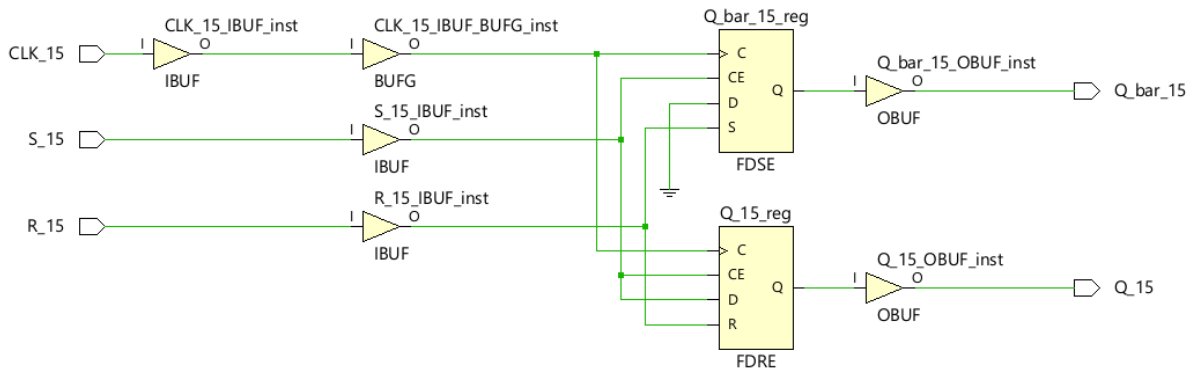
RTL Schematic:



Function Verification:



Post synthesis schematic:



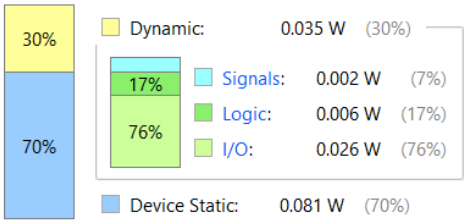
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.116 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W

On-Chip Power

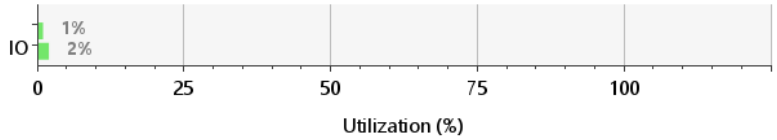


Post synthesis timing summary:

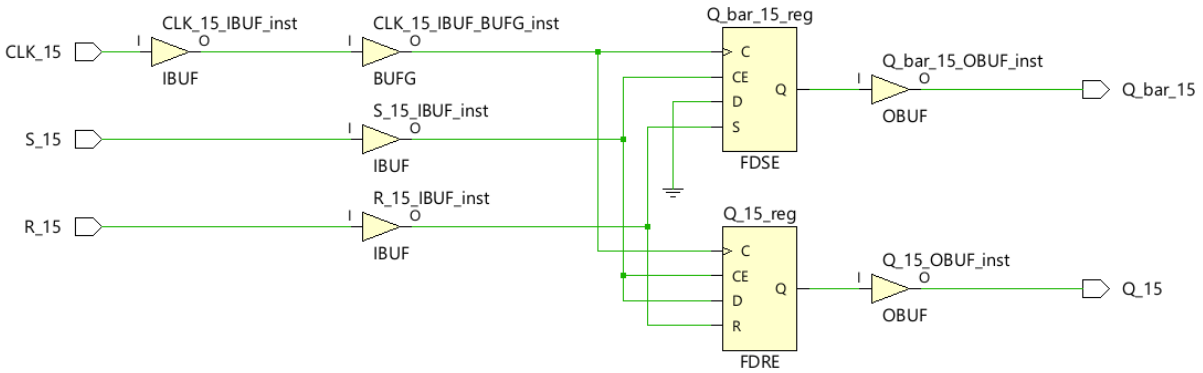
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	1	Q_15_reg/C	Q_15	3.419	2.836	0.584	∞	
Path 2	∞	2	2	1	Q_bar_15_reg/C	Q_bar_15	3.419	2.836	0.584	∞	
Path 3	∞	1	2	3	S_15	Q_15_reg/CE	1.413	0.830	0.584	∞	input port clock
Path 4	∞	1	2	3	S_15	Q_15_reg/D	1.413	0.830	0.584	∞	input port clock
Path 5	∞	1	2	2	R_15	Q_15_reg/R	1.413	0.830	0.584	∞	input port clock
Path 6	∞	1	2	3	S_15	Q_bar_15_reg/CE	1.413	0.830	0.584	∞	input port clock
Path 7	∞	1	2	2	R_15	Q_bar_15_reg/S	1.413	0.830	0.584	∞	input port clock

Post utilization/ area summary

Resource	Utilization	Available	Utilization %
FF	2	82000	0.00
IO	5	300	1.67



Post implementation schematic:



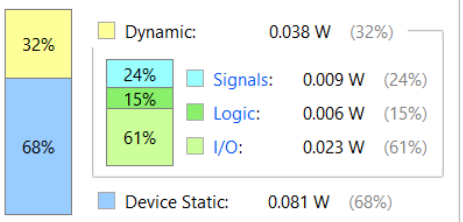
Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.119 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**25.2°C**
Thermal Margin:	59.8°C (31.5 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

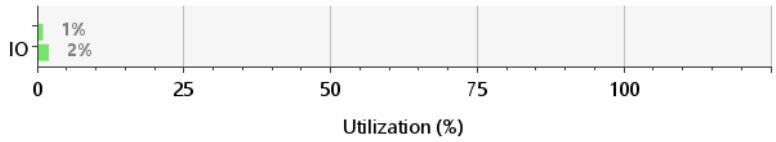


Post implementation timing summary:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	1	1	Q_15_reg/C	Q_15	3.997	2.703	1.295	∞	
Path 2	∞	2	1	1	Q_bar_15_reg/C	Q_bar_15	3.991	2.720	1.272	∞	
Path 3	∞	1	1	3	S_15	Q_15_reg/D	1.669	0.787	0.881	∞	input port clock
Path 4	∞	1	1	2	R_15	Q_15_reg/R	1.570	0.814	0.756	∞	input port clock
Path 5	∞	1	1	2	R_15	Q_bar_15_reg/S	1.570	0.814	0.756	∞	input port clock
Path 6	∞	1	1	3	S_15	Q_15_reg/CE	1.522	0.787	0.734	∞	input port clock
Path 7	∞	1	1	3	S_15	Q_bar_15_reg/CE	1.522	0.787	0.734	∞	input port clock

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
FF	2	82000	0.00
IO	5	300	1.67



Code:

Behavioural Verilog code for D flip flop:

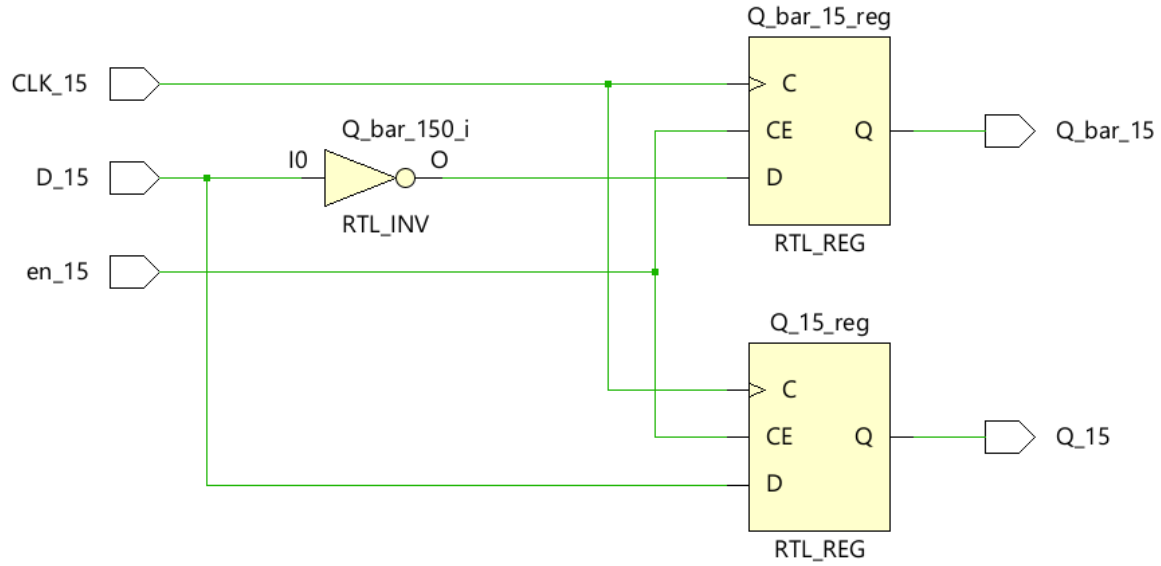
```
module d_flip_flop (
    input CLK,
    input D,
    input en,
    output Q,
    output Q_bar
);

reg Q, Q_bar;

always @(posedge CLK) begin
```

```
    if (en) begin
        Q <= D;
        Q_bar <= ~D;
    end
end

endmodule
```

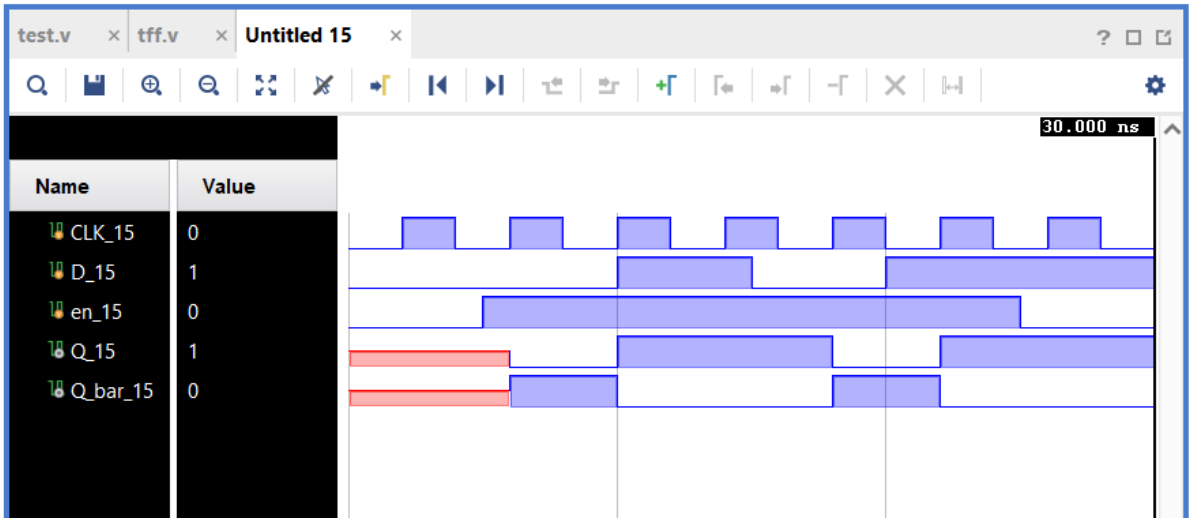
Testbench for D flip flop:

```
module testbench;

reg CLK;
reg D;
reg en;
wire Q;
wire Q_bar;

d_flip_flop uut (
    .CLK(CLK),
    .D(D),
    .en(en),
    .Q(Q),
    .Q_bar(Q_bar)
);

initial begin
    CLK = 0;
    D = 0;
    en = 0;
    #5 en = 1;
    #5 D = 1;
    #5 D = 0;
    #5 D = 1;
    #5 en = 0;
    #5 $finish;
end

always begin
    #2 CLK = ~CLK;
end

endmodule
```

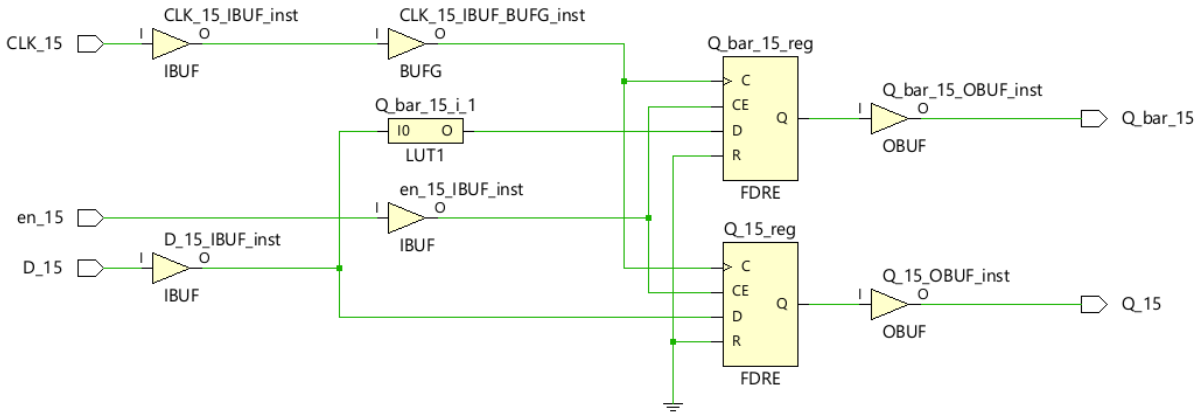
RTL Schematic:



Function Verification:



Post synthesis schematic:



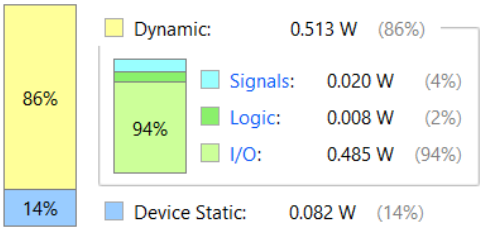
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.595 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.1°C**
Thermal Margin:	58.9°C (31.1 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

On-Chip Power

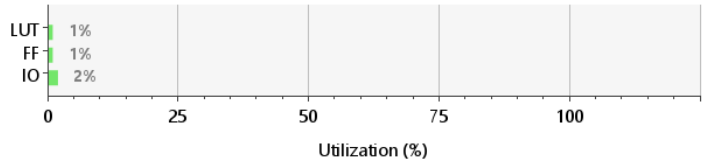


Post synthesis timing summary:

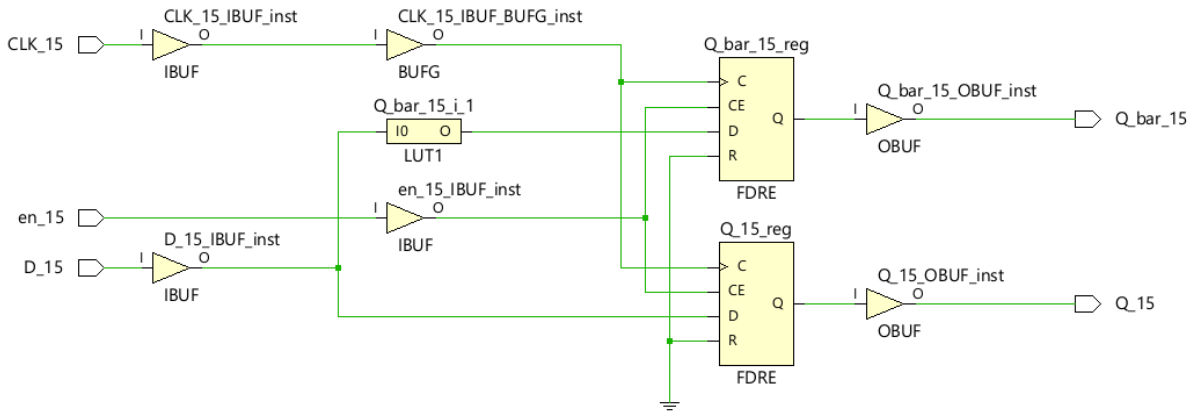
Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	1	Q_15_reg/C	Q_15	3.419	2.836	0.584	∞	
Path 2	∞	2	2	1	Q_bar_15_reg/C	Q_bar_15	3.419	2.836	0.584	∞	
Path 3	∞	2	3	2	D_15	Q_bar_15_reg/D	1.466	0.883	0.584	∞	input port clock
Path 4	∞	1	2	2	en_15	Q_15_reg/CE	1.413	0.830	0.584	∞	input port clock
Path 5	∞	1	2	2	D_15	Q_15_reg/D	1.413	0.830	0.584	∞	input port clock
Path 6	∞	1	2	2	en_15	Q_bar_15_reg/CE	1.413	0.830	0.584	∞	input port clock

Post utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
FF	2	82000	0.00
IO	5	300	1.67



Post implementation schematic:

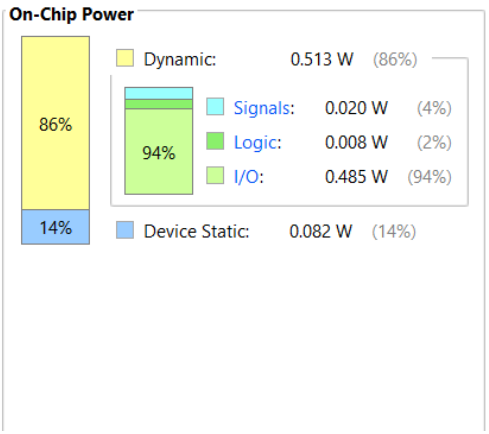


Post implementation power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**0.595 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**26.1°C**
Thermal Margin:	58.9°C (31.1 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W

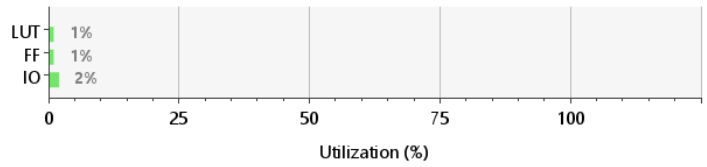


Post implementation timing summary:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	2	2	1	Q_15_reg/C	Q_15	3.419	2.836	0.584	∞	
Path 2	∞	2	2	1	Q_bar_15_reg/C	Q_bar_15	3.419	2.836	0.584	∞	
Path 3	∞	2	3	2	D_15	Q_bar_15_reg/D	1.466	0.883	0.584	∞	input port clock
Path 4	∞	1	2	2	en_15	Q_15_reg/CE	1.413	0.830	0.584	∞	input port clock
Path 5	∞	1	2	2	D_15	Q_15_reg/D	1.413	0.830	0.584	∞	input port clock
Path 6	∞	1	2	2	en_15	Q_bar_15_reg/CE	1.413	0.830	0.584	∞	input port clock

Post implementation utilization/ area summary:

Resource	Utilization	Available	Utilization %
LUT	1	41000	0.00
FF	2	82000	0.00
IO	5	300	1.67



Conclusion:

- In this experiment, we written Verilog code for a circuit of T flip flop, SR flip flop, D flip flop verified its output and Schematic using its test bench and we got desired output.