Experiment 1

Aim: Write Verilog codes for all basic logic gates having structural, data flow and behavioural model and perform synthesis by generating different synthesis and timing waveforms.

Theory:7

Basic Logic Gates

There are seven fundamental types of logic gates: AND, OR, XOR, NAND, NOR, XNOR, and NOT. These essential digital devices operate based on Boolean functions and are employed to perform logical operations on single or multiple binary inputs, resulting in a single binary output.

(1) OR Gate:

The OR gate produces an output of 1 if at least one of its inputs is set to 1. Its Boolean expression is represented as:

Y = A OR B

(2) AND Gate:

An AND gate generates an output of 1 only when all of its inputs are set to 1. Its Boolean expression is:

Y = A AND B

(3) NAND Gate:

The NAND gate is a digital circuit with two or more inputs that outputs the logical AND of all those inputs, but inverted. Its expression is:

Y = NOT (A AND B)

(4) NOR Gate:

A NOR gate, with two or more inputs, produces an output that is the logical OR of all those inputs, but inverted:

Y = NOT (A OR B)

(5) XOR Gate:

Known as the Exclusive-OR gate, the XOR gate outputs 1 when the number of true inputs is odd. Its expression is:

Y = A XOR B

(6) XNOR Gate:

The XNOR gate is the logical complement of the XOR gate, producing an output of 1 when the inputs are equal. Its expression is:

Y = NOT (A XOR B)

Code:

1) Structural

```
module basicgate_s(
   input a, b,
   output c
   );
   and(and, a, b);
   or(or, a, b);
   nand(nand, a, b);
   nor(nor, a, b);
   xor(xor, a, b);
   xnor(xnor, a, b);
endmodule
```

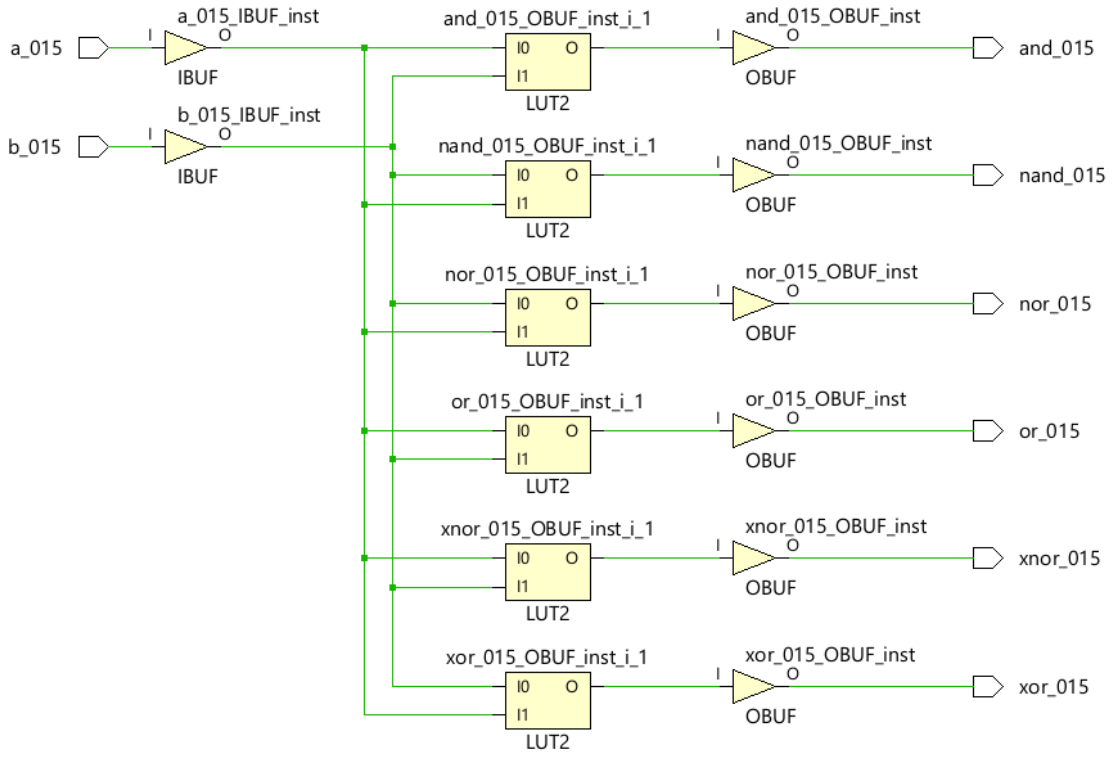
2) Data Flow

```
module basicgate_d(
   input a, b,
   output c
   );
   assign and = a & b;
   assign or = a | b;
   assign nand = ~(a & b);
   assign nor = ~(a | b);
   assign xor = a ^ b;
   assign xnor = ~(a ^ b);
endmodule
```

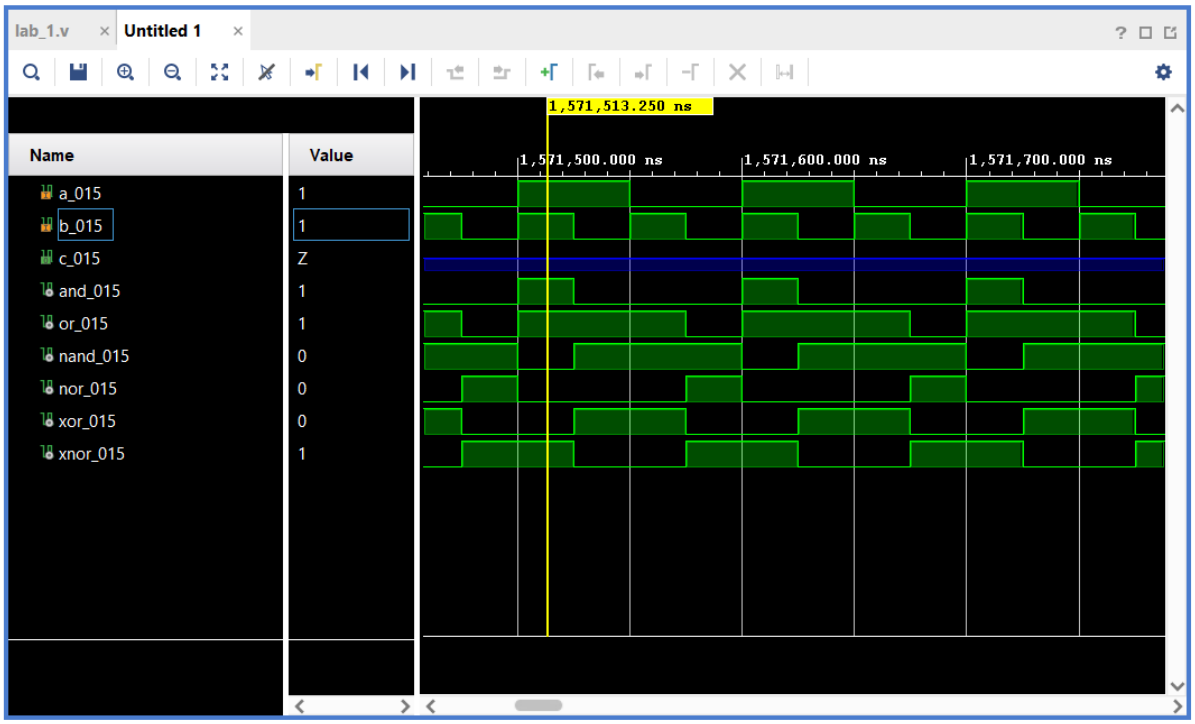
3) Behavioural

```
module basicgate_b(
   input a, b,
   output reg and, or, nand, nor, xor, xnor
   );
   always @(a, b)
   begin
      and = a & b;
      or = a | b;
      nand = ~(a & b);
      nor = ~(a | b);
      xor = a ^ b;
      xnor = ~(a ^ b);
   end
endmodule
```

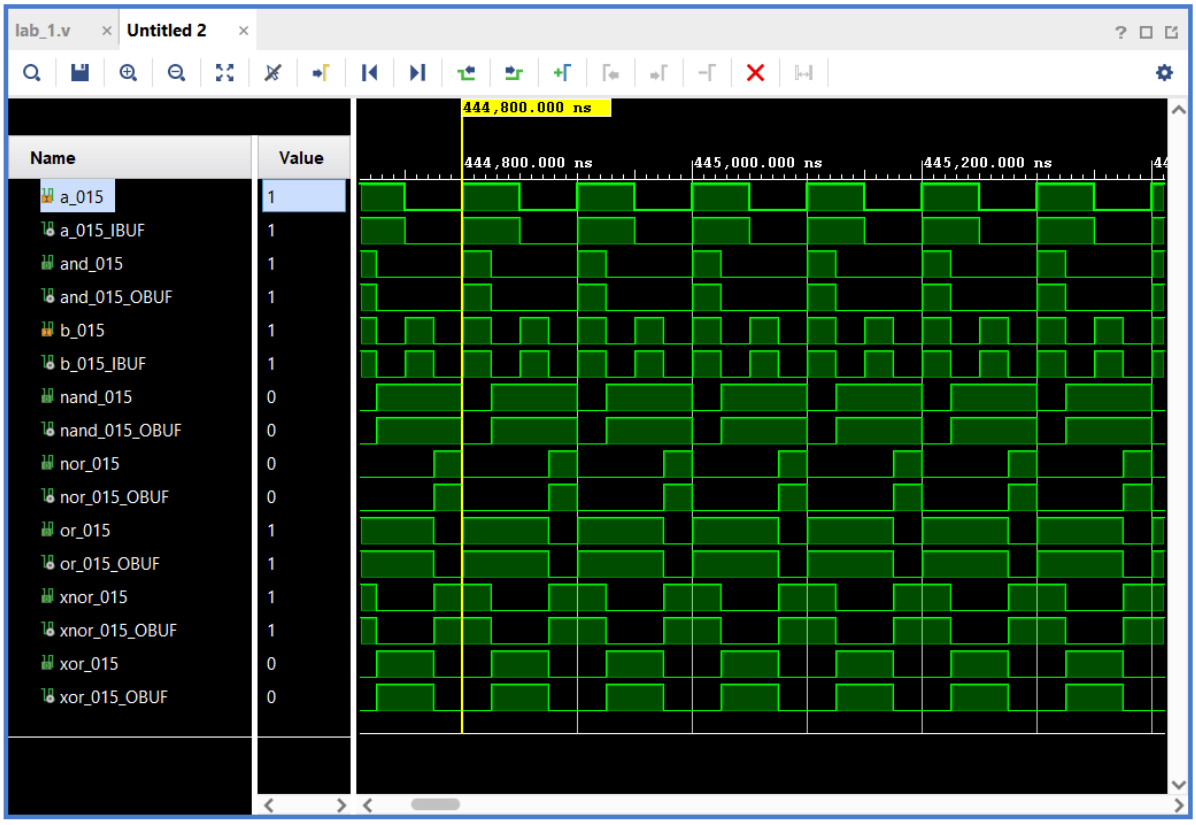
RTL Schematic:



Function Verification:



Post synthesis schematic:



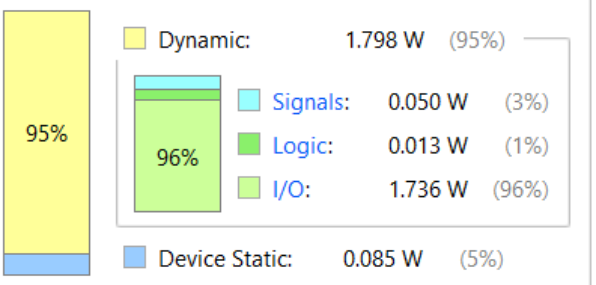
Post power report:

Summary

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**1.883 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.5°C**
Thermal Margin:	56.5°C (29.8 W)
Ambient Temperature:	25.0 °C
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

On-Chip Power



Post synthesis timing summary:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	inf	Worst Hold Slack (WHS):	inf	Worst Pulse Width Slack (WPWS):	NA
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	NA
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	NA
Total Number of Endpoints:	6	Total Number of Endpoints:	6	Total Number of Endpoints:	NA

There are no user specified timing constraints.

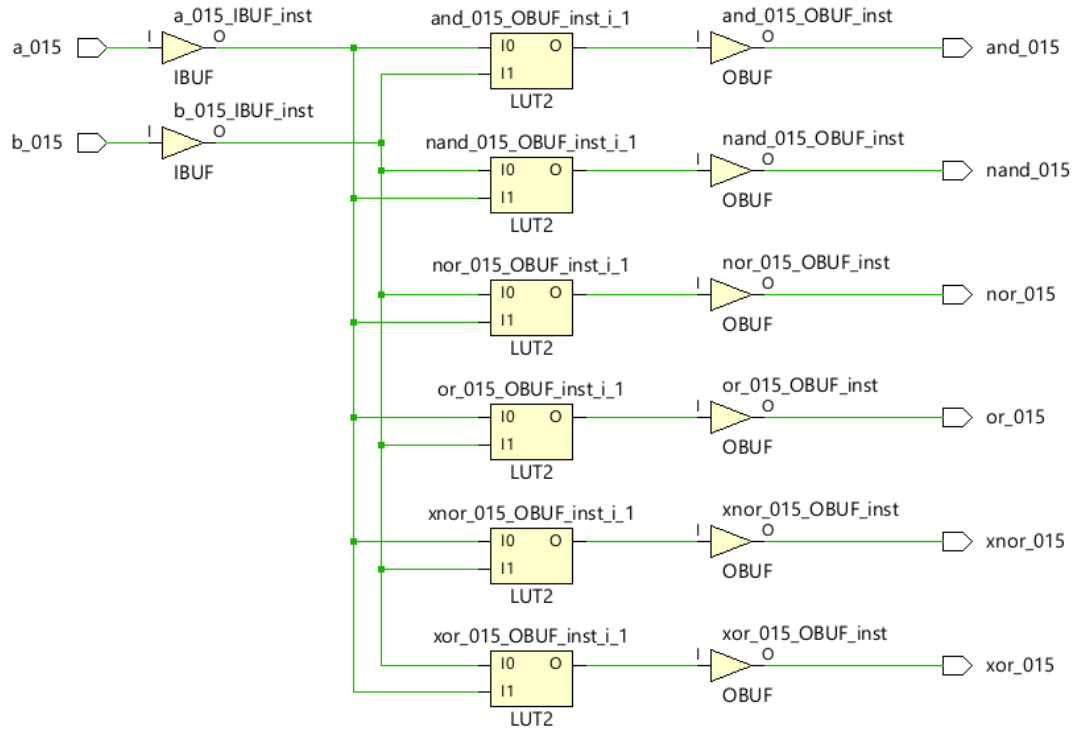
Post utilization/ area summary:

Reports | Design Runs | **Utilization** | Timing | Power

Hierarchy

Name	Slice LUTs (41000)	Bonded IOB (300)
basicgate_s	3	8

Post implementation schematic:



Post implementation power report:

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.855 W**
Design Power Budget:	**Not Specified**
Process:	typical
Power Budget Margin:	**N/A**
Junction Temperature:	**28.5°C**
Thermal Margin:	56.5°C (29.8 W)
Ambient Temperature:	25.0 °C
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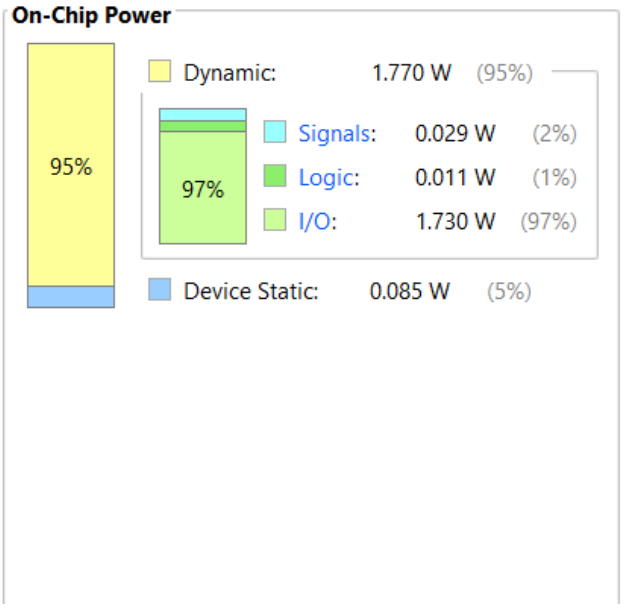
Launch Power Constraint Advisor to find and fix



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Post implementation utilization/ area summary: