

```
1 -----Shubham Prakash
2 -----EC - B
3 -----Roll: 36
4 -----Reg. no: 20319084
5 -----Full Adder testBench (Behavioral)
6
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity FullAdder_tb is
12 end entity;
13
14 architecture tb of FullAdder_tb is
15 component fAdderBhv is
16 Port ( A : in std_logic_vector (2 downto 0);
17 O : out std_logic_vector (1 downto 0));
18 end component;
19
20 signal A : std_logic_vector(2 downto 0);
21 signal O : std_logic_vector(1 downto 0);
22
23 begin
24
25 uut: fAdderBhv port map(
26 A => A, O => O);
27
28 stim: process
29 begin
30
31 A <= "000";
32 wait for 20 ns;
33
34 A <= "001";
35 wait for 20 ns;
36
37 A <= "010";
38 wait for 20 ns;
39
40 A <= "011";
41 wait for 20 ns;
42
43 A <= "100";
44 wait for 20 ns;
45
46 A <= "101";
47 wait for 20 ns;
48
49 A <= "110";
50 wait for 20 ns;
51
52 A <= "111";
53 wait for 20 ns;
54
55 wait;
56
57 end process;
```

58 **end** tb;