

```
1 ----Shubham Prakash
2 ----EC - B
3 ----Roll: 36
4 ----Reg.: 20319084
5 -----Full Adder testBench (Structural)
6
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity full_adder_tb is
12 end full_adder_tb;
13
14 architecture testArch of full_adder_tb is
15     component full_adder is
16         port(
17             in1, in2, c_in : in std_logic;
18             sum, c_out : out std_logic
19         );
20     end component;
21
22     signal a, b, c : std_logic;
23     signal sum, cout : std_logic;
24 begin
25     uut : full_adder port map (in1 => a,in2 => b,c_in => c,sum => sum,c_out => cout);
26
27     process
28     begin
29         a <= '0'; b <= '0'; c <= '0';
30         wait for 1 ns;
31
32         a <= '0'; b <= '0'; c <= '1';
33         wait for 1 ns;
34
35         a <= '0'; b <= '1'; c <= '0';
36         wait for 1 ns;
37
38         a <= '0'; b <= '1'; c <= '1';
39         wait for 1 ns;
40
41         a <= '1'; b <= '0'; c <= '0';
42         wait for 1 ns;
43
44         a <= '1'; b <= '0'; c <= '1';
45         wait for 1 ns;
46
47         a <= '1'; b <= '1'; c <= '0';
48         wait for 1 ns;
49
50         a <= '1'; b <= '1'; c <= '1';
51         wait for 1 ns;
52
53         a <= '0'; b <= '0'; c <= '0';
54         wait;
55
56     end process;
57 end testArch;
```

