

```
1 -----Shubham Prakash
2 -----EC - B
3 -----Roll: 36
4 -----Reg. no: 20319084
5 -----Full Adder (Behavioral)
6
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity fAdderBhv is
12 Port ( A : in std_logic_vector (2 downto 0);
13       O : out std_logic_vector (1 downto 0));
14 end fAdderBhv;
15
16 architecture bArch of fAdderBhv is
17
18 begin
19 process (A)
20 begin
21
22 if (A = "001" or A = "010" or A = "100" or A = "111") then
23 O(1) <= '1';
24
25 else
26 O(1) <= '0';
27 end if;
28
29 if (A = "011" or A = "101" or A = "110" or A = "111") then
30 O(0) <= '1';
31 else
32 O(0) <= '0';
33 end if;
34
35 end process;
36 end bArch;
```