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1 -----Shubham Prakash
2 -----EC - B
3 -----Roll: 36
4 -----Reg. no: 20319084
5 -----Full Adder testBench (Dataflow)
6
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity full_adder_tb is
12 end full_adder_tb;
13
14 architecture testArch of full_adder_tb is
15     component fa is
16         port (
17             a: in std_logic;
18             b: in std_logic;
19             c: in std_logic;
20             sum: out std_logic;
21             cout: out std_logic
22         );
23     end component;
24
25     signal a, b, c : std_logic;
26     signal sum, cout : std_logic;
27 begin
28     uut : fa port map (a, b, c, sum, cout);
29
30     process
31     begin
32         a <= '0'; b <= '0'; c <= '0';
33         wait for 1 ns;
34
35         a <= '0'; b <= '0'; c <= '1';
36         wait for 1 ns;
37
38         a <= '0'; b <= '1'; c <= '0';
39         wait for 1 ns;
40
41         a <= '0'; b <= '1'; c <= '1';
42         wait for 1 ns;
43
44         a <= '1'; b <= '0'; c <= '0';
45         wait for 1 ns;
46
47         a <= '1'; b <= '0'; c <= '1';
48         wait for 1 ns;
49
50         a <= '1'; b <= '1'; c <= '0';
51         wait for 1 ns;
52
53         a <= '1'; b <= '1'; c <= '1';
54         wait for 1 ns;
55
56         a <= '0'; b <= '0'; c <= '0';
57         wait;
```

```
58  
59     end process;  
60 end testArch;
```