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1 -----Shubham Prakash
2 -----EC - B
3 -----Roll: 36
4 -----Reg. no: 20319084
5 -----Full Adder (Structural)
6
7
8 library ieee;
9 use ieee.std_logic_1164.all;
10
11 entity full_adder is
12     port(
13         in1, in2, c_in : in std_logic;
14         sum, c_out : out std_logic
15     );
16 end full_adder;
17
18 library ieee;
19 use ieee.std_logic_1164.all;
20 entity half_adder is
21     port(
22         x,y : in std_logic;
23         sum, carry : out std_logic
24     );
25 end half_adder;
26
27 library ieee;
28 use ieee.std_logic_1164.all;
29 entity or_2 is
30     port(
31         x,y : in std_logic;
32         z : out std_logic
33     );
34 end or_2;
35
36 architecture haArch of half_adder is
37 begin
38     sum <= x xor y;
39     carry <= x and y;
40 end haArch;
41
42 architecture orArch of or_2 is
43 begin
44     z <= x or y;
45 end orArch;
46
47 architecture strArch of full_adder is
48     component half_adder is
49         port(
50             x,y : in std_logic;
51             sum, carry : out std_logic
52         );
53     end component;
54
55     component or_2 is
56         port(
57             x,y : in std_logic;
```

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58         z : out std_logic
59     );
60 end component;
61
62 signal s1, s2, s3 : std_logic;
63 begin
64     h1 : half_adder port map (in1, in2, s1, s2);
65     h2 : half_adder port map (c_in, s1, sum, s3);
66     or1 : or_2 port map (s2, s3, c_out);
67 end strArch;
```