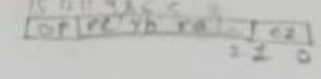
R type



DATE | | | PAGE

* Add rc, ra, rb

Add
NDU

S1: PC → mem_a, alu_a
mem_d → IR
+1 → alu_b
alu_out → PC

rc = ra + rb

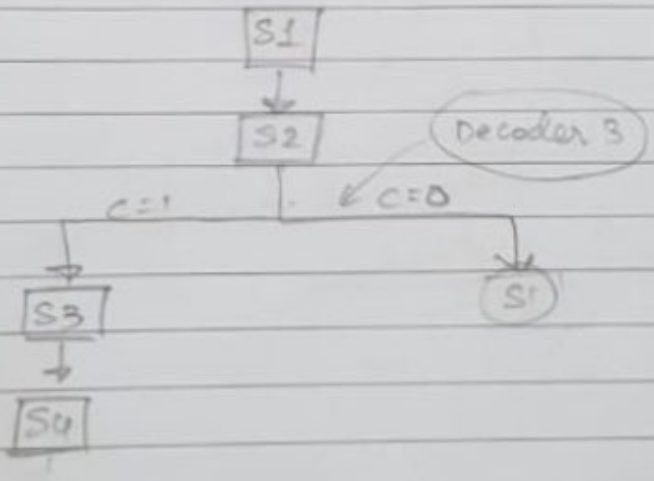
Here PC = r7

S2: IR_{6-8} → rf_a1
IR_{3-5} → rf_a2
rf_d1 → t1
rf_d2 → t2

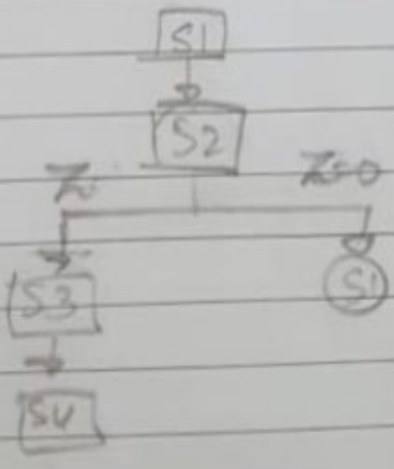
S3: t1 → alu_a
t2 → alu_b
alu_out → t1

S4: t1 → rf_d3
IR_{9-11} → rf_a3
→ 1

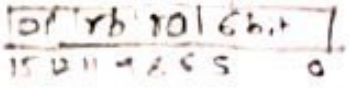
* ADC rc, ra, rb ; NDC rc, ra, rb



* ND2 rc, ra, rb ; ND2 rc, ra, rb



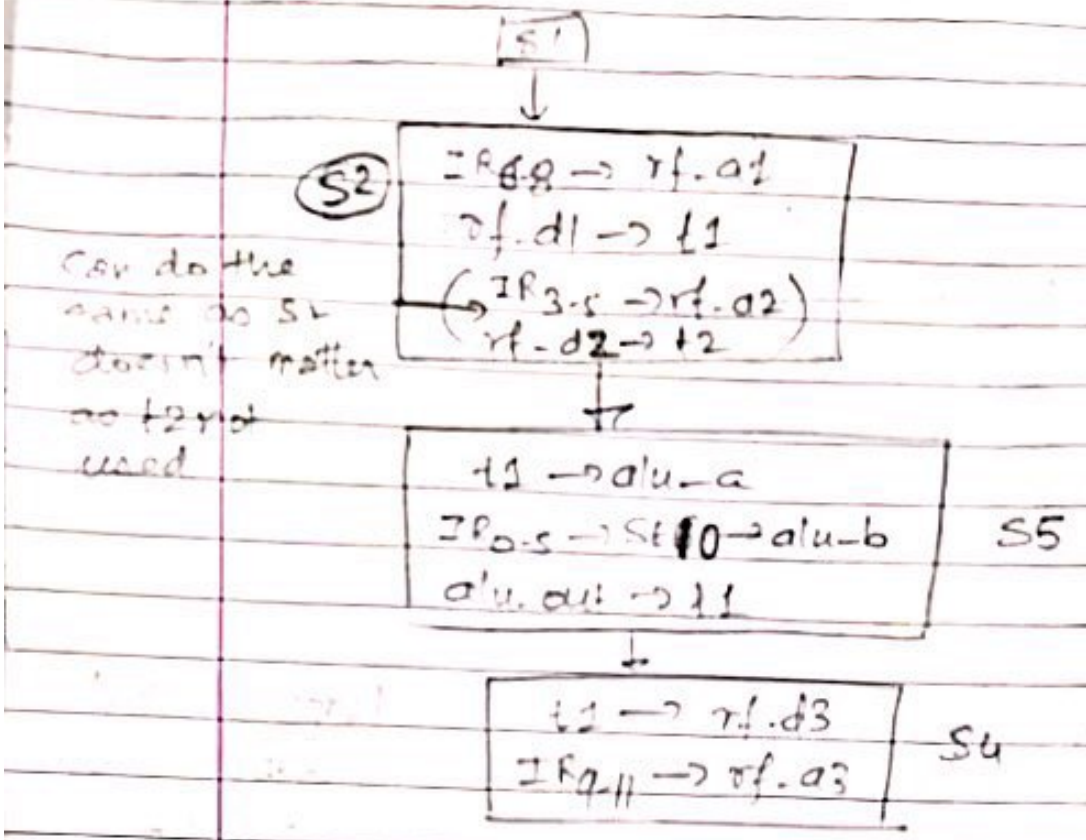
I-type



DATE / / PAGE

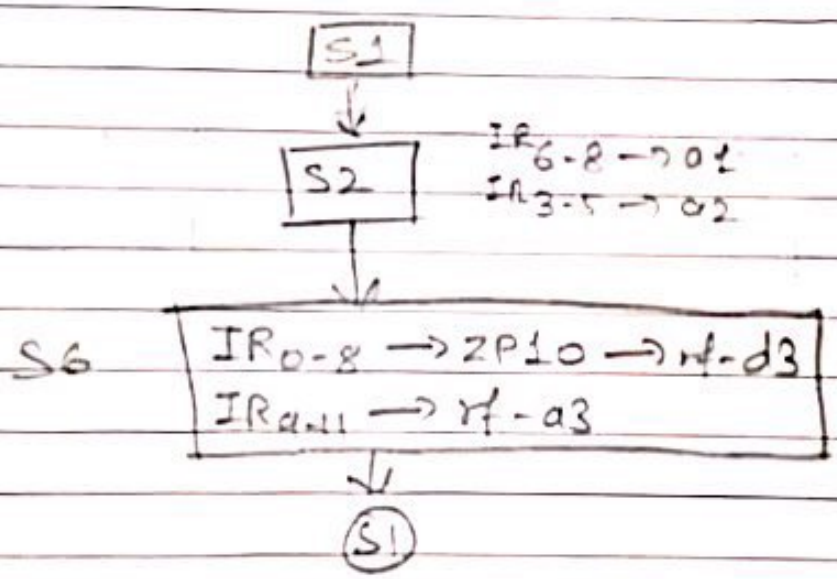
* ADI

$rB = rA + SE(6bit)$



* LHI rA, (abit)

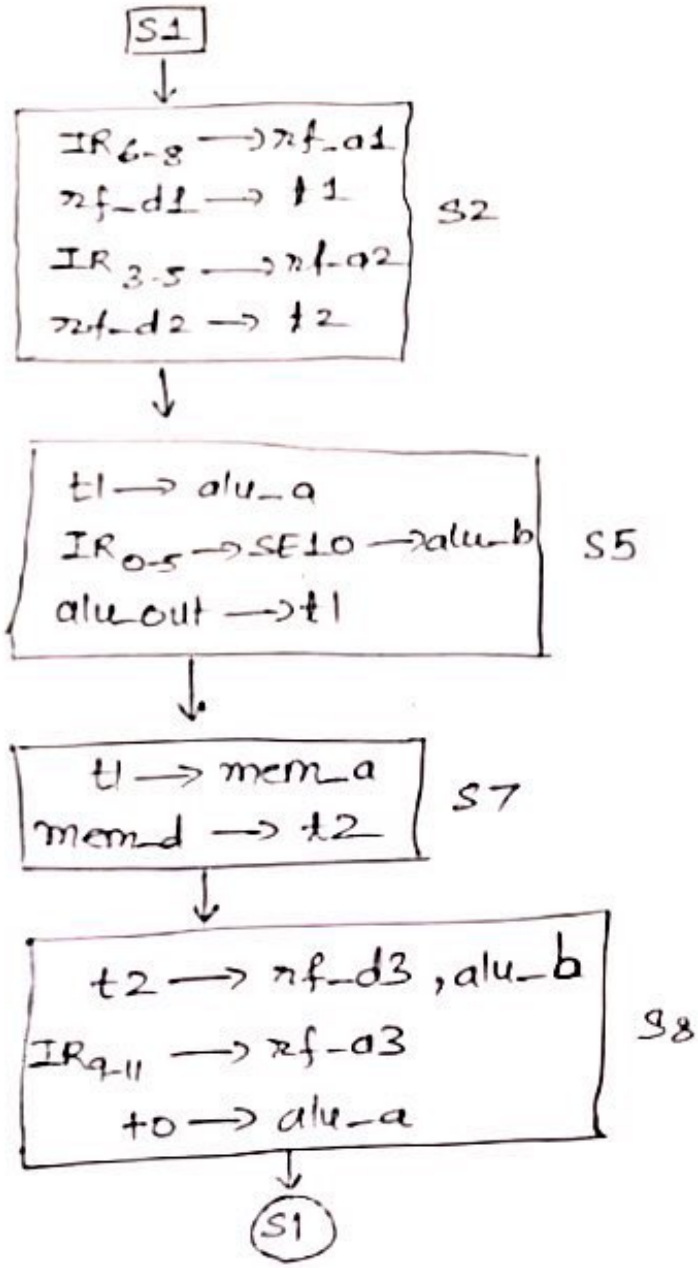
$rA = $ 'abit' 0000000



* LW rA, rB, Imm(6bit)

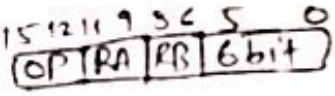
15	9	8	6	5	0
OP	RA	RB	6bit		

rA ← [rB+6bit]

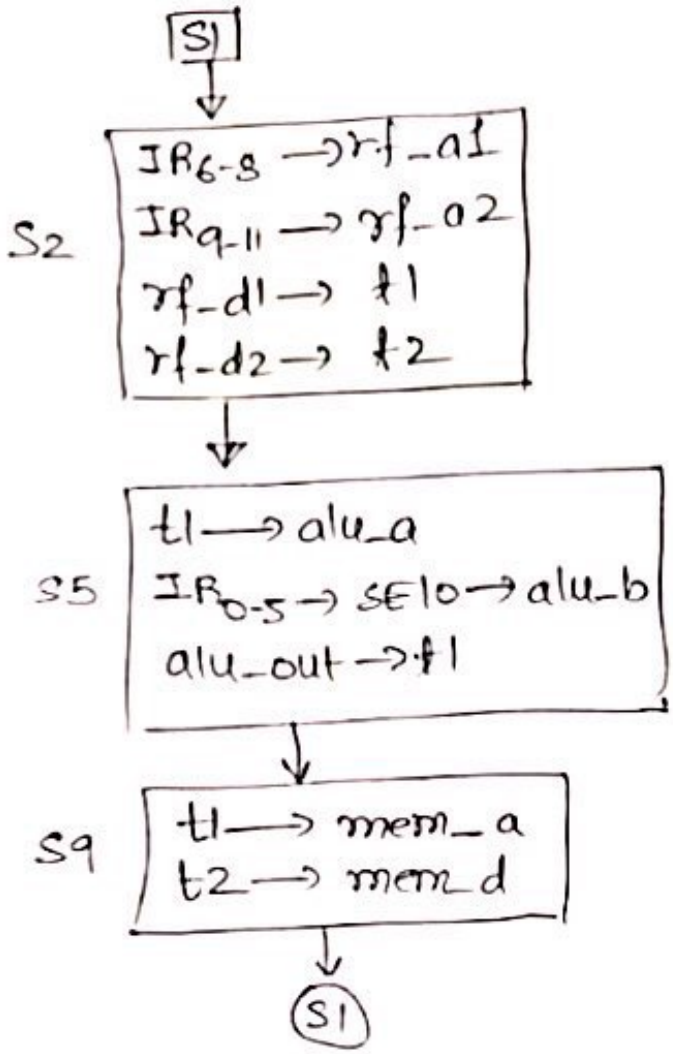


Affect zero flag

* SW ra, rb, Imm(6bit)

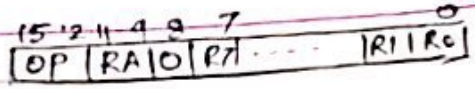


[rb+6bits] ← ra

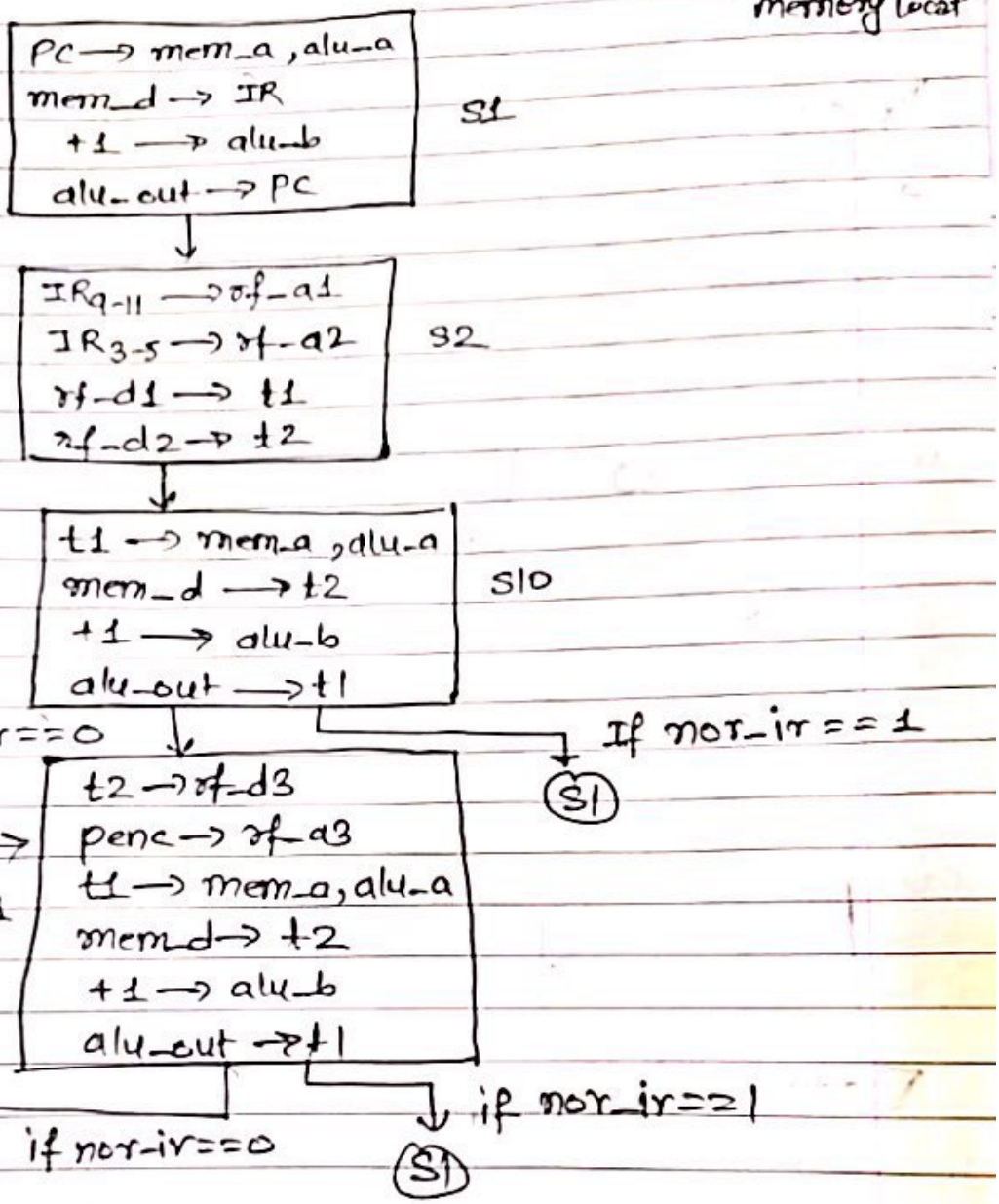


DATE / / PAGE

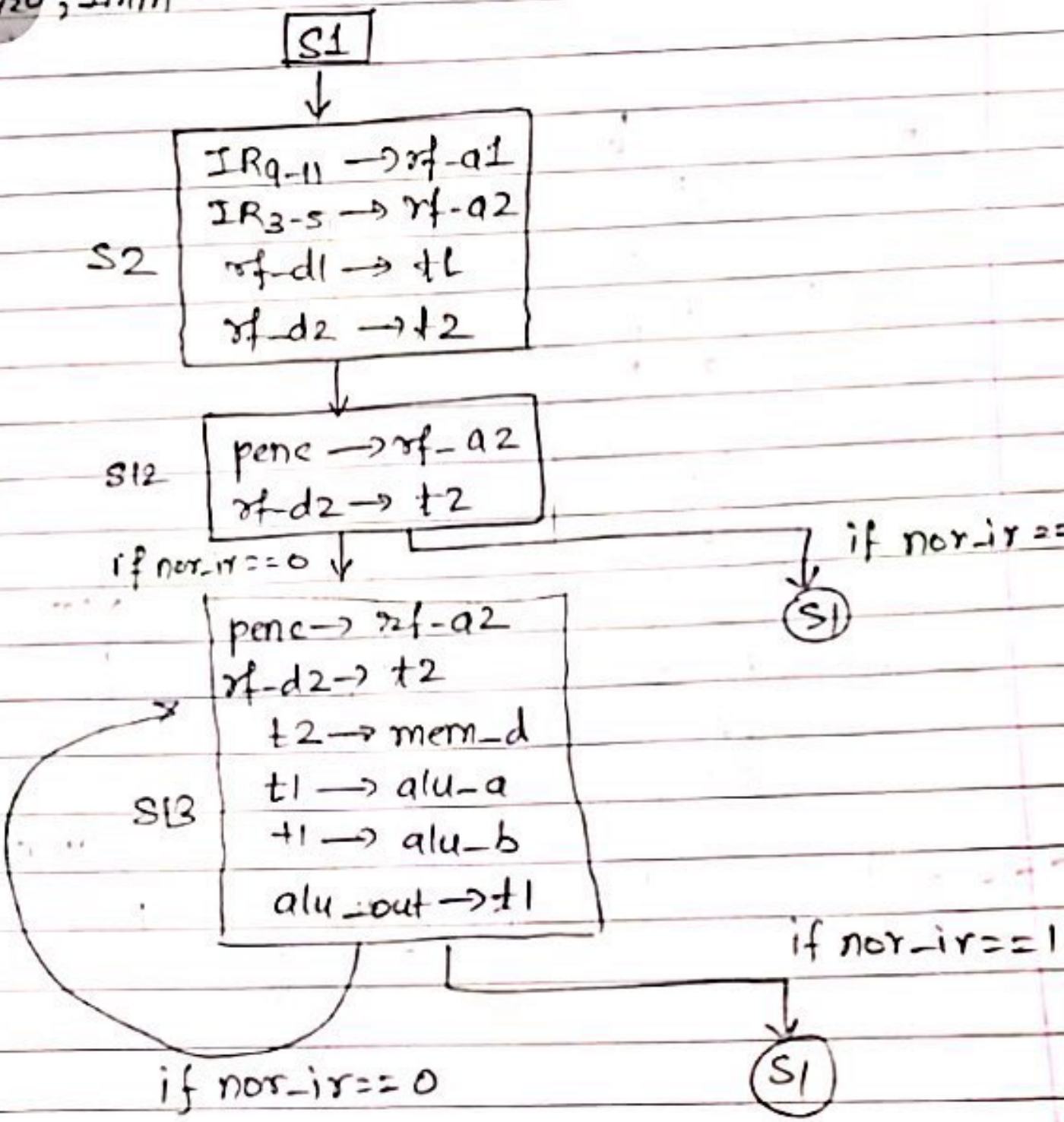
* LM Ra, IMM



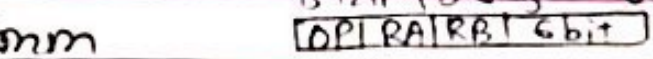
Ra → addr. of memory locat^n



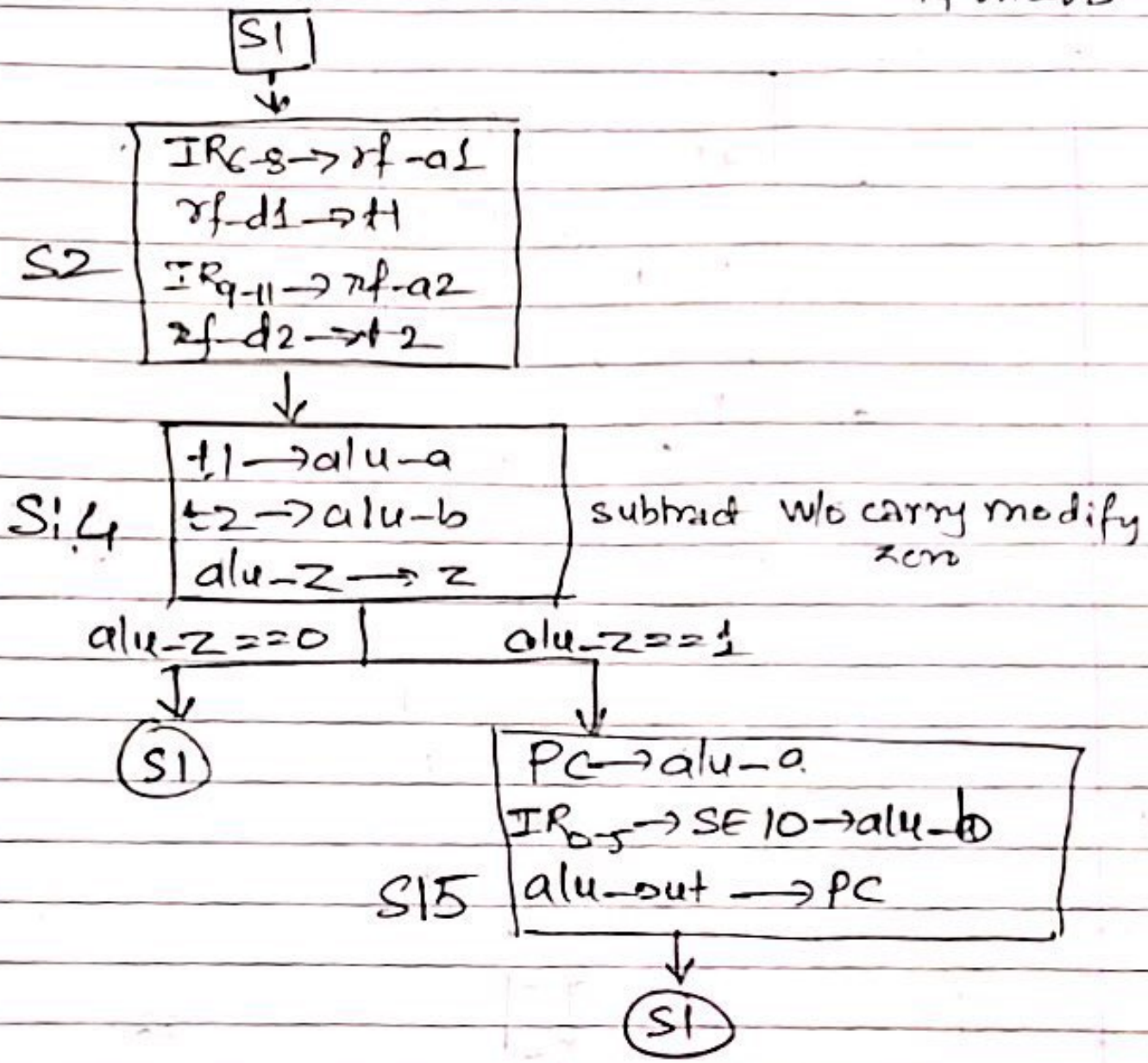
- SW1 r0, Imm



BEQ rA, rB, Imm



PC ← PC+1+imm if rA == rB

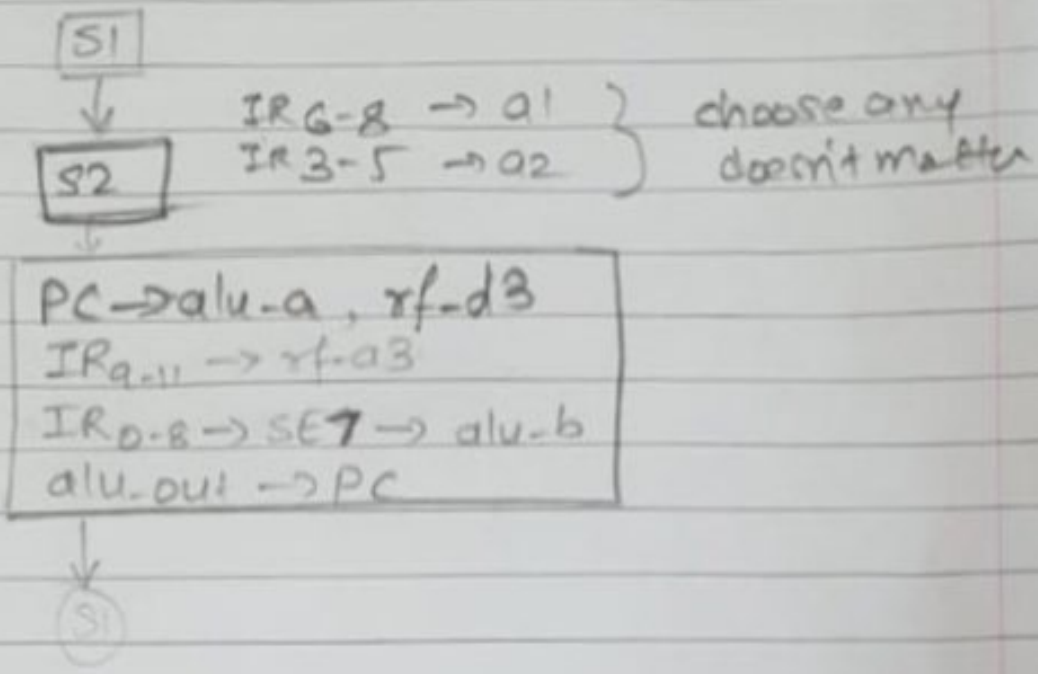


DATE / / PAGE

* JAL ra, imm

OP	RA	9bit

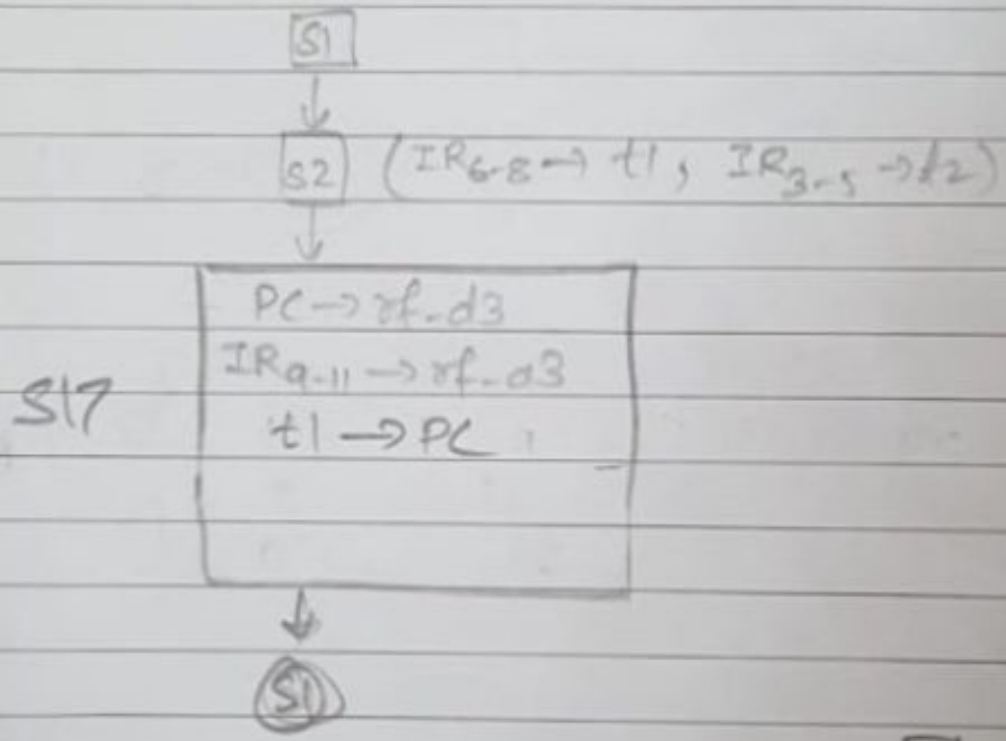
PC ← PC+1+Imm
rA ← PC+1

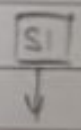


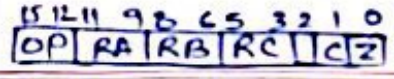
* JALR ra, rb.

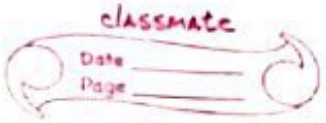
OP	RA	RB	000000

PC ← rb ; ra ← PC+1



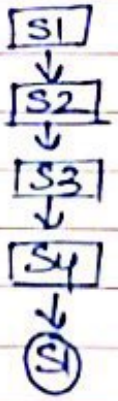






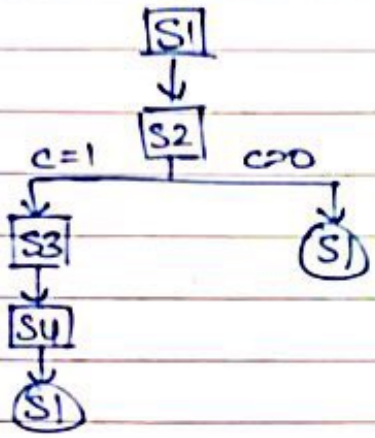
(15 ... 12) (1 0)

* ADD :



0000 00

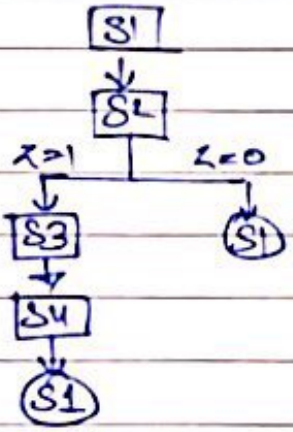
* ADC



(15... 12) (1 0)

0000 10

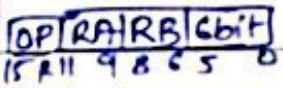
* ADZ



(15 .. 12) (1 0)

0000 01

* ADI



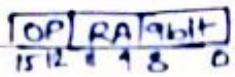
(15 .. 12)

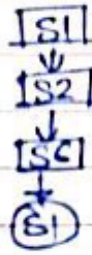
0001

(15 . . 12) (1 0)

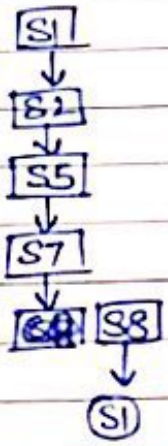
* NDU = ADD (change alu-signal) 0010 00
* NDC = ADC (—"—) 0010 10
* NDZ = ADZ (—"—) 0010 01

* LHI (15 . . 12) 0011



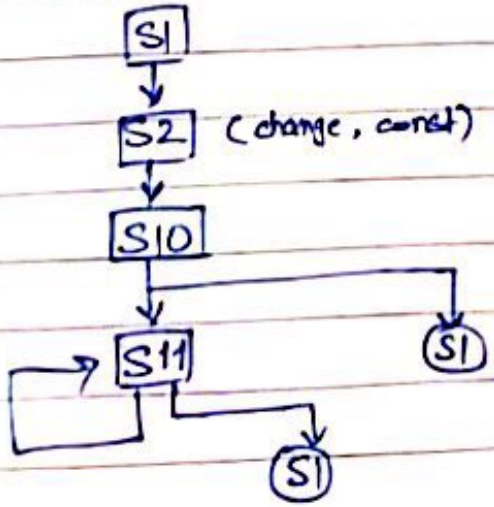


* LW (15 . . 12) 0100



* SW (15 . . 12) 0101

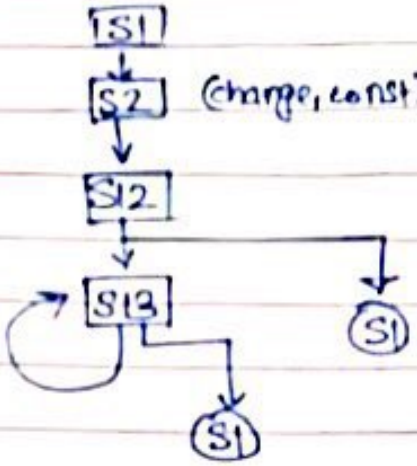
* LM (15 . . 12) 0110



(15..12)

* SM

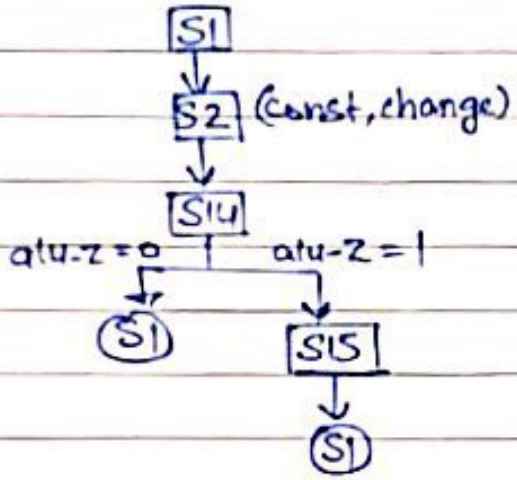
0111



(15..12)

* BEQ

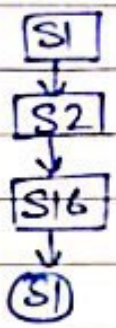
1100



(15..12)

* JAL

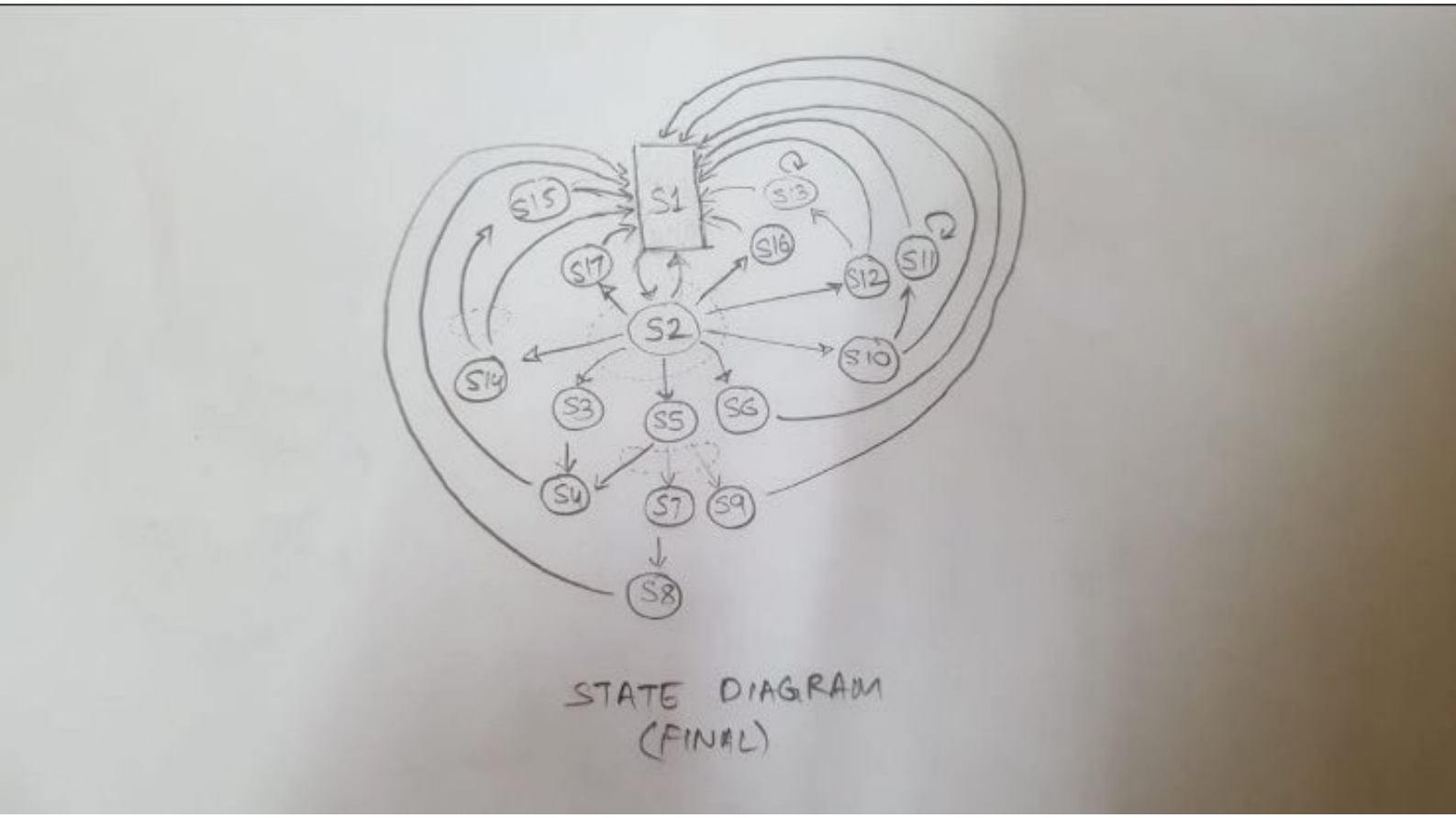
1000



(15..12)

* JALR

1001



STATE DIAGRAM
(FINAL)

t1

	t1_in0	t1_in1
alu_out → t1	0	1
rf_d1 → t1	1	0
none	0	0

	t1_oute	t1_out1
t1 → alu_a	0	1
t1 → rf_d3	1	0
t1 → mem_adua	1	1
none	0	0

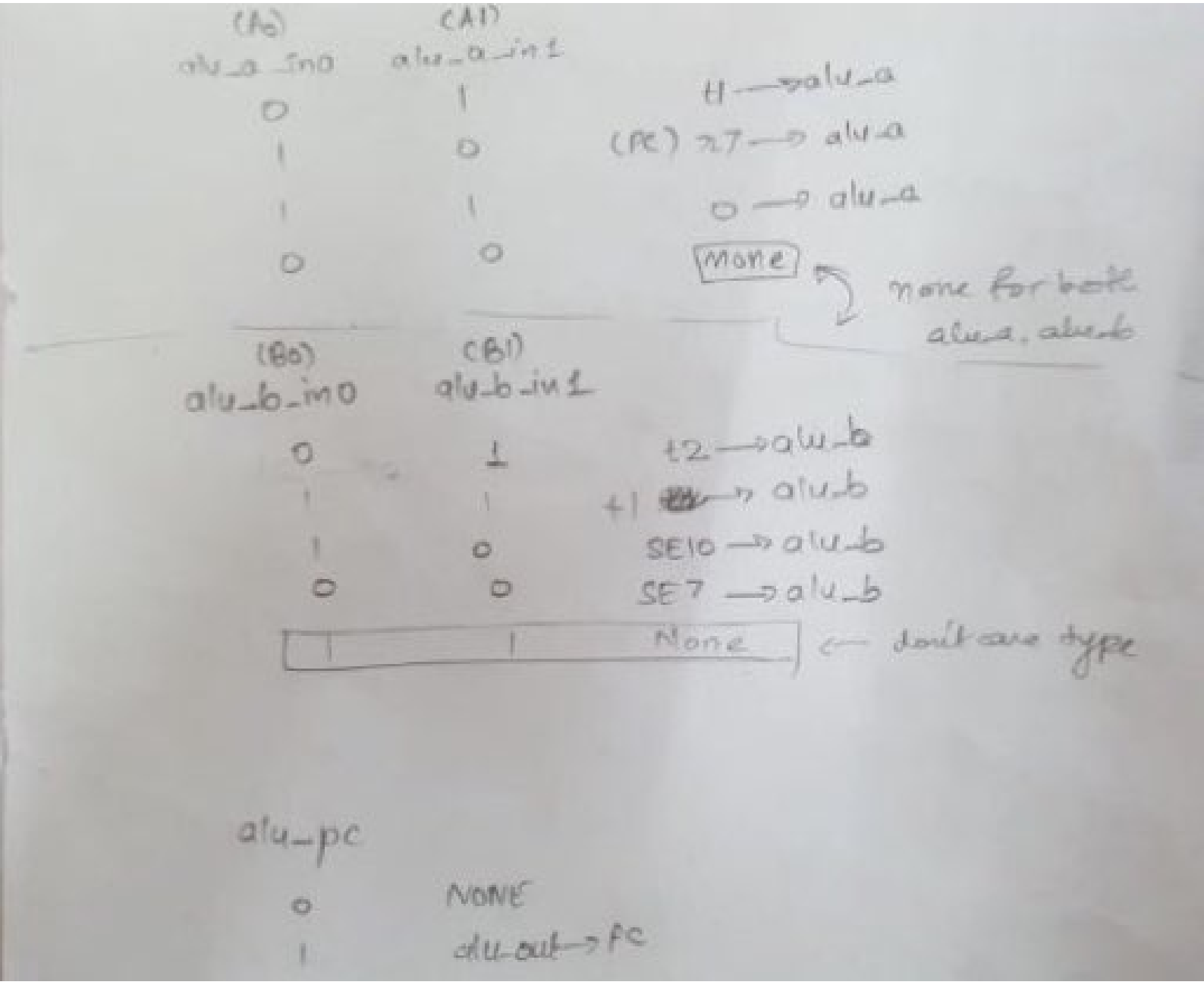
both always occur simultaneously

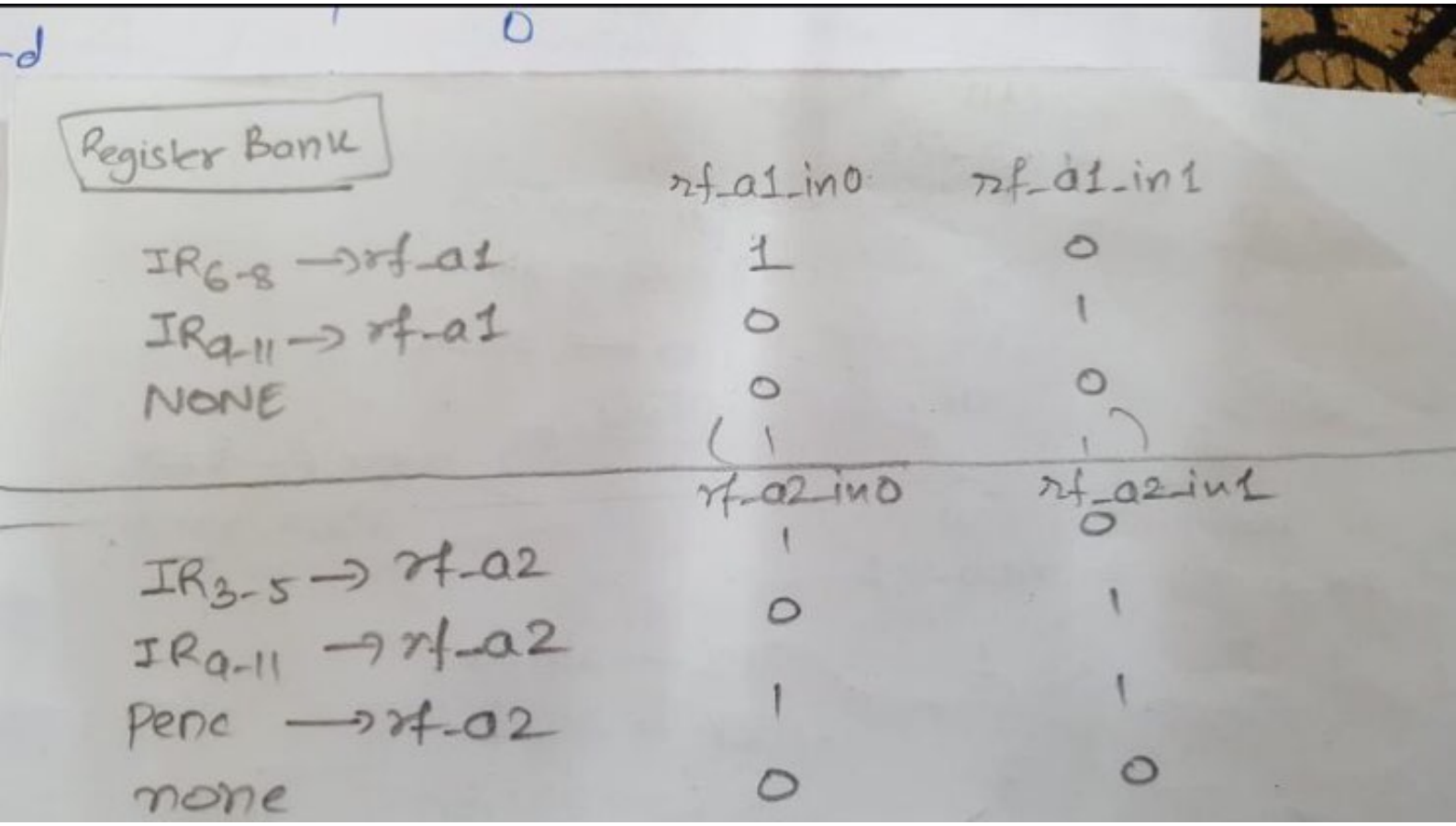
S3

(*) t2 :

	t2_in0	t2_in1
rf-d2 → t2	1	0
mem-d → t2	0	1
none	0	0

	t2_out0	t2_out1
t2 → alu_b	0	1
t2 → rf-d3	1	0
t2 → mem-d	1	1
none	0	0





alu_b

	0	1
	rf_WR	
OFF	0	
ON	1	

	rf_d3_in
PCinc	0
IR_{0-11}	1

	rf_d3_in0	rf_d3_in1
t1 → rf_d3	0	0
ZP10 → rf_d3	0	1
t2 → rf_d3	1	0
PC → rf_d3	1	1

S2 conditions:-

$IR_{6-8} \rightarrow a1$
$IR_{3-5} \rightarrow a2$
} ADD, ADC, ADZ, NDU, NDZ, NDC, ADI, LHI, LW, JAL, JALR

$IR_{6-8} \rightarrow a1$
$IR_{9-11} \rightarrow a2$
} SW, BEQ

$IR_{9-11} \rightarrow a1$
$IR_{3-5} \rightarrow a2$
} LM, SM

PC → mem_a ; alu_a ; alu_out → PC ---- x

PC → alu_a ; alu_out → PC ---- y

PC → alu_a ; rf_d3 ; alu_out → PC ---- z

PC → rf_d3 ; t1 → PC ---- w

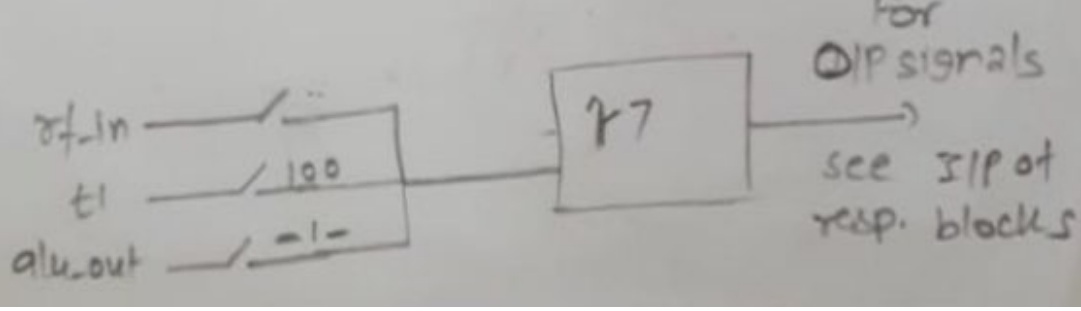
NONE

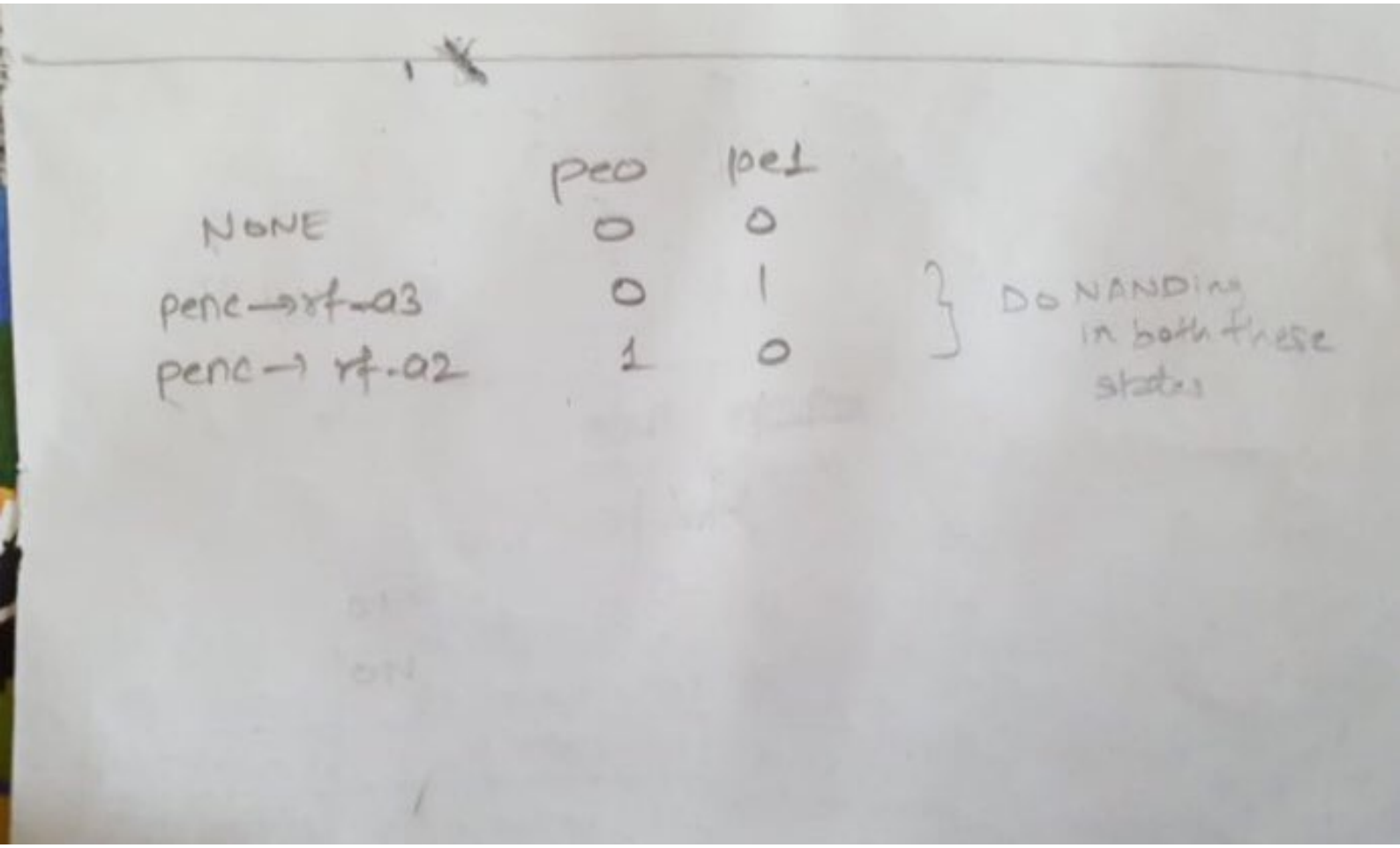
PC→rf_d3	pc→alu_a	,PC→mem_a	
0	0	0	none
1	0	0	w
1	1	0	z
0	1	0	y
0	1	1	x

pc_out0	pc_out1	pc_out2
0	0	0
1	0	0
1	1	0
0	1	0
0	1	1

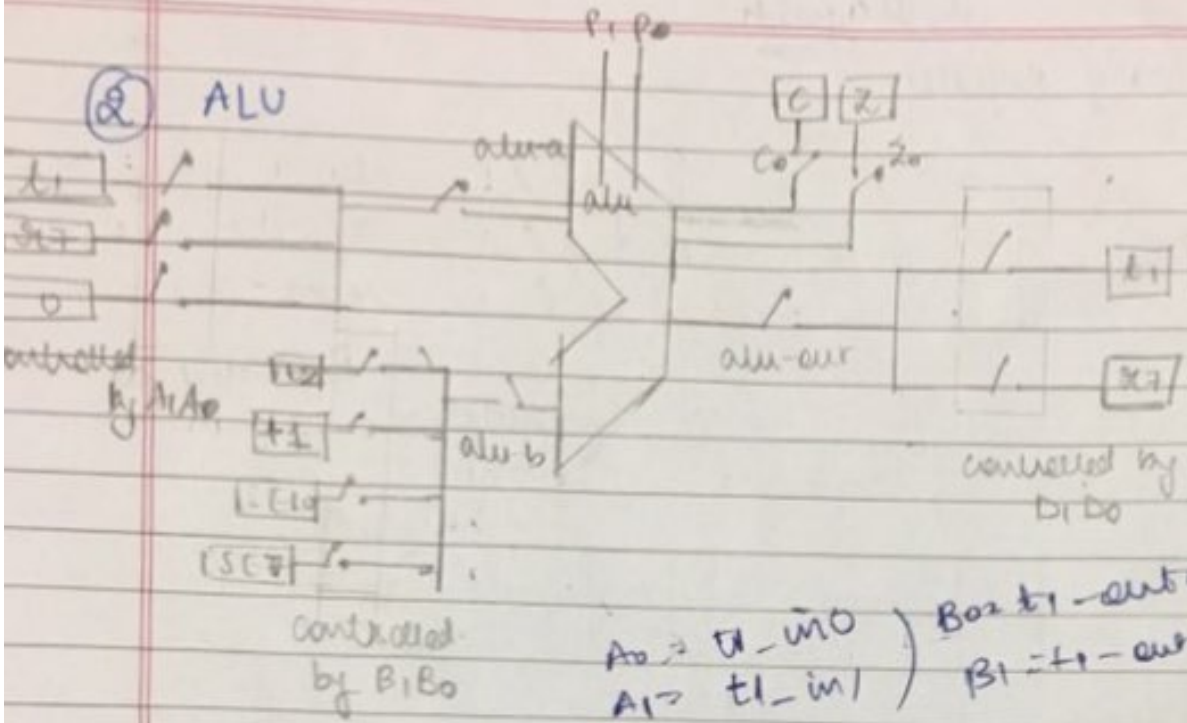
NONE

Pc→rf_d3	t1→Pc
pc→alu_a, rf_d3	alu_out→Pc
Pc→alu_a	alu_out→Pc
pc→mem_a, alu_a	alu_out→Pc





alu_ctl



(2) ALU

A0 → tl_in0
A1 → tl_in1
B0 → t1-out0
B1 → t1-out1

(i) t0 → alu-a (10) ≡ $A_1\bar{A}_0$
t7 → alu-a (01) ≡ $\bar{A}_1 A_0$
0 → alu-a (11) ≡ $A_1 A_0$
none (00) ≡ $\bar{A}_1 \bar{A}_0$ (alu1 alu0 / alu3 alu2)

(ii) t2 → alu-b (10) ≡ $B_1 \bar{B}_0$
+1 → alu-b (11) ≡ $B_1 B_0$
SE10 → alu-b (01) ≡ $\bar{B}_1 B_0$
SE7 → alu-b (00) ≡ $\bar{B}_1 \bar{B}_0$
none for alu-b is controlled by $\bar{A}_1, \bar{A}_0$

(iii) C, Z are controlled by C_0, Z_0 respectively.
$C_0 = 0$ (off)
1 (on)
$Z_0 = 0$ (off)
1 (on)

(iv) alu has 3 operations (controlled by $P_1 P_0$)
ADD (11) ≡ $P_1 P_0$
NAND (01) ≡ $\bar{P}_1 P_0$
SUBTRACT (10) ≡ $P_1 \bar{P}_0$

	alu_op0	alu_op1
Nand	1	0
Subtract	0	1
Add	1	1