

R-type

OP RF RA RB C2

3 2 0

Add rc, ra, rb

rc = ra + rb

Add
NDU

PC \rightarrow mem_a, alu_a
mem_d \rightarrow IR
+1 \rightarrow alu_b
alu_out \rightarrow PC

Here PC = r7

S1

S2

S3

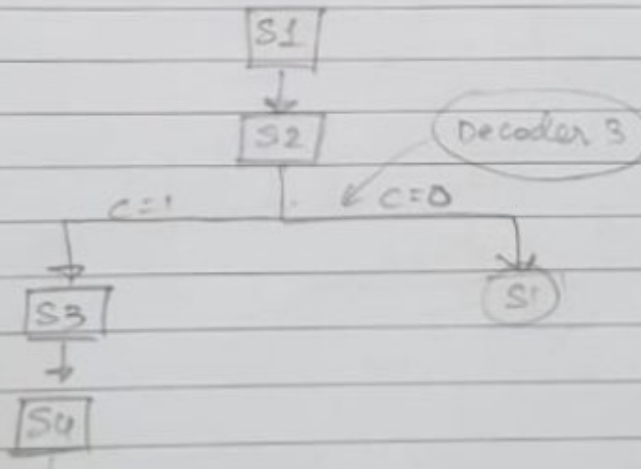
S4

IR₆₋₈ \rightarrow rf_a2
IR₃₋₅ \rightarrow rf_a2
rf_d1 \rightarrow t1
rf_d2 \rightarrow t2

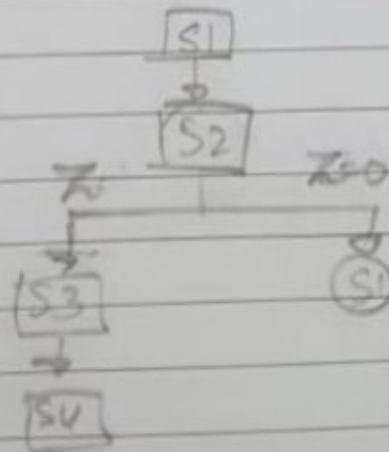
t1 \rightarrow alu_a
t2 \rightarrow alu_b
alu_out \rightarrow t1

t1 \rightarrow rf_d3
IR₉₋₁₁ \rightarrow rf_a3

* ADC rc, ra, rb; NDC rc, ra, rb



* AD2 rc, ra, rb; ND2 rc, ra, rb



I type

OP rb 10 | 6b | 15b | 2.55 0

DATE

PAGE

*

ADI

$rb = ra + SE(6b)$

S1

S2

IR₆₋₈ → rf.a1
rf.d1 → t1
(IR₃₋₅ → rf.a2)
rf.d2 → t2

Can do the same as S1 doesn't matter as t2 not used

t1 → alu.a
IR₀₋₅ → SE10 → alu.b
alu.out → t1

S5

t1 → rf.d3
IR₉₋₁₁ → rf.a3

S4

*

L111 RA₀ (4bit)

OP RA 4bit 0

RA = '9b14' 00000000

S1

S2

IR₆₋₈ → a1
IR₃₋₅ → a2

S6

IR₀₋₈ → ZP10 → rf.d3
IR_{ani} → rf.a3

S1

* LW rA, rB, Imm(6bit)

15	12	9	8	6	5	0
OP	RA	RB	6bit			

rA ← [rB + 6bit]

S1

IR₆₋₈ → rf_a1
 rf_d1 → t1
 IR₃₋₅ → rf_a2
 rf_d2 → t2

S2

t1 → alu_a
 IR₀₋₅ → SE10 → alu_b
 alu_out → t1

S5

t1 → mem_a
 mem_d → t2

S7

Affect
Zero
flag

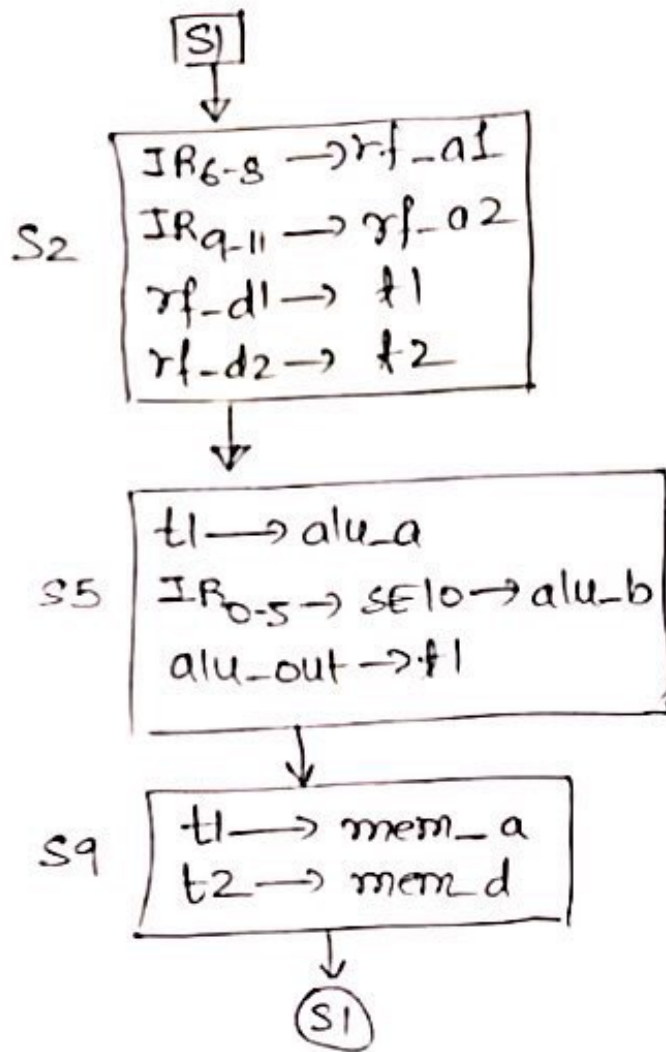
t2 → rf_d3, alu_b
 IR₉₋₁₁ → rf_a3
 t0 → alu_a

S8

S1

15 12 11 9 8 5 0

OP	RA	RB	6bit
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$$[2b+6bits] \leftarrow 2a$$


* LM 2a. IMM

15-12-11 4 9 7
OP RA IO PT ... RI RC

ra → addr. of memory locatⁿ

PC → mem_a, alu_a
mem_d → IR
+1 → alu_b
alu_out → PC

S1

IR₉₋₁₁ → rf_a1
IR₃₋₅ → rf_a2
rf_d1 → t1
rf_d2 → t2

S2

t1 → mem_a, alu_a
mem_d → t2
+1 → alu_b
alu_out → t1

S10

not_ir == 0

If not_ir == 1

(S1)

S11

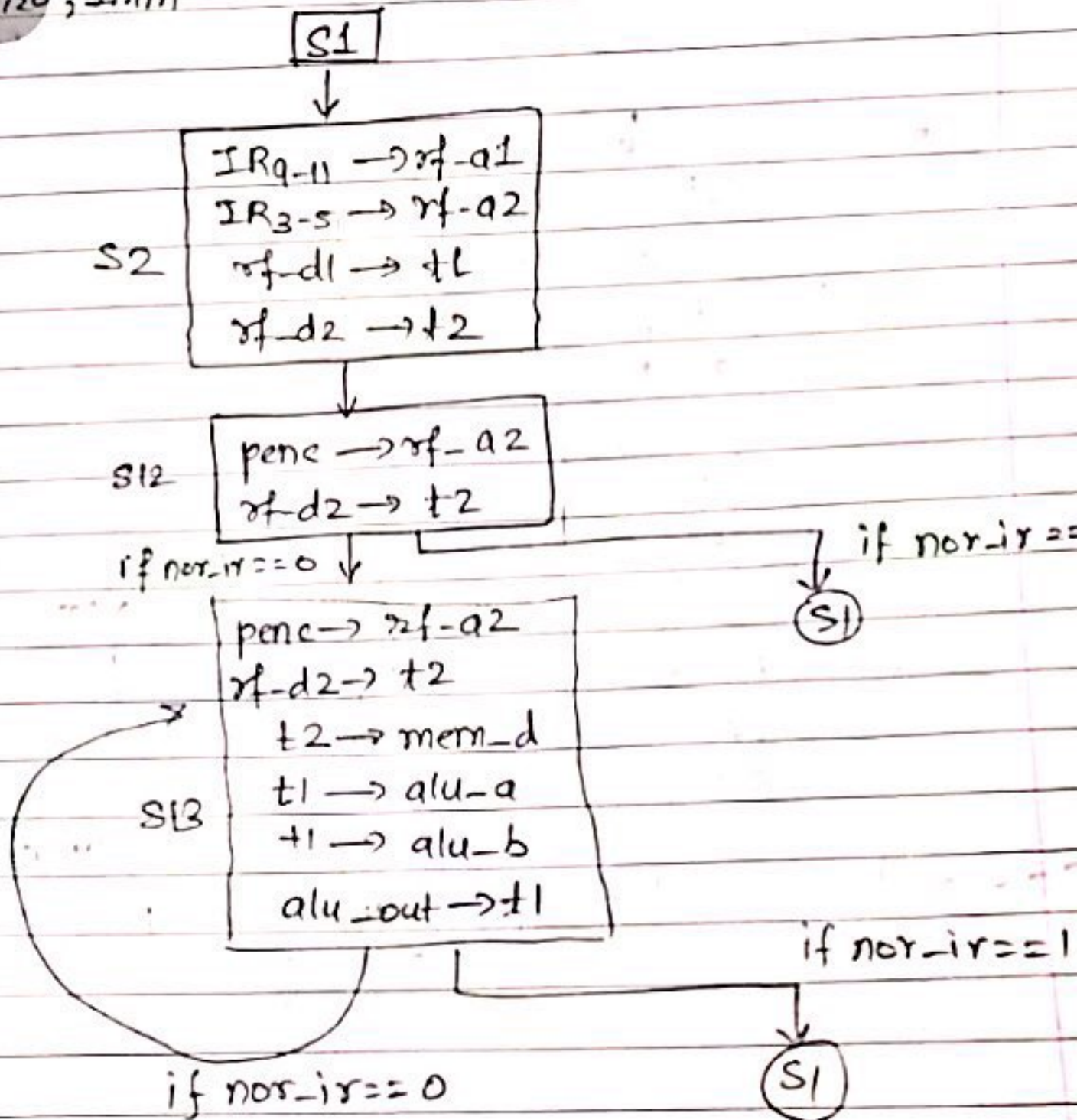
t2 → rf_d3
penc → rf_a3
t1 → mem_a, alu_a
mem_d → t2
+1 → alu_b
alu_out → t1

if not_ir == 0

if not_ir == 2

(S1)

Sr1 20, Imm



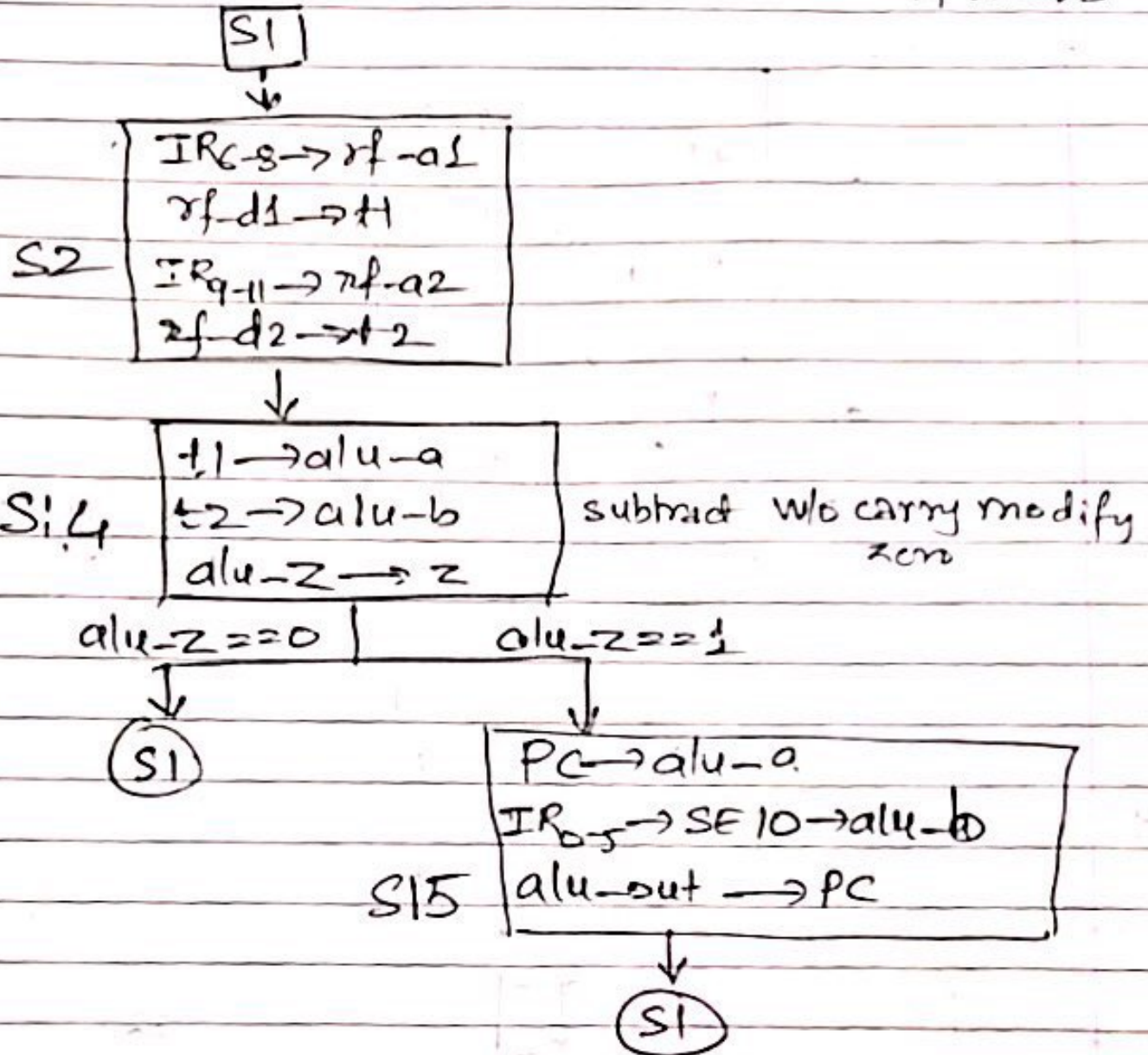
BEO rA, rB, Imm

15 14 11 9 8 5 0
OP RA RB C bit

DATE

PAGE

$PC \leftarrow PC + Imm$
if $rA == rB$

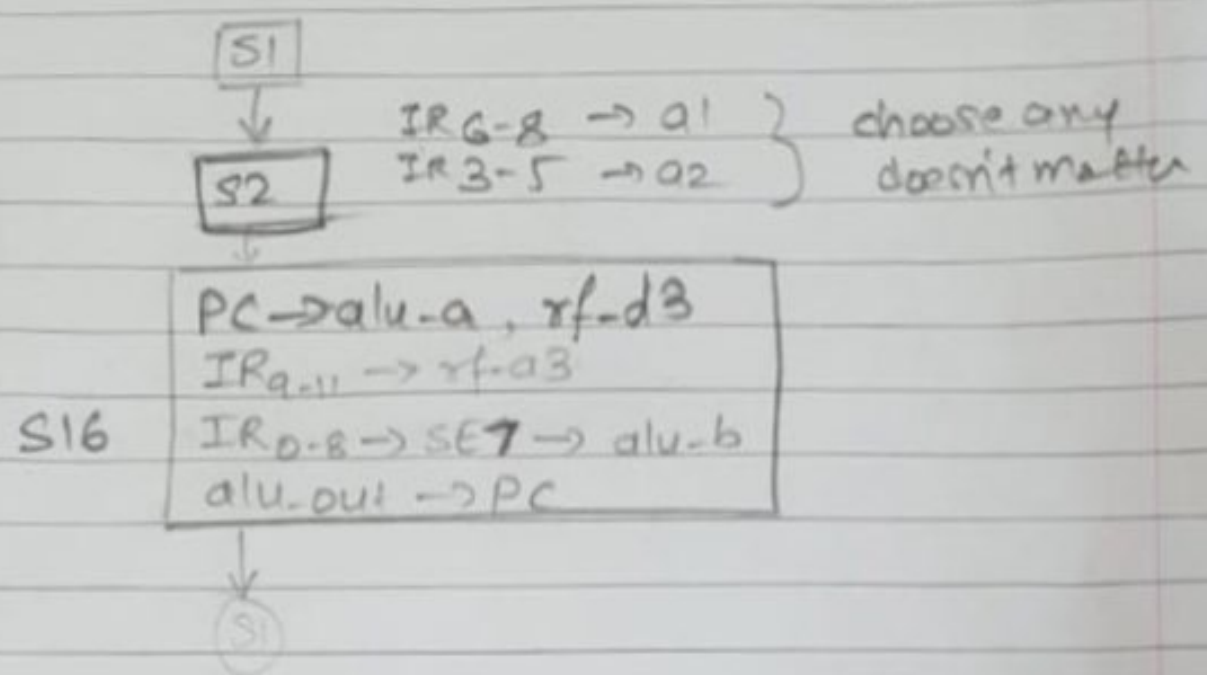


* JAL ra, imm

OP	RA	imm
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PC ← PC + 1 + imm
ra ← PC + 1

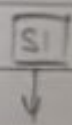
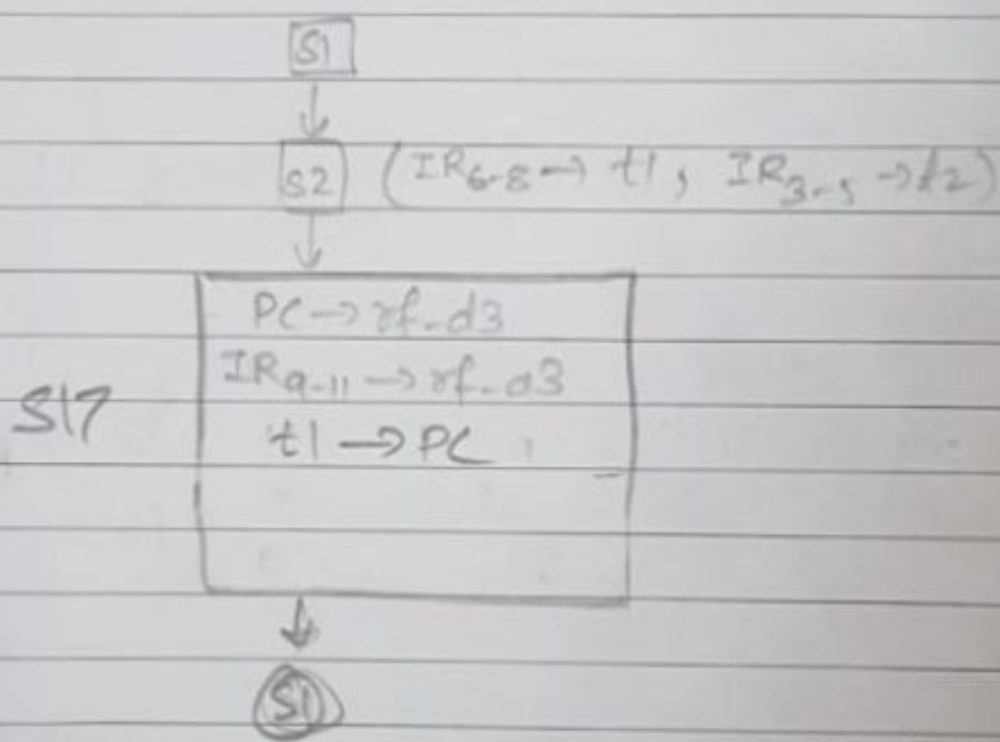
✓



* JALR ra, rb

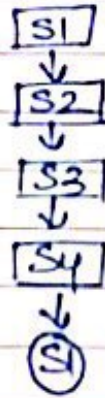
OP	RA	RB	imm
----	----	----	-----

PC ← rb ; ra ← PC + 1



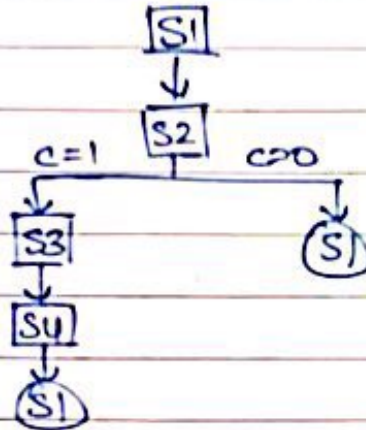
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
 OP RA RB RC C2

* ADD :



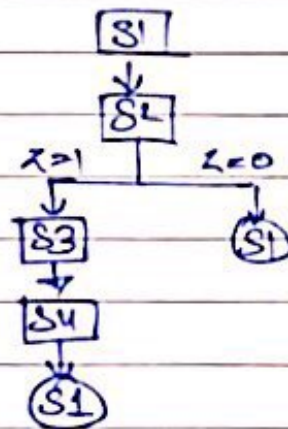
(15...12) (10)
 0000 00

* ADC



(15...12) (10)
 0000 10

* ADZ



(15...12) (10)
 0000 01

* AOI

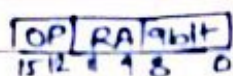
OP RA RB Cbit
 15 14 13 12 11 10 9 8 7 6 5 4



(15...12)
 0001

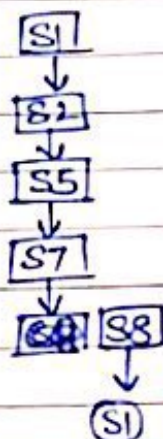
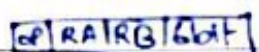
- * ~~LD~~ NDU = ADD (change alu-signal)
- * NDC = ADC (" ")
- * NDZ = ADZ (" ")
- * LHI

(15..12) (10)
0010 00
0010 10
0010 01
(15..12)
0011



* LW

(15..12)
0100



* SW

(15..12)
0101

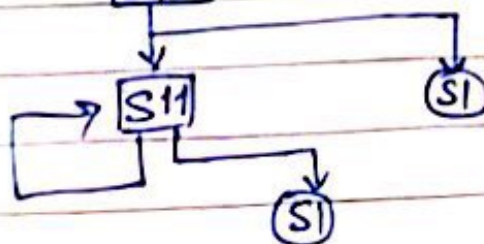


* LM

(15..12)
0110



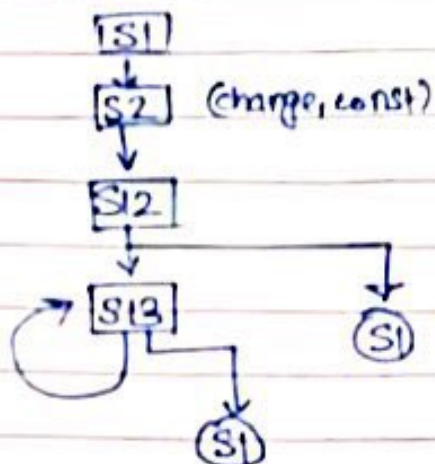
(change, const)



* SM

(15...12)

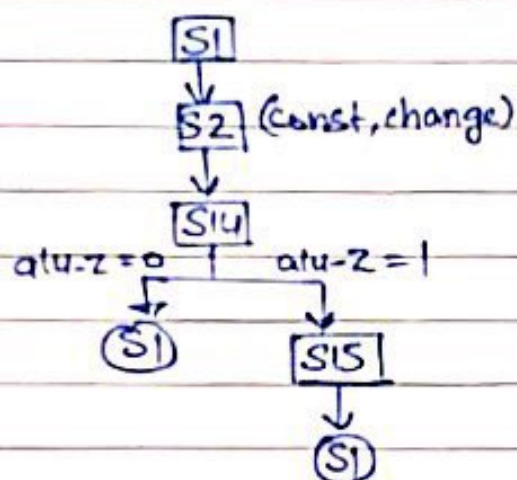
0111



* BEQ

(15...12)

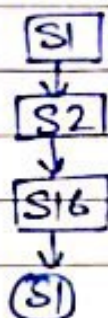
1100



* JAL

(15...12)

1000

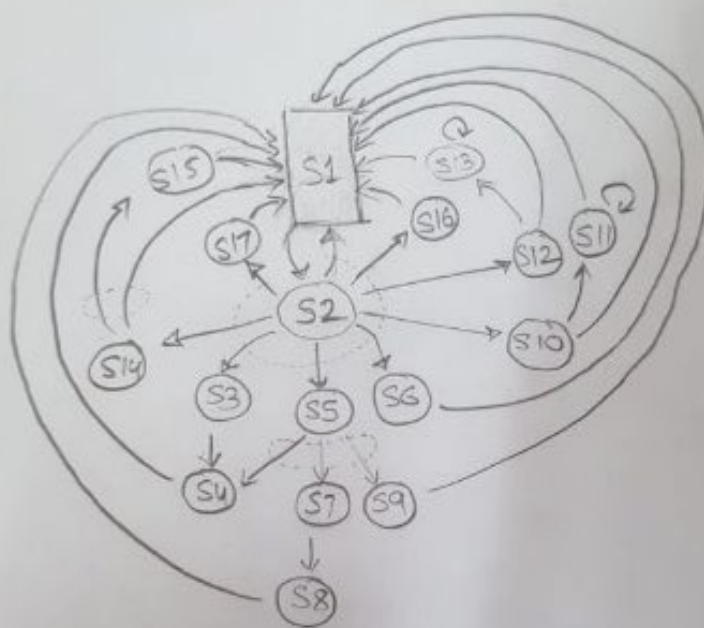


* JALR

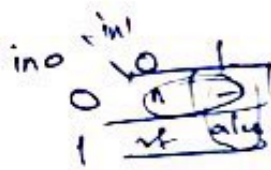
(15...12)

1001





STATE DIAGRAM
(FINAL)



* t1

	tl-ino	tl-inl
alu-out → t1	0	1
rf-d1 → t1	1	0
none	0	0

	tl-act0	tl-out1
t1 → alu-a	0	1
t1 → rf-d3	1	0
t1 → mem-a, alu-a	1	1
none	0	0

both always occur simultaneously

S3

(*) t2 :

rf-d2 → t2

mem-d → t2

none

t2-in0 t2-in1

1 0

0 1

0 0

~~t2-out0 t2-out1~~

t2-out0 t2-out1

0 1

1 0

1 1

0 0

t2 → alu-b

t2 → rf-d3

t2 → mem-d

none

(A0)
alu_a_in0
0
1
1
0

(A1)
alu_a_in1
1
0
1
0

H → alu_a
(PC) 27 → alu_a
0 → alu_a

None

none for both
alu_a, alu_b

(B0)
alu_b_in0
0
1
1
0

(B1)
alu_b_in1
1
1
0
0

t2 → alu_b
+1 ~~alu~~ → alu_b
SE10 → alu_b
SE7 → alu_b

None

don't care type

alu_pc

0

NONE

1

alu_out → pc

Register Bank

IR₆₋₈ → rf-a1

IR₉₋₁₁ → rf-a1

NONE

rf-a1-in0

1

0

0

(1

rf-a1-in1

0

1

0

1)

rf-a2-in0

1

0

1

0

rf-a2-in1

0

1

1

0

IR₃₋₅ → rf-a2

IR₉₋₁₁ → rf-a2

Penc → rf-a2

none

data-bus

0

1

rf-WR

OFF
ON

0
1

rf.d3.in

pend

0

IR₉₋₁₁

1

rf.d3.in0

rf.d3.in1

t1 → rf.d3

0

0

zp10 → rf.d3

0

1

t2 → rf.d3

1

0

PC → rf.d3

1

1

S2 conditions:-

IR₆₋₈ → a1 } ADD, ADC, AD2, NDU, NDZ, NDC, ADI, LHI,
IR₃₋₅ → a2 } LW, JAL, JALR

IR₆₋₈ → a1 } SW, BEQ
IR₉₋₁₁ → a2 }

IR₉₋₁₁ → a1 } LM, SM
IR₃₋₅ → a2 }

PC \rightarrow mem-a, alu-a, alu-out \rightarrow PC x

PC \rightarrow alu-a, alu-out \rightarrow PC y

PC \rightarrow alu-a, rf-d3 ; alu-out \rightarrow PC z

PC \rightarrow rf-d3 ; t1 \rightarrow PC w

NONE

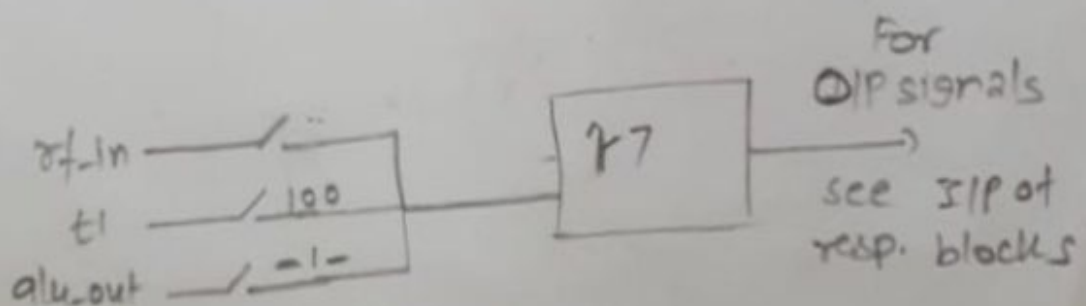
PC \rightarrow rf-d3, pc \rightarrow alu-a, pc \rightarrow mem-a			
0	0	0	none
1	0	0	w
1	1	0	z
0	1	0	y
0	1	1	x

pc-out0 pc-out1 pc-out2

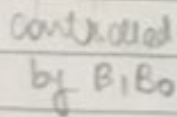
0	0	0
1	0	0
1	1	0
0	1	0
0	1	1

NONE

PC \rightarrow rf-d3	t1 \rightarrow PC
PC \rightarrow alu-a, rf-d3	alu-out \rightarrow PC
PC \rightarrow alu-a	alu-out \rightarrow PC
PC \rightarrow mem-a, alu-a	alu-out \rightarrow PC



	peo	pet	
NONE	0	0	
perc → rf-a3	0	1	} Do NANDing in both these states
perc → rf-a2	1	0	



$A_0 \rightarrow t_1 - m_0$
 $A_1 \rightarrow t_1 - m_1$

Box 1 - auto
B1 - 1 - auto

- (i) $t_1 \rightarrow a_{lu} - a(10) \equiv \bar{A}_1 \bar{A}_0$
 $t_2 \rightarrow a_{lu} - a(01) \equiv \bar{A}_1 A_0$
 $0 \rightarrow a_{lu} - a(11) \equiv A_1 A_0$
 none (00) $\equiv \bar{A}_1 \bar{A}_0$ (also $a_{lu1} a_{lu0}$ and $a_{lu3} a_{lu2}$)

- (iv) Also has 3 operations
(controlled by P_1P_0)
ADD (11) $\equiv \overline{P_1}P_0$
NAND (01) $\equiv P_1\overline{P_0}$
SUBTRACT (10) $\equiv P_1P_0$

- (ii)
- $$\begin{aligned} t_2 &\rightarrow \text{alut-b}(10) \equiv B_1 B_0 \\ +1 &\rightarrow \text{alut-b}(01) \equiv B_1 B_0 \\ SE10 &\rightarrow \text{alut-b}(01) \equiv \overline{B_1} B_0 \\ SE7 &\rightarrow \text{alut-b}(00) \equiv \overline{B_1} \overline{B_0} \end{aligned}$$

Gene for albinism is controlled by \bar{A}_1, \bar{A}_0

- (iii) C_0, Z_0 are controlled by C_0, Z_0 respectively.
- $C_0 = 0$ (off)
1 (on)
- $Z_0 = 0$ (off)
1 (on)

Nand	1	0
Subtract	0	1
Add	1	1