Low Voltage Low Power Sub-threshold Operational Amplifier in 180nm CMOS

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***Abstract*—A two-stage operational amplifier for biomedical applications is presented in this paper. In the Op-Amp design, all transistors have been operated in sub-threshold region for low voltage low power application. The proposed Op-Amp has been designed based on TSMC foundry 180nm process and simulated in Cadence analog design environment. The proposed circuit generates a 40dB gain, 114 KHz UGBW, 72 deg phase margin & total power consumption is just 112nW with 0.8V battery.**

Keywords—Operational Amplifier; Sub-threshold; Low Power; Analog IC design; Biomedical

I. INTRODUCTION

The implantable devices in biomedical application such as pacemaker & monitoring of Neuro-muscular activities etc require biomedical sensors with very low power consumption so that implanted battery can work for more numbers of years. For reducing power consumption in the operational amplifier, we will operate MOSFETs at low supply voltage and low current. The current consumption & characteristics of a MOSFET varies with respect to its operating region. Among these different regions sub-threshold region is used for ultra low power circuit designing. Sub-threshold biased MOSFET can operate with lower voltage power supply. It is generally assumed that the current through the MOSFET is zero when gate voltage drops below threshold voltage, but in fact it decreases exponentially. And if a MOSFET is operated with the gate voltage just below threshold voltage i.e. in sub-threshold or weak inversion region, the power consumption is reduced[2]. The biomedical signals are low frequency signals with frequency less than few kilohertz. Also biomedical signals are very weak signals order of a few microvolts. The biomedical signals are slow & does not require very high slew rate[1]. These requirements can be met with operational amplifier operating in sub-threshold region.

II. SUB-THRESHOLD OPERATED MOSFET

The different operating regions of MOSFET are shown in fig 1. The MOSFET will operate in sub-threshold or weak inversion region for $V_{gs} < V_{TH}$ & V_{ds} approximately greater than 4* KT/q . The current of MOSFET in the sub-threshold region is a diffusion current[3-5].

$$I_d = I_o \frac{W}{L} exp\left(q \frac{V_{gs} - V_{th}}{nkT}\right)\left[1 - e^{-\frac{V_{ds}}{V_T}}\right]$$

Where W= gate width, L = gate length, V_{gs} = applied gate to source voltage, V_{th}= Threshold voltage of the MOSFET,V_T = kT/q=26mv (at room temperature), n=non ideality factor (≈1.53 for PMOS ≈1.48 for NMOS), I_0 is a process parameter.

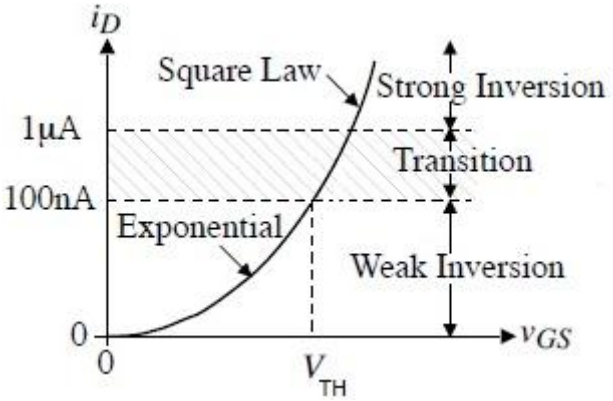

Fig 1: Different operating regions of MOSFET

Normally $e^{-\frac{V_{ds}}{V_T}} << 1$

This diffusion current is given by:

$$I_d = I_o \frac{W}{L} \exp\left(q \frac{V_{gs} - V_{th}}{nkT}\right)$$

The current of MOSFET varies exponentially similar to current of a BJT. Therefore the MOSFET behaves similar to BJT in the sub-threshold region.

In sub-threshold region, the trans-conductance and drain resistance are given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \frac{I_d}{nV_T}$$

Where $V_T = \frac{nKT}{q}$

$$r_d = \frac{\partial I_d}{\partial V_{ds}} = \frac{1}{\lambda_D I_D}$$

Where, λ_D is the DIBM coefficient.

978-1-5090-4929-5

III. SUBTHRESHOLD OPERATIONAL AMPLIFIER

The first stage of the op amp is a differential amplifier. The input of first stage has been implemented using NMOS pair. The load is implemented using PMOS current mirror. This combination of NMOS input transistors with PMOS current mirror load provides high gain because trans-conductance of NMOS transistor is higher compared to PMOS. For output stage a common source amplifiers has been used which provides higher gain as well as higher output voltage swing. A complete schematic of op amp is shown in figure 2.

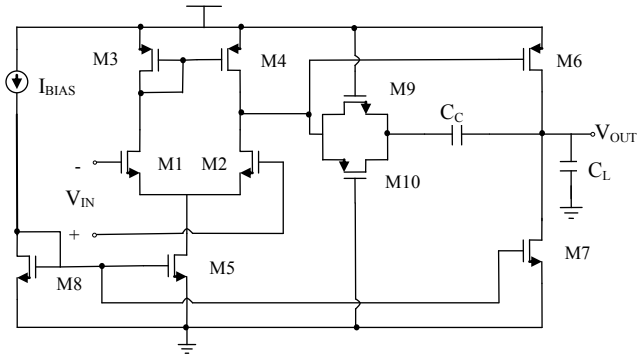

Fig 2: Two stage Sub-threshold Operational Amplifier

$$A_v = g_{m2}\, g_{m6} \left(\frac{r_{02}\, r_{04}}{r_{02} + r_{04}}\right)\left(\frac{r_{06} r_{07}}{r_{06} + r_{07}}\right)$$

$$= \frac{1}{n_2 n_6 \left(\frac{kT}{q}\right)^2 (\lambda_2+\lambda_4)(\lambda_6+\lambda_7)}$$

Gain bandwidth product

$$GB = \frac{I_{D1}}{\left(n_1 \frac{kT}{q}\right) C_c}$$

Slew rate

$$SR = \frac{I_{D5}}{C_c}$$

Resistance of NMOS M9 in parallel with PMOS M10 used as variable resistor shall be

$$R_{M9} \parallel R_{M10} = \frac{1}{g_{m6}} \left(\frac{C_L + C_c}{C_c}\right)$$

For reducing effect of right hand plane zero, a nulling resistor R_Z along with Compensation capacitor Cc is used. The nulling resistor has been implemented using a transmission gate (TG). The gate of NMOS transistor is connected to VDD while gate of PMOS transistor M10 is biased at VSS. The resistance of PMOS in deep triode region is given by

$$R_{op} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (|V_{GS}| - |V_{Thp}|)}$$

The resistance of NMOS in deep triode region

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Thn})}$$

The nulling resistor is implemented using transmission gate for increasing input signal dynamic range.

IV. SIMULATION RESULTS

The sub-threshold operational amplifier circuit given in Fig. 2 has been simulated using TSMC 180nm CMOS process library and Cadence Analog Design Environment. The power supply of +0.8V is used for biasing operational amplifier. The capacitor of 0.5pF is used as load at the output for simulation.

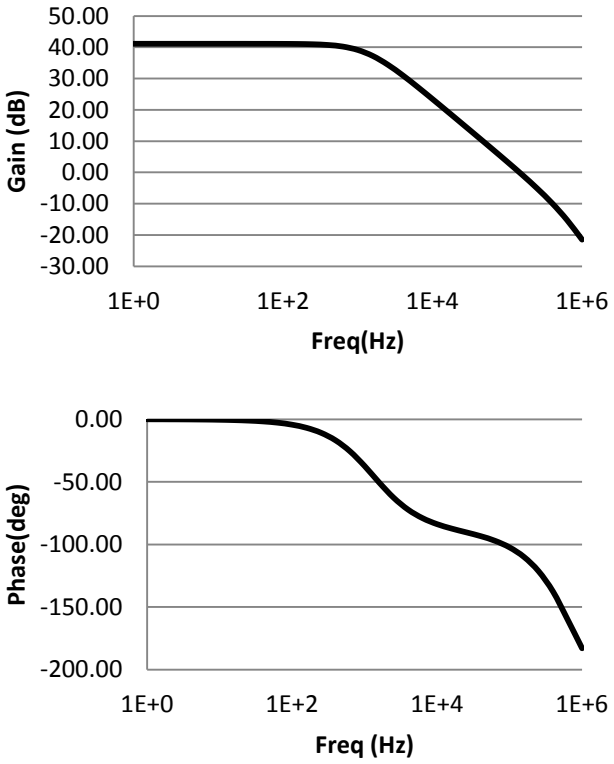

Fig 3: Gain and Phase plot of op amp with frequency

Figure 3 shows the frequency response of op amp. The result shows small-signal voltage gain which is 40 dB and phase margin of 72°. It can also be seen that the unity gain bandwidth (UGB) of op amp is 114 KHz.

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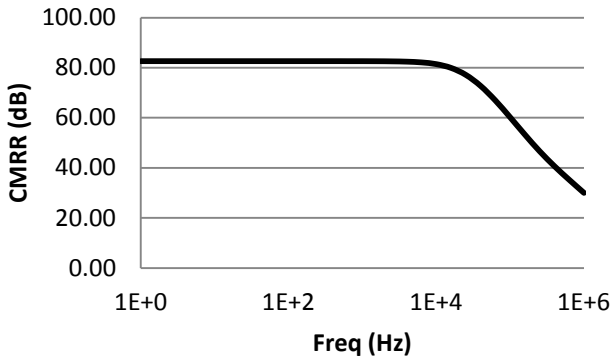

Fig 4: CMRR of OP AMP with Frequency

The operational amplifier was simulated using differential-mode and common mode inputs. The ratio of differential mode and common mode gain provides the CMRR of 80 dB. This implies that op amp has a very good rejection to the common-mode noise.

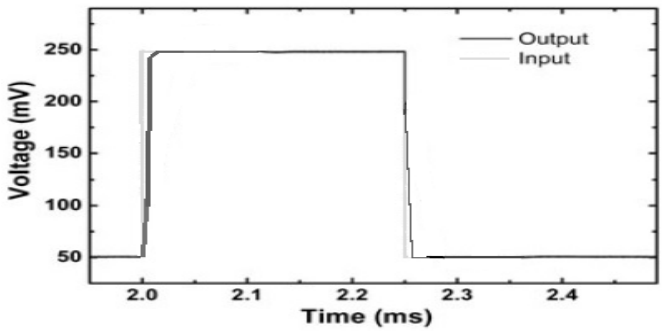

Fig 5: Slew rate of Operational Amplifier

Using transient analysis, the change between the output-voltage with respect to time is obtained for calculating the slew rate. The slope of output-voltage with respect to time calculated as 5V/msec.

The OP amp consumes 140nA current at power of 0.8V. The total power consumption is 112nW which is quite low.

The simulated results of OP Amp are summarized in table below

Parameters	Simulated results
Supply Voltage	0.8V
Current Consumption	140nA
Power Consumption	112nW
DC Gain	40dB
Unity gain BW	114KHz
CMRR	80dB
PSRR	50dB
Slew Rate	5V/msec
Phase Margin	72 Deg
Chip Area	0.009mm^2
Process	180nm CMOS

V. LAYOUT

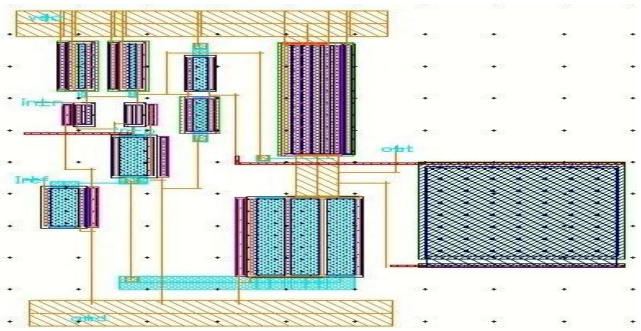

Fig 6: Layout of Sub-threshold Operational Amplifier

The layout of Sub-threshold OP AMP is shown in fig 6. The DRC and LVS check on layout were successfully completed. Post layout simulation after Parasitic extraction provides approximately same results. The chip area required for the layout is approximately 0.009mm^2.

VI. CONCLUSION

In this paper, we presented design of a two-stage operational amplifier for low voltage and low power systems using 180nm CMOS technology. The designed circuit has been validated using professional software of Cadence. This OP AMP provides 40dB gain, 72 degree phase margin, 80dB CMRR & consumes just 112nW making it fit for biomedical systems such as cardiac pacemaker, electrocardiogram (ECG) etc. where there is no requirement of high bandwidth and slew rate.

ACKNOWLEDGMENT

Authors would like to give special thanks to faculty members of VLSI department of CDAC NOIDA for their support & encouragement. Authors are thankful to the director & Scientists/ Engineers of Semiconductor Laboratory (ISRO) Mohali, India for their expert guidance.

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978-1-5090-4929-5