# CSCI 6461: Computer System Architecture – Homework 4

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### 3.14.a)

To find: execution time per element of result vector, unscheduled and scheduled

| Without Scheduling | | Clock Cycle Issued |
|---|---|---|
| addi | x4, x1, #800 | 1 |
| fld | f2, 0(x1) | 2 |
| | stall | 3 |
| fmul.d | f4, f2, f0 | 4 |
| fld | f6, 0(x2) | 5 |
| | stall | 6 |
| | stall | |
| | stall | |
| | stall | |
| fadd.d | f6, f4, f6 | 7 |
| | stall | 8 |
| | stall | 9 |
| | stall | 10 |
| fsd | f6, 0(x2) | 11 |
| addi | x1, x1, #8 | 12 |
| addi | x2, x2, #8 | 13 |
| sltu | x3, x1, x4 | 14 |
| | stall | 15 |
| bnez | x3, foo | 16 |
| | stall | 17 |

| With Scheduling | | Clock Cycle Issued |
|---|---|---|
| addi | x4, x1, #800 | 1 |
| fld | f2, 0(x1) | 2 |
| fld | f6, 0(x2) | 3 |
| fmul.d | f4, f2, f0 | 4 |
| addi | x1, x1, #8 | 5 |
| addi | x2, x2, #8 | 6 |
| sltu | x3, x1, x4 | |
| | stall | |
| | stall | |
| fadd.d | f6, f4, f6 | 7 |
| | stall | 8 |
| | stall | 9 |
| bnez | x3, foo | 10 |
| fsd | f6, -8(x2) | 11 |

From the above table at the left, we can see that without any scheduling the execution time per element of result vector is 16 cycles per element. Whereas, with scheduling, the execution time per element of result vector is only 10 clock cycles per element.

i.e. with scheduling, the complier's execution time is $\frac{16-10}{10} = \frac{6}{10} = 0.6 = 60\%$ faster than one without scheduling. Therefore, processor hardware alone must have **60%** faster clock to match the performance improvement achieved by the scheduling compiler.

3.14.b)

To find: execution time per element and number of times must the loop be unrolled

| With Scheduling | | Clock Cycle Issued |
|---|---|---|
| addi | x4, x1, #800 | 1 |
| fld | f2, 0(x1) | 2 |
| fld | f6, 0(x2) | 3 |
| fmul.d | f4, f2, f0 | 4 |
| fld | f2, 8(x1) | 5 |
| fld | f10, 8(x2) | 6 |
| fmul.d | f8, f2, f0 | 7 |
| fld | f2, 8(x1) | 8 |
| fld | f14, 8(x2) | 9 |
| fmul.d | f12, f2, f0 | 10 |
| fadd.d | f6, f4, f6 | 11 |
| addi | x1, x1, #24 | 12 |
| fadd.d | f10, f8, f10 | 13 |
| addi | x2, x2, #24 | 14 |
| sltu | x3, x1, x4 | 15 |
| fadd.d | f14, f12, f14 | 16 |
| fsd | f6, -24(x2) | 17 |
| fsd | f10, -16(x2) | 18 |
| bnez | x3, foo | 19 |
| fsd | f14, -8(x2) | 20 |

From the above table, we can see that, in order to schedule it without any stalls, we need to unroll **three times**. Also, the execution time per element of the result is 19 clock cycles.