CSCI 6461: Computer System Architecture – Homework 2

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Case Study 3: Studying the Impact of Various Memory System Organizations

2.36)

To find: independent memory channels

Given:

Core: 8

Workload in CPI: 2.0

CMP: 3GHz

L2 cache line size: 32 bytes

Workload incurs L2 misses: 6.67 per 1k instruction

System uses DDR2-667 DIMMs

Instructions per second = $\frac{8\ cores * 3\ GHz}{2.0\ CMP} = \frac{8*3*10^9}{2}$ = $12 * 10^9$

L2 misses per second = $\frac{6.67}{1000} * 12 * 10^9$ = $80.04 * 10^6$

For 32 bytes L2 cache line size, it would be $80.04 * 10^6 * 32 = 2561.28 * 10^6 \frac{bytes}{sec}$ = 2561.28 MB/s

As mentioned, that memory bandwidth is sometimes required twice than average, therefore, it would be 2561.28 * 2 = 5122.56 MB/s, which is within DDR2-667 DIMMs bandwidth. Hence, we can say that only one memory channel is required.

2.38.a)

It is given that both DRAM's; 2 GB of memory using either 8-bank 2 Gb x8 DDR2 DRAMs or 8-bank 1 Gb x8 DRAMs have same speed, page size, and cache line size. But the system with 1 Gb DRAMs will have double banks as compared with the system with 2 Gb DRAMs. Hence, we can conclude that as system with 1 Gb DRAMs can have a greater number of banks simultaneously open, it might have better performance than 2 Gb DRAMs system.

2.38.b)

The page activated system on both x4 and x8 part is similar and approximately takes same activation energy. Also, both the x8 DDR2 DRAMs system and x4 DDR2 DRAMs system require same power to drive the output lines, but x4 DDR2 DRAMs system require activating banks on 18 DRAMs, whereas x8 DDR2 DRAMs system require only 9 DRAMs. Hence, we can conclude that system with x8 parts would require less power as less DRAMs are being activated as compared to x4 parts.