

REPORT LAB6

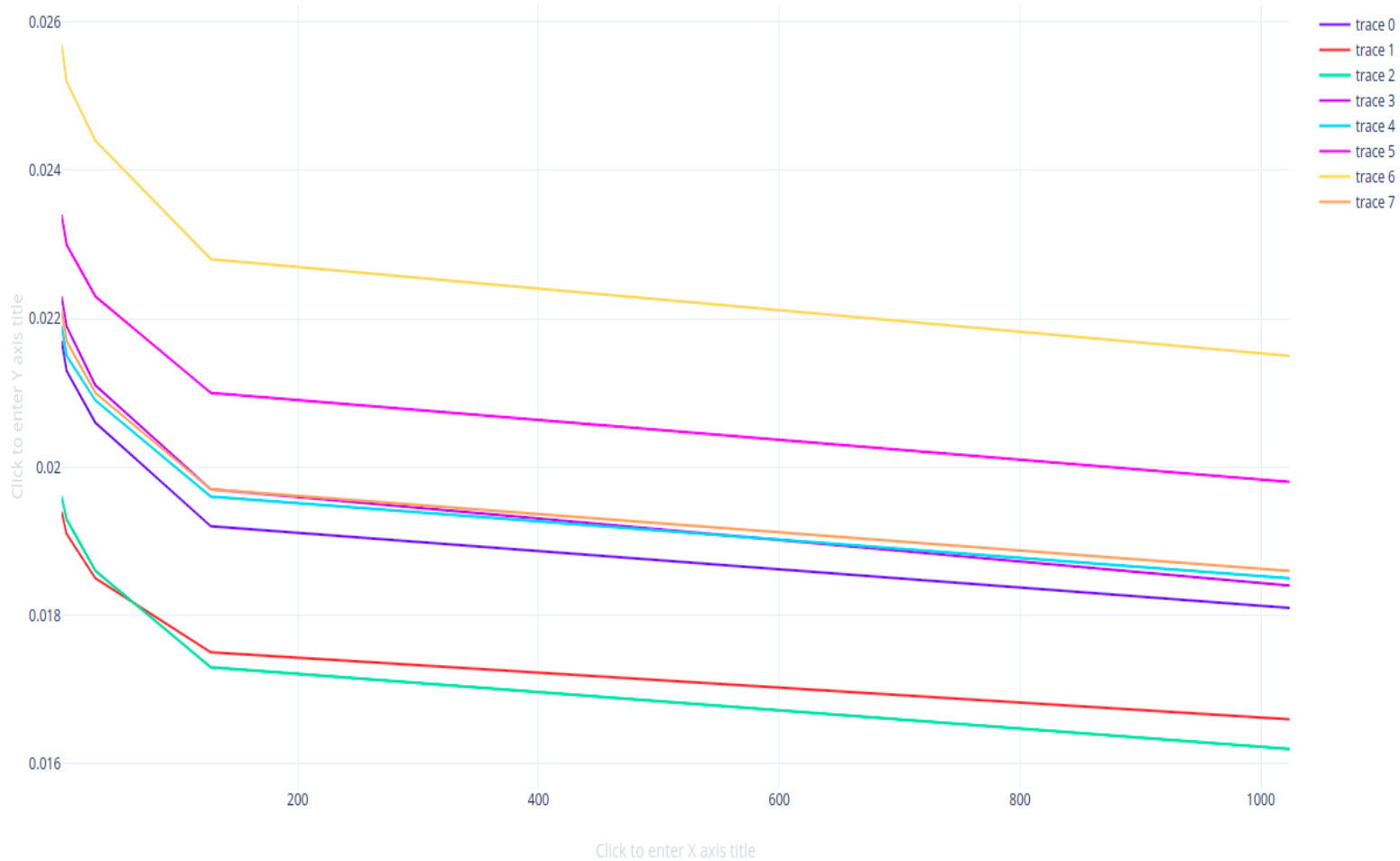
IPC FOR DIFFERENT VALUES OF L1D AND LiD

Program	L1d = 1024 B L1i = 4 B	L1d = 1024 B L1i = 8 B	L1d = 1024 B L1i = 32 B	L1d = 1024 B L1i = 128 B	L1d = 1024 B L1i = 1024 B	L1i = 1024 B L1d = 4 B	L1i = 1024 B L1d = 8 B	L1i = 1024 B L1d = 32 B	L1i = 1024 B L1d = 128 B
evenorodd	0.0217	0.0213	0.0206	0.0192	0.0181	0.0182	0.0182	0.0182	0.0182
descending	0.0194	0.0191	0.0185	0.0175	0.0166	0.0171	0.0171	0.0170	0.0169
1-even	0.0196	0.0193	0.0186	0.0173	0.0162	0.0166	0.0166	0.0165	0.0164
2-prime	0.0223	0.0219	0.0211	0.0197	0.0184	0.0186	0.0186	0.0186	0.0186
3-descending	0.0219	0.0215	0.0209	0.0196	0.0185	0.0187	0.0187	0.0185	0.0187
4-histogram	0.0234	0.0230	0.0223	0.0210	0.0198	0.0212	0.0211	0.0208	0.0203
5-fibonacci	0.0257	0.0252	0.0244	0.0228	0.0215	0.0220	0.0219	0.0219	0.0217
6-arithmetic	0.0221	0.0217	0.0210	0.0197	0.0186	0.0188	0.0188	0.0188	0.0188

PLOTTED GRAPHS FOR GIVEN DATA

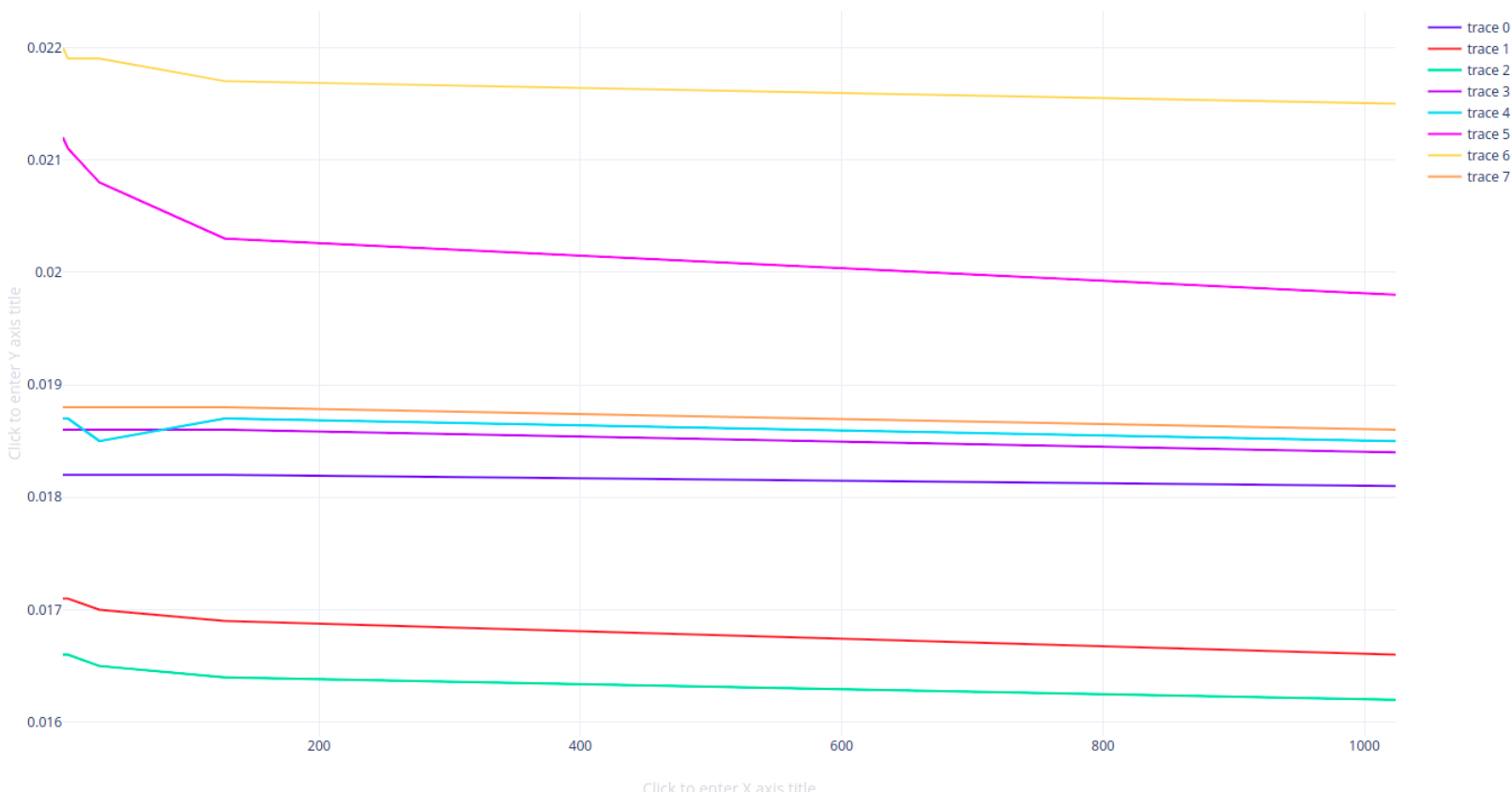
TRACE - 0 - EVENORODD ,
TRACE - 1 - DESCENDING
TRACE - 2 - 1-EVEN
TRACE - 3 - 2-PRIME
TRACE - 4- 3-DESCENDING
TRACE- 5 - 4-HISTOGRAM
TRACE - 6 -5-FIBONACCI
TRACE - 7 -6-ARITHMETIC

IPC FOR PROGRAMS WITH L1D CONSTANT EQUAL TO 1024B



THIS GRAPH IS FOR IPC WITH L1D CONSTANT

IPC FOR PROGRAMS WITH L1i CONSTANT EQUAL TO 1024B



THIS GRAPH IS FOR L1i CONSTANT

CONCLUSION

We observed by increasing cache size we got high hit rate but due to high latency there was a total decrease in value of instruction per cycle