CMOS Logic

The term 'Complementary Metal-Oxide-Semiconductor' (CMOS), refers to the device technology for fabricating integrated circuits using both n- and p-channel MOSFET's. Today, CMOS is the major technology in manufacturing digital IC's and is widely used in microprocessors, memories, and other digital IC's. The input to a CMOS circuit is always to the gate of the input MOS transistor. The gate offers a very high resistance because it is isolated from the channel by an oxide layer. The current flowing through a CMOS input is virtually zero, and the device is operated mainly by the voltage applied to the gate, which controls the conductivity of the device channel. The low input currents required by a CMOS circuit results in lower power consumption, which is the major advantage of CMOS over TTL. In fact, power consumption in a CMOS circuit occurs only when it is switching between logic levels. Moreover, CMOS circuits are easy and cheap to fabricate resulting in high packing density than their bipolar counterparts. CMOS circuits are quite vulnerable to ESD damage, mainly by gate oxide punchthrough from high ESD (Electro static Discharge) voltages. Therefore, proper handling CMOS IC's is required to prevent ESD damage and generally, these devices are equipped with protection circuits.

Fig. 2(a) and Fig. 2(b) show the circuit symbols of an n-channel and a p-channel transistor respectively. An nMOS transistor is 'ON' if the gate voltage is at logic '1', or more precisely if the potential between the gate and the source terminals (V_{GS}) is greater than the threshold voltage V_T. An 'ON' transistor implies the existence of a continuous channel between the source and the drain terminals. On the other hand, an 'OFF' nMOS transistor indicates the absence of a connecting channel between the source and the drain. Similarly, a pMOS transistor is 'ON' if the potential V_{GS} is lower (or more negative) than the threshold voltage V_T..

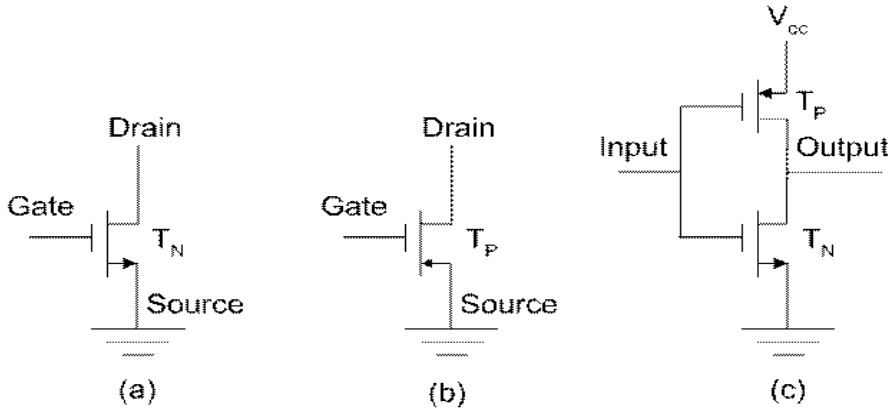

Fig.2 : (a) symbol of an n-channel transistor (b) symbol of an a p-channel transistor (c) a CMOS inverter circuit (NOT gate)

Fig.2(c) shows a CMOS inverter circuit (NOT gate), where a p-channel and an n-channel MOS transistor is connected in series. A logic '1' input voltage would make T_p (p-channel) turn off and T_n (n-channel) turn on. Hence, the output will be low, pulling Output to logic '0'. A logic '0' Vin voltage, on the other hand, will make T_p turn on and T_n turn off, pulling Output to near V_{CC}, or logic '1'. The p- and n-channel MOS transistors in the circuit are complementary and they are always in opposite states, i.e., when one of them is 'on' the other is 'off'.

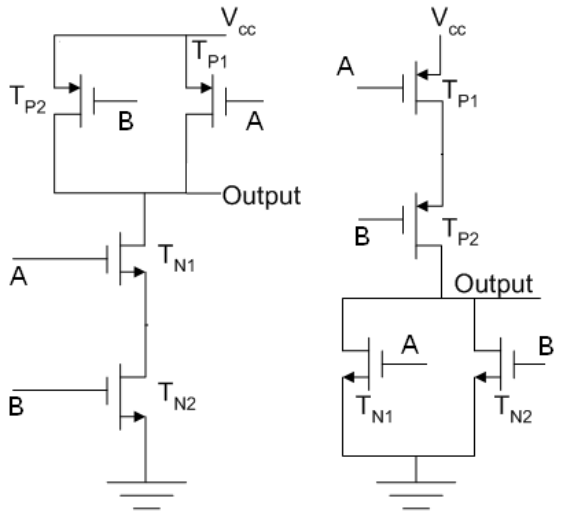

Fig. 3 : (a) 2 input CMOS NAND Gate (b) 2 input CMOS NOR Gate

Figure 3(a) shows a 2 input CMOS NAND Gate where the T_{N1} and T_{P1} have the same input A and T_{N2} and T_{P2} has the same input B. When both the A and B are high, T_{N1} and T_{N2} are ON and T_{P1} and T_{P2} are OFF. Therefore, the output is at logic 0. On the other hand, when both input A and input B are logic 0, T_{N1} and T_{N2} is OFF and T_{P1} and T_{P2} are ON. Hence, the output is at V_{CC} , logic 1. Similar situation arises when any one of the input is logic 0. In such a case, one of the bottom series transistors i.e. either T_{N1} or T_{N2} would be OFF forcing the output to logic 1.

Figure 3(b) shows a 2 input CMOS NOR Gate where the T_{N1} and T_{P1} have the same input A and T_{N2} and T_{P2} has the same input B. When both the A and B are logic 0, T_{N1} and T_{N2} are OFF and T_{P1} and T_{P2} are ON. Therefore, the output is at logic 1. On the other hand, when at least one of the inputs A or B is logic 1, the corresponding nMOS transistor would be ON making the output logic 0. The output is disconnected from V_{CC} in such case because at least one of the T_{P1} or T_{P2} is OFF. Thus the CMOS circuit of Figure 3(b) acts as a NOR Gate.

Logic Threshold Voltage Levels

The Fig. 3 provides a comparison between the Input and Output [I / O] logic switching levels for CMOS, and TTL logic families. V_{OH} and V_{OL} represent the high and the low logic output levels of a gate, respectively. The regions of acceptable high and low voltages are determined by the V_{IH} and V_{IL} voltage levels, respectively. Consider the TTL logic, the range for V_{IL} is from 0 to 0.8 V as shown and the range for V_{OL} is from 0 to 0.35 V. The region between 0.8 V to 2.0 V is called undefined region. The range for V_{IH} is from 2.0 V to V_{CC} and the range of V_{OH} is from 2.0 V to V_{CC}. Similarly, for a CMOS the values can be inferred from the diagram.

If one use a CMOS IC for reduced current consumption and a TTL IC feeds the CMOS chip, then you need to either provide a voltage translation or use one of the mixed CMOS/TTL devices. The mixed TTL/CMOS devices are CMOS devices, which just happen to have TTL input trigger levels, but they are CMOS ICs. Let us consider the TTL to CMOS interface briefly. TTL device need a supply voltage of 5 V, while CMOS devices can use any supply voltage from 3 to 10 V. One approach to TTL/CMOS interfacing is to use a 5V supply for both the TTL driver and the CMOS load. In this case, the worst case TTL output voltages are almost compatible with the worst case CMOS input voltages. There is no problem with the TTL low state window (0 to 0.35 V) because it fits inside the CMOS low state window (0 to 1.3 V). This means the CMOS load always interprets the TTL low state drive as low.

The problem is with TTL high state, which can be as low as 2.0 V. The CMOS device needs at least 3.7V for high-state input. Typically what is done is to use a pull-up resistor between the TTL driver and the CMOS load. The other end of pull up resistor is connected to V_{CC}. When the TTL output is low, this pull up resistor does not have any effect on this output voltage. Nevertheless, when the TTL output is high, the pull up resistor raises this output to approximately 5 V.

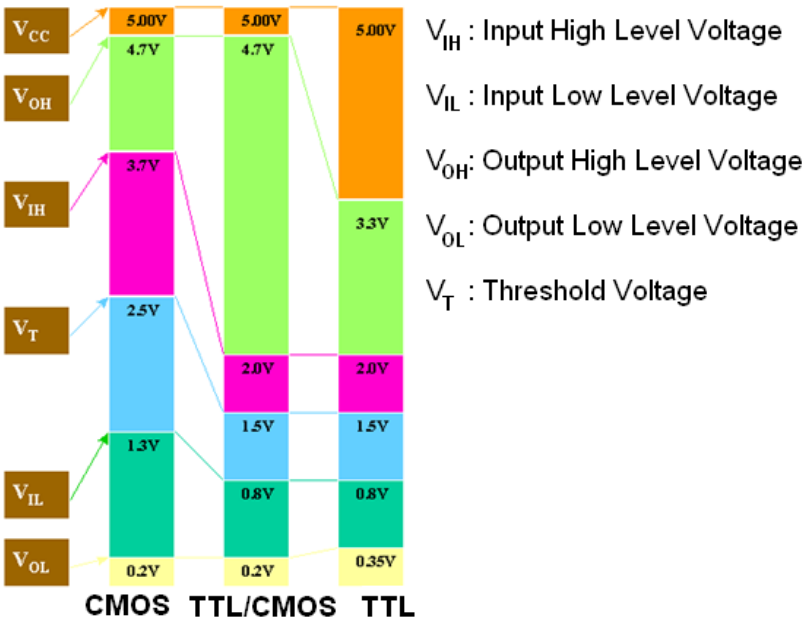

Fig. 4 : Logic Threshold Voltage Levels

Similarly for a CMOS to TTL interface, one need to make sure that the CMOS low-state output is less than 0.8 V and the high-state out is greater than 2 V. Additionally, TTL operates with a low sate input current of ~1.6 mA which is a far too much current for a CMOS device to sink without entering the TTL indeterminate region. Therefore the solution would be to use a CMOS/TTL buffer.

Integrated Injection Logic (IIL , I^2L)

Integrated Injection Logic eliminates the need for any resistors, capacitors or transistor isolation. This enables an extremely compact logic circuit to be formed which has low power consumption while maintaining the normal speed of transistor-transistor logic. I^2L is built with multiple collector bipolar junction transistors. Although the logic levels are very close (High: 0.7V, Low: 0.2V), I^2L has high noise immunity because it operates by current instead of voltage. It is also known as merged-transistor logic.

Emitter Coupled Logic (ECL)

Emitter coupled logic (ECL) gates use differential amplifier configurations at the input stage. (ECL) is a non saturated logic, which means that transistors are prevented from going into deep saturation, thus eliminating storage delays. In other words, the transistor is switched on, but not completely on. This is the fastest logic family. ECL circuits operate using a negative 5.2 V supply and the voltage level for high is -0.9 V and for low is -1.7V; thus biggest problem with ECL is a poor noise margin.