Transistor-Transistor Logic (TTL)

TTL is the short form of Transistor Transistor Logic. As the name suggests they refers to the digital integrated circuits that employ logic gates consisting primarily of bipolar transistors. The most basic TTL circuit is an inverter. It is a single transistor with its emitter grounded and its collector tied to V_{CC} with a pull-up resistor, and the output is taken from its collector. When the input is high (logic 1), the transistor is driven to saturation and the output voltage i.e. the drop across the collector and emitter is negligible and therefore output voltage is low (logic 0).

A two input NAND gate can be realized as shown in Fig.1a. When, at least any one of the input is at logic 0, the multiple emitter base junctions of transistor T_A are forward biased whereas the base collector is reverse biased. The transistor T_A would be ON forcing a current away from the base of T_B and thereby T_B is OFF. Almost all V CC would be dropping across an OFF transistor and the output voltage would be high (logic l). For a case when both Input1 and Input 2 are at V_{CC} , both the base emitter junctions are reverse biased and the base collector junction of the transistor T_A is forward biased therefore the transistor T_B is on making the output at logic 0, or near ground .

However, most TTL circuits use a totem pole output circuit instead of the pull-up resistor as shown in Fig.1b. It has a V_{CC} -side transistor (T_C) sitting on top of the GND-side output transistor (T_D). The emitter of the T_C is connected to the collector of T_D by a diode. The output is taken from the collector of transistor T_D. T_A is a multiple emitter transistor having only one collector and base but with multiple emitters. The multiple base emitter junction behaves just like an independent diodes. Applying a logic '1' input voltage to both emitter inputs of T_A reverse-biases both base-emitter junctions, causing current to flow through R_A into the base of T_B, which is driven into saturation. When T_B starts conducting, the stored base charge of T_C dissipates through the T_B collector, driving T_C into cut-off. On the other hand, current flows into the base of T_D , causing it to saturate and its collector emitter voltage is 0.2 V and the output is equal to 0.2 V, i.e. at logic 0. In addition, since T_C is in cut-off, no current will flow from V_{CC} to the output, keeping it at logic '0'. Since T_D is in saturation, its input voltage is ~0.8 V. Therefore the output voltage at the collector of transistor T_B is 0.8 V + V_{CESat} (saturation voltage between conductor and emitter of a transistor is equal to ~0.2 V) = 1 V. T B always provides complementary inputs to the bases of T_C and T_D, such that T_C and T_D always operate in opposite regions, except during momentary transition between regions. The output impedance is low independent of of the logic state because one transistor (either T_C or T_D) is ON. When at least one of inputs are at 0 V, the multiple emitter base junctions of transistor T_A are forward biased whereas the base collector is reverse biased and transistor T_B remains off and therefore the output voltage is equal to V_{CC} . Since the base voltage for transistor T_C is

V_{CC} , this transistor is on and the output is also V_{CC} . And the input to transistor T_D is 0 V, hence it remains off.

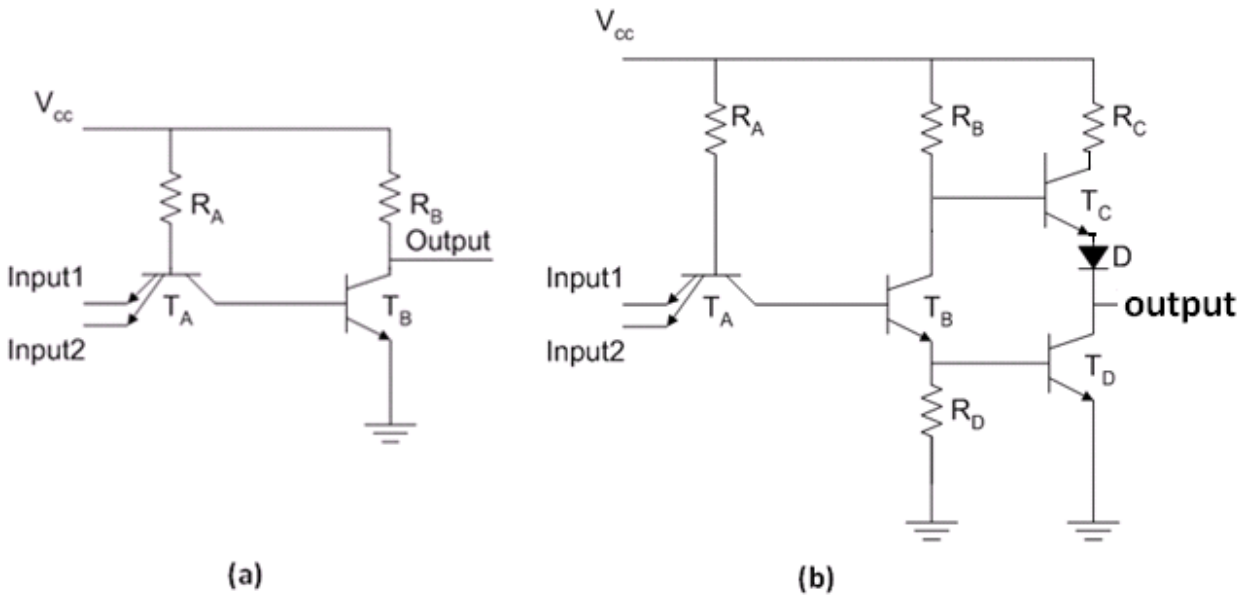

Figure 1: A 2-input TTL NAND Gate with a Totem Pole Output Stage

TTL overcomes the main problem associated with DTL (Diode Transistor Logic), i.e., lack of speed. The input to a TTL circuit is always through the emitter(s) of the input transistor, which exhibits a low input resistance. The base of the input transistor, on the other hand, is connected to the V_{CC} , which causes the input transistor to pass a current of about 1.6 mA when the input voltage to the emitter(s) is logic '0'. Letting a TTL input 'float' (left unconnected) will usually make it go to logic '1'. However, such a state is vulnerable to stray signals, which is why it is good practice to connect TTL inputs to V_{CC} using 1 kΩ pull-up resistors