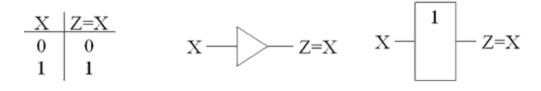
Additional Logic Operations

For two inputs, there are 16 ways we can assign output values. Besides AND and OR, there are five other operations which are useful.

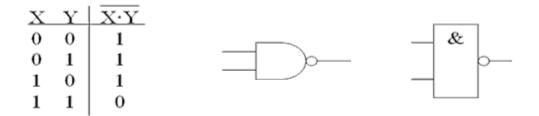
BUFFER

The unary Buffer operation is useful in the real world



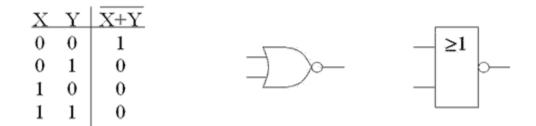
NAND

NAND (NOT - AND) is the complement of the AND operation



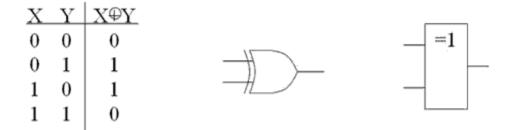
NOR

NOR (NOT - OR) is the complement of the OR operation



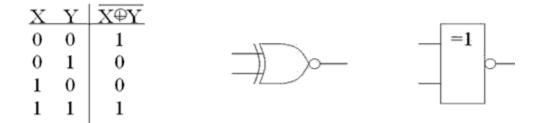
XOR

Exclusive OR is similar to the inclusive OR except output is 0 for 1. It is stated in other words as the output is 1 when modulo 2 input sum is equal to 1.



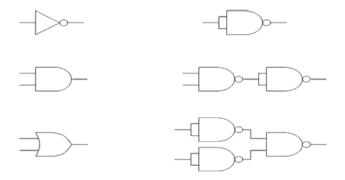
XNOR

Exclusive NOR is the complement of the XOR operation. Alternatively, the output is 1 when the modulo 2 input sum is not equal to 1.

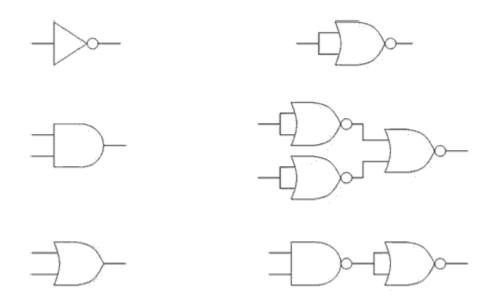


Minimal Logic Operator Sets

AND, OR, NOT are all that's needed to express any combinational logic function as a switching algebra expression. However, two other minimal logic operator sets are also possible with NAND gates or NOR gates. The following is a demonstration of how just NANDs or NORs can do AND, OR, NOT operations.



NOR as a Minimal Set



Three State Outputs

Standard logic gate outputs only have two states; high and low. Outputs are effectively either connected to +V or ground, that means there is always a low impedance path to the supply rails. In certain applications require a logic output that we can "turn off" or disable. It means that the output is disconnected (high impedance state). This is the three-state output and can be implemented by a stand-alone unit (a buffer) or part of another function output. This circuit is so-called tri-state because it has three output states: high (1), low (0), and high impedance (Z).

In the logic circuit of Fig. 15(a), there is an additional switch to a digital buffer, which is called as enabled input denoted by E. When E is low, the output is disconnected from the input circuit. When E is high, the switch is connected and the circuit behaves like a digital buffer. All these states are listed in Truth Table 15(b). Figure 8.14(c) depicts the symbol of a Tri-state Buffer.

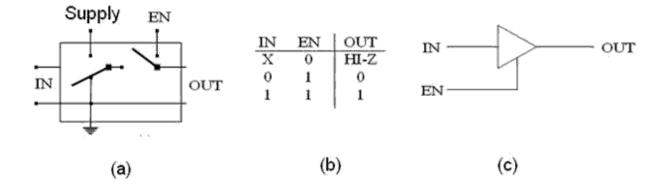


Fig. 15: (a) Switch Configuration, (b) Truth Table, and (c) Symbol of a Tri-state Buffer