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Design and Analysis of a Novel Low-Power Exclusive-OR Gate Based on Quantum-Dot Cellular Automata*

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Recently reported quantum-dot cellular automata (QCA) exclusive-OR gate designs are usually made with the AND–OR–INVERTER method in which it is difficult to optimize the XOR gate. This paper presents a novel low-power exclusive-OR (XOR) gate which is mainly based on cell-level format. Compared with the previous XOR gates, the proposed XOR gate performs in a different manner. This XOR gate design is accomplished by the intercellular effects method. For better performance comparison with previous relevant works, 4-, 8-, 16- and 32-bit parity generators are implemented in this paper. The simulation results show that there is a reduction of 32.5% cell count and 21.5% area in comparison with the existing advanced 32-bit parity generator. Especially in the aspect of clock cycle, the proposed design reduces the delay by 50% compared to the previous design. For simulation analysis, QCADesigner tool is used to verify the correctness of the proposed design. QCApro tool is used to evaluate the power dissipation of this design.

Keywords: Quantum-dot cellular automata; exclusive-OR gate; intercellular effect; parity generator; energy dissipation.

1. Introduction

As the nanometer-scale CMOS devices are facing new realization challenges, such as large leakage current, high power density, complex wiring, crosstalk and so on, there is a serious impact on the development of integrated circuits.[1] Therefore, the

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necessity for an alternative technology that could provide a revolutionary approach to nanoscale work seems more important than ever.[2] Quantum-dot cellular automata (QCA), proposed by Lent *et al.*,[3] provides a new mode of computing and information processing because of its unique structural characteristics and assembly form. Compared with the classic circuit, it is connected by quantum interactions between quantum dots. Quantum dots do not represent information by voltage or current, but characterize binary information by the positions occupied by electrons. QCA consumes lower power, is more integrated and is faster. It can solve the problems which are brought in by the narrowing of the device size in the traditional CMOS circuits. Many virtues make it an attractive alternative to traditional CMOS technology.

Since no electrical current is involved in the QCA computations, the power consumption is much lower than the conventional CMOS circuit. However, it is necessary to characterize all aspects of the new technology, and several studies have been carried out in the field of QCA power.[4–7] Furthermore, many different circuits and structures have been implemented by QCA in recent years. Full adder as one of the most common digital arithmetic units,[2,8–11] memory circuits,[12,13] reversible circuits,[14–16] new designs for five-input majority gate[17,18] and new designs for exclusive-OR (XOR) gate[19,20] have been presented.

In this paper, we propose a new low-power XOR gate, which is different from the traditional way to achieve the XOR gate, based on QCA. The proposed XOR design achieved the XOR function through the interaction between cells rather than using the logic function directly. In order to display the performance of the proposed XOR gate, the proposed XOR gate is used to design the parity generator circuit. We compare and analyze the power consumptions and other parameters of the proposed parity generator and the previous parity generator.

The rest of this paper is organized as follows: we provide a brief introduction to the background knowledge of QCA in Sec. 2. In Sec. 3, we first describe the previous XOR designs, then introduce our proposed design and finally build a 32-bit parity generator. In Sec. 4, we use QCADesigner tool to compare some parameters of XORs and parity generators. In Sec. 5, we used QCApro tool to evaluate the energy dissipation of the proposed design. Finally, we conclude this paper in Sec. 6.

2. QCA Preliminaries

2.1. *QCA cell*

A QCA cell is square-shaped. For a QCA cell, there are two different structures. In the first structure, four quantum dots of the cells are located at the four corners of a square, which we call 90° normal cells, as shown in Fig. 1(a); the other structure is where the four quantum dots are located on the four sides of the square, these constructed cells are called 45° rotated cells, as shown in Fig. 1(b).

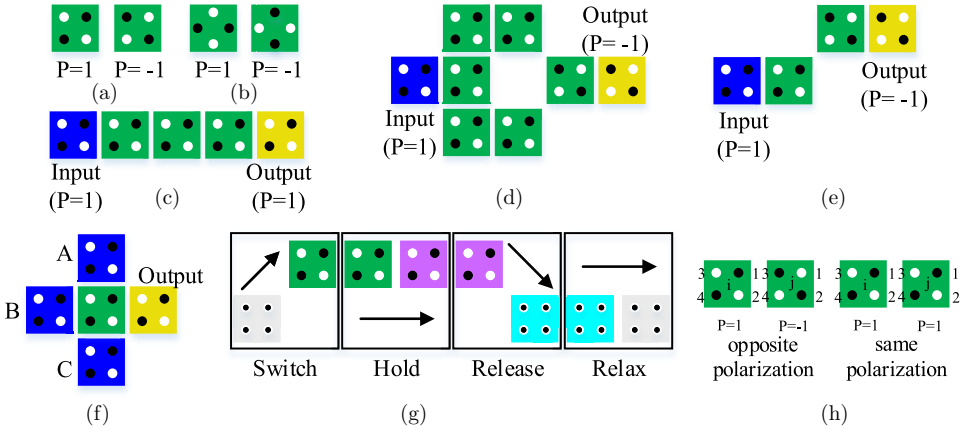

Fig. 1. (a) Normal cells, (b) rotated cells, (c) QCA binary wire, (d) inverter gate, (e) alternate inverter gate, (f) majority gate, (g) QCA clocking and (h) kink energy.

A QCA cell consists of four quantum dots and two extra mobile electrons, and electrons can quantum mechanically tunnel between dots, but not cells. The electrons are forced to the corner positions by Coulomb repulsion. As a result, the four quantum dots in each cell have two stable arrangements. As shown in Fig. 1(a), polarizations $P = +1$ and -1 are represented as logic "1" and logic "0," respectively.[3,21] Usually, the two polarization states of the cell will be energetically equivalent. But if other cells are nearby, the two polarization states of the cell will not be energetically equivalent. Consider two cells close to one another as shown in Fig. 2. When cell 2 has a polarization of +1, it is clear that the ground state

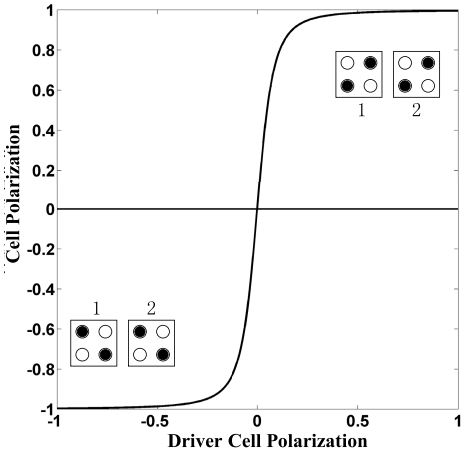

Fig. 2. The cell–cell response function.

configuration of cell 1 is also a +1 polarization. Similarly, if cell 2 has a polarization of −1, the ground state of cell 2 will match the same.

2.2. *QCA logical gates*

The binary wire, the inverter gate and the three-input majority gate are the fundamental logic devices of QCA circuits. Figure 1(c) shows a typical example of a binary wire realization in QCA cell array. Through the intercellular Coulomb force, the cells will be completely polarized one by one. An array of QCA cells is capable of transmitting a "1" or a "0" from the first cell to the last cell. Figures 1(d) and 1(e) show two kinds of implementations of the inverter. A three-input majority gate is shown in Fig. 1(f), the middle cell is driven by three inputs, marked A, B and C. The polarization of the middle cell depends on the polarization of the majority of these inputs. The logic expression of a three-input majority gate is $M(A, B, C) = AB + AC + BC$. An OR or AND gate can be realized with a majority gate by setting one of the inputs to be $P = +1$ or $P = -1$. Then, any logic function can be realized by using such ORs and ANDs, plus inverters.

2.3. *QCA clocking*

In order to enable the circuit to run properly, it is necessary to introduce the clock to control the transmission of information in QCA circuits. The design of QCA circuits requires a clock signal which not only determines the flow of information, but also provides energy against power dissipation. The clock cycle in QCA has four phases, denoted as switch, hold, release and relax,[22] as shown in Fig. 1(g). Considering a 90° out of phase between successive phases, a QCA system is synchronized. In the switch phase, the barrier between quantum dots is steadily raised and a QCA cell is polarized to one of the states due to the influence of neighbor cells. The interdot barriers are kept high and their polarity is retained in the hold phase. In the release phase, the interdot barriers decrease and the cells begin to lose their polarity. During the relax phase, there is no interdot barrier and cells have no polarity.[23]

2.4. *Kink energy*

The way to calculate the energy of a cell is to sum up the kink energies of all dots. The electrostatic energy between cell i and cell j can be calculated by summing up the electrostatic energies of all pairs of dots between cell i and cell j, as shown in the following equation:

$$E_{i,j}^{m,n} = \frac{1}{4\pi\varepsilon_0\varepsilon_r} \sum_{m=1}^{4} \sum_{n=1}^{4} \frac{q_i^m - q_j^n}{|r_i^m - r_j^n|}\,, \tag{1}$$

where ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of the material used, q_i^m is the electron charge on the mth dot in cell i and $|r_i^m - r_j^n|$

reflects the distance between the mth dot in cell i and the nth dot in cell j, as shown in Fig. 1(h).

The kink energy $E_{i,j}^{\text{kink}}$ between two adjoining cells is defined as the difference in the electrostatic energy between the two polarization states. The kink energy of cell i and cell j is determined by maintaining the original state of cell i constant while changing the state of polarization of cell j, then finding the difference between two kinds of energy as follows:

$$E_{i,j}^{\text{kink}} = E_{i,j}^{\text{opp.polarization}} - E_{i,j}^{\text{same.polarization}} . \tag{2}$$

2.5. *QCA simulation tool*

All circuit design researches require the support of related tools. QCA circuit research and design are also no exception. QCADesigner provides the designer with the ability to simulate quickly and accurately and present a QCA circuit design.[24] At present, QCA simulation engine has two different kinds, bistable approximation and coherence vector. In this paper, we use the bistable simulation engine whose simulation accuracy is high. Besides, this engine can dynamically reflect the changes in cell polarity. The basis of the bistable simulation engine is the Hamiltonian model, which can be written as follows:

$$H_i = \sum_j \begin{bmatrix} -\frac{1}{2} P_j E_{i,j}^k & -\gamma_i \\ -\gamma_i & \frac{1}{2} P_j E_{i,j}^k \end{bmatrix}, \tag{3}$$

where P_j is the polarization value of the cell j. $E_{i,j}^k$ is the kink energy between the cells i and j. γ is the tunneling energy of electrons within the cell. The summation is

Table 1. Bistable approximation parameters.

Parameter	Value
Cell size	$18 \times 18\,\text{nm}^2$
Dot diameter	5 nm
Center-to-center distance	20 nm
Number of samples	102,400
Convergence	0.001
Radius of effect	65 nm
Relative permittivity	12.9
Clock high	9.8×10^{-22} J
Clock low	3.8×10^{-23} J
Clock shift	0
Clock amplitude factor	2
Layer separation	11.5 nm
Maximum iterations per sample	100
Relaxation time	$4.1356675 \times 10^{-14}$ s

over all cells within an effective radius of cell i, and it can be set prior to the simulation. The various parameter values used in this paper are listed in Table 1.

3. Related Works

3.1. *Previous XOR designs*

The XOR gate is widely used in the design of various circuits, such as parity generator, detection and correction operations in the receiver and sender units.[25] Various designs of XOR have been proposed previously.[19,20,25–33] These designs change the numbers of majority gates and inverter gates in the circuit by changing the equation of the XOR gate. The output of a three-input majority gate discussed in Ref. 26 simplifies according to Eq. (4) to produce the XOR output. The schematic diagram of this design and its implementation in QCA are shown in Figs. 3(a) and 3(b), respectively:

$$\begin{aligned}\mathrm{MAJ3}(\mathrm{MAJ3}(A,B,0),\mathrm{MAJ3}(A,B,1),1) &= \mathrm{MAJ3}(\overline{A}B, A\overline{B}, 1)\\ &= \overline{A}B + A\overline{B}\,. \end{aligned} \tag{4}$$

Another design based on Eq. (5) using one five-input majority gate and one three-input majority gate was presented in Ref. 25. Figure 4 shows its circuit diagram and QCA implementation:

$$\begin{aligned}\mathrm{MAJ5}(2\mathrm{MAJ3}(A,B,1),\overline{A},\overline{B},0) &= \mathrm{MAJ5}(2(A+B),\overline{A},\overline{B},0)\\ &= \overline{A}B + A\overline{B}\,. \end{aligned} \tag{5}$$

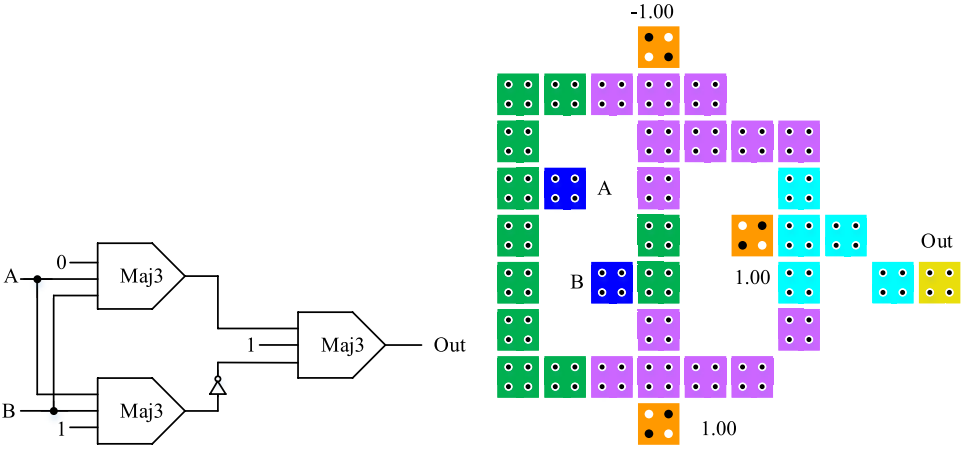

Fig. 3. (a) Circuit diagram of the XOR gate discussed in Ref. 25 and (b) its QCA implementation.

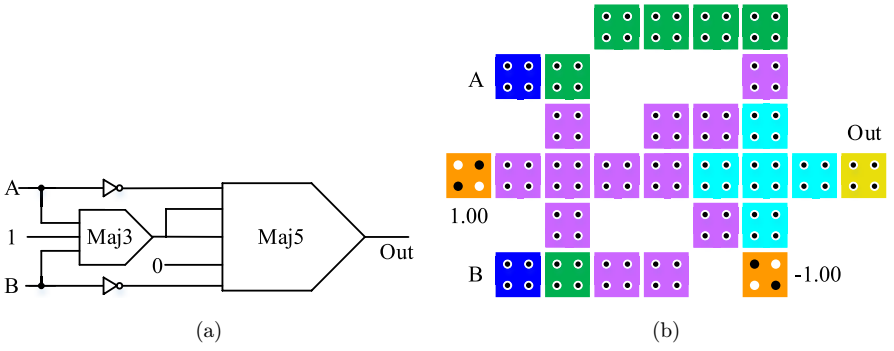

Fig. 4. (a) Circuit diagram of the XOR gate discussed in Ref. 24 and (b) its QCA implementation.

Another design has been reported in Ref. 27 that uses an NNI gate which results in a more compact structure with less number of cells, as shown in Fig. 5.

In Ref. 28, the design uses multilayer wire crossing function to achieve XOR gate. Similarly, another design has been reported that uses the rotated cell.[29] Another design that uses the cell-level method has also been reported.[19,20]

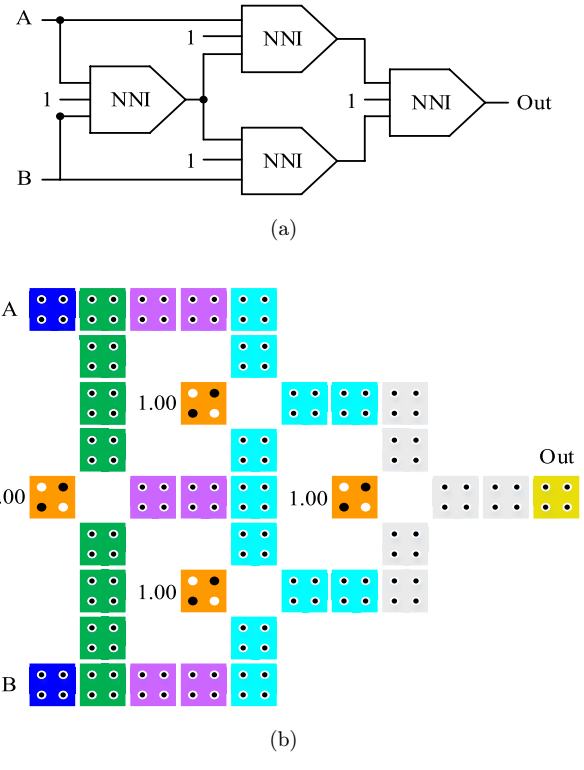

Fig. 5. (a) Circuit diagram of the XOR gate discussed in Ref. 26 and (b) its QCA implementation.

3.2. *Proposed XOR gate*

The traditional XOR gate design is implemented by the AND–OR–INVERTER method in QCA. However, in this paper, we used a new method to propose the novel low-power XOR gate. Implementation of this design is accomplished by intercellular effects method. The output would be affected by the cells in the radius of effect.

In this paper, we propose a two-input XOR gate which is designed by intercellular effects. Figure 6 depicts the layout of the proposed XOR gate, where there are a total of nine QCA cells. The latency is 0.25 clock cycle, and the area amounts to $0.0009\,\mu m^2$. Figure 7 depicts the correct functioning of the proposed XOR gate via the input/output signal patterns. As shown in Fig. 7, when the inputs (AB) are "00" or "11," the output is "0" and when the inputs (AB) are "01" or "10," the output is "1." Thus, the proposed XOR gate simulation results are correct. Compared with other related designs, the proposed XOR gate has a greater advantage in terms of area, cells and clock. Thus is very suitable to build a large-scale circuit.

3.3. *Physical verifications of the proposed XOR gate*

In order to verify the function of the proposed XOR gate, it is necessary to calculate the electrostatic energy of the electrons in different cells. The quantum dots in the output cell are marked with X and Y and other cells are marked from 1 to 14 as shown in Fig. 8. Electrostatic energy at position X due to the electron position at 1–14 is calculated by Eqs. (6) and (7). Equation (6) is used to calculate the electrostatic energy, r is the distance between two electrons. U_T represents the total

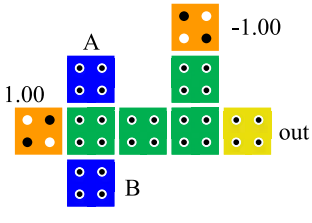

Fig. 6. Layout of the proposed XOR gate.

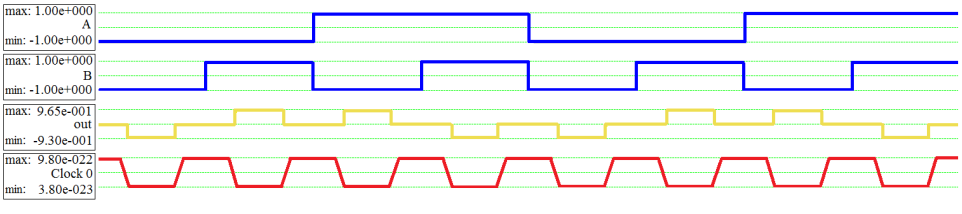

Fig. 7. Simulation results for the proposed XOR gate.

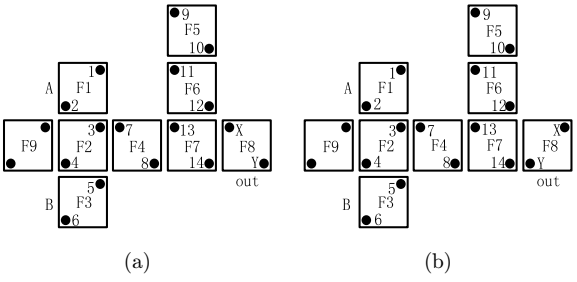

Fig. 8. Cell positions of XOR gate for (a) case 1 and (b) case 2.

electrostatic energy. The calculated results are shown in Table 2:

$$U = \frac{k_{\text{eq}}}{r}\,, \tag{6}$$

$$k_{\text{eq}} = \frac{q^2}{4\pi\varepsilon_0\varepsilon_r} = 23.04 \times 10^{-29} = A\,. \tag{7}$$

As described in Table 2, it is clear that case 1 has lower electrostatic energy than case 2, which means that the output cell in case 1 is more stable. This proves that the output value is "0" when the input vector AB is (1, 1). Likewise, an analogous method can be applied for all other cells, providing similar results.

Table 2. Physical verification for the radius of effect of 65 nm.

Electron X	Electron Y
Case 1 [Fig. 8(a)]	
$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{46.52\times10^{-9}} \approx 0.50 \times 10^{-20}$ J	$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{71.02\times10^{-9}} \approx 0.32 \times 10^{-20}$ J
$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{60.03\times10^{-9}} \approx 0.38 \times 10^{-20}$ J	$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{80.52\times10^{-9}} \approx 0.29 \times 10^{-20}$ J
$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{42\times10^{-9}} \approx 0.55 \times 10^{-20}$ J	$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{62.64\times10^{-9}} \approx 0.37 \times 10^{-20}$ J
$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{62.64\times10^{-9}} \approx 0.37 \times 10^{-20}$ J	$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{78\times10^{-9}} \approx 0.30 \times 10^{-20}$ J
$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{46.52\times10^{-9}} \approx 0.50 \times 10^{-20}$ J	$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{60.03\times10^{-9}} \approx 0.38 \times 10^{-20}$ J
$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{71.02\times10^{-9}} \approx 0.32 \times 10^{-20}$ J	$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{80.52\times10^{-9}} \approx 0.29 \times 10^{-20}$ J
$U_7 = \frac{A}{r_7} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58 \times 10^{-20}$ J	$U_7 = \frac{A}{r_7} = \frac{23.04\times10^{-29}}{60.73\times10^{-9}} \approx 0.38 \times 10^{-20}$ J
$U_8 = \frac{A}{r_8} = \frac{23.04\times10^{-29}}{28.43\times10^{-9}} \approx 0.81 \times 10^{-20}$ J	$U_8 = \frac{A}{r_8} = \frac{23.04\times10^{-29}}{40\times10^{-9}} \approx 0.58 \times 10^{-20}$ J
$U_9 = \frac{A}{r_9} = \frac{23.04\times10^{-29}}{44.72\times10^{-9}} \approx 0.52 \times 10^{-20}$ J	$U_9 = \frac{A}{r_9} = \frac{23.04\times10^{-29}}{69.34\times10^{-9}} \approx 0.33 \times 10^{-20}$ J
$U_{10} = \frac{A}{r_{10}} = \frac{23.04\times10^{-29}}{22.09\times10^{-9}} \approx 1.04 \times 10^{-20}$ J	$U_{10} = \frac{A}{r_{10}} = \frac{23.04\times10^{-29}}{44.72\times10^{-9}} \approx 0.52 \times 10^{-20}$ J
$U_{11} = \frac{A}{r_{11}} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.81 \times 10^{-20}$ J	$U_{11} = \frac{A}{r_{11}} = \frac{23.04\times10^{-29}}{53.74\times10^{-9}} \approx 0.43 \times 10^{-20}$ J
$U_{12} = \frac{A}{r_{12}} = \frac{23.04\times10^{-29}}{2.83\times10^{-9}} \approx 8.14 \times 10^{-20}$ J	$U_{12} = \frac{A}{r_{12}} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.81 \times 10^{-20}$ J
$U_{13} = \frac{A}{r_{13}} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.15 \times 10^{-20}$ J	$U_{13} = \frac{A}{r_{13}} = \frac{23.04\times10^{-29}}{42.05\times10^{-9}} \approx 0.55 \times 10^{-20}$ J
$U_{14} = \frac{A}{r_{14}} = \frac{23.04\times10^{-29}}{18.11\times10^{-9}} \approx 1.27 \times 10^{-20}$ J	$U_{14} = \frac{A}{r_{14}} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.15 \times 10^{-20}$ J
$U_{T1} = 23.64 \times 10^{-20}$ J	
Case 2 [Fig. 8(b)]	
$U_{T2} = 27.07 \times 10^{-20}$ J	

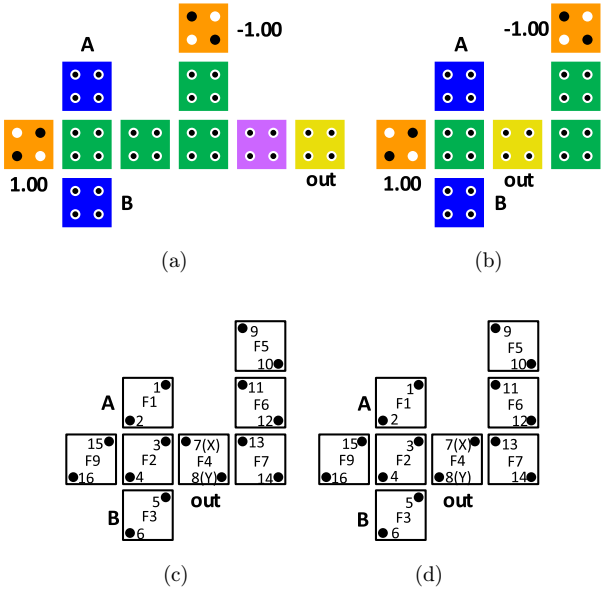

Fig. 9. (a), (b) The layouts of QCA circuits. Cell positions for (c) case A and (d) case B.

Since the polarization of the cell F4 is unclear, further studies will be needed to calculate the electrostatic energy of the cell F4. As shown in Fig. 9(a), when the clock of the output cell of the proposed XOR gate is turned into clock 1, the simulation results are in line with the previous simulation results shown in Fig. 7. The same simulation results show that the output cell has no effect on cell F4. Thus, we can obtain the polarization of the cell F4 in Fig. 9(a) by calculating the electrostatic energy of the cell F4 in Fig. 9(b). When calculating the electrostatic energy of the cell F4, we will treat the cell F4 as the output cell to discuss its polarization. The deliberation of the total electrostatic energy at cell F4 is shown below. For case A, $U_{TA} = 30.522 \times 10^{-20}$ J. For case B, $U_{TB} = 33.616 \times 10^{-20}$ J. It is clear from the

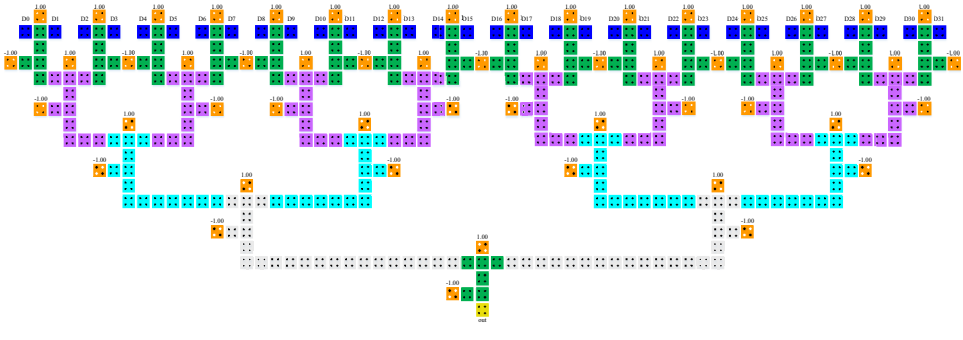

Fig. 10. Layout of the 32-bit parity generator.

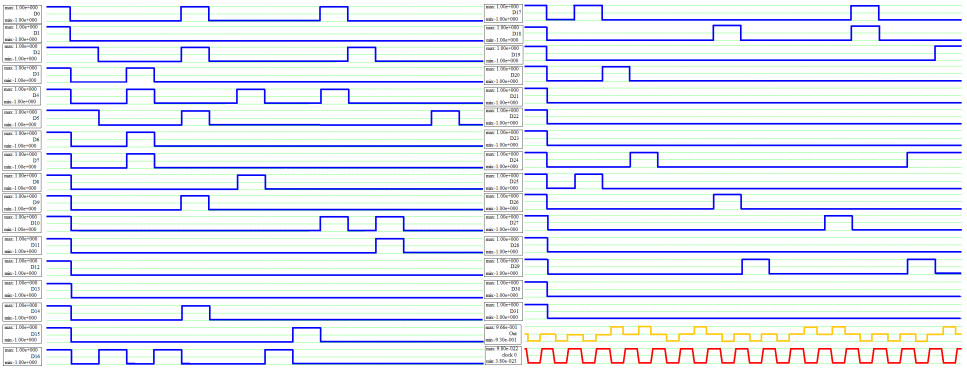

Fig. 11. Simulation results for a 32-bit parity generator with the proposed XOR gate.

above calculated results that case A has lower kink energy and is more stable. Thus, the value of cell F4 is "0" when the input vector AB is (1, 1).

3.4. *Parity generator design*

In order to prove that the proposed XOR gate is better in terms of the cell count, area and clock cycle, our proposed design is used for implementing the parity generator circuit. Parity generators play an important role in the design of digital circuits. We designed 4-, 8-, 16- and 32-bit parity generators in this study by adopting the proposed XOR gate. Figure 10 shows the layout of 32-bit parity generator with the proposed XOR gate. Figure 11 shows the simulation results of 32-bit parity generator. QCADesigner has been used to check the proper functionality of the circuits.[24]

4. Simulation Results

To verify the performance of the proposed XOR gate, we implement the proposed design in the simulator QCADesigner version 2.0.3 using the coherence vector simulation engine. The various parameter values used are listed in Table 1. Table 3 provides a comparison of the different two-input XOR gates in terms of area, cell count and delay. The proposed XOR design uses only nine cells and occupies 0.009 μm^2 area. Compared with other XOR designs in Refs. 19 and 25, the proposed XOR design occupies 25% and 55% less areas and has 31% and 68% less numbers of cells, respectively. The proposed XOR gate has only 0.25 clock cycle, while 0.5 clock cycle and 0.75 clock cycle are reported in Refs. 19 and 25.

In order to evaluate performance of the proposed XOR gate in complex circuits, the 4-, 8-, 16- and 32-bit parity generators are implemented. Figure 12(a) shows the layout of the 4-bit parity generator, the simulation result is shown in Fig. 12(b). When the 4-bit input vector "1" is an odd number, the output of the parity generator is "1." Conversely, when the 4-bit input vector "1" is an even number, the output of

Table 3. Comparison results of two-input XOR gates.

Two-input XOR gate	Area (μm^2)	Cell count	Delay (clock phases)	Cross-over type
Proposed XOR	0.009	9	0.25	Not required
Ref. 19	0.012	13	0.5	Not required
Ref. 20	0.014	14	0.5	Not required
Ref. 25	0.020	28	0.75	Not required
Ref. 26	0.030	36	0.75	Not required
Ref. 27	0.030	37	1	Not required
Ref. 30	0.020	32	1	Not required
Ref. 29	0.090	60	1.5	Coplanar
Ref. 33	0.080	54	1.5	Coplanar
Ref. 31	0.020	30	0.75	Coplanar
Ref. 32	0.030	39	0.75	Multilayer

the parity generator is "0." The output appears after 0.5 clock cycle delay of the input vector. Table 4 compares the proposed parity generator with the previously available parity generators. The 32-bit parity generator design occupies 32% less area and 33% less number of cells than the best reported designs in Ref. 19. This shows

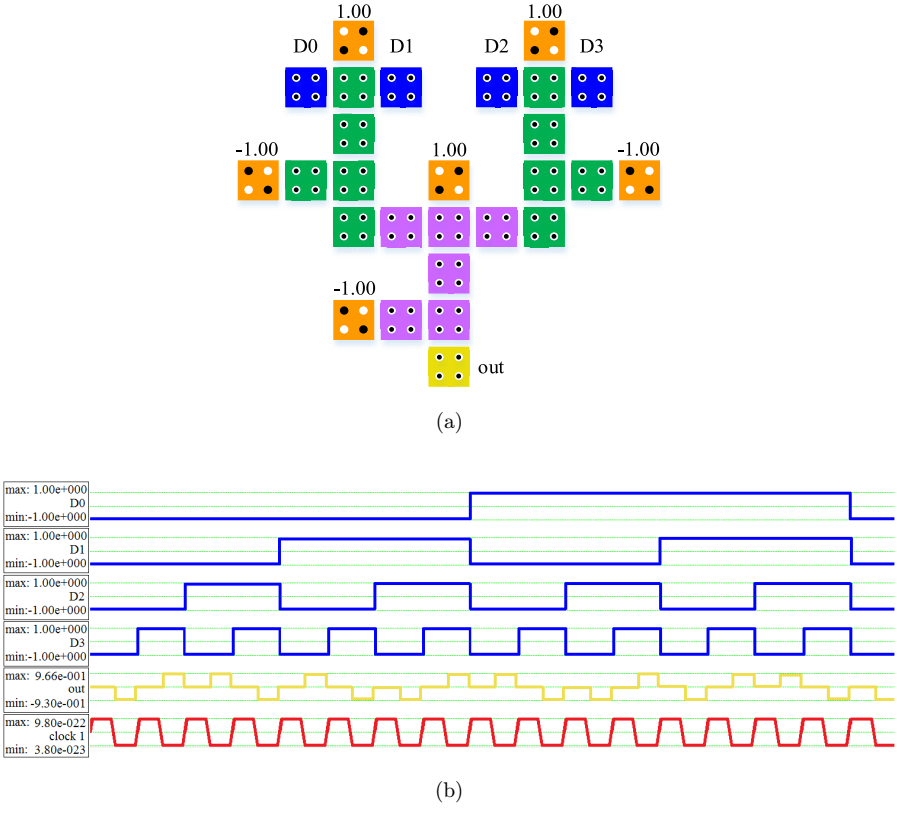

Fig. 12. (a) The layout of 4-bit parity generator. (b) Simulation results for the 4-bit parity generator.

Table 4. Comparison results of parity generators.

Parity generator	No. of bits	Cell count	Circuit area (μm^2)	Delay (clock phases)
Proposed	4	26	0.029	0.5
	8	68	0.096	0.75
	16	158	0.21	1
	32	354	0.52	1.25
Ref. 19	4	45	0.06	1
	8	113	0.19	1.5
	16	237	0.34	2
	32	525	0.76	2.5
Ref. 25	4	87	0.10	1.75
	8	213	0.30	2.75
	16	480	0.81	3.75
	32	1,044	2.08	4.75
Ref. 27	4	111	0.14	2
	8	269	0.43	3
	16	603	1.13	4
	32	1,312	2.81	5
Ref. 30	4	98	0.11	2
	8	241	0.37	3
	16	537	1.04	4
	32	1,167	2.67	5
Ref. 31	4	97	0.1	1.75
	8	235	0.3	2.75
	16	523	0.76	3.75
	32	1,126	1.82	4.75

that the proposed new design has a big advantage in terms of area and the number of cells with the increasing complexity. More importantly, the proposed design is superior in latency in comparison with the previous designs.

5. Power Dissipation Results

Power dissipation is analyzed to evaluate the power loss of the proposed XOR gate and parity generator. According to the nonadiabatic power dissipation model,[6] the instantaneous power equation for the QCA cell[4,34] can be written as

$$P_{\text{total}} = \frac{d}{dt}E = \frac{\hbar}{2}\left(\frac{d}{dt}\vec{\Gamma}\right)\cdot\vec{\lambda} + \frac{\hbar}{2}\vec{\Gamma}\left(\frac{d}{dt}\vec{\lambda}\right) = P_1 + P_{\text{diss}}\,, \tag{8}$$

where P_1 represents the power between the input and output due to the difference in the power transferred from clock cycle delay signal to the cell. P_{diss} represents the dissipated power. This power model has been used in QCApro tool.[35] The QCApro tool has been used to calculate the power dissipation of the proposed QCA XOR design and previous designs. All designs have been examined under three tunneling energy levels: $0.5E_k$, $1.0E_k$ and $1.5E_k$ at 2-K temperature. Table 5 lists the power

Table 5. Power dissipation results of XOR gate.

Two-input XOR gate	Average leakage power dissipation (meV)			Average switching power dissipation (meV)			Total power dissipation (meV)		
	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$
Proposed	2.71	7.53	12.84	7.80	6.60	5.56	10.51	14.13	18.41
Ref. 19	5.40	13.43	21.81	5.96	4.99	4.21	11.36	18.42	26.02
Ref. 20	5.58	13.99	23.90	5.55	5.1	4.56	11.13	19.09	27.46
Ref. 25	10.78	28.57	48.15	25.43	21.71	18.4	36.20	50.28	66.58
Ref. 30	11.51	31.91	54.69	35.78	30.48	25.66	47.28	62.39	80.34
Ref. 27	14.82	40.32	68.10	32.17	26.23	21.41	46.99	66.54	89.51
Ref. 31	11.64	31.85	53.68	27.42	21.78	17.40	39.06	53.63	71.08

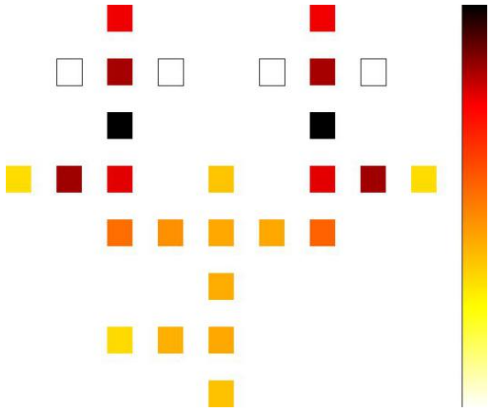

Fig. 13. The power dissipation maps for 4-bit parity generator at 2-K temperature with $0.5E_k$ tunneling energy level.

dissipation results for the two-input XOR gates. The results contain the average leakage power dissipation, average switching power dissipation and average power dissipation. From the results, we can see that the proposed XOR gate's average energy consumption is increasing slowly with the increase in tunneling energy levels. It is observed that the proposed XOR design has 29.2% less total power dissipation than the best reported design in Ref. 19 at $1.5E_k$ tunneling energy level.

Figure 13 shows the power dissipation map for 4-bit parity generator at 2-K temperature with tunneling energy level of $0.5E_k$. The darker cells represent higher average power dissipations. White squares represent the input cells. This map is generated by the QCApro tool.

6. Conclusions

Most of the QCA XOR gate designs use the AND–OR–INVERTER method, while there are few design realizations that use QCA cell intercellular effects method.

This paper used the cell intercellular effects method to design a novel low-power XOR gate, whose cell count, area consumption, delay and total power dissipation are superior to all previous designs. The simulation results show that the proposed XOR design occupies 25% less area, has 31% less number of cells and exhibits 29.2% less total power dissipation than those of the best reported design. We have used the proposed design in the realization of 4-, 8-, 16- and 32-bit QCA parity generators, where 32.5–42.2% improvement in cell count and 21.5–51.5% reduction in area consumption have been achieved, with regard to the best previous QCA parity generator. Also, our parity generator is faster than the previous ones. Further, the proposed design has a great advantage in terms of delay with the increase of the size of the parity generator.

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