Efficient Synthesis of Reversible Circuits

Using Quantum Dot Cellular Automata (QCA)

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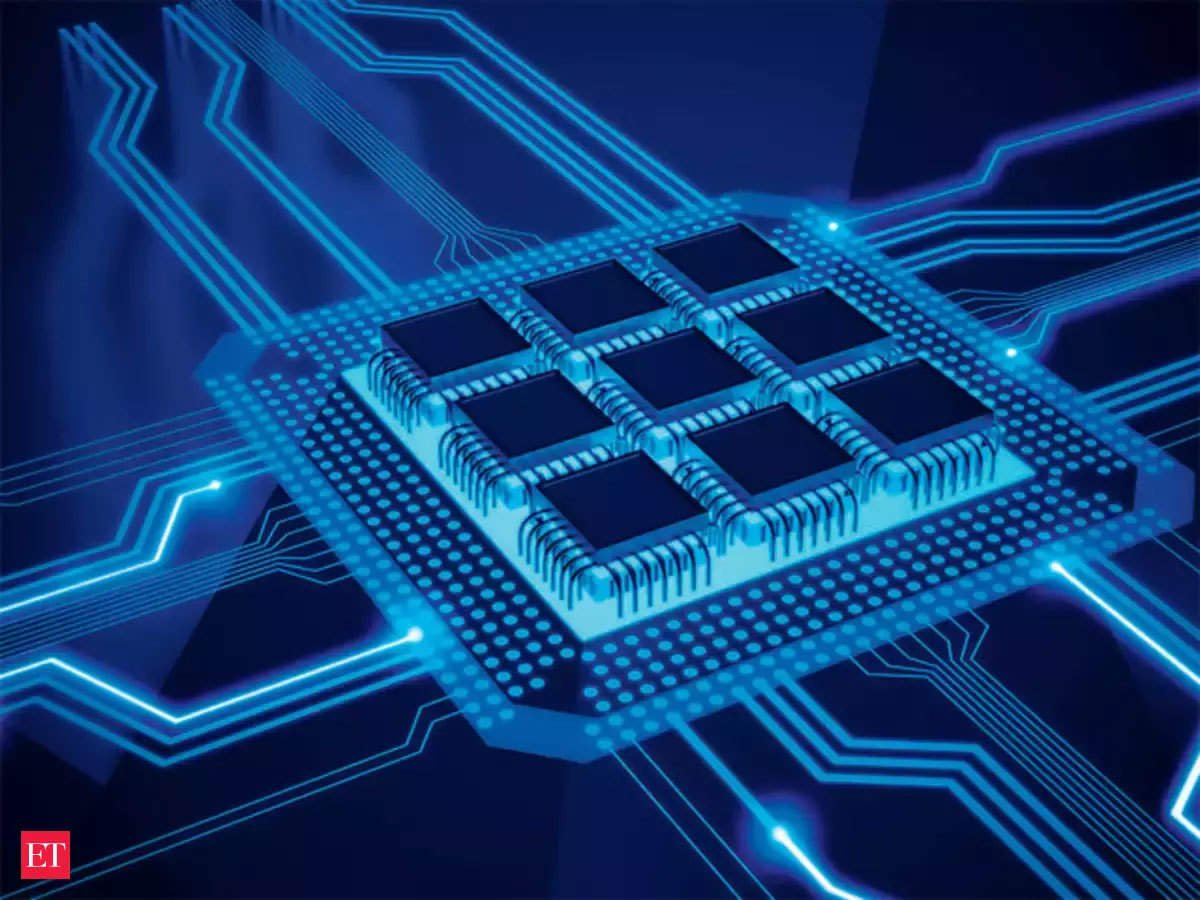
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TEAM : 23



**Abstract:**

Quantum-dot cellular automata (QCA) offer a promising nanoscale computing technology, capitalizing on quantum mechanical electron tunneling and electrostatic interactions between adjacent quantum dots. QCA exhibits potential advantages such as higher speed, lower power consumption, and a reduced physical footprint compared to traditional complementary metal-oxide semiconductor (CMOS) technology. Notably, heat dissipation remains a pressing concern in modern electronic device design, primarily attributed to bit loss. To mitigate this issue, reversible circuits have emerged as a viable solution. This study evaluates the efficacy of reversible computing in QCA, with a particular focus on CNOT and TOFFOLI gates. As QCA designs evolve, a significant reduction in cell size, time delay, circuit area, and the use of majority gates becomes evident. Furthermore, this research expands the scope of reversible circuits by introducing additional components, including the reversible XOR gate, half adder, half subtractor, 2-to-1 multiplexer, 4-to-1 multiplexer, reversible arithmetic unit (AU), reversible logic unit (LU), and reversible arithmetic logic unit (ALU). This extension contributes to the ongoing advancement of reversible computing within the QCA framework.

**INDEX TERMS:** Quantum-dot cellular automata, Reversible gates, CNOT gate, TOFFOLI gate, SWAP Circuit, CNOT Gate, TOFFOLI Gate, Electron Tunnelling, Quantum Dots, Reversible Logic Gates, XOR Gate, Half Adder, Half Subtractor, Multiplexer, Arithmetic Unit (AU), Logic Unit (LU), Arithmetic Logic Unit (ALU).

Introduction:-

In the ever-evolving landscape of electronic devices and computing technologies, quantum-dot cellular automata (QCA) has emerged as a promising nanoscale computing solution. Leveraging quantum mechanical electron tunneling and electrostatic interactions among adjacent quantum dots, QCA offers a potential paradigm shift. It boasts the allure of higher computational speeds, lower power consumption, and a notably reduced physical footprint when compared to the conventional framework of complementary metal-oxide semiconductor (CMOS) technology. However, amid these advancements, a persistent challenge looms large: the dissipation of heat in electronic devices. This challenge is intrinsically tied to the concept of bit loss, a phenomenon that poses significant hindrances to the efficiency and durability of electronic equipment. In response to this challenge, the research community has turned to the innovative approach of reversible circuits as a viable solution. Reversible computing has proven to be a compelling strategy to address the issue of heat dissipation. This study embarks on a comprehensive assessment of the efficacy of reversible computing within the realm of QCA, with a particular emphasis on the utilization of CNOT and TOFFOLI gates. As the designs of QCA continue to evolve, the findings of this research unveil a notable transformation in various critical parameters. These include a substantial reduction in cell size, diminished time delay, a more compact circuit area, and a decreased reliance on majority gates. Moreover, the scope of reversible circuits is expanded to encompass an array of essential components, including the reversible XOR gate, half adder, half subtractor, 2-to-1 multiplexer, 4-to-1 multiplexer, reversible Arithmetic Unit (AU), Logic Unit (LU), and Arithmetic Logic Unit (ALU). This extension contributes significantly to the perpetual advancement of reversible computing within the QCA framework. This research paper delves into the intersection of quantum-dot cellular automata, reversible computing, and the ongoing quest to overcome the formidable challenge of heat dissipation in modern electronic device design. It explores not only the theoretical underpinnings but also practical implementations that promise to shape the future of nanoscale computing.

Reversible Circuits:-

CNOT Gate:-The CNOT gate acts on two qubits, with one as the control and the other as the target. If the control qubit is in the state |1>, it flips the state of the target qubit; otherwise, it leaves the target qubit unchanged. It's a fundamental gate for creating quantum entanglement and implementing conditional logic operations.

TOFFOLI Gate:-The Toffoli gate operates on three qubits, with the first two as control qubits and the third as the target. It performs a NOT operation on the target qubit only when both control qubits are in the state |1>. This gate is crucial for implementing reversible classical computations and constructing quantum error correction codes.

Double CNOT Gate:-The Double CNOT gate is an extension of the CNOT gate that operates on two target qubits. It flips the states of both target qubits when the control qubit is in the state |1>. It's used to create complex entanglement(the state of one quantum dot is directly related to the state of another, even if they are physically separated.)patterns and perform conditional operations on multiple qubits simultaneously.

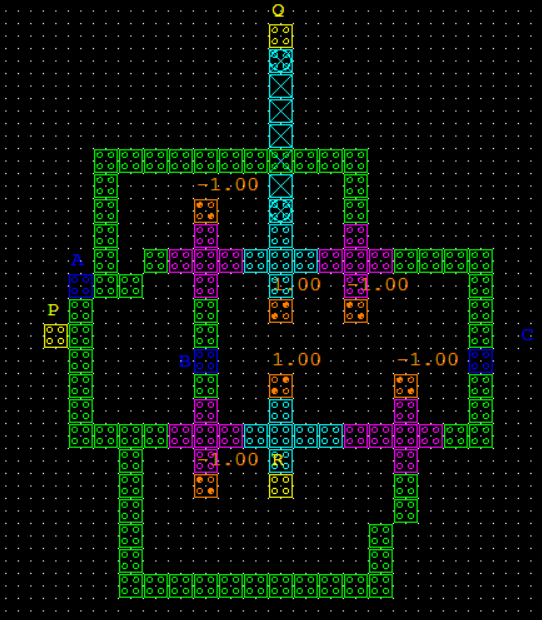
Double TOFFOLI Gate:-Similar to the Toffoli gate, the Double Toffoli gate operates on Four qubits. It performs **NOT operations** on both target qubits when both control qubits are in the state |11>. This gate is valuable for implementing more intricate logic and multi-qubit entanglement operations in quantum circuits.

SWAP Circuit:-The Swap circuit is a basic quantum circuit that exchanges the states of two qubits. It effectively swaps the quantum information between the two qubits without altering it. This operation is essential for various quantum algorithms, such as quantum sorting and quantum teleportation, where precise qubit state exchange is required.

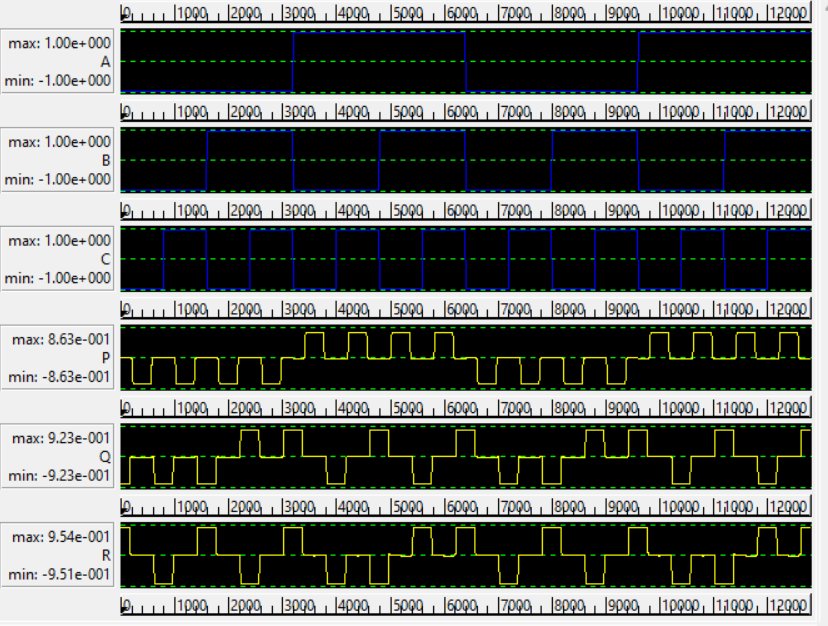
**OUR IDEAS :-**

1. To Study the energy efficiency of reversible circuits compared to traditional circuits.
2. Extension of the work.
3. Correct the swap circuit.
4. Add a new Reversible circuit.

To correct the previous Batch Base paper swap circuit we implemented a swap circuit using a reversible fredkin gate to swap the bit here we have a three bit gate that swaps the last two bits if, and only if ,the first bit(A) is one (1) And if it is not(A) bit is one then It works as a Buffer .



**FIGURE 6(c)**-Swap\_circuit\_using Fredkin Simulation



Logically and Physically Reversible Design Methodology

In QCA circuits, energy dissipation is primarily attributed to the irreversible nature of the majority gate, which has three inputs and a single output [32]. This irreversibility leads to information loss and consequent energy wastage in the environment. Figure (7a) represents the logical design (schematic) of the conventional irreversible majority gate, illustrating its functionality. Figure (7b), on the other hand, presents the physical design (layout) of this gate, revealing how it is implemented on the QCA chip.Efforts to address the energy dissipation challenge in QCA circuits focus on the development of logically and physically reversible design methodologies, aiming to enhance energy efficiency while preserving information integrity.

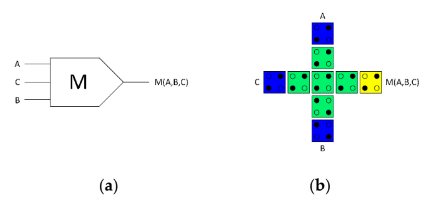


Figure 7.(a) Logical synthesis of the standard irreversible majority gate, Figure 7.(b) physical layout of the standard irreversible QCA majority gate.

To create a highly energy-efficient QCA Arithmetic Logic Unit (ALU), we introduced a pivotal innovation: a fully reversible majority gate. This gate, central to our design, duplicates input data, yielding an equal number of binary inputs and outputs. Figure 8 showcases this groundbreaking fully reversible majority gate, equipped with three inputs and three outputs due to data replication. This design strategy averts data loss and, crucially, safeguards against energy dissipation into the environment. Figure (8a) portrays the logical design (schematic), while Figure (8b) exhibits the physical layout (layout) of our fully reversible QCA majority gate.

Our study adopts a two-stage design approach, featured in Figure 9, to craft logically and physically reversible QCA ALU components. At the heart of this methodology lies the fully reversible majority gate, as detailed in Figure 8, which serves as the foundational building block. This approach marks a significant stride towards achieving enhanced energy efficiency and information integrity in quantum-dot cellular automata.

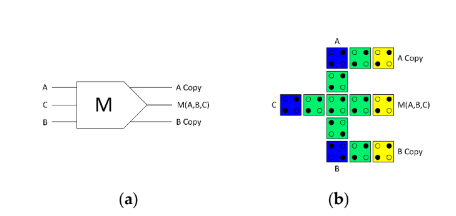


Figure 8. (a) Logical synthesis of the reversible majority gate; Figure 8.(b) physical layout of the reversible QCA majority gate

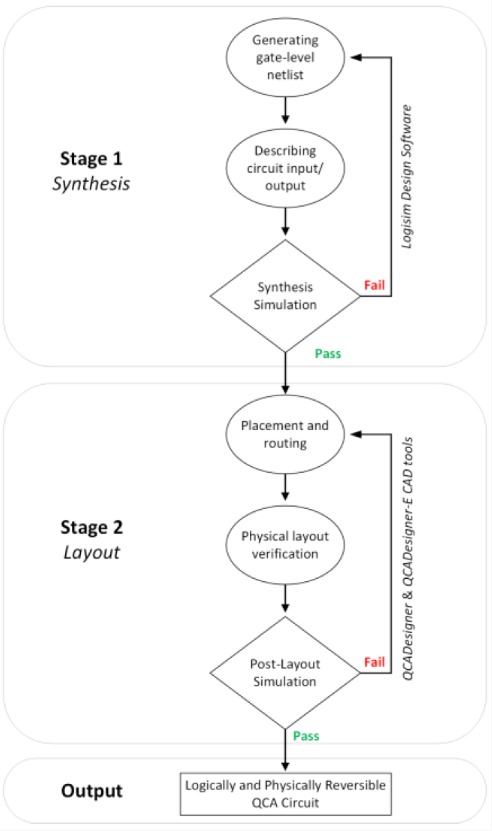
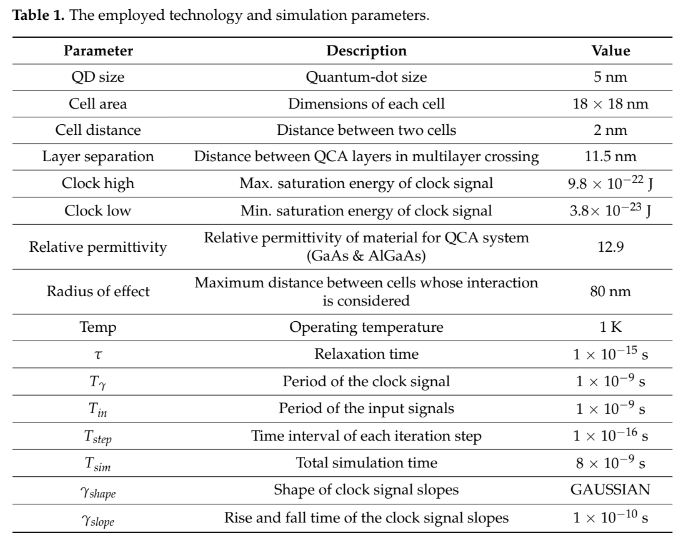


Figure 9. The methodology of designing logically and physically reversible QCA circuits.



1. Proposed Logically and Physically Reversible QCA ALU Design

The ALU, a pivotal component of the CPU, executes logical and arithmetic operations on incoming data, providing results to other registers, memory, or devices. Our study introduces a fully logically and physically reversible QCA ALU designed for ultralow-energy efficiency. It leverages a combination of logic circuits crafted around the fully

reversible QCA majority gate from Figure 8.

The development process commenced with the creation of a high-level block diagram, as depicted in Figure 10. This reversible ALU architecture comprises three key components: the Logic Unit (LU), the Arithmetic Unit (AU), and the Control Unit (CU). The LU handles logical operations like AND, NAND, OR, NOR, XOR, XNOR, NOT, and data transfer. The AU tackles arithmetic operations, including addition, subtraction, multiplication, and division of binary numbers. The CU, guided by input S0, determines the operation type, be it arithmetic or logical.

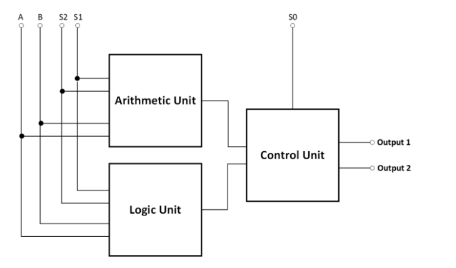


Figure 10. The High-level block diagram of the proposed reversible QCA ALU.

The reversible QCA ALU circuit takes two input operands, A and B, and generates two output values, Output1 and Output2. This reversibility allows the ALU to execute two arithmetic or two logical operations simultaneously, offering a total of 16 operations, encompassing eight logical and eight arithmetic operations, as detailed in Table 2. To specify the ALU's operation and operand selection, three input pins—S0, S1, and S3—are employed.

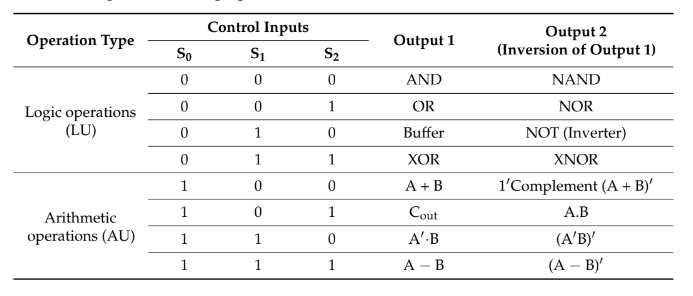


Table 2. The operations of the proposed reversible QCA ALU.

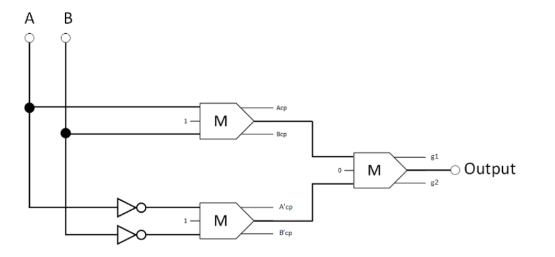




Figure 11. The synthesis of the proposed reversible XOR (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

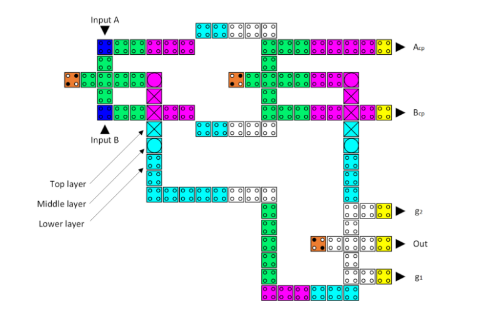


Figure 11(a). The layout of the proposed reversible QCA XOR (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

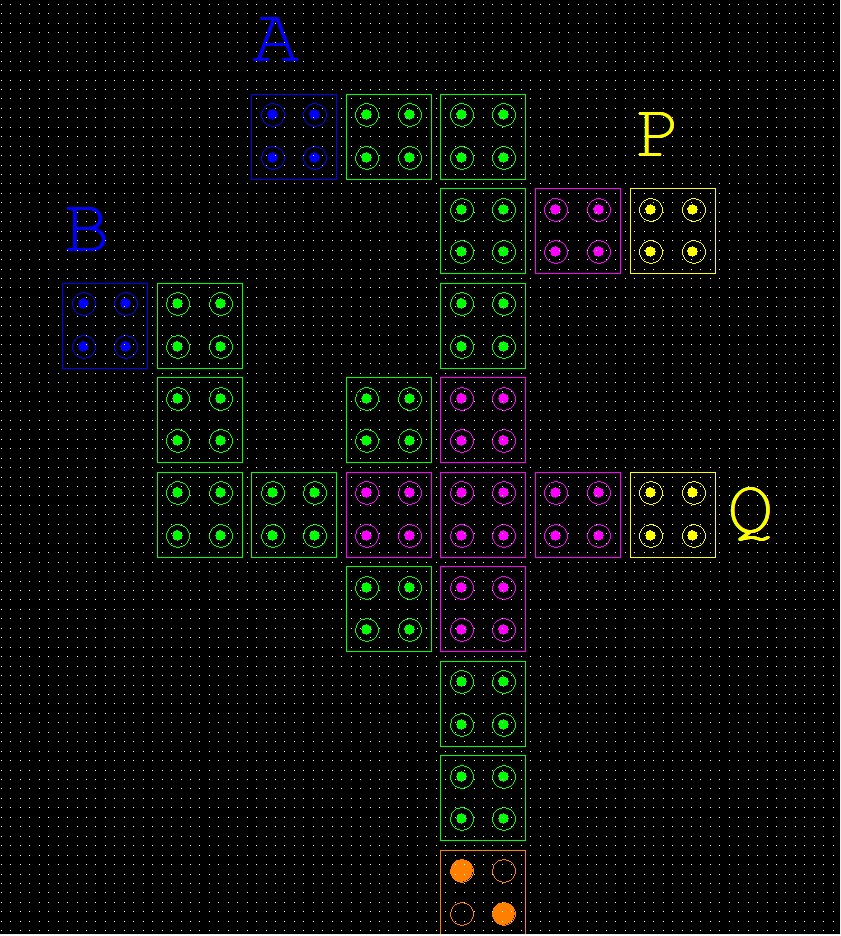


Figure 11(b). The layout of the proposed reversible QCA XOR Gate

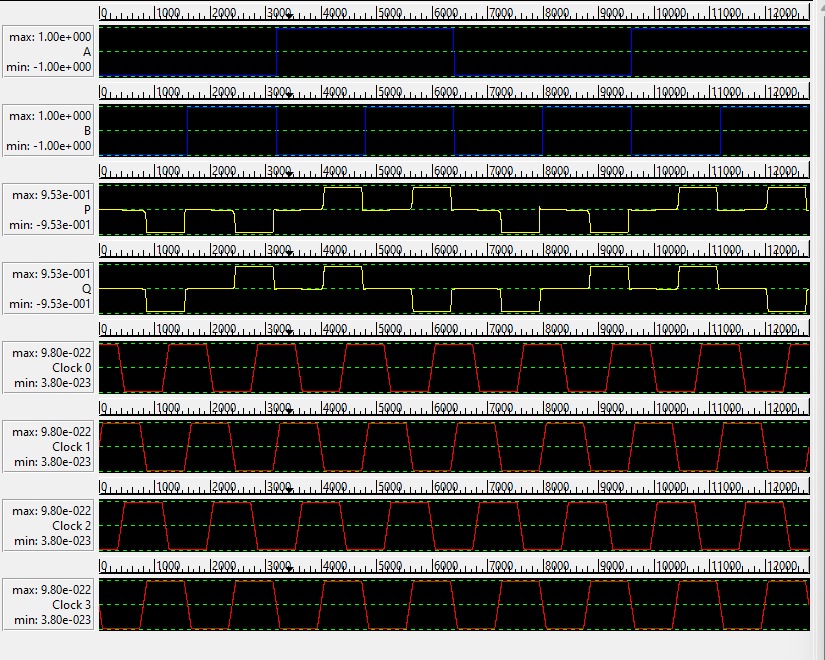


Figure 11(b). Output of the proposed XOR Gate.

A 2:1 multiplexer (mux) selects one of two input signals and passes it to the output based on a control signal. It acts as a data switch, allowing one of the inputs to be transmitted to the output line.

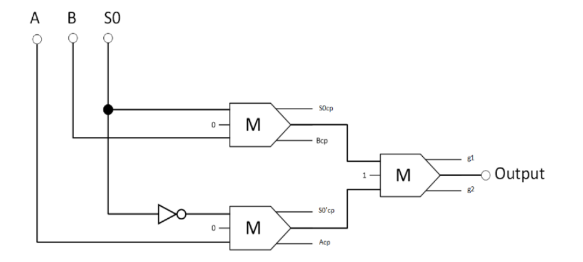


Figure 12. The synthesis of the proposed reversible 2:1 multiplexer (Acp, Bcp, S0cp, and S0′cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs.)

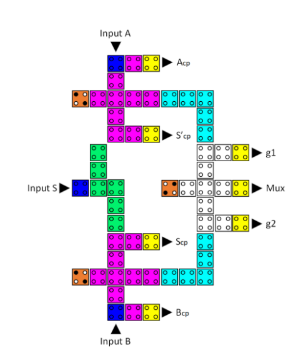


Figure 12(a). The layout of the proposed reversible QCA 2-to-1 multiplexer (Acp, Bcp, Scp, and S’cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

A 4:1 multiplexer (mux) takes four input signals and, based on a control signal, chooses one of those inputs to send to the output. It acts as a data selector, enabling the selection of one input from a set of four.

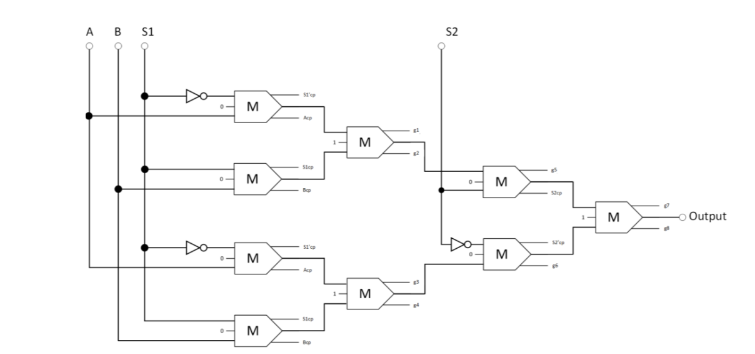


Figure 12.The synthesis of the proposed reversible 4:1 multiplexer (Acp, Bcp, S1cp, S2cp, S10cp, and S20cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs)

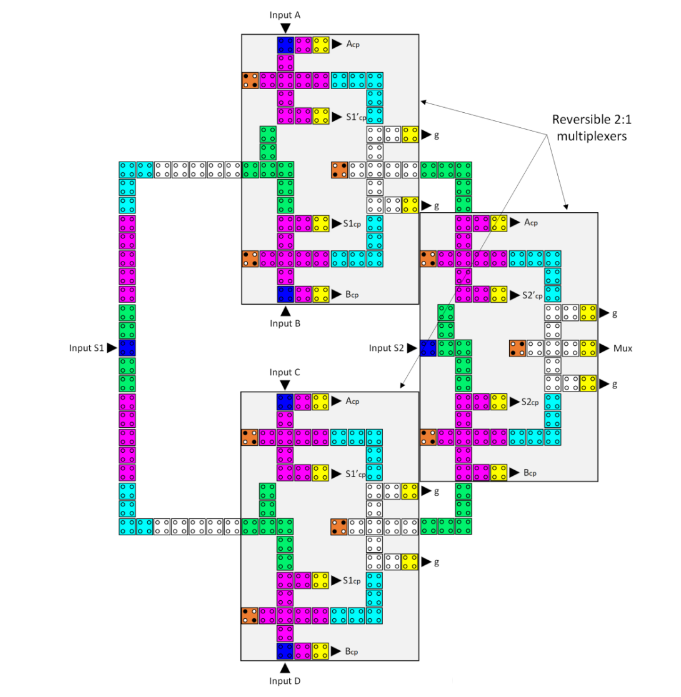
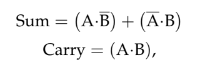


Figure 12(a) The layout of the proposed reversible QCA 4-to-1 multiplexer (Acp, Bcp, Ccp, Dcp,S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

A reversible half-adder is a digital logic circuit that computes the sum and carries outputs for two binary inputs while maintaining reversibility, meaning it can accurately recover the original inputs from the outputs.



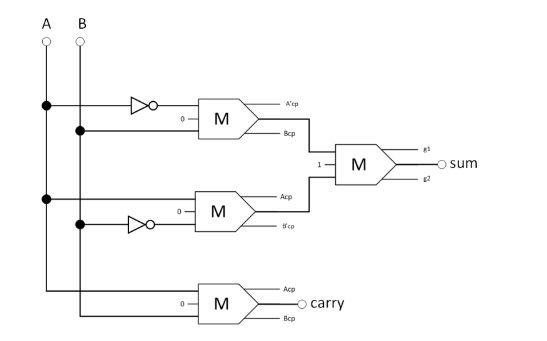


Figure 13. The synthesis of the proposed reversible half-adder (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

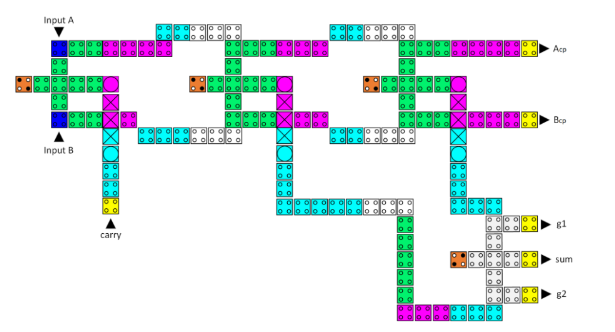
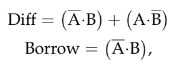
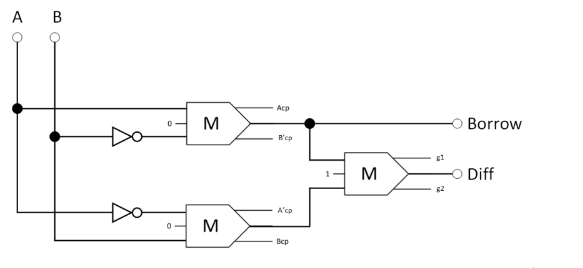


Figure 13(a). The layout of the proposed reversible QCA half-adder (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

A reversible half-subtractor is a digital logic circuit that computes the difference and borrows outputs for two binary inputs while remaining reversible, allowing the original inputs to be recovered from the outputs.



Figure 14. The synthesis of the proposed reversible half-subtractor (Acp, Bcp, A'cp, and B'cp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

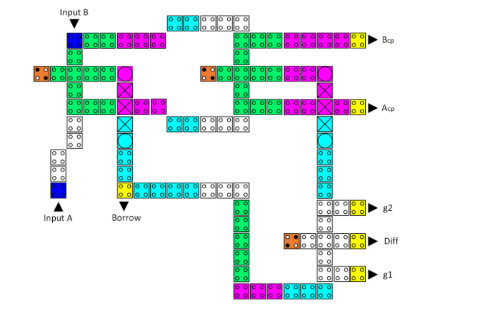


Figure 14(a). The layout of the proposed reversible QCA half-subtractor (Acp and Bcp refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

**Reversible Circuit (Logical Unit):**

A reversible QCA LU (Logic Unit) is a component in quantum-dot cellular automata that performs logical operations while maintaining reversibility. It can compute operations like AND, OR, XOR, and more, and it ensures that the original inputs can be accurately retrieved from the outputs.

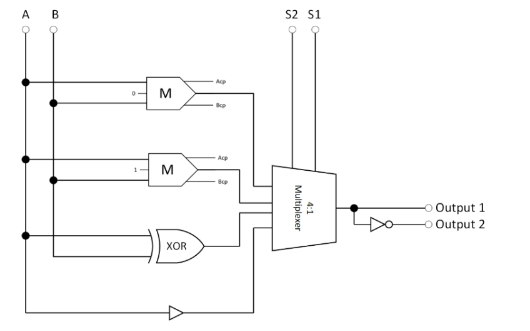


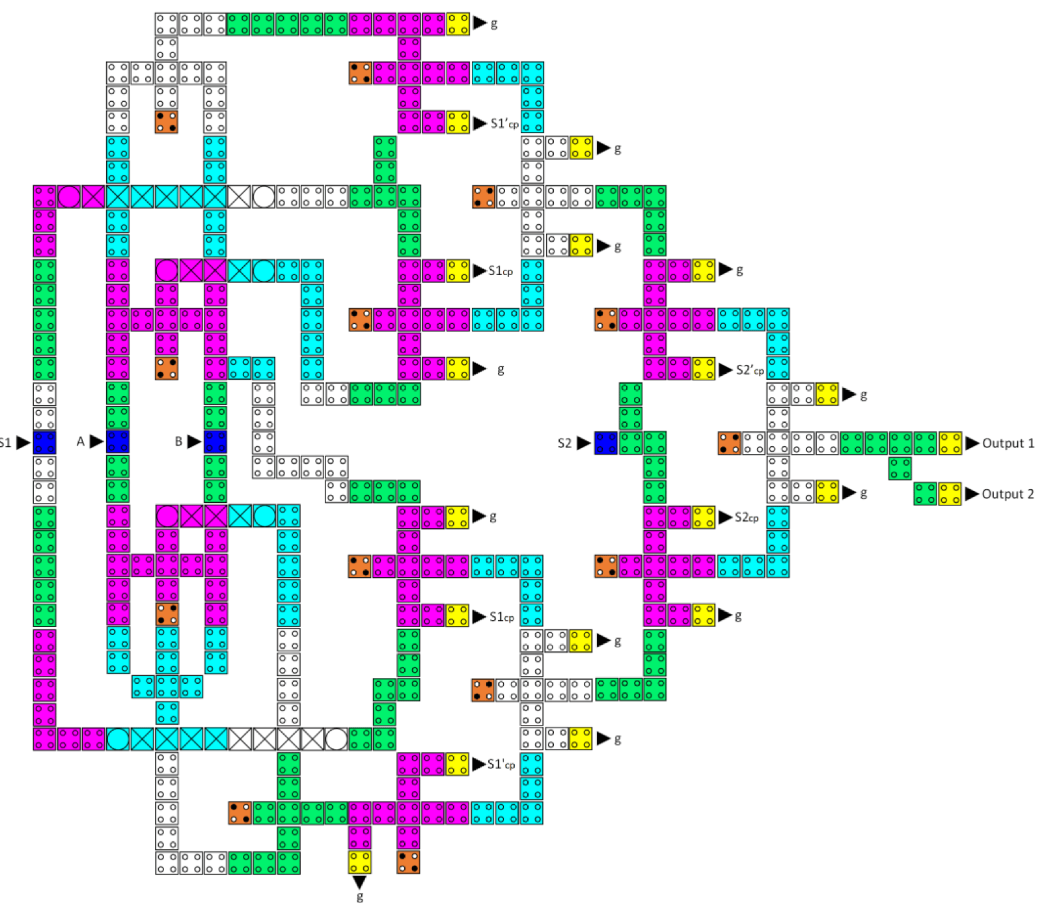
Figure 15. The synthesis of the proposed reversible LU (Acp and Bcp refer to copies of the inputs).  


Figure 15(a). The layout of the proposed reversible QCA LU (S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

**Reversible Circuit (AU):**

A reversible QCA AU (Arithmetic Unit) in Quantum-dot Cellular Automata handles arithmetic operations like addition, subtraction, multiplication, and division while preserving reversibility, allowing the original inputs to be recovered from the outputs.

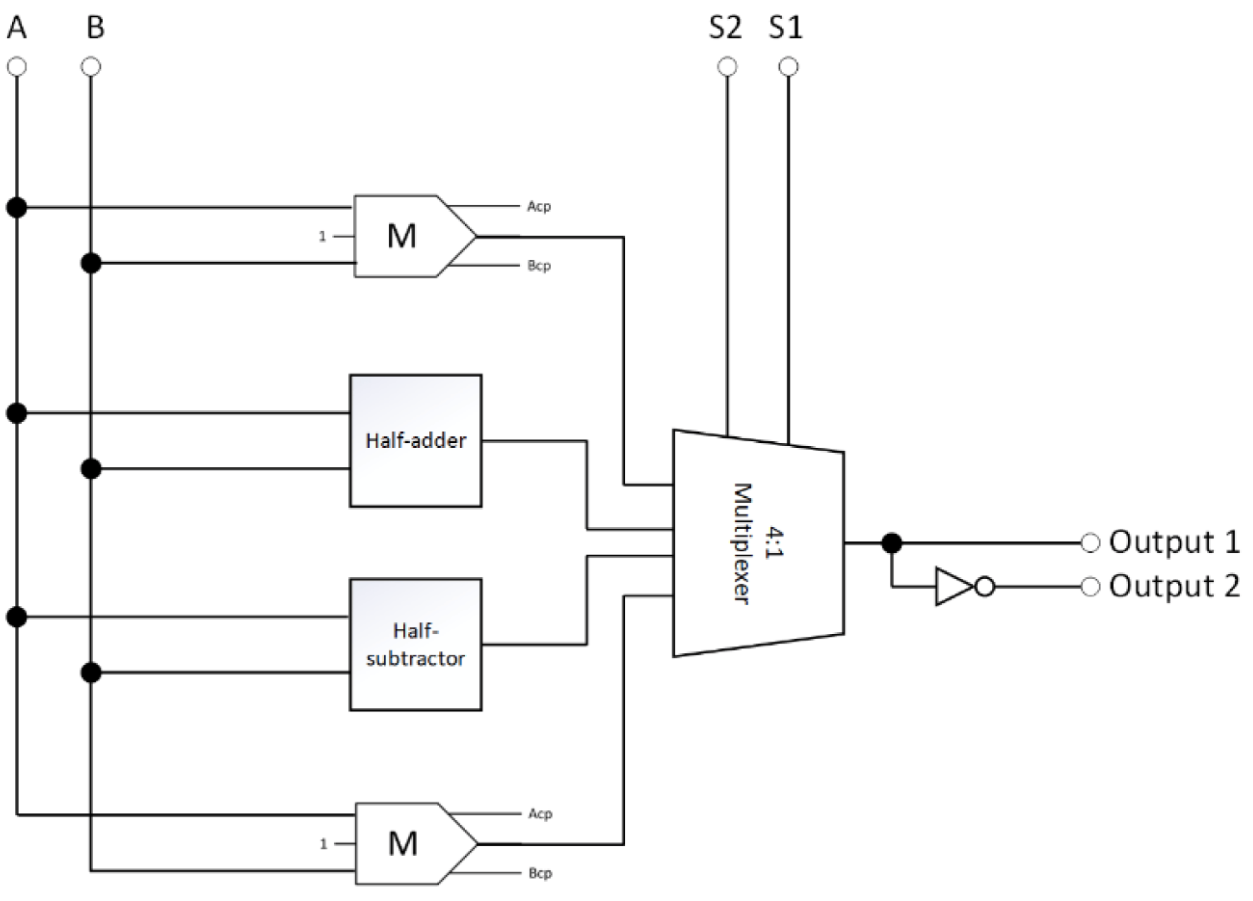


Figure 16. The synthesis of the proposed reversible AU (Acp and Bcp refer to copies of the inputs).

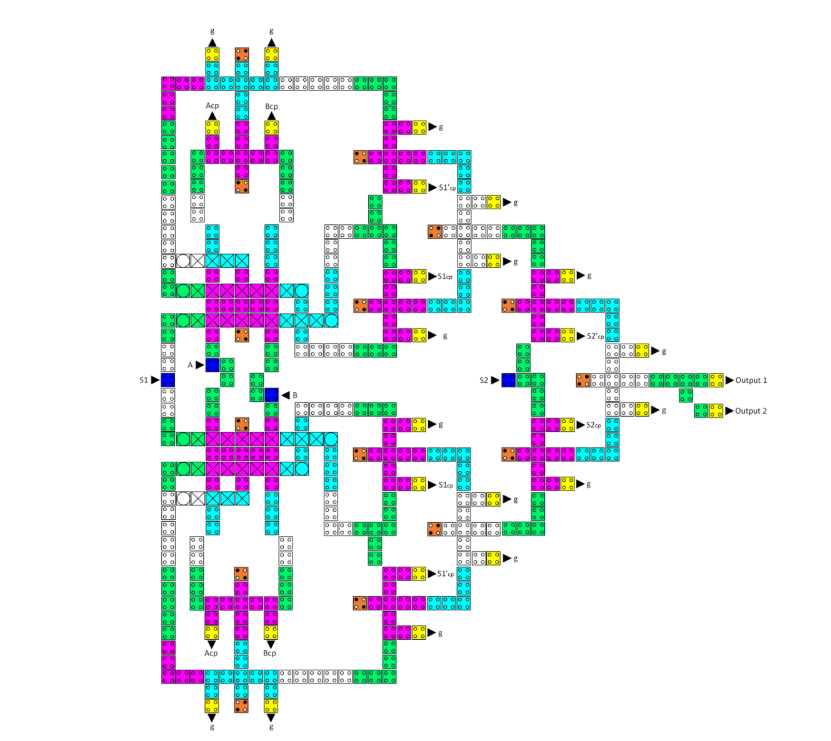


Figure 16(a). The layout of the proposed reversible QCA AU (Acp, Bcp, S1cp, S1'cp, S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

**Reversible Circuit (ALU):**

A reversible ALU is a digital circuit that performs arithmetic and logical operations while ensuring that the original input data can be perfectly reconstructed from the outputs. It's designed for energy efficiency and is crucial in low-power computing systems like Quantum-dot Cellular Automata (Q CA).

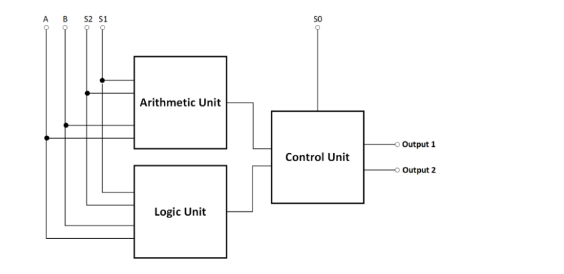


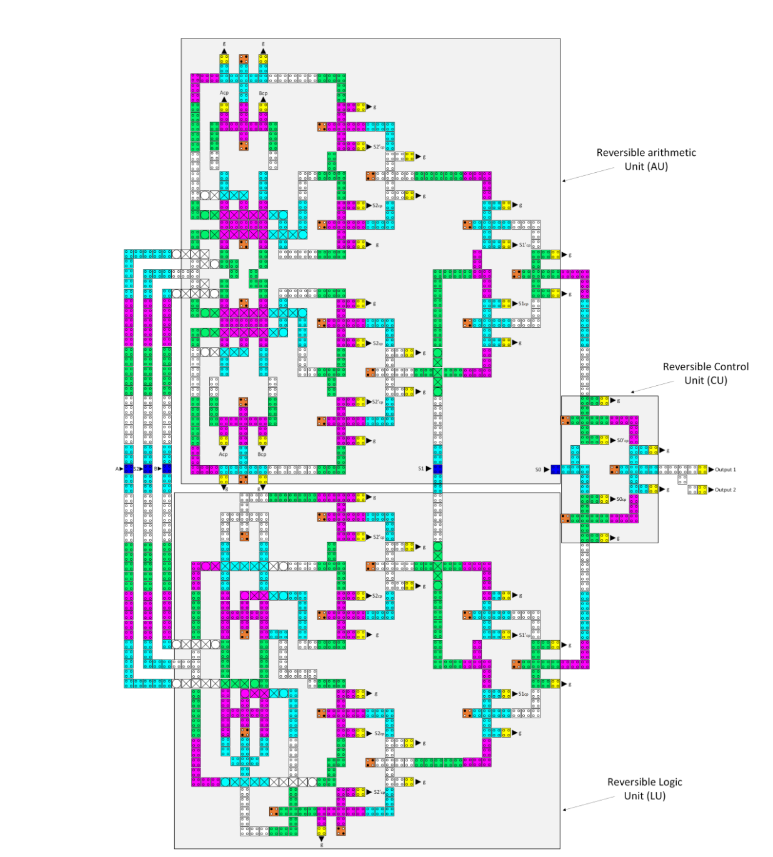
Figure 10. The High-level block diagram of the proposed reversible QCA ALU. 

Figure 10(a). The layout of the proposed reversible QCA ALU (Acp, Bcp, Ccp, Dcp, S1cp, S1'cp, S1cp, S1'cp,S2cp, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).

**Conclusions :**

In conclusion, this research has tackled a critical challenge in electronic devices: heat dissipation, through the innovative application of reversible QCA circuits. By introducing advanced gate designs like the CNOT and TOFFOLI gates, the study has not only reduced cell counts significantly but also enhanced energy efficiency. The introduction of a logically and physically reversible QCA ALU represents a major breakthrough, achieving exceptional energy efficiency and, critically, zero information loss. Through meticulous simulations, the study demonstrates minimal energy loss across the proposed designs. The proposed QCA ALU outperforms existing designs by a substantial 88.8% improvement in energy efficiency, accompanied by a marked reduction in cell count and physical footprint. As a prospect for the future, this research can pave the way for further advancements, including the extension of these

**References:**

1. Design and Analysis of a Novel Low-Power Exclusive-OR Gate Based on Quantum-Dot Cellular Automata (Research paper)
2. Nanomaterials-13-02445 (Research Paper)

**Contribution: Group Lead: Alkesh Shukla (S20210020252)**

I have Implemented the Toffoli Gate 2017, Proposed Double Toffoli Gate, Proposed Double Toffoli Gate and 5 NoT Gate, Proposed CNOT Gate, Reversible 2:1 MUX, CNOT Gate 2018, Reversible Half Adder, Reversible LU and Reversible AU.

**Anish Kamble (S20210020253)**

I have implemented Toffoli Gate 2019, Swap Circuit,Proposed Toffoli Gate, Proposed Double CNOT Gate, Reversible Half Subtractor, CNOT Gate 2019, Reversible 4:1 MUX, Reversible ALU, Reversible XOR Gate.

**Implemented Noval Circuit Circuit:**

We're teaming up to create a super-efficient Reversible Circuit. Our latest achievements include a Reversible XOR gate using a Majority Gate and a swap circuit using the Fredkin gate. These innovations are not only highly effective but also take up fewer cells.