Efficient Synthesis of Reversible CircuitsUsing Quantum Dot Cellular Automata

ABSTRACT: Heat dissipation in electronic devices is the main issue that needs to be taken into consideration. The primary source of heat dissipation in electrical equipment is bit-loss. Utilizing reversible circuits is the current fix for this issue. To show the efficiency of reversible computing of QCA, CNOT and TOFFOLI gates are mainly used. As QCA designs advanced, we saw a significant decrease in cell size, time delay, circuit area, and the quantity of majority gates.

INDEX TERMS: Quantum-dot cellular automata, Reversible gates, CNOT gate, TOFFOLI gate, SWAP Circuit, Polarization, Time Delay, Kink Energy.

INTRODUCTION:

The quantum-dot cellular automata (QCA) is a novel computing paradigm that uses charge configurations within cells to represent binary information rather than the more traditional use of current switches. The cells contain no current. For computing, the coulomb interaction is adequate.

Bit loss is an issue that is solved using reversible circuits. One of the outputs is used as the computation's input by these circuits. As a result, the electrical component won't suffer from data loss. To compile, QcaDesigner is being used. A nanoscale device is the QCA. Multiple cells are placed in the circuit in accordance with the design. The four clock stages in these cells are switch, hold, release, and relax. In general, there will be less delay, more speed, and less power dissipation as the size of the circuit lowers. A reversible circuit's principal gate is the CNOT gate, and its universal gate is TOFFOLI.

We will analyze many reversible CNOT gates, DOUBLE CNOT gates, TOFFOLI gates, and SWAP circuits from a particular data set. In terms of the cell count, circuit area, and delay, they differ. We must confirm that there is a reduction in computing latency from the circuit with more cells to the circuit with fewer cells.

In the CNOT gate, TOFFOLI gate, and SWAP circuit, we can see a large discrepancy in the latency, size of the circuits, and the number of cells employed. We looked at simulations to determine how to compute output delays.

QCA Basics

Ⅰ.Basics of quantum dot construction:

In general there are three statuses in the polarization of cells. Primary, secondary and tertiary status. Primary status in which electrons are not placed in any polarized manner. In secondary electrons are polarized positively and in tertiary electrons are polarized negatively.positive polarization denoted by (P=+1) and negative is denoted by (P= -1).

FIGURE Ⅰ. Polarization of the cell

Below equation represents KINK energy or says about the polarization of cells.

$$E^{i,j} = \frac{1}{4\prod \varepsilon_0 \varepsilon_r} \sum_{n=1}^{4} \sum_{m=1}^{4} \frac{qn^i qm^i}{|rn^i - rm^j|}$$

EQUATION - I

In the above equation ε0 permittivity of free space, εr is dielectric constant, qn_i is charge in dot n of cell

i, rn_i i is the position of the dot in cell i,$|rm_i - rm_i|$ is the distance between the cells

Kink energy is the Energy difference between two cells with opposite polarity or the same polarity. Where E is the energy, P is the polarization of the cells n and P is the polarization of the cell m.

$$Ekink^{n,m} = E^{n,m}_{Pn \neq Pm} - E^{n,m}_{Pn=Pm}$$

EQUATION - Ⅱ. **Kink energy**

P_i gives the measurement of the polarization of each cell. Where pi is the polarization state of the cell, P is the polarization state of the neighboring cell, γ is the tunneling energy of the electron within the cell.

$$P_i = \frac{\frac{Ekink^{i,j}}{2\gamma}\sum jP_j}{\sqrt{1 + \left(\frac{Ekink^{i,j}}{2\gamma}\sum jP_j\right)^2}}$$

EQUATION -Ⅲ

Ⅱ. Qca wires

QCA cells perform computation by interfacing coulombically with neighboring cells to influence each other's polarization. The binary signal propagates from left to right because of the coulombic interactions between cells.

FIGURE Ⅱ represents 90 degrees-oriented cells whereas in **FIGURE** Ⅲ the cells are in 45 degrees orientation.

For example, if we are having input cell-1 with polarization (p = -1) and the next cell-2 with (p = +1) polarization, then a binary " 0 " (due to the input cell being polarized to -1) will propagate down the length of the wire because of the coulombic interaction between cells.

The main advantage of 45 deg wire is that we will get both the transmitted signal and its complement value without using an external inverter circuit.

FIGURE Ⅱ **45-degrees cells**

FIGURE Ⅲ

Figure 4 and Figure 5 says about the planarity of the QCA wires, in fig 4 the wires are crossing in a single layer and in fig-5 the wires are in multilayer so it is called multilayer crossing. The information transfers throw 'via' in multilayer crossing.

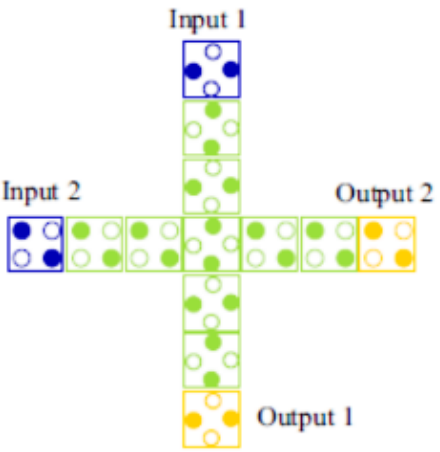

FIGURE Ⅳ. Coplanar Crossing

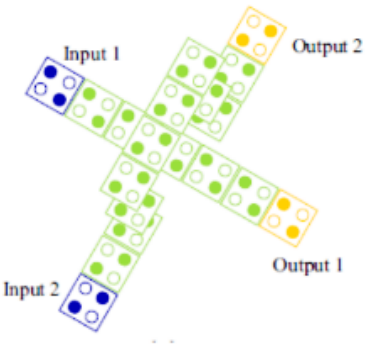

FIGURE Ⅴ**. Multi-Layer Crossing**

Ⅲ. Qca majority gate and inverter:

Majority Voting(MV) gate has 5 cells in total. The general output equation of the MV gate is xy+yz+zx, where x, y and z are inputs to the MV gate.MV gate is in the form of '+'.

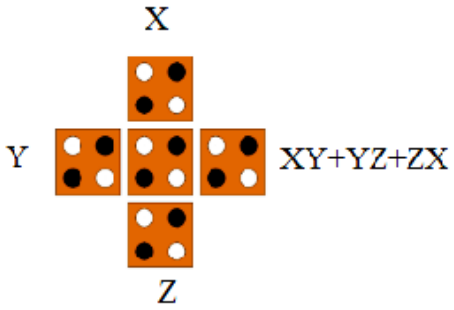

FIGURE Ⅵ. MV Gate

MV gate can also be used as AND gate and OR gate. This can be done by setting one of the input cells to a positive or negative polarization. Positive polarization gives OR gate functionality to the MV gate f(X, Y) = X+Y.

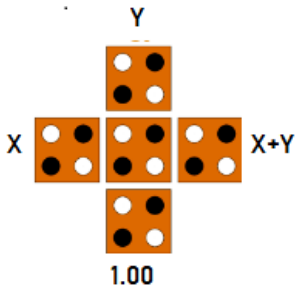

FIGURE Ⅶ. OR gate using MV gate

Negative polarization gives AND gate functionality to the MV gate f(X, Y) = X.Y.

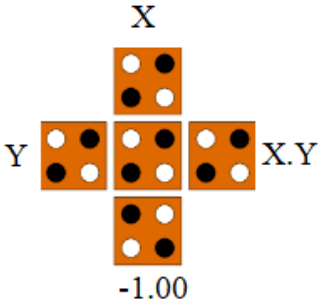

FIGURE Ⅷ. AND Gate using MV Gate

NOT Gates are also known as inverters.NOT gate inverts the inputs i.e, It converts 0 to 1 and vice versa. FIGURE Ⅸ and FIGURE Ⅹ are examples of NOT gates. FIGURE Ⅸ also called a ROBUST inverter because it has 2 ways to reach the output, chance of data loss is decreased due to multiple inputs. whereas FIGURE Ⅹ has only 1 way.

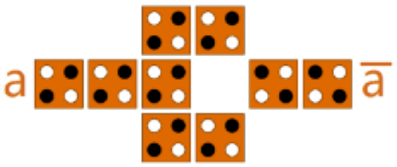

FIGURE Ⅸ. ROBUST inverter

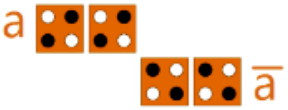

FIGURE Ⅹ. Inverter

The functionality of the FIGURE Ⅹ Ⅰ QCA Design is NAND Gate. It is the combination of NOT gate and AND gate with negative polarization.

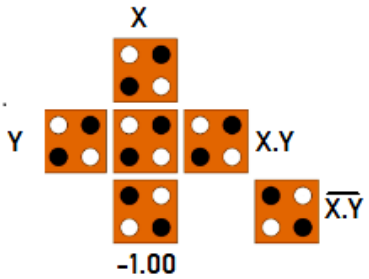

FIGURE Ⅹ Ⅰ. NOR Gate Using MV Gate

Ⅳ. Qca clocking

The clocking of QCA is achieved by measuring capacity barriers to the connected quantum dots. It controls the information flow and the synchronization in the circuit.

This clocking contains four phases 1)Switch 2)Hold 3)Release 4)Relax.

1) Switch phase: In this phase, the unpolarised electrons in cells are driven by some input and get polarized depending on their neighbor's polarization.

2) Hold: In this cells are held in some finite polarization either in high or low, simply a binary state.

3) Release: Here the given potential decreases gradually so that the cells lose their polarization slowly.

4) Relax: finally potential decreased completely hence cells remain in an unpolarised state or NULL state.

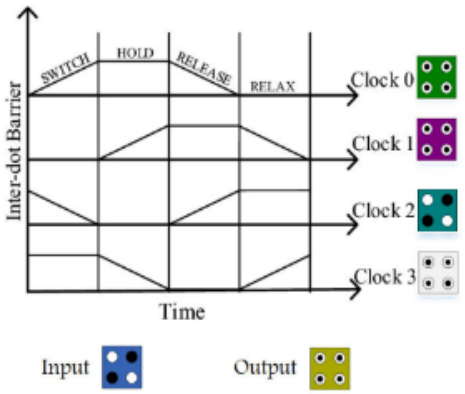

FIGURE Ⅹ Ⅰ I. Clock phases

Ⅴ. Layout design rules

1) A single clock zone with the most cells possible: If the cells present in the same clock zone are maximum then it leads to maximum errors in the circuit. So to prevent this problem we use EQUATION-IV, which says about the number of cells to be present in the same clock zone.

$$N \leq \frac{E_k}{e^{kB}T}$$

EQUATION -IV

In this equation N represents the cell count in an array, T represents the operating temperature, and Ek represents the kink energy. As the number of cells is inversely proportional to the operating temperature, if the size of the cell decreases then the count of cells increases in the wire hence the operating temperature decreases as it is inversely proportional to T . If we run our circuit at higher temperatures the size of the cell decreases.

The data transferring speed decreases if the size of the wire is long and it will take more time to propagate the signal from one input to another. To increase the data transfer speed we divided long wires into smaller ones with different clock zones.

2) A single clock zone with the fewest possible cells:
After dividing the large wire into smaller ones then each cell presents in its corresponding clock zone. If only one cell is present in one clock zone then there is a sudden change in direction of the signal that we are sending because of this sudden change errors will occur in results.

Therefore, we are limited to having a minimum of two cells in each clock zone in order to prevent this issue.

3) Possible Crossover:
As we have discussed earlier in the QCA WIRES section FIGURE Ⅳ and FIGURE Ⅴ represent coplanar and multilayer crossover.

In FIGURE IV, we correctly aligned both the 45 and 90-degree cells to avoid interference. A reliable operation of coplanar crossing is dependent on the temperature of the operation. As our main focus is on the condition of the wire, data transmission in the wire and power dissipation in QCA circuits.

We can choose the second type of crossover instead of coplanar crossover, it contains different layers on top of each other which reduces space and increases data transmission rate than coplanar circuits. We have advantages with multilayer crossover over coplanar but it is difficult to create multilayer wires.
So at present, we are bound to use coplanar crossover.

4) Timing design rules:
For instance, if two wires are connected in a coplanar crossover with inputs 1 and 2, practically both inputs must arrive at the junction simultaneously.

However, this won't happen in our reality circuit since the two wires are different lengths, therefore we must design the wires so that they are both in the same clocking zone and that there is a cell at the junction as well.

Temperature	1.000000
Cell Width(nm)	18.000000
Cell Height(nm)	18.000000
Relaxation Time	1.000000×10^(-15)
Time Step	1.000000×10^(-16)
Total Simulation Time	7.000000×10^(-11)
Clock High	9.800000×10^(-22)
Clock Low	3.800000×10^(-23)
Clock Shift	0.000000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000
Relative Permittivity	12.900000
Layer Separation	11.500000

REVERSIBLE LOGIC GATE:

The gates with the attribute of having an equal number of inputs and outputs are known as reversible gates or reversible logic gates. The amount of energy lost will be minimized when the number of inputs and outputs is equal.QCADesigner is used to simulate circuits and generate graphs of the outcomes. Different logic gates with various circuit layouts have been compared at various periods. We compared cell count, cell area, delay, MV gates, and wire crossover at the conclusion of each of the different gate circuits.

1] CNOT GATE

One qubit serves as the "control" and the other as the "target" in the controlled-NOT gate, also known as the controlled-x (CX) gate. Every time the control is in the state, it executes a NOT on the target. This gate induces entanglement in the case of a superposition of the control qubit.

The truth table of the CNOT gate. They are used to compare the output from the simulation for the verification of correctness.

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

TABLE 1: **CNOT Gate**

A) Feynman Gate - 2019

Feynman gate is proposed in the year 2019

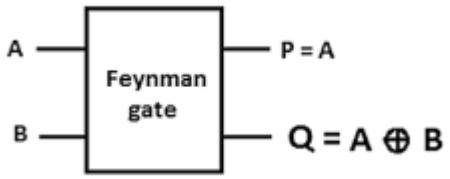

FIGURE 1(A) - Circuit representation of CNOT gate

The logical equation of the outputs are represented as

P = A
Q = A^B

In the logical expression ' ^ ' is referred to as XOR.

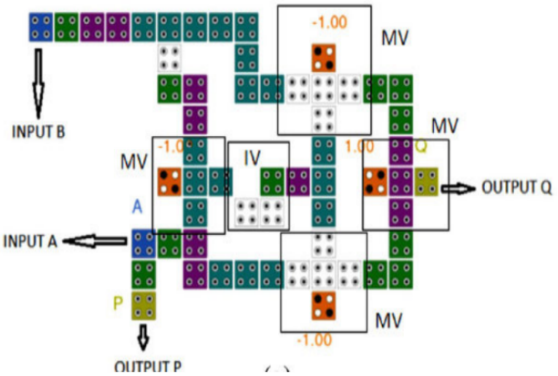

FIGURE 1(A) Feynman - 2019

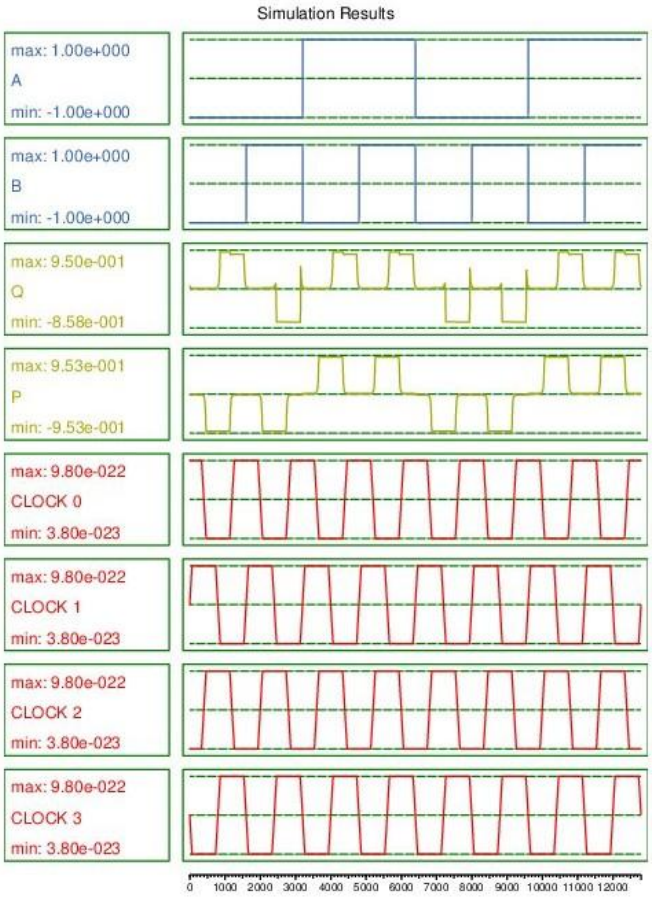

FIGURE1(A) - Feynman - 2019 Simulation

B) Feynman Gate - 2018

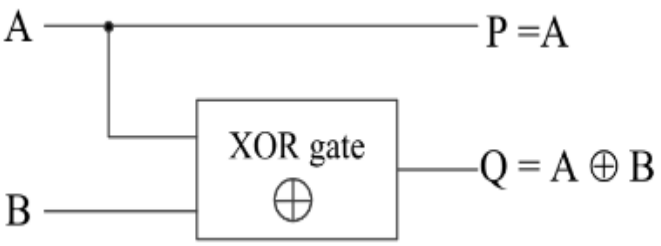

FIGURE 1(B) - Circuit representation of CNOT gate

For the circuit representation of CNOT Gate, A and B are inputs, P and Q are the Outputs. The logical equation of the outputs is represented as

$$P = A$$

$$Q = A \hat{} B$$

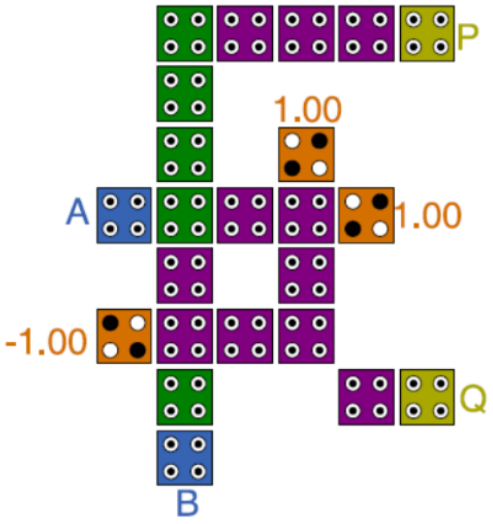

FIGURE 1(B) -Feynman Gate- 2018

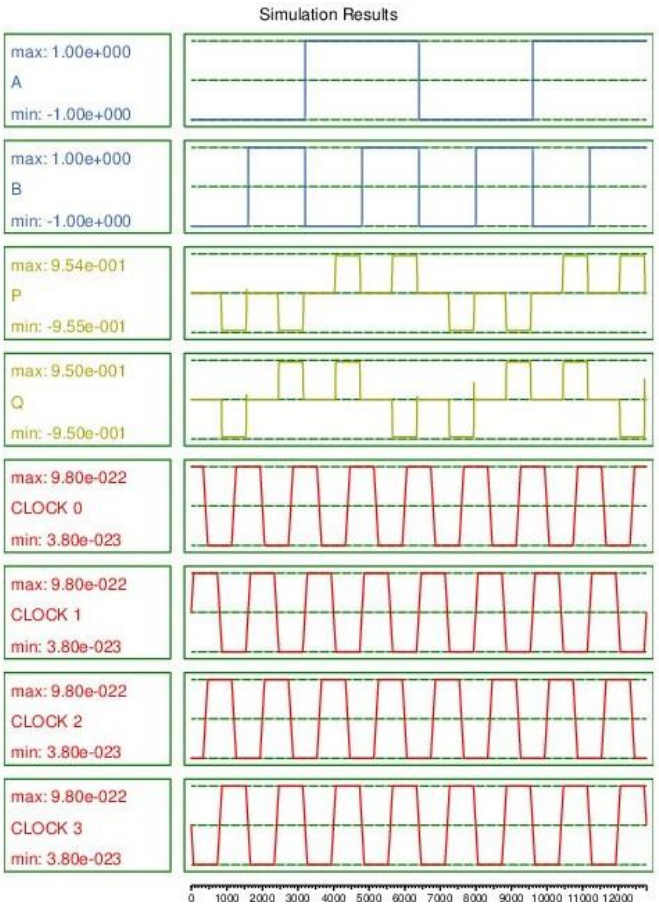

FIGURE1(B) - Feynman Gate Simulation-2019

C) Proposed CNOT Gate:

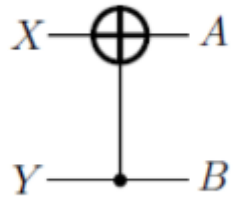

FIGURE 1(C) - Circuit representation of CNOT gate

From the circuit representation of the CNOT gate, X and Y are inputs, and A and B are the outputs of the circuit. The logical equation of the outputs is represented as

A = X^Y

B = Y

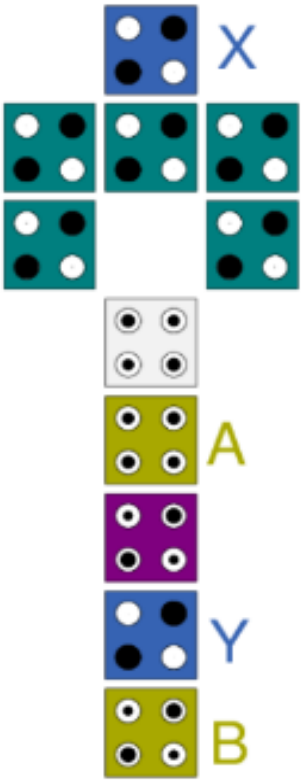

FIGURE 1(C) - proposed CNOT Gate

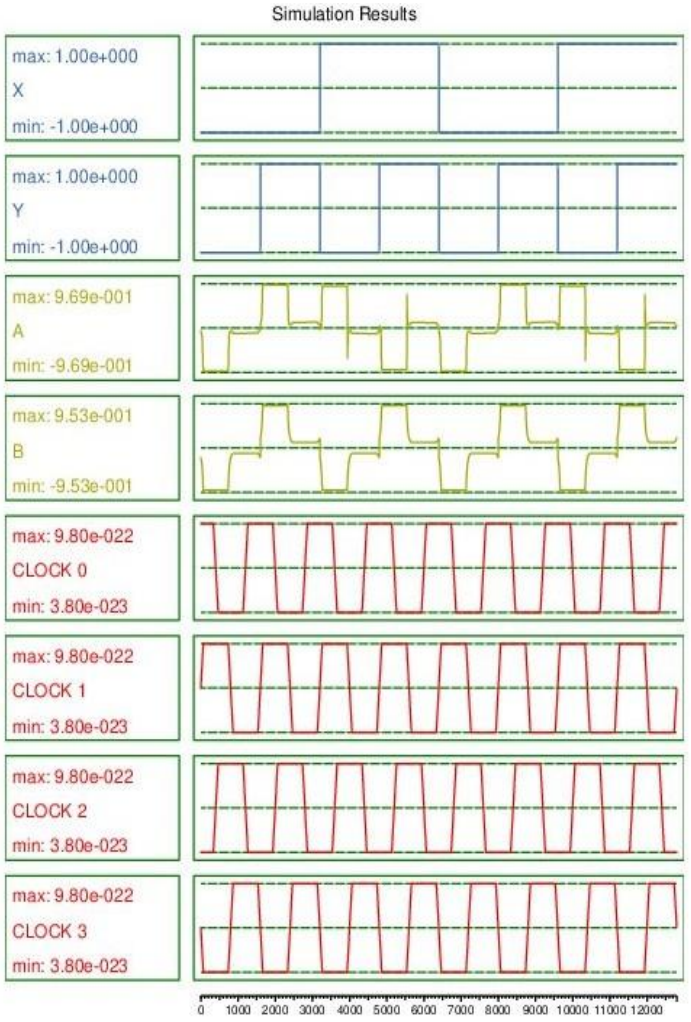

FIGURE 1(C) - proposed CNOT Gate Simulation

Comparison:

CNOT Gate	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
1(A)	58	15660	1.5	4	coplanar
1(B)	23	7452	0.5	2	Not required
1(C)	11	3564	0	0	None

Majority voter(MV) gates cause a delay in the circuit. The Delay of the proposed circuit is zero. It is due to zero mv gates and doesn't carry any garbage values in the Output. From the graph, There is no delay between the rising edge of the input to the corresponding output that is negligible.

2] DOUBLE CNOT GATE

The QCA layout standards, which require that all input cells should arrive in the same time zone, are followed by all of the recommended designs. Long QCA wires should be separated into numerous clock zones while taking into account the maximum number of cells and the minimum number of cells in the same zone to minimize excessive signal propagation and switching delays. There are no crossover options in any of the proposed designs.

Truth Table:

Two input and 2 output

X	Y	A	B
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

TABLE 2: Double CNOT Gate 2 INPUTS

Three inputs and three outputs

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE 3: Double CNOT Gate 3 INPUTS

A) Double Feynman gate - 2017

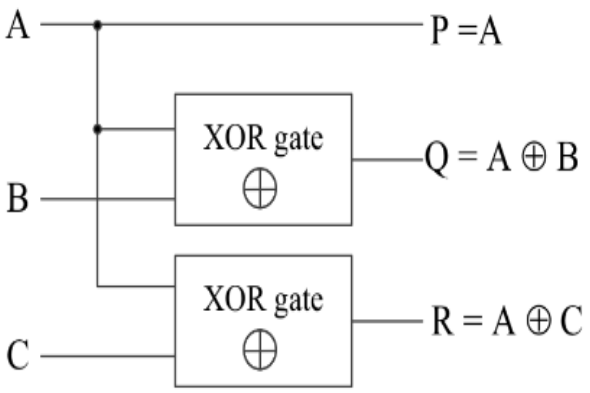

FIGURE 2(A) - Circuit representation of Double CNOT gate-2017

9A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A

Q = A ^ B

R = A ^ C

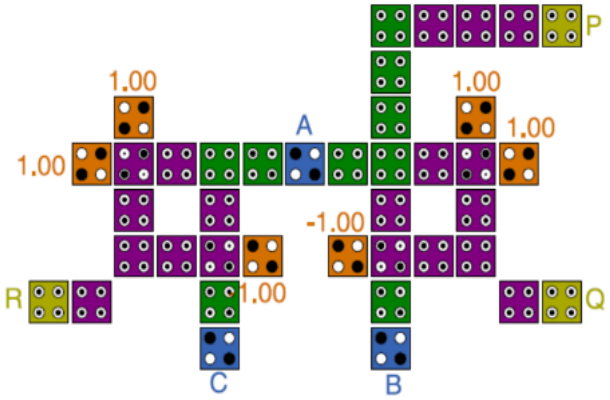

FIGURE 2(A)- Double CNOT Gate-2017

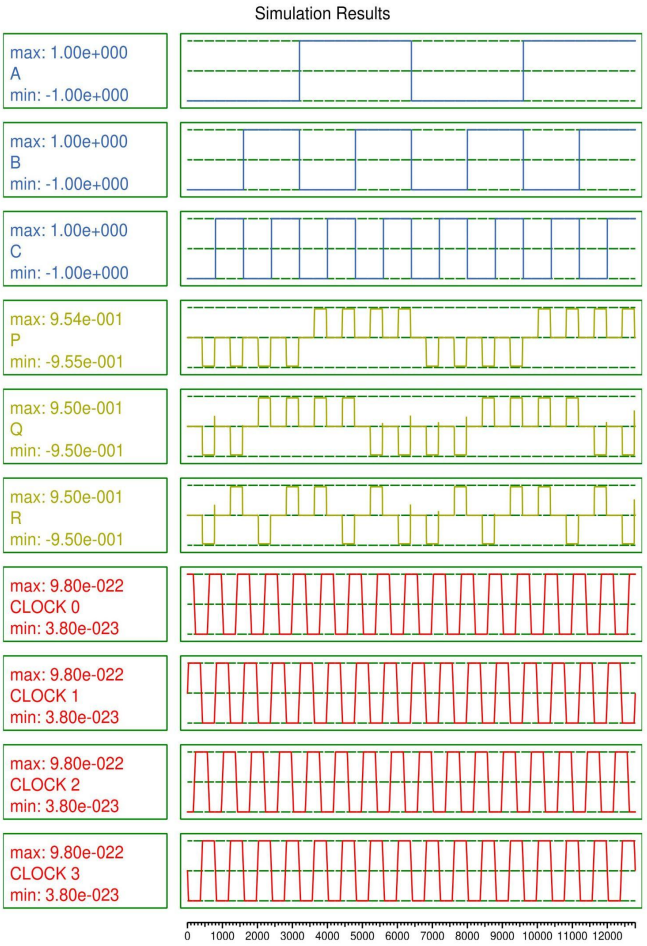

FIGURE 2(A) -Double Feynman Simulation-2017

B) Proposed Double CNOT Gate:

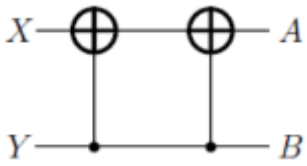

FIGURE 2(B) - Circuit representation of Double CNOT gate

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 1(C) Circuit representation is

$$A = (X \hat{} Y) \hat{} Y$$

$$B = Y$$

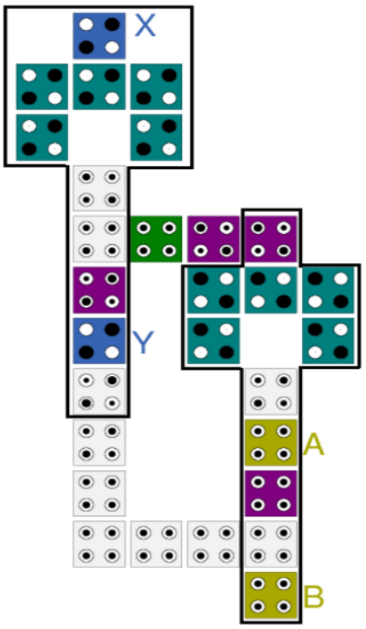

FIGURE 2(B) - Proposed Double CNOT Gate

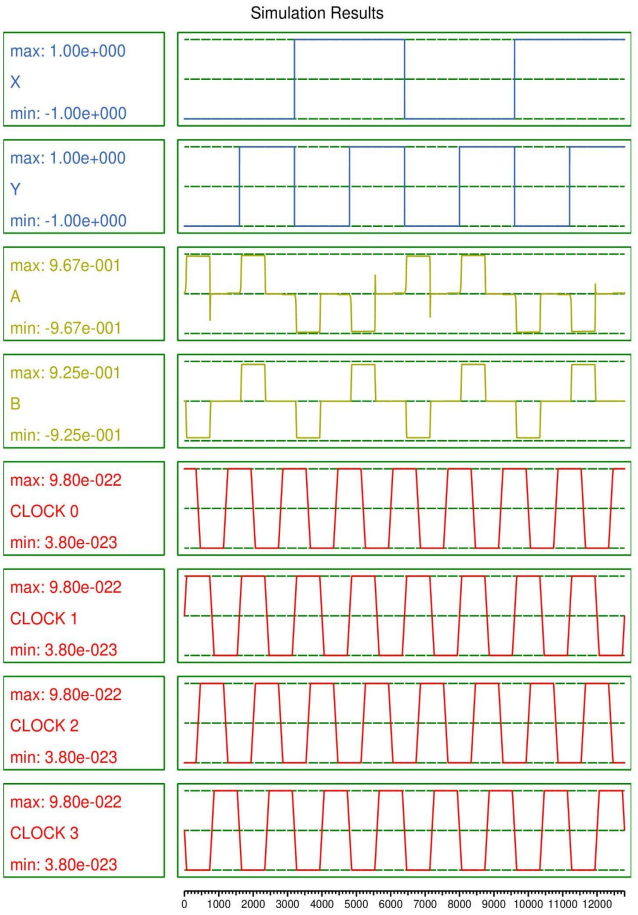

FIGURE 2(B) - Proposed Double CNOT Gate Simulation

Comparison:

DOUBLE CNOT Gate	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
2(B)	29	9396	2	0	None
2(A)	40	12960	4	4	Coplanar

3] TOFFOLI GATE

A universal reversible gate, or TOFFOLI gate was proposed by Tommaso Toffoli and can be used to create the reversible analogue of any classical gate. It is also known as the "controlled-controlled-not" gate. It inverts the third bit if the first and second bits are 1.

Truth Table:

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	0	1	1

TABLE 3: TOFFOLI GATE

A) TOFFOLI GATE - 2019

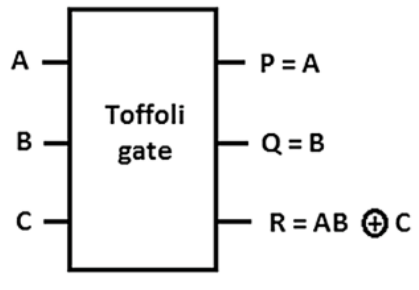

FIGURE 3(A) - Circuit representation of TOFFOLI gate-2019

A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A
Q = B
R = (A . B) ^ C

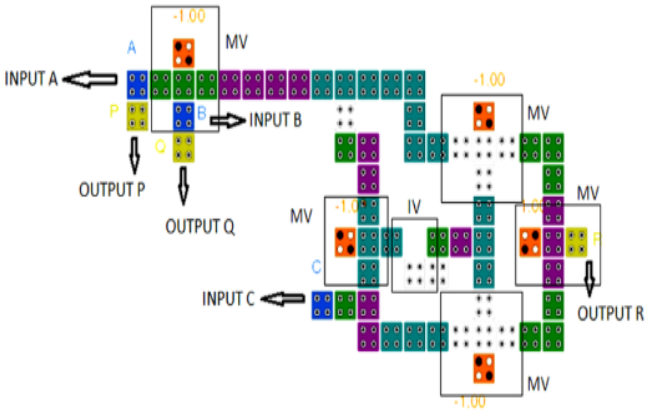

FIGURE 3(A) - TOFFOLI gate-2019

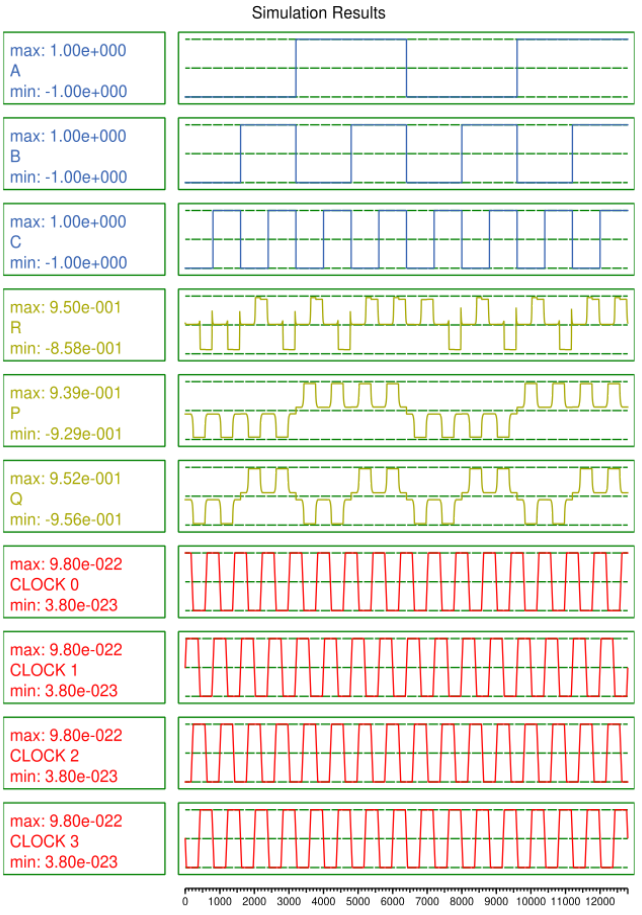

FIGURE 3(A) - Simulation

B) TOFFOLI GATE - 2017

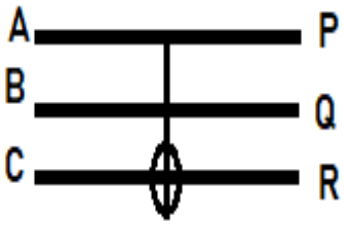

FIGURE 3(B) - Circuit representation of TOFFOLI gate

A, B and C are inputs of the circuit and P, Q and R ate outputs. The logical equation of the outputs of figure 2(A) Circuit representation is

P = A

Q = B

R = (A . B) ^ C

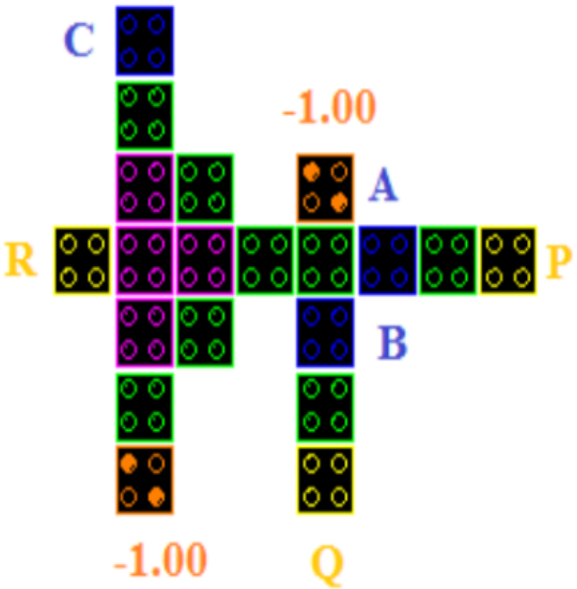

FIGURE 3(B).TOFFOLI Gate-2017

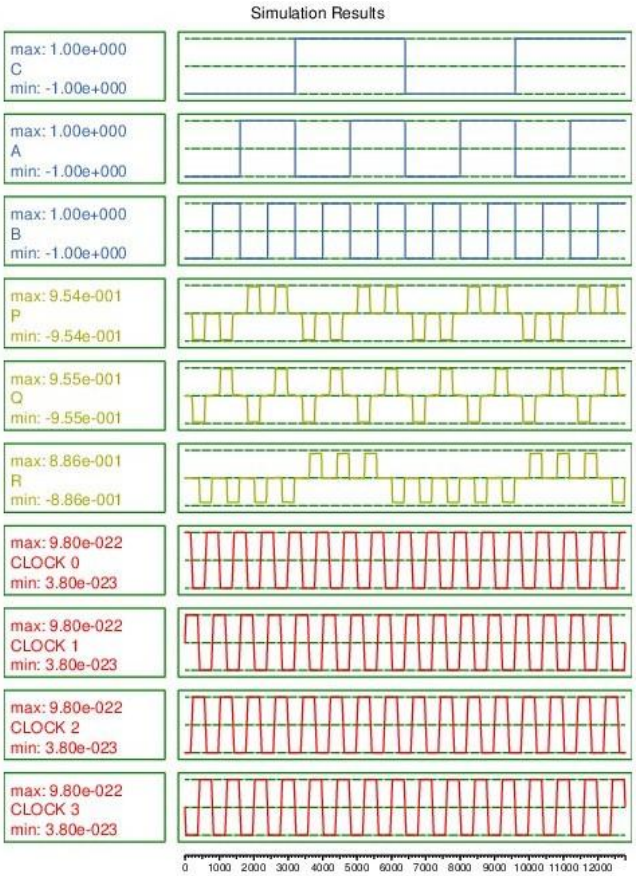

FIGURE 3(B) TOFFOLI Gate-2017- Simulation

C) Proposed TOFFOLI gate:

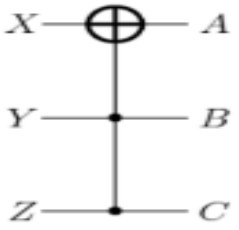

FIGURE 3(C) - Circuit representation of TOFFOLI gate

X, Y, and Z are the inputs and A, B, and C outputs. The logical equation of the outputs of figure 3(C) Circuit representation is

A = X^ (Y.Z)

B = Y

C = Z

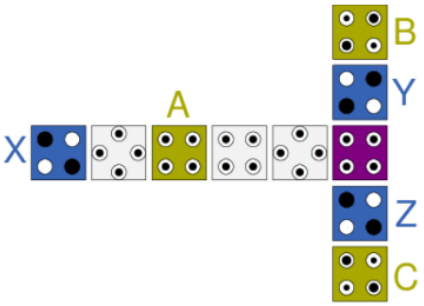

FIGURE 3(C) - proposed Toffoli Gate

In the proposed TOFFOLI Gate X, Y and Z are the Inputs of the circuits. There is the direct Transfer of the data from outputs A, B and C respectively.

FIGURE 3(C) -proposed Toffoli Gate simulation

Comparison:

TOFFOLI Gate	Cell count	Cell area (nm2)	Dela y	MV gates	Wire crossover
3(A)	64	20736	1.5	5	Coplanar
3(B)	34	11016	0.75	3	Multilayer
3(C)	10	3240	1	0	None

4] DOUBLE TOFFOLI GATE

Truth Table:

X	Y	Z	A	B	C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

TABLE 4: DOUBLE TOFFOLI GATE

A) Proposed DOUBLE TOFFOLI gate

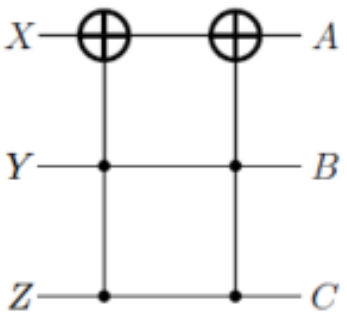

FIGURE 4(A) - Circuit representation of DOUBLE TOFFOLI gate

X, Y, Z are the inputs and A, B, C outputs. The logical equation of the outputs of figure 4(A) Circuit representation is

A = (X^(Y.Z))^(Y.Z)

B =Y

C = Z

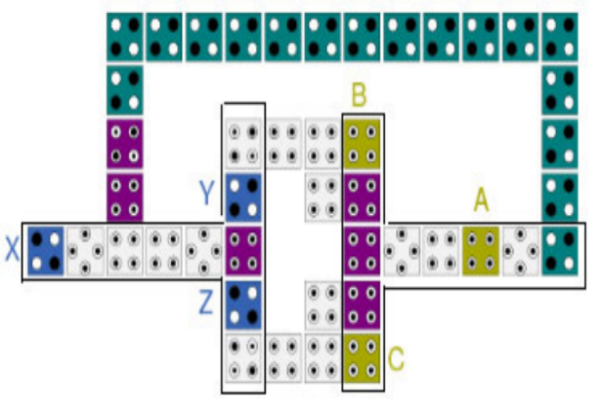

FIGURE 4(A)-proposed Double TOFFOLI Gate

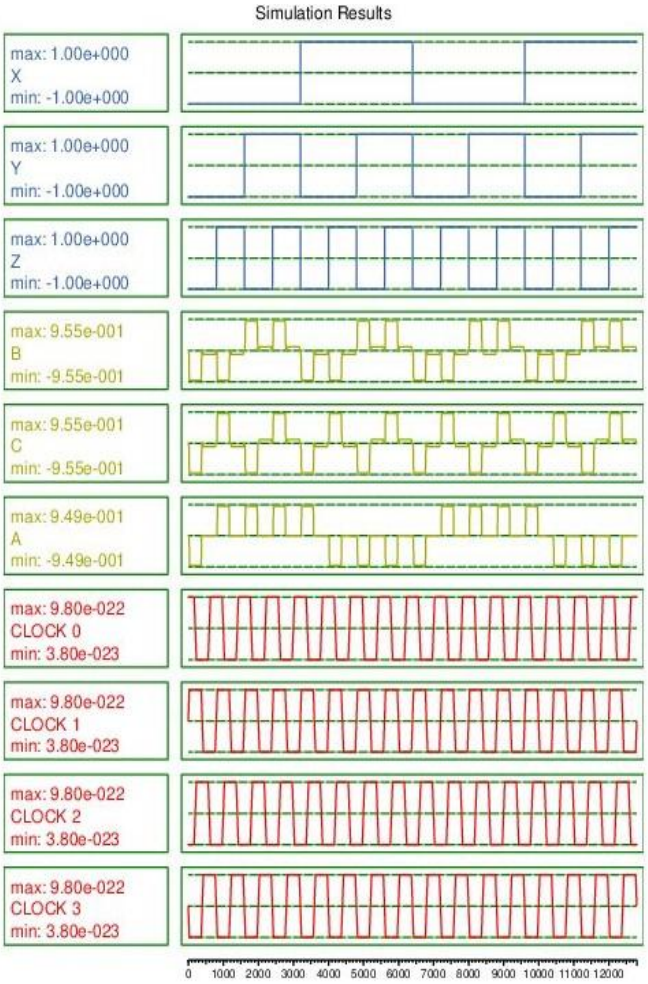

FIGURE 4(A)-proposed Double TOFFOLI GateSimulation

5]SINGLE TOFFOLI WITH 5 NOT GATES

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

TABLE 5: SINGLE TOFFOLI GATE AND 5 NOT GATES

A) Proposed SINGLE TOFFOLI GATE AND 5 NOT GATES

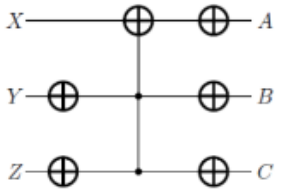

FIGURE 5(A) - Circuit representation of SINGLE TOFFOLI GATE AND 5 NOT GATES

X, Y, Z are the inputs and A, B, C outputs. The logical equation of the outputs of figure 5(A) Circuit representation is

A = [~(X^(~Y . ~Z))]

B = Y

C = Z

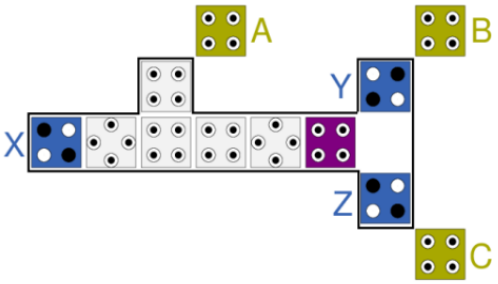

FIGURE 5(A)-proposed SINGLE TOFFOLI GATE AND 5 NOT GATES

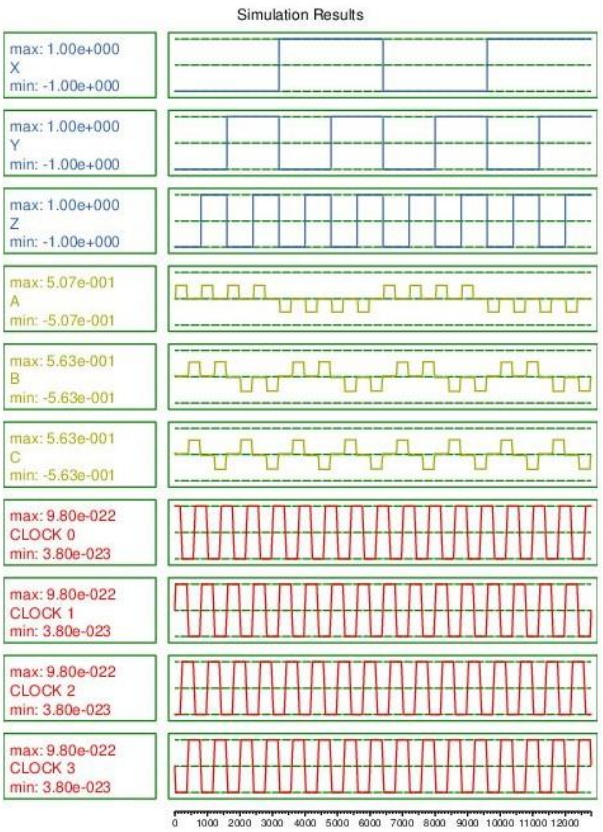

FIGURE-5(A)-SINGLE TOFFOLI GATE AND 5 NOT GATES Simulation

6) SWAP CIRCUIT

The inputs of the swap circuits are swapped and shown as the outputs in this circuit.

Truth Table:

X	Y	A	B
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

TABLE 6: SWAP CIRCUIT

A)SWAP Circuit 2017

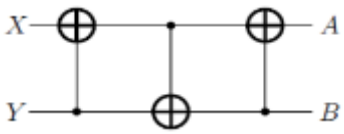

FIGURE 6(A) - Circuit representation of SWAP Circuit

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 6(A) Circuit representation is

$$A = (X \wedge Y) \wedge (Y \wedge (X \wedge Y))$$

$$B = Y \wedge (X \wedge Y)$$

FIGURE 6(A)-SWAP Circuit-2017

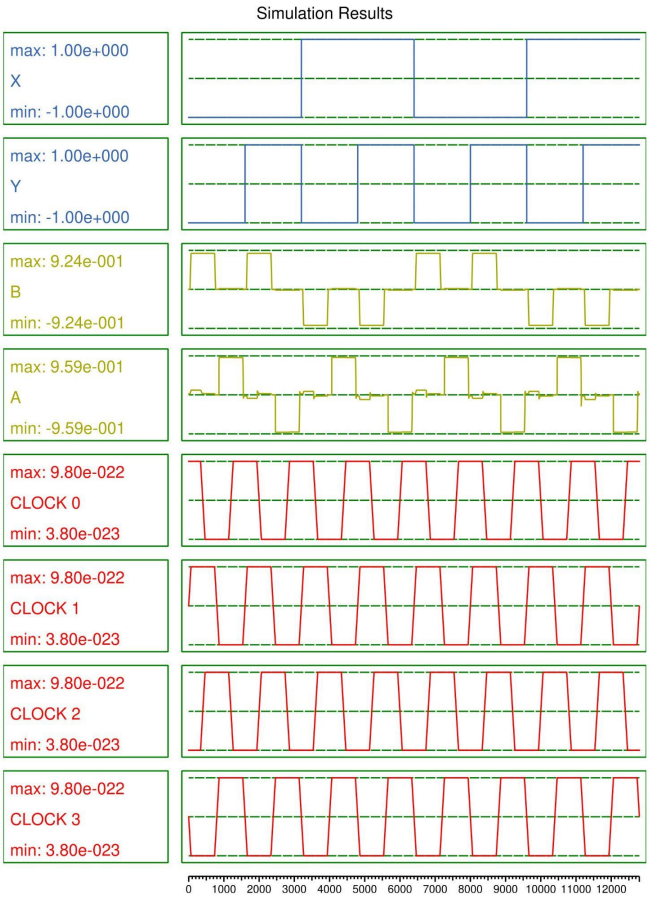

FIGURE 6(A)-Swap Circuit Simulation-2017

B) proposed SWAP circuit

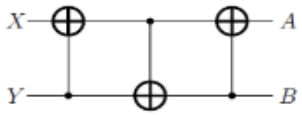

FIGURE 6(B) - Circuit representation of SWAP Circuit

X and Y are inputs of the circuit and A and B are the outputs. The logical equation of the outputs of figure 6(A) Circuit representation is

A =(X^Y)^(Y^(X^Y))

B = Y^(X^Y)

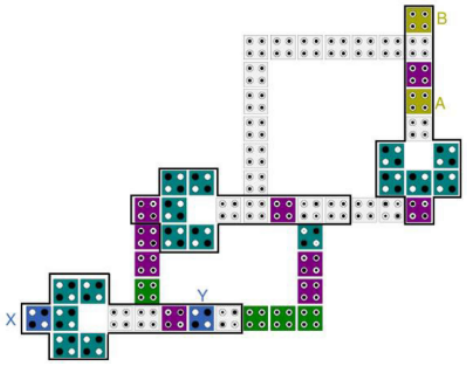

FIGURE 6(B)-proposed SWAP Circuit

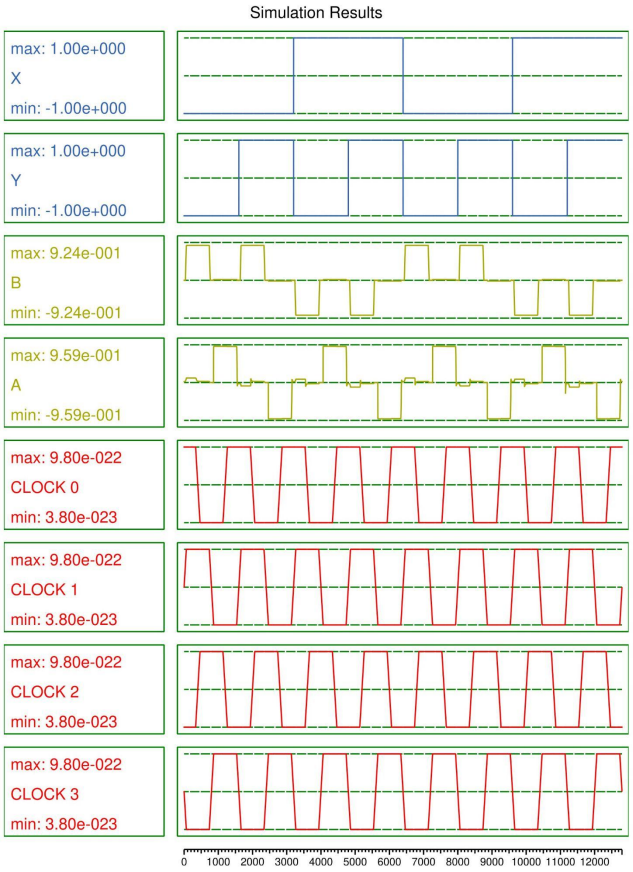

FIGURE 6(B)-Swap Circuit Simulation

Comparison:

SWAP Circuit	Cell count	Cell area (nm2)	Delay	MV gates	Wire crossover
6(A)	135	43750	2.75	0	Multilayer
6(B)	55	17820	2	0	None

CONCLUSION:

The fundamental problem with electronic devices is heat dissipation, which may be solved by adopting reversible QCA circuits. A primary gate is CNOT, while a universal gate is TOFFOLI. They have used mainly these gates and proposed the latest versions of the CNOT gate, DOUBLE CNOT gate, TOFFOLI gate, DOUBLE CNOT gate, single TOFFOLI with 5 NOT gates and SWAP circuit. The circuit's efficiency is affected by a number of factors, including (i) cell count, (ii) cell areas, and (iii) polarization. Delay varies depending on the arrangement, and if the delay is lower and the power dissipation is lower, we may claim that the circuit is efficient.In the given paper they have proposed a QCA design for a CNOT gate, DOUBLE CNOT gate, TOFFOLI gate, DOUBLE CNOT gate, single TOFFOLI with 5 NOT gates and a SWAP circuit which contains less number of cells. We simulated the proposed designs in the QCA software and got exactly the correct outputs. But noticed the wrong results in the swap circuit simulation which is different from the truth table and we got the matching outputs with the truth table in our simulation.

The proposed CNOT and TOFFOLI gates contain only 11, and 10 cells respectively, which is a drastic reduction in the cell count, and indirect area and finally results in less power dissipation and less delay. We calculated the delays and compared them with older and existing proposed QCA designs. Designing QCA circuit logic that performs even in the presence of certain mistakes is the best strategy to prevent such problems. These designs enable other cells that are in a healthy state to balance out some flaws.